SFF-TA-1045

Specification for

Pin and Signal Definition for the Hybrid Orthogonal EDSFF Connector Specification

Rev 1.0 March 13, 2026

SECRETARIAT: SFF TWG
This specification is made available for public review at https://www.snia.org/sff/specifications. Comments may be submitted at https://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

This document has been released by SNIA. The SFF TWG believes that the ideas, methodologies, and technologies described in this document are technically accurate and are appropriate for widespread distribution.

The description in this specification does not assure that the specific component is available from suppliers. If such a component is supplied, it should comply with this specification to achieve interoperability between suppliers.

ABSTRACT: This specification defines the pin and signal definition for the Hybrid Orthogonal EDSFF Connector and Plug.

POINTS OF CONTACT:
SNIA Technical Council Managing Director
Email: TCA@snia.org

Chairman SFF TWG
Email: SFF-Chair@snia.org

EDITORS:
Josh Sinykin, Broadcom
Jason Stuhlsatz, Broadcom

INTELLECTUAL PROPERTY

The user's attention is called to the possibility that implementation of this specification may require the use of an invention covered by patent rights. By distribution of this specification, no position is taken with respect to the validity of a claim or claims or of any patent rights in connection therewith.

This specification is covered by the SNIA IP Policy and as a result goes through a request for disclosure when it is published.

Additional information can be found at the following locations:

- Results of IP Disclosures: https://www.snia.org/sffdisclosures
- SNIA IP Policy: https://www.snia.org/ippolicy

COPYRIGHT

DISCLAIMER

The information contained in this publication is subject to change without notice. SNIA makes no warranty of any kind with regard to this specification, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. SNIA shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this specification.

Suggestions for revisions should be directed to https://www.snia.org/feedback/.

FOREWORD

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, as well as since SFF's transition to SNIA in 2016, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/join.

REVISION HISTORY

Rev 1.0 *March 13, 2026*:
-Initial Specification

CONTENTS

FIGURES

TABLES

1. Scope

This specification defines the Hybrid Orthogonal Connector and Plug signal descriptions. Additional informative information such as Cable topologies are included in an appendix.

2. References

2.1 Industry Documents

The following documents are relevant to this specification:

- PCI-SIG PCI Express SFF-8639 Module Specification
- PCI-SIG PCI Express Base Specification, Revision 3.0, 4.0, 5.0, 6.3, 7.0
- SFF-TA-1005 Universal Backplane Management (UBM)
- SFF-TA-1009 Enterprise and Datacenter Standard Form Factor Pin and Signal Specification
- SFF-TA-1016 Internal Unshielded High Speed Connector System
- SFF-TA-1044 Hybrid Orthogonal EDSFF Connector System
- CopprLink PCI Express - CopprLink Internal Cable Specification for PCI Express 5.0 and 6.0
- REF-TA-9402 Cross Reference to Select SFF Connectors
-

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

Other standards may be obtained from the organizations listed below:

Standard	Organization	Website
ASME	American Society of Mechanical Engineers (ASME)	https://www.asme.org
Electronic Industries Alliance (EIA)	Electronic Components Industry Association (ECIA)	https://www.ecianow.org/eia-technical-standards
IEEE	Institute of Electrical and Electronics Engineers (IEEE)	https://ieeexplore.ieee.org/browse/standards/get-program/page/series?id=68
InfiniBand	InfiniBand Trade Association (IBTA)	https://www.infinibandta.org
JEDEC	Joint Electron Deice Engineering Council (JEDEC)	https://www.jedec.org
OIF	Optical Internetworking Forum (OIF)	https://www.oiforum.com/technical-work/implementation-agreements-ias/
PCIe	PCI-SIG	https://www.pcisig.com/specifications
SAS and other ANSI standards	International Committee for Information Technology Standards (INCITS)	https://www.incits.org

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS: Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a. red (i.e., one of the following colors):
    A. crimson; or
    B. pink;
b. blue; or
c. green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1. top;
2. middle; and
3. bottom.

Lists are associated with an introductory paragraph or phrase and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

DIMENSIONING CONVENTIONS: The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	**French**	**ISO**
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be implemented as defined by the specification. Describing a feature as optional in the text is an informational callout to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Where the term is used for a signal on a connector contact, the function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies to the restricted designation, then the restricted bit, byte, word, or field shall be treated as a value whose definition is not in scope of this document, and is not interpreted by this specification.

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

CPRSNT#: Cable Present signal, an active-low signal provided by an Endpoint to indicate that it is both present and its power is within tolerance
PCIe: PCI Express
PERST#: A PCI signal which provides a reset to a PCIe device.
SMBRST#: A Serial Management Bus (SMBus) Reset signal which provides a reset to the DFC SMBus logic.
UBM: Universal Backplane Management represents this specification.
PCB: Printed Circuit Board
SMT: Surface Mount Technology

3.3 Definitions

2Wire Master: Industry standard two wire protocol responsible for initiating communication

2Wire Slave: Industry standard two wire protocol responsible for accepting communication when addressed by a 2Wire Master

Host: A Storage Controller Adapter, PCIe Switch, and/or Root Complex port.

Port: Groupings of the high speed transmit and receive differential signals.

RefClk: PCIe Reference Clock

UBM: Universal Backplane Management (SFF-TA-1005)

Alignment guides: A term used to describe features that pre-align the two halves of a connector interface before electrical contact is established. Other common terms include: guide pins, guideposts, blind mating features, mating features, alignment features, and mating guides.

Basic (dimension): The theoretical exact size, profile, orientation, or location of a feature. It is used as the basis from which permissible variations are established by tolerances in notes or in feature control frames (GD&T).

Connector: Each half of an interface that, when joined together, establish electrical contact and mechanical retention between two components. In this specification, the term connector does not apply to any specific gender; it is used to describe the receptacle, the plug or the card edge, or the union of receptacle to plug or card edge. Other common terms include: connector interface, mating interface, and separable interface.

Contact mating sequence: A term used to describe the order of electrical contact established/ terminated during mating/un-mating. Other terms include: contact sequencing, contact positioning, mate first/break last, EMLB (early mate late break) staggered contacts, and long pin/short pin.

Contacts: A term used to describe connector terminals that make electrical connections across a separable interface.

Datum: A point, line, plane, etc. assumed to be exact for the purposes of computation or reference, as established from actual features, and from which the location or geometric relationship of either feature is established.

Frontshell / Backshell: A term used to describe the metallic part of a module that provides mechanical and shielding continuity between the plug and receptacle. Other terms commonly used are: housing, snout, and metal shroud.

Module: In this specification, module may refer to a plug assembly at the end of a copper (electrical) cable (passive or active), an active optical cable assembly, an optical transceiver, or a loopback.

Plug: A term used to describe the connector that contains the penetrating contacts of the connector interface as shown in Figure 3-1. Plugs typically contain stationary contacts. Other common terms include male, pin connector, and card edge.

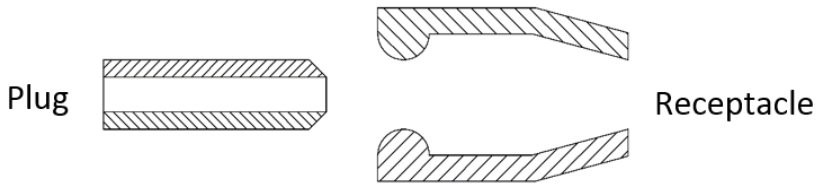


Figure 3-1 Plug and Receptacle Definition

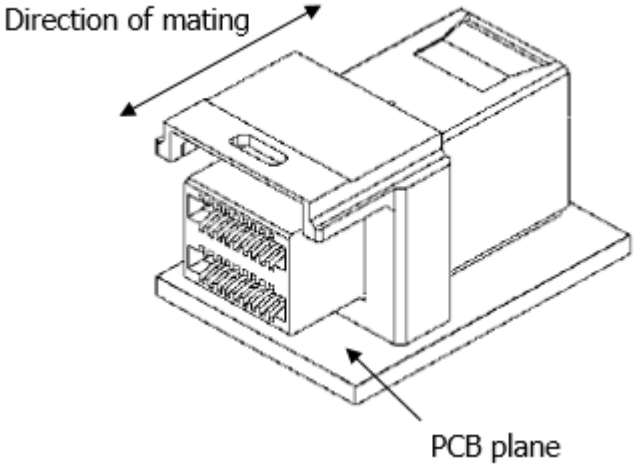
Plated through hole termination: A term used to describe a termination style in which rigid pins extend into or through the PCB. Pins are soldered to keep the connector or cage in place. Other common terms are through hole or PTH.

Press fit: A term used to describe a termination style in which collapsible pins penetrate the surface of a PCB. Upon insertion, the pins collapse to fit inside the PCB's plated through holes. The connector or cage is held in place by the interference fit between the collapsed pins and the PCB.

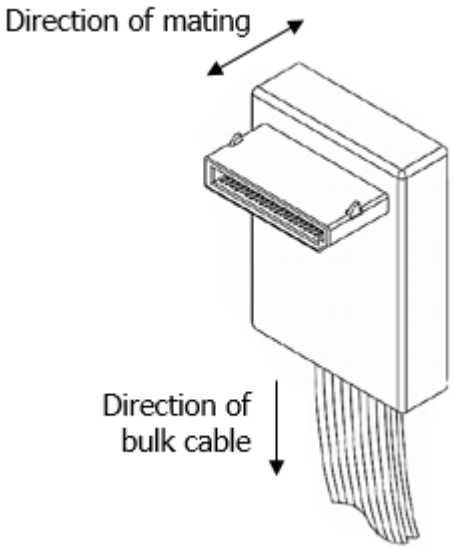
Receptacle: A term used to describe the connector that contains the contacts that accept the plug contacts as shown in Figure 3-1. Receptacles typically contain spring contacts. Other common terms include female and socket connector.

Reference (dimension): A dimension provided for information or convenience. It has no tolerance and is not to be used for inspection or conformance. It can be calculated from other tolerance dimensions or can be found elsewhere on the drawing with a tolerance. If removed, it would have no impact on the defined object or the ability or reproduce it.

Right Angle: A term used to describe either a connector design where the mating direction is parallel to the plane of the printed circuit board upon which the connector is mounted or a cable assembly design where the mating direction is perpendicular to the bulk cable.



a) Right angle connector



b) Right angle cable assembly

Figure 3-2 Right Angle Connector and Cable Assembly

Straddle mount: A term used to describe a termination style that uses surface mount termination points on both sides of a PCB.

Straight: A term used to describe a connector design where the mating direction is parallel to the bulk cable.

Surface mount: A term used to describe a termination style in which solder tails sit on pads on the surface of a PCB and are then soldered to keep the connector or cage in place. Other common terms are surface mount technology or SMT.

Termination: A term used to describe a connector's non-separable attachment point such as a connector contact to a bulk cable/ a cage to a PCB or flex circuit/ bulk cable to a PCB or flex circuit/ solder tail to PCB. Common PCB

terminations include: surface mount (SMT), plated through hole termination (PTH), and press fit (PF). Common cable terminations include insulation displacement contact (IDC), insulation displacement termination (IDT), wire slots, solder, welds, crimps, and brazes.

Vertical: A term used to describe a connector design where the mating direction is perpendicular to the printed circuit board upon which the connector is mounted.

Wipe: The distance a contact travels on the surface of its mating contact during the mating cycle as shown in Figure 3-3.

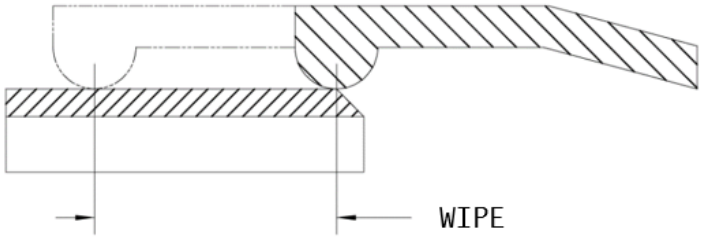


Figure 3-3 Wipe for a Continuous Contact

4. General Description

4.1 Configuration Overview/Descriptions

The SFF-TA-1044 Hybrid Orthogonal EDSFF Connector System specification describes a connector (i.e., connector receptacles) and a connector plug (i.e., Cable End). An EDSFF device connector is inserted into the connector such that high speed signaling is routed directly to the connector plug (i.e., cable end). Low speed signaling is routed through the receptacle connector to the midplane which contains the supporting management circuitry. Additionally, the connector plug (i.e., Cable end) also contains low speed signaling to enable the management of the device via the receptacle connector. In Figure 4-1, the SFF-TA-1044-RS24 receptacle and plug are depicted. This is the receptacle and plug that is defined in this specification.

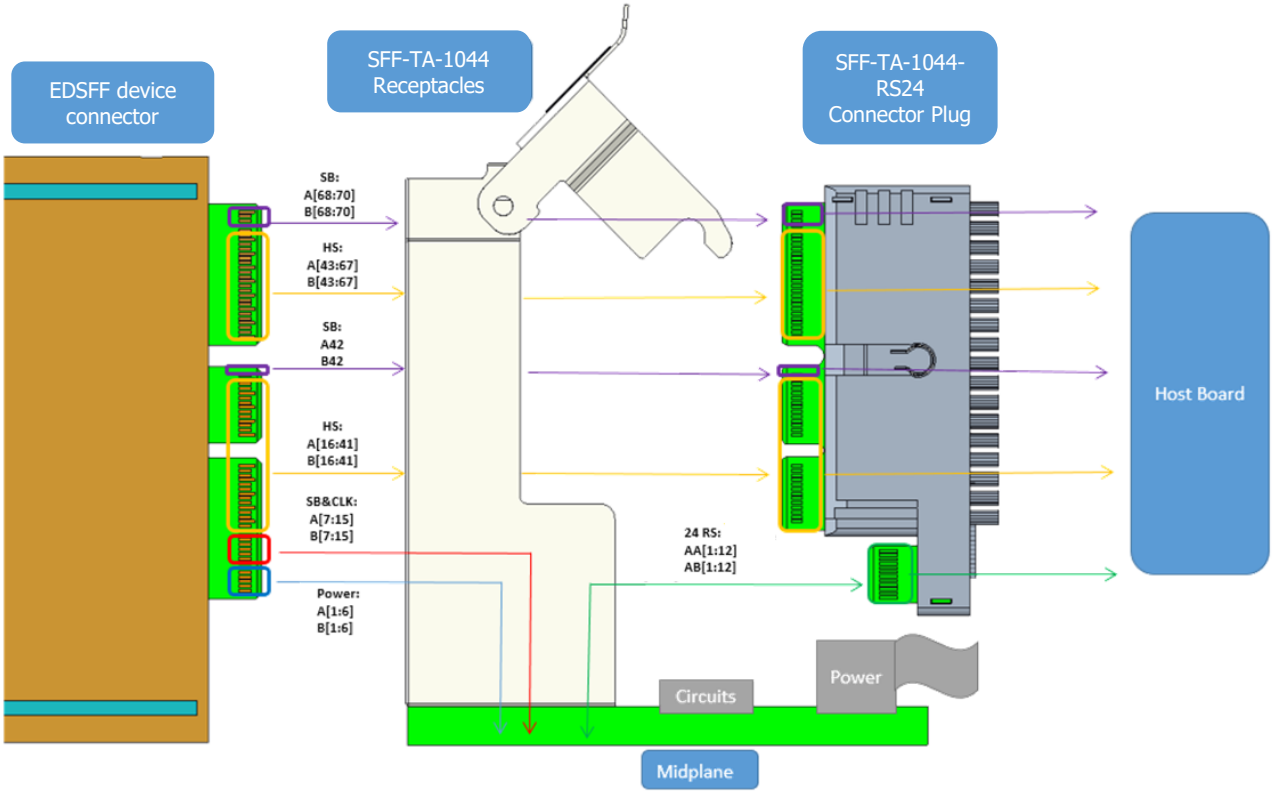


Figure 4-1 SFF-TA-1044-RS24 Receptacle and Plug

5. Signal List

The signals of the Hybrid Orthogonal Connector plug and receptacles are broken down into four subcategories:

- EDSFF to Midplane
- Midplane to Connector Plug
- High-speed signals from the EDSFF to the Connector Plug
- Passthrough signals from EDSFF to the Connector Plug

5.1 EDSFF to Midplane

The EDSFF device signals that are routed to the midplane are listed in Table 5-1.

Table 5-1 EDSFF to Midplane Signals

Signal Name from SFF-TA-1009
GND
SMBCLK/I3CCLK
SMBDATA/I3CDATA
SMRST#
LED
PERST1#/CLKREQ#
PRSNT0#
REFCLKn1
REFCLKp1
12 V
MFG
RFU
DUALPORTEN#
PERST0#
3.3 Vaux
PWRDIS
REFCLKn0
REFCLKp0

All signals listed above are defined in SFF-TA-1009.

5.2 Midplane to Connector Plug

The signals that route from the midplane to the SFF-TA-1044 Connector Plug are listed in Table 5-2.

Table 5-2 Midplane to SFF-TA-1044 Connector Plug

Connector Signal Name	Function
REFCLKn0	See SFF-TA-1009 Definition
REFCLKp0	See SFF-TA-1009 Definition
REFCLKn1	See SFF-TA-1009 Definition
REFCLKp1	See SFF-TA-1009 Definition
BPTYPE_A/B_VOLTAGE_SOURCE_A/B	Backplane Type signal requirement is defined in the SFF-8448 specification. A UBM Controller shall pull this signal HIGH to indicate a 2Wire backplane interface.,

	Voltage Source is an alternative behavior of this pin enabled during a CCC Process defined in SFF-TA-1005 (UBM).
HFC_2W_RESET_A/B	SFF-TA-1005 definition of 2W_RESET
HFC_2W_CLK_A/B	2W-CLK (See SFF-9402)
HFC_2W_DAT_A/B	2W-DATA (See SFF-9402)
HFC_PERST_A/B	SFF-TA-1005 definition of HFC_PERST
HFC_CHANGE_DETECT_N_A/B	SFF-TA-1005 definition of HFC_CHANGE_DETECT
CABLE_TYPE_DETECT	See Section 8.2.2
MAX_CABLE_LEG_COUNT	See Section 8.2.3
CONNECTOR_PLUG_LEG_SENSE	See Section 8.2.3
GND	Ground

5.3 High-speed signals from EDSFF to Connector Plug

PCIe names the signals on the device from the host perspective (i.e., for PCIe products, a receiver on the device has a transmitter signal name). The high-speed EDSFF signals are listed in Table 5-3, these signals route from the EDSFF and passthrough to the SFF-TA-1044 Connector Plug.

Table 5-3 High-speed signals from EDSFF to SFF-TA-1044 Connector Plug

Device Receptacle Connector Name	SFF-9402 Equivalent Signal Name	Function	Connectors
PETn0,n1,n2,n3	Rx-[0:3]	Represents the Device ASIC Receive negative	Supported x4,x8,x16 connections
PETp0,p1,p2,p3	Rx+[0:3]	Represents the Device ASIC Receive positive	Supported x4,x8,x16 connections
PERn0,n1,n2,n3	Tx-[0:3]	Represents the Device ASIC Transmit negative	Supported x4,x8,x16 connections
PERp0,p1,p2,p3	Tx+[0:3]	Represents the Device ASIC Transmit positive	Supported x4,x8,x16 connections
PETn4,n5,n6,n7	Rx-[4:7]	Represents the Device ASIC Receive negative	Supported x8,x16 connections
PETp4,p5,p6,p7	Rx+[4:7]	Represents the Device ASIC Receive positive	Supported x8,x16 connections
PERn4,n5,n6,n7	Tx-[4:7]	Represents the Device ASIC Transmit negative	Supported x8,x16 connections
PERp4,p5,p6,p7	Tx+[4:7]	Represents the Device ASIC Transmit positive	Supported x8,x16 connections
PETn8,n9,n10,n11,n12,n13,n14,n15	Rx-[8:15]	Represents the Device ASIC Receive negative	Supports x16 connections
PETp8,p9,p10,p11,p12,p13,p14,p15	Rx+[8:15]	Represents the Device ASIC Receive positive	Supports x16 connections
PERn8,n9,n10,n11,n12,n13,n14,n15	Tx-[8:15]	Represents the Device ASIC Transmit negative	Supports x16 connections

PERp8,p9,p10,p11,p12,p13,p14,p15	Tx+[8:15]	Represents the Device ASIC Transmit positive	Supports x16 connections

High speed signaling follows the SFF-TA-1009 EDSFF Receptacle Connector (Figure 5-1 from SFF-TA-1009) definition of PETp/n and PERp/n.

In Figure 5-1 the Host connector represents an SFF-TA-1016 connector and the SFF-TA-1045 Connector Plug represents itself as a Device Straight connector via the Cable Type Detect signal (See 8.2.2).

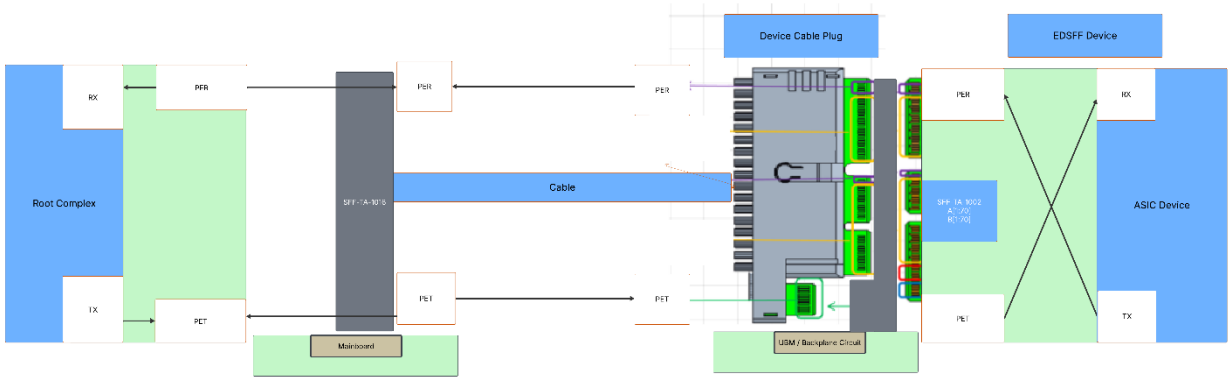


Figure 5-1 Root Complex main board connect to SFF-TA-1044 Receptacle High Speed Routing Example

If the Cable Type Detect indicates Root Straight cable type, the Rx and Tx routing at the Cable Plug are swapped. This is depicted in Figure 5-2.

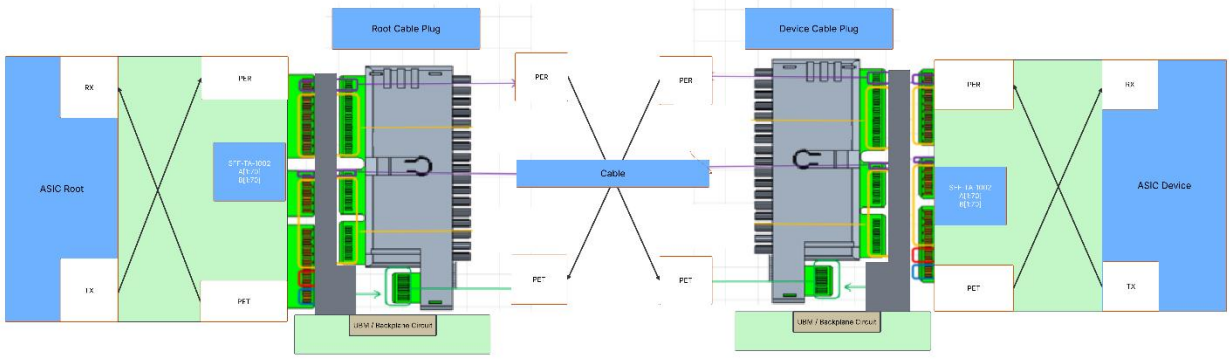


Figure 5-2 SFF-TA-1044 Receptacle to SFF-TA-1044 Receptacle High Speed Routing Example

5.4 Passthrough from EDSFF to SFF-TA-1044 Connector Plug

The EDSFF low-speed signals that passthrough to the SFF-TA-1044 Connector Plug directly (i.e., avoiding the midplane) are listed in Table 5-4.

Table 5-4 Passthrough Signals from the EDSFF connector to the SFF-TA-1044 Connector Plug

CONNECTOR SIGNAL
RFU
PRSNT1#
PRSNT2#

6. Connector Receptacle Contact Numbering

The Connector Receptacle contains signals that route to the midplane, and signals that route directly through to the Connector Plug.

6.1 Connector Receptacle Contact Numbering

6.1.1 Direct Passthrough Contacts

The direct passthrough contacts consist of the high-speed signals from EDSFF/SFF-TA-1002 connector to the Hybrid Orthogonal Connector Plug.

Table 6-1 Direct Passthrough Contacts from the EDSFF connector to the SFF-TA-1044 Connector Plug

PIN/PAD	CONNECTOR SIGNAL
A16	GND
A17	PERn0
A18	PERp0
A19	GND
A20	PERn1
A21	PERp1
A22	GND
A23	PERn2
A24	PERp2
A25	GND
A26	PERn3
A27	PERp3
A28	GND
A29	GND
A30	PERn4
A31	PERp4
A32	GND
A33	PERn5
A34	PERp5
A35	GND
A36	PERn6
A37	PERp6
A38	GND
A39	PERn7
A40	PERp7
A41	GND
A43	GND
A44	PERn8
A45	PERp8

A46	GND
A47	PERn9
A48	PERp9
A49	GND
A50	PERn10
A51	PERp10
A52	GND
A53	PERn11
A54	PERp11
A55	GND
A56	PERn12
A57	PERp12
A58	GND
A59	PERn13
A60	PERp13
A61	GND
A62	PERn14
A63	PERp14
A64	GND
A65	PERn15
A66	PERp15
A67	GND
B16	GND
B17	PETn0
B18	PETp0
B19	GND
B20	PETn1
B21	PETp1
B22	GND
B23	PETn2
B24	PETp2
B25	GND
B26	PETn3
B27	PETp3
B28	GND
B29	GND
B30	PETn4
B31	PETp4
B32	GND
B33	PETn5
B34	PETp5
B35	GND

B36	PETn6
B37	PETp6
B38	GND
B39	PETn7
B40	PETp7
B41	GND
B43	GND
B44	PETn8
B45	PETp8
B46	GND
B47	PETn9
B48	PETp9
B49	GND
B50	PETn10
B51	PETp10
B52	GND
B53	PETn11
B54	PETp11
B55	GND
B56	PETn12
B57	PETp12
B58	GND
B59	PETn13
B60	PETp13
B61	GND
B62	PETn14
B63	PETp14
B64	GND
B65	PETn15
B66	PETp15
B67	GND

6.1.2 Passthrough from SFF-TA-1002/EDSFF to the SFF-TA-1044 Connector Plug

Table 6-2 Passthrough Signals from the EDSFF Connector to the SFF-TA-1044 Connector Plug

PIN/PAD	CONNECTOR SIGNAL
A42	RFU
A68	RFU
A69	RFU

A70	RFU
B42	PRSNT#1
B68	RFU
B69	RFU
B70	PRSNT2#

6.1.3 Midplane Contacts

The Connector Receptacle routes SFF-TA-1009 signals A[1:15] and B[1:15] to the midplane.

Table 6-3 EDSFF Connector Signals that route to the midplane

PIN/PAD	CONNECTOR SIGNAL
A1	GND
A2	GND
A3	GND
A4	GND
A5	GND
A6	GND
A7	SMBCLK/I3CCLK
A8	SMBDATA/I3CDATA
A9	SMRST#
A10	LED
A11	PERST1#/CLKREQ#
A12	PRSNT0#
B1	12 V
B2	12 V
B3	12 V
B4	12 V
B5	12 V
B6	12 V
B7	MFG
B8	RFU
B9	DUALPORTEN#
B10	PERST0#
B11	3.3 Vaux
B12	PWRDIS

6.2 Connector Plug Contact Numbering

6.2.1 Common Sideband Connector Plug Signals

Table 6-4 SFF-TA-1044-RS24 Connector Plug signals that route to the midplane

PIN/PAD	CONNECTOR SIGNAL
AA1	BPTYPE_A_VOLTAGE_SOURCE_A
AA2	HFC_2W_RESET_A
AA3	GND
AA4	REFCLKn0
AA5	REFCLKp0
AA6	GND
AA7	BPTYPE_B_VOLTAGE_SOURCE_B*
AA8	HFC_2W_RESET_B*
AA9	GND
AA10	REFCLKn1*
AA11	REFCLKp1*
AA12	GND
AB1	HFC_2W_CLK_A
AB2	HFC_2W_DAT_A
AB3	CABLE_TYPE_DETECT
AB4	HFC_PERST_A
AB5	HFC_CHANGE_DETECT_N_A
AB6	GND
AB7	HFC_2W_CLK_B*
AB8	HFC_2W_DAT_B*
AB9	MAX_CABLE_LEG_COUNT
AB10	HFC_PERST_B*
AB11	HFC_CHANGE_DETECT_N_B*
AB12	CONNECTOR_PLUG_LEG_SENSE

Note: Signals with an asterisk (*) denote the second domain management interface of an EDSFF device (e.g., DUALPORTEN# signal is asserted to the EDSFF device). In single domain deployments these signals may be left unconnected.

6.2.1.1 Contact Numbering for 1C Connector Plug

The pins or electrical contacts in the 1C connector are numbered as shown in Figure 6-1.

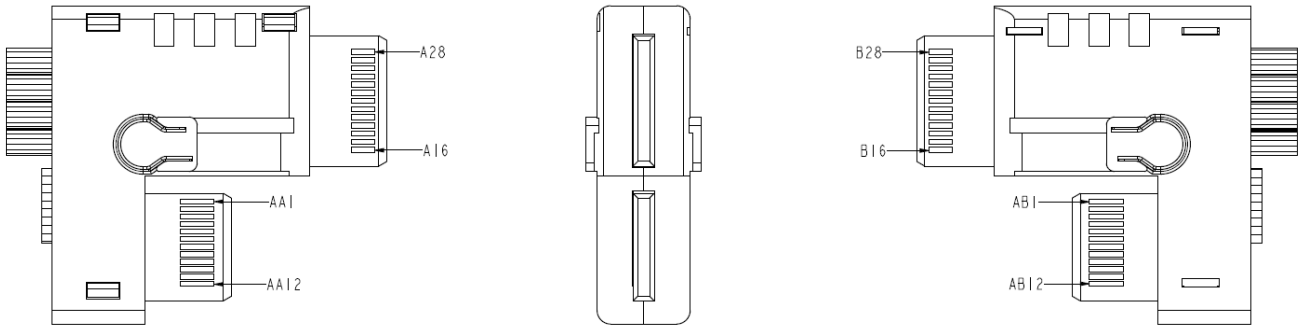


Figure 6-1 Contact Numbering for 1C-RS24 Connector Plug

6.2.1.2 Contact Numbering for 2C Connector Plug

The pins or electrical contacts in the 2C connector are numbered as shown in Figure 6-2.

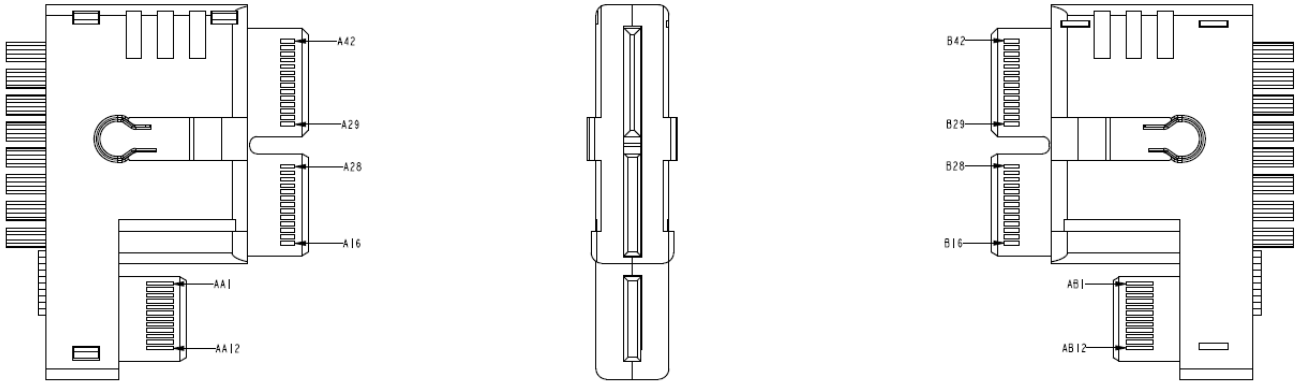


Figure 6-2 Contact Numbering for 2C-RS24 Connector Plug

6.2.1.3 Contact Numbering for 4C Connector Plug

The pins or electrical contacts in the 4C connector are numbered as shown in Figure 6-3.

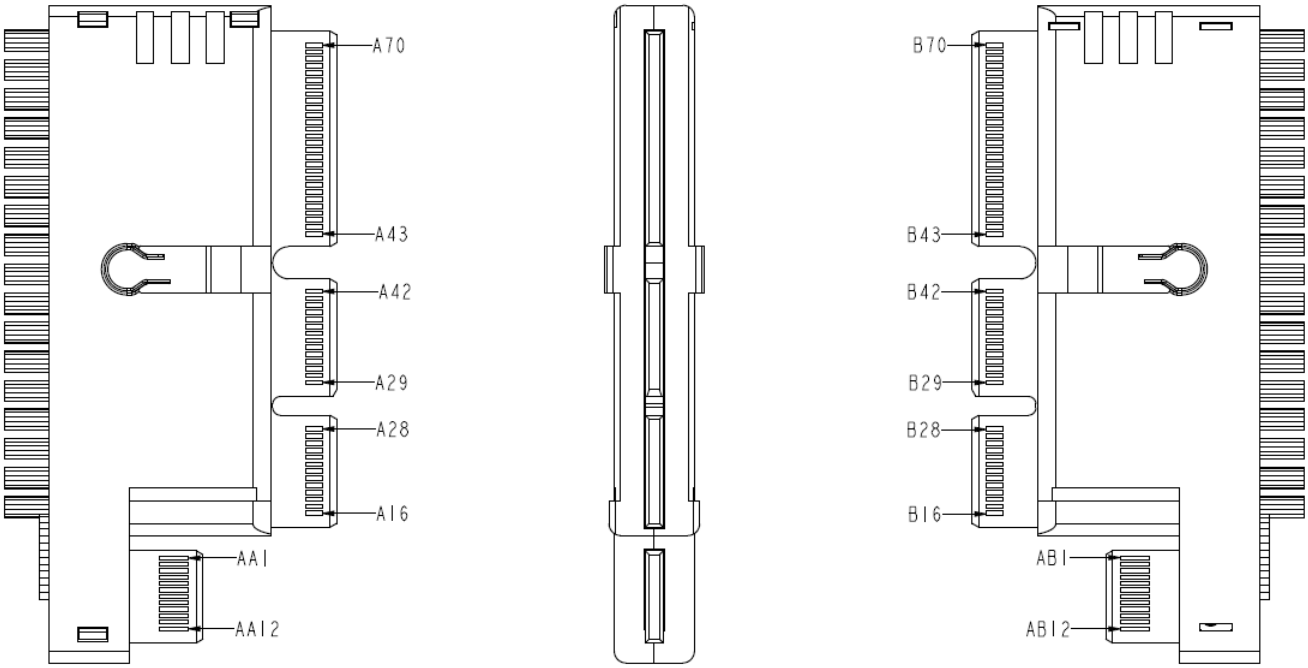


Figure 6-3 Contact Numbering for 4C-RS24 Connector Plug

7. Connector Mechanical Specification

See SFF-TA-1044 for mechanical implementation details.

8. Electrical Characteristics

8.1 Overview

The electrical signals follow SFF-TA-1009 signal definitions except for the detection mechanisms defined in this standard and described in the following sections. The detection mechanisms are a method to inform the backplane what type of cable has been connected and the context related to the leg (i.e., the branch portion of a cable with a connector plug) of a cable that is installed in relation to the total number of cable legs.

8.2 Detection Mechanisms

The Hybrid Orthogonal Connector Plug provides the following cable detection signals:

- Voltage Source Reference via the BPTYPE_VOLTAGE_SOURCE signal
- Cable Type Detect via the CABLE_TYPE_DETECT signal
- Cable Plug Identifier
    - Consisting of two signals
        - CONNECTOR_PLUG_LEG_SENSE
        - MAX_CABLE_LEG_COUNT

8.2.1 Voltage Source

The Voltage Source shall be present during the connector plug leg sense and max cable leg count measurement. The Voltage Source shall be provided over the BPTYPE_VOLTAGE_SOURCE sideband signal by the Host and received by the midplane circuitry. The Voltage Source reference shall only be valid during a CCC Process (see SFF-TA-1005). Upon completion of the CCC Process the Host shall remove the Voltage Source before proceeding to further backplane discovery.

Note: This signal is available for alternative usage before and after the host system has completed the CCC Process (e.g., BPType detection, 3.3 V AUX Mgmt). Midplane circuity shall account for existing BPTYPE_VOLTAGE_SOURCE signal requirements when the Voltage Source is not being used for measurements.

The Host shall supply the voltage of 3.3 V +/- 5.5% and a minimum of 1.2 mA current for the measurement process on the Voltage Source reference signal. See the SFF-9402 specification for guidance relating to the host signals associated with the BPTYPE_VOLTAGE_SOURCE signal.

8.2.2 Cable Type Detect

The CABLE_TYPE_DETECT signal uses the local backplane 3.3 V +/- 5% voltage source as the voltage reference in a simple voltage divider circuit. To decode the cable type connected to the receptacle. A voltage divider circuit is created between the backplane local voltage source (e.g., Vin), the backplane with the common resistor (e.g., R1), and the SFF-TA-1044 plug containing the variable resistor (e.g., R2) specific to the cable deployment strategy. Table 8-1 defines the cable deployment strategies that can be conveyed using the R2 resistor in the cable plug. The resistor layout between the backplane and the plug is depicted in Figure 8-2.

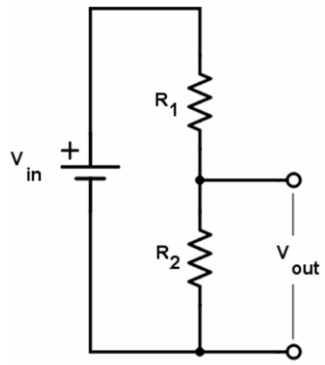


Figure 8-1 Voltage Divider Circuit Example

Table 8-1 Cable Type Detect Identifier Resistor definition

Cable Type Detect Identifier	R1 (ohm) +/- 1% Tolerance	R2 (ohm) +/- 1% Tolerance	Detection Vmin (mV) across R2	Detection Vmax (mV) across R2
Reserved	10000	2200	585	595
Reserved	10000	2700	691	702
Reserved	10000	3300	807	819
Reserved	10000	3900	913	926
Reserved	10000	4700	1041	1055
Root Straight	10000	5600	1169	1185
Reserved	10000	6800	1320	1336
Device Single Lane	10000	8200	1470	1487
Reserved	10000	10000	1634	1650
Device Bifurcated	10000	12000	1784	1800
Reserved	10000	15000	1964	1980
Device Dual Domain	10000	18000	2106	2121
Reserved	10000	22000	2255	2269
Device Straight	10000	27000	2395	2408
Reserved	10000	33000	2521	2533
Reserved	10000	39000	2616	2627
No Cable Attached	10000	N/A		Vmax

A Root Straight Connector Plug is a Connector Plug that manages the attachment to a Root/Host interface. The midplane circuitry detection utilizes the CABLE_TYPE_DETECT signal to properly posture I/O associated to the attached Root/Host.

A Device Straight Connector Plug is a Connector Plug that provides all the lanes of the attached End Device. The midplane circuitry shall deassert the DUALPORTEN# signal to the End Device.

A Device Bifurcated Connector Plug is a Connector Plug that provides half of the lanes of the attached End Device. The midplane circuitry shall deassert the DUALPORTEN# signal to the End Device.

A Device Dual Domain Connector Plug is a Connector Plug that provides both halves of the attached End Device to two separate Host connector. The midplane circuitry shall assert the DUALPORTEN# signal to the End Device.

A Device Single Lane Connector Plug is a Connector Plug that provides only lane 0 of the attached End Device. The midplane circuitry shall deassert the DUALPORTEN# signal to the End Device.

The detection of No Cable Attached occurs when there is no Connector Plug inserted into the Connector Receptacle.

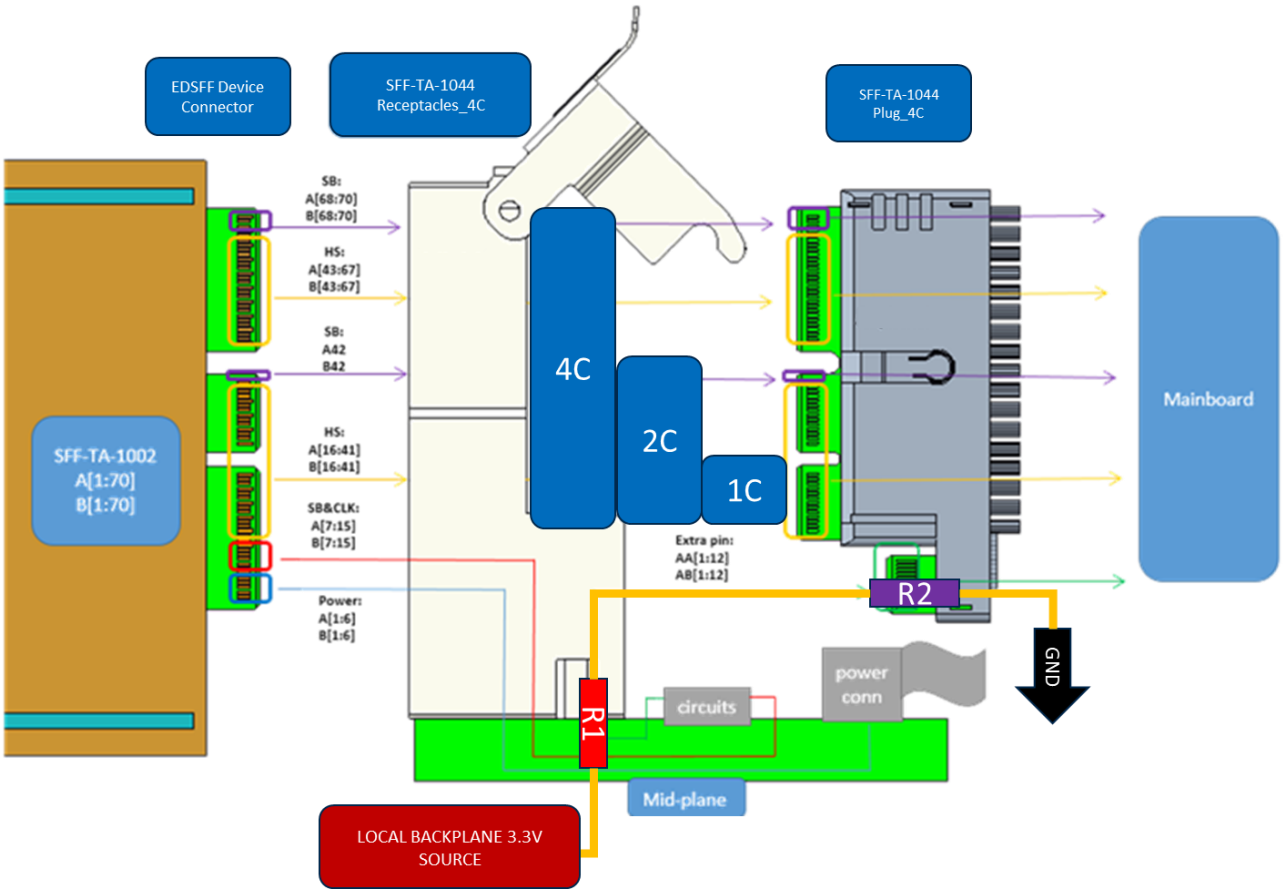


Figure 8-2 Cable Type Detect Resistor Layout Example

8.2.3 Cable Plug Identifier

The Cable Plug Identifier is used by the cable manufacturers to inform the backplane about the cable design. The Cable Plug Identifier value is used for the CONNECTOR_PLUG_LEG_SENSE signal and the MAX_CABLE_LEG_COUNT. Each signal has its own Cable Plug Identifier value. Table 8-2 is used to decode the CONNECTOR_PLUG_LEG_SENSE and MAX_CABLE_LEG_COUNT signals. These signals are referenced by the corresponding BPTYPE_VOLTAGE_SOURCE signal which is provided by the Host. To decode the Cable Plug Identifier a voltage divider circuit (See Figure 8-1) is created between the BPTYPE_VOLTAGE_SOURCE signal (e.g., Vin) and the connector plug containing the variable resistor (e.g., R1) specific to the deployment strategy and the backplane with the common resistor (e.g., R2). The resistor layout between the backplane and the plug is depicted in Figure 8-3.

Table 8-2 Connector Plug Leg Sense and Max Cable Leg Count Resistor definition

Cable Plug Identifier	R1 (ohm) +/- 1% Tolerance	R2 (ohm) +/- 1% Tolerance	Detection Vmin (mV) across R2	Detection Vmax (mV) across R2
1	2200	10000	2695	2705
2	2700	10000	2587	2598
3	3300	10000	2469	2481
4	3900	10000	2361	2374

5	4700	10000	2230	2245
6	5600	10000	2100	2115
7	6800	10000	1948	1964
8	8200	10000	1797	1813
9	10000	10000	1634	1650
10	12000	10000	1484	1500
11	15000	10000	1304	1320
12	18000	10000	1163	1179
13	22000	10000	1017	1031
14	27000	10000	879	892
15	33000	10000	756	767
16	39000	10000	663	673

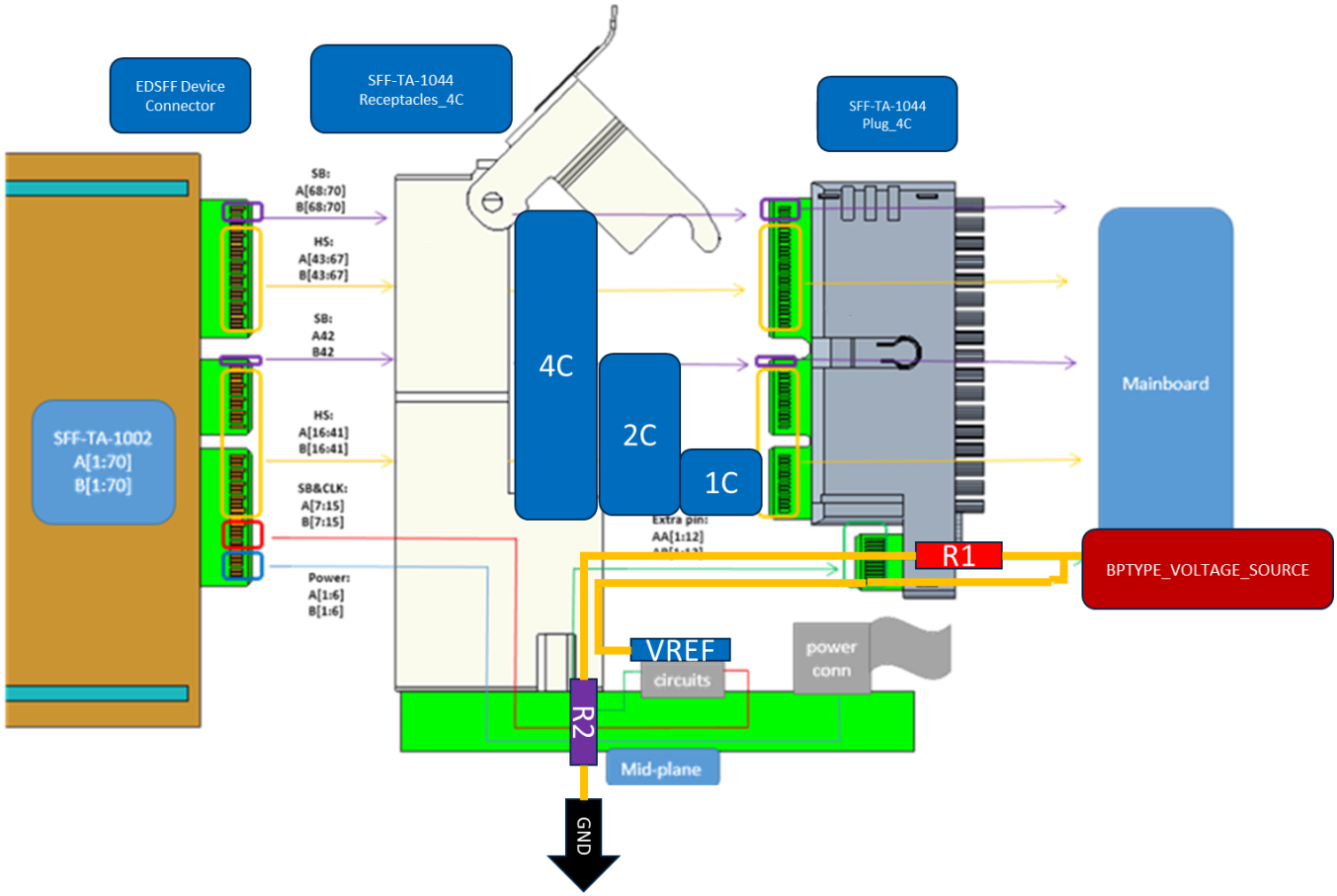


Figure 8-3 Cable Plug Identifier Resistor Layout Example

Appendix A. Cabled Deployments (Informative)

A.1. Host x16 connection to 4 EDSFF devices at x4 connectivity

In the cable in Figure A-1, the MAX_CABLE_LEG_COUNT signal is defined as 4 in each connector plug. Each cable leg identifies uniquely in the cable from 1 to 4 via the CONNECTOR_PLUG_LEG_SENSE signal. The CABLE_TYPE_DETECT signal in the connector plug is set for Device Straight.

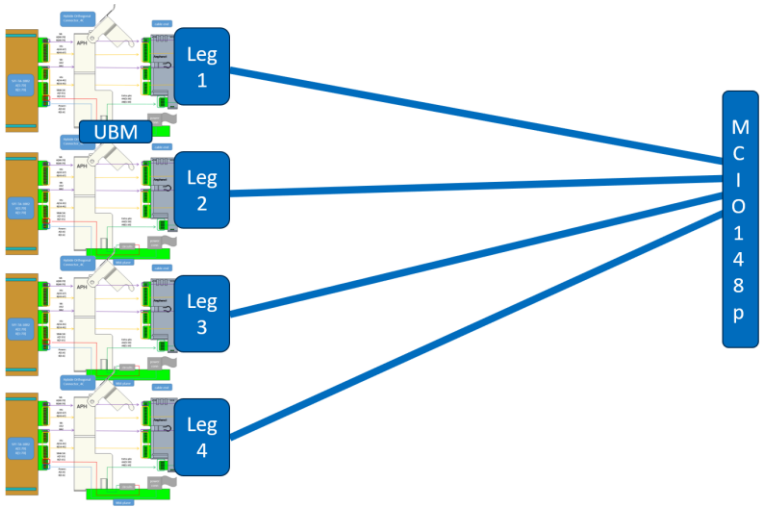


Figure A-1 Qty 4 EDSFF x4 Cabled Deployment

A.2. Two Host x16 connections to 4 EDSFF devices at x4 connectivity

In the cable in Figure A-2, the MAX_CABLE_LEG_COUNT signal is defined as 4 in each connector plug. Each cable leg identifies uniquely in the cable from 1 to 4 via the CONNECTOR_PLUG_LEG_SENSE signal. The secondary domain utilizes the second host facing connector sideband signal set in the connector plug (i.e., sideband set B). The CABLE_TYPE_DETECT signal in the connector plug is set for Device Dual Domain.

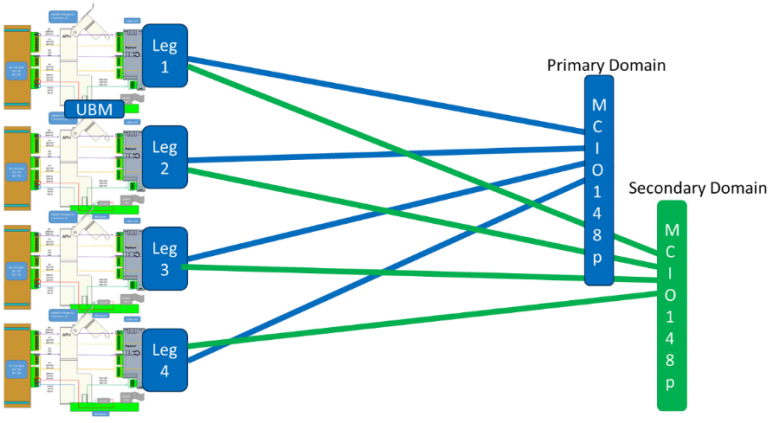


Figure A-2 Device Dual Domain Example

A.3. A root x16 connection to 4 EDSFF devices at x4 connectivity using SFF-TA-1044 connectors

In Figure A-3, the cable depicted represents an SFF-TA-1044 Connector Plug on both ends of the cable. The Plug

that is responsible for root connection indicates Root via the Cable Type detect. The Plugs connecting to end devices indicate Device in the Cable Type detect. Transmit and receive high-speed signaling must be properly routed inside the cable to ensure the Root and End device can communicate PCIe correctly. In this cable example, the end device connector plugs MAX_CABLE_LEG_COUNT signal represents a value of 4. Each end device cable leg identifies uniquely in the cable from 1 to 4 via the CONNECTOR_PLUG_LEG_SENSE signal. The CABLE_TYPE_DETECT signal in the end device connector plug is set for Device Straight.

The root facing connector plug has the MAX_CABLE_LEG_COUNT signal representing a value of 1 and the cable type detection of a value of Root Straight.

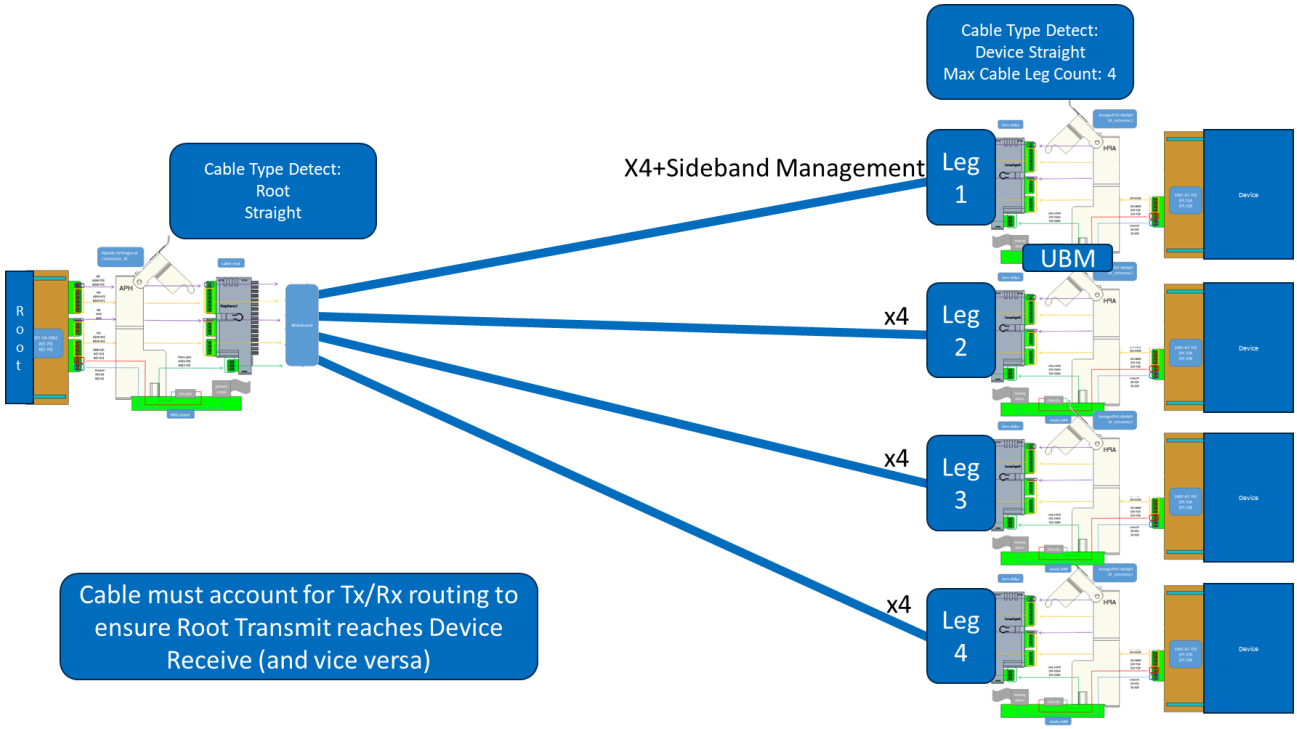


Figure A-3 Root Connection to 4 EDSFF Devices at x4