SFF-8419

Specification for

SFP+ Power and Low Speed Interface

Rev 1.3.3 May 7, 2026

SECRETARIAT: SFF TWG

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This document has been released by SNIA. The SFF TWG believes that the ideas, methodologies, and technologies described in this document are technically accurate and are appropriate for widespread distribution.

ABSTRACT: This draft specification defines the low speed electrical and management interface specifications for SFP+ (enhanced Small Formfactor Pluggable) modules and hosts. The SFP+ module is a hot pluggable small footprint serial-to-serial data-agnostic optical transceiver.

This document provides a common specification for systems manufacturers, system integrators, and suppliers.

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FOREWORD

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/join.

REVISION HISTORY

Rev 1.0 March 31, 2015

-
- Content derived from SFF-8431 Rev 4.2 Sections 2.1-2.7 and 4.
  Updated with current template, but modified numbering to retain Section 2 as the beginning of technical content as per SFF-8431 and retained sequential Table/Figure numbering instead of within section.
- Converted symbols to text and editorial corrections made to case, consistency of expression, etc.
  Corrected references to SFF-8083 to be SFF-8071.
-

Rev 1.1 May 8th, 2015

- Added cross-references to SFF-8431 sections/tables/figures.

Rev 1.2 May 29th, 2015

- Corrected references to SFP+ Module Power Supply Requirements in Section 2.6.

Rev 1.3 June 3rd, 2015

- Transferred power supply Section 2 and Appendix D.17 from SFF-8418
- Title changed to reflect the transferred content.

Rev 1.3.1 February 19th, 2026

- Added new pinout definitions for SFP112/224 modules managed by CMIS in 7.2.2
- Added new timing requirements in Table 9.3, graph on the pull-up resistor values for I2C at 1MHz in Table 9.3, a pull-up value
- Added power classes 3-5 in Table 6-1 and new current limits in Table 6-2
- Updated Test methodology in Appendix A with new inductor value
- Moved the document to new template.

Rev 1.3.2 April 2nd, 2026

- Editorial changes from review ballot

Rev 1.3.3 May 7th, 2026

- Editorial changes from approval ballot

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1. Scope

This draft specification defines the low speed electrical and management interface specifications for SFP+ (enhanced Small Formfactor Pluggable) modules and hosts. The SFP+ module could be an electrical-to-optical or an electrical-to-electrical device.

2. References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:

- Common Management Interface Specification (CMIS)
- Formfactor Specific Hardware Management CMIS-FF
- IEEE Std 802.3, P802.3db, P802.3ck, P802.3cw, P802.3df
- INCITS FC-PI-4, FC-PI-5, FC-PI-6, FC-PI-6p, FC-PI-7, FC-PI-8
- INF-8077 XFP 1X 10 Gb/s Pluggable Module
- ITU-T G.709/Y.1331
- ITU-T G.Sup58
- REF-TA-1011 Cross Reference to Select SFF Connectors and Modules
- SFF-8071 SFP+ 1X 0.8mm Card Edge Connector
- SFF-8081 SFP+ 1X 16 Gb/s Pluggable Transceiver Solution (SFP16)
- SFF-8083 SFP+ 1X 10 Gb/s Pluggable Transceiver Solution (SFP10)
- SFF-8084 SFP+ 1X 4 Gb/s Pluggable Transceiver Solution
- SFF-8402 SFP+ 1X 28 Gb/s Pluggable Transceiver Solution (SFP28)
- SFF-8418 SFP+ 10 Gb/s Electrical Interface
- SFF-8419 SFP+ Power and Low Speed Interface
- SFF-8432 SFP+ Module and Cage
- SFF-8433 SFP+ Ganged Cage
- SFF-8472 Management Interface for SFP+

2.2 Sources

The complete list of SFF documents which have been completed, are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

Copies of the standards and specifications can be obtained from the organizations' websites listed below:

Table 2-1 Sources for Industry Standards and Specifications

Standards and Specifications	Organization	Website
100G CWDM and 100G 4WDM Specifications	CWDM4 MSA	https://www.cwdm4-msa.org/
100G-FR, 100G-LR, 400G-FR4 and 400G-LR4-10 Specifications	100G Lambda MSA	https://100glambda.com/
25G and 50G Specifications	Ethernet Technology Consortium (formerly 25G Gigabit Ethernet Consortium)	https://ethernettechnologyconsortium.org/
Electronic Industry Alliance (EIA)	Electronic Components Industry Association (ECIA)	https://www.ecianow.org
IEEE 802 standards	Institute of Electrical and Electronics Engineers (IEEE)	https://ieeexplore.ieee.org/browse/standards/get-program/page/series?id=68 or https://www.ieee.org

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INCITS/Fibre Channel	International Committee for Information Technology Standards (INCITS)	https://www.incits.org/standards-information/purchase-standards-or-download-dpans
InfiniBand	InfiniBand Trade Association (IBTA)	https://www.infinibandta.org
LPO Specification	LPO MSA	https://www.lpo-msa.org/home/specifications-and-white-papers.html
OIF Implementation Agreements including CMIS	Optical Internetworking Forum	https://www.oiforum.com/technical-work/implementation-agreements-ias/
Open XR Optics	Open XR Optics Forum	https://openxropticsforum.org/
OpenZR+	OpenZR+ MSA	https://openzrplus.org
Open ROADM Specifications	Open ROADM MSA	http://www.openroadm.org
OSFP Specifications	OSFP MSA	https://www.osfpmsa.org/
PCIe	PCI-SIG	https://pcisig.com
QSFP-DD Specification	QSFP-DD MSA	https://www.qsfp-dd.com/
SAS	International Committee for Information Technology Standards (INCITS)	https://www.incits.org/standards-information/purchase-standards-or-download-dpans
Terabit BiDi MSA Technical Specification	Terabit BiDi MSA	https://terabit-bidi-msa.com/

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	**French**	**ISO**
0.6	0,6	0.6
1,000.0	1 000,0	1 000.0
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

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Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be implemented as defined by the specification. Describing a feature as optional in the text is an informational callout to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Where the term is used for a signal on a connector contact, the function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies to the restricted designation, then the restricted bit, byte, word, or field shall be treated as a value whose definition is not in scope of this document, and is not interpreted by this specification.

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

AOC:	Active optical cable
CMIS:	Common Management Interface Specification
DSFP:	Dual Small Form Factor Pluggable
LC:	Lucent Connector
MPO:	Multi-fiber Push-On connector
MT-RJ:	Mechanical transfer registered jack connector
PAM4:	Pulse Amplitude Modulation 4 levels
SC:	Standard connector
SFI:	SFP+ high speed electrical interface
SFP:	Small Form Factor Pluggable
UI:	Unit Interval

3.3 Definitions

Connector: Each half of an interface that, when joined together, establishes electrical contact and mechanical retention between two components. In this specification, the term connector does not apply to any specific gender; it is used to describe the receptacle, the plug or the card edge, or the union of receptacle to plug or card edge. Other common terms include connector interface, mating interface, and separable interface.

Contact mating sequence: A term used to describe the order of electrical contact established/ terminated during mating/un-mating. Other terms include contact sequencing, contact positioning, mate first/break last, EMLB (early mate late break) staggered contacts, and long pin/short pin.

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Contacts: A term used to describe connector terminals that make electrical connections across a separable interface.

Module: In this specification, module may refer to a plug assembly at the end of a copper (electrical) cable (passive or active), an active optical cable assembly, an optical transceiver, or a loopback.

Plug: A term used to describe the connector that contains the penetrating contacts of the connector interface as shown in Figure 3-1. Plugs typically contain stationary contacts. Other common terms include male, pin connector, and card edge.

Receptacle: A term used to describe the connector that contains the contacts that accept the plug contacts as shown in Figure 3-1. Receptacles typically contain spring contacts. Other common terms include female and socket connector.

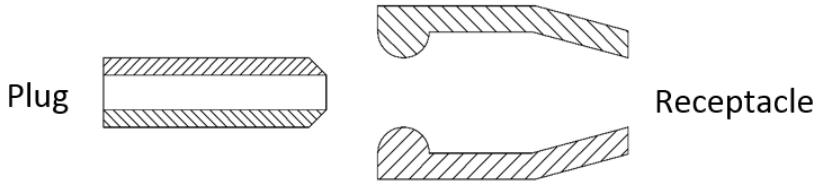

Figure 3-1 Plug and Receptacle Definition

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4. General Description

4.1 Configuration Overview/Descriptions

This draft specification covers the following items:

- Electrical specifications for SFP+ modules including host connector contact assignments.
- Descriptions for data, control, status and management interface signals.
- Power supply requirements.
- Electrostatic discharge (ESD) tolerance requirements.
- Environmental and thermal requirements (case temperatures).
- Timing requirements.

This specification may be compatible with the example optical and electrical specifications in Table 4-1.

Table 4-1 Example uses for SFP+

ITU-T Recommendation G.957	STM-1, STM-4, STM-16
Telcordia Technologies GR-253-CORE	OC-3, OC-12, OC-48, OC-192
IEEE Std. 802.3	10 GbE, 25 GbE, 40 GbE, 50 GbE, 100 GbE, 200 GbE
Infiniband Architecture Specification	SDR, DDR, QDR, FDR, EDR, HDR, NDR
Fibre Channel	8GFC, 16GFC, 32GFC, 128GFC, 256GFC
Serial Attached SCSI	SAS-3, SAS-4, SAS-4.1

The Application Reference Model in Figure 4-1 **Application reference model**
Figure 4- shows the high-speed data interface between an ASIC (SerDes) and the module. A duplex LC fiber connector can be used for the optical interface.

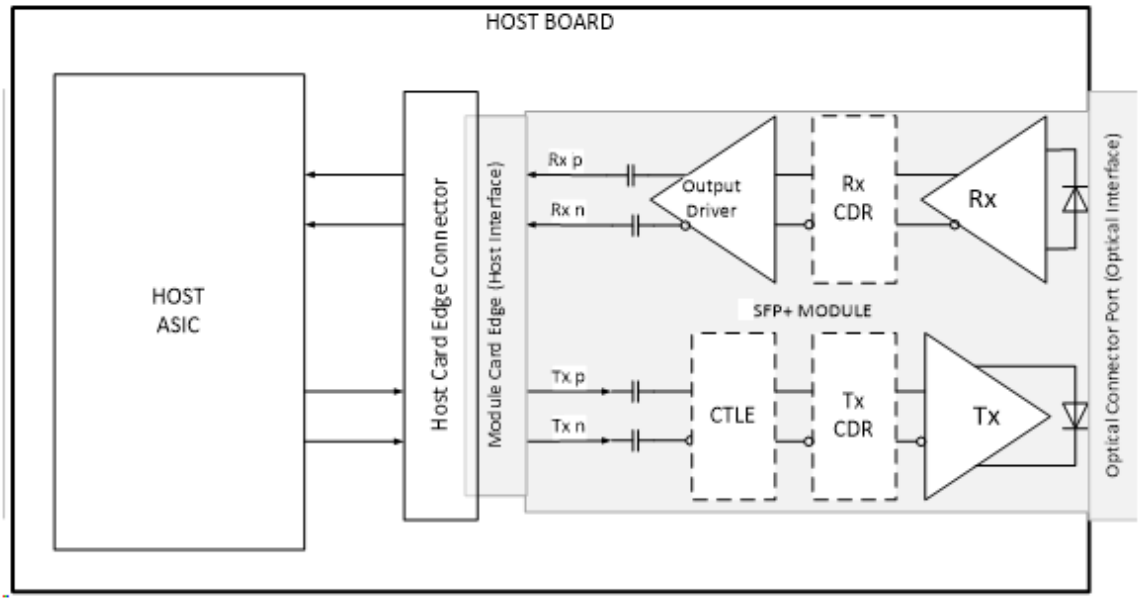

Figure 4-1 Application reference model

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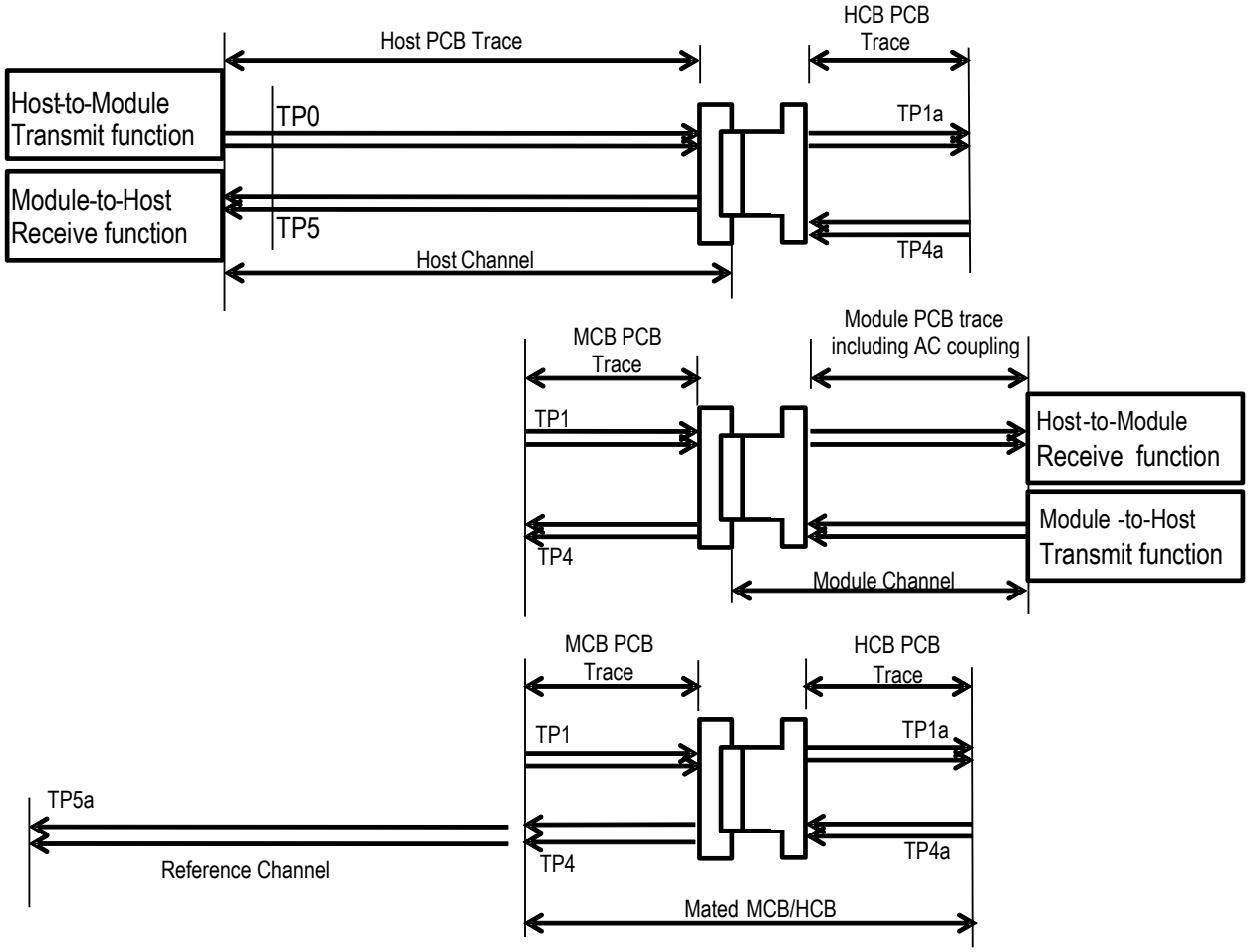

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6. Power Supply Requirements

The module host has two 3.3 V power contacts, one supplying the module transmitter voltage (VccT) and the other supplying the module receiver voltage (VccR).
SFP+ module maximum power consumption shall meet one of the following power classes:

Table 6-1 SFP+ Module Power Classes

Power Class	Maximum power consumption per module (W)
1	1.0
2	1.5
3	2.0
4	3.5
5	5.0
6	reserved
7	reserved
8	>5W (Note)
Note: For Power Class 8, maximum power consumption is declared by the module in SFF-8472, Page 02h, Byte 66 or CMIS, Page 00h, Byte 201. Maximum power is limited by current rating of power supply pins.	

To avoid exceeding system power supply limits and cooling capacity, all modules at power up shall operate with up to 1.0 W by default. Hosts supporting higher Power Level operation may enable a higher Power Level module through the 2-wire interface. Higher Power Level modules shall advertise their power level in Page 00h, Byte 64 in SFF-8472 or Page 00h, Byte 200 in CMIS.

The maximum power level is allowed to exceed the classified power level for 500 ms following hot insertion or power up, or High Power Level authorization, however the current is limited to values given by Table 6-2 and illustrated in Figure 6-16-.
At host power up the host shall supply VccT and VccR to the module within 100 ms of each other.

6.1 Module Power Supply Requirements

SFP+ module operates from the host supplied VccT and VccR. To protect the host and system operation, each SFP+ module during hot plug and normal operation shall follow the requirements listed in Table 6-2 and illustrated by Figure 6-16-. The requirements for current apply to the current through each inductor of Figure A-8-10 while the power supply voltages are defined at the SFP+ connector.

6.1.1 Host Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than 25 mV in the frequency range 40 Hz to 10 MHz, according to the methods of 1.1.1.1.1.1A.1.1.

6.1.2 Module Power Supply Noise Output

The module shall generate less than 30 mV RMS noise at point X of Figure A-8-10 in the frequency range 10Hz to 10MHz, according to the methods of 1.1.1.1.1.1A.1.2.

6.1.3 Power Supply Noise Tolerance

SFP+ modules shall meet all electrical requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 6-2 swept from 10 Hz to 10 MHz according to the methods of 1.1.1.1.1.1A.1.3. This emulates the worst-case noise of the host.
It is also desirable for a module and host to each tolerate a degree of random or semi-random noise on both VccT

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1 and VccR simultaneously, but the characteristics of this noise are beyond the scope of this document.

2 **Table 6-2 SFP+ Module Power Supply Requirements**

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccT, VccR including ripple, droop and noise below 100 kHz[1]		3.135	3.3	3.465	V
Host RMS noise output 40 Hz to 10 MHz (eN_Host)				25	mV
Module RMS noise output 10 Hz to 10 MHz				30	mV
Power supply noise tolerance including ripple (peak-to-peak)	PSNR_Mod	66			mV
Module inrush - instantaneous peak duration	T_ip	-	-	50	µs
Module inrush - initialization time	T_init	-	-	500	ms
Power Class 1 module and Low Power Mode for other modules					
Power consumption	P_1	-	-	1.0	W
Instantaneous peak current at hot plug[2,3,5]	Icc_ip_1	-	-	400	mA
Sustained peak current at hot plug[2,3]	Icc_sp_1	-	-	330	mA
Steady state current	Icc_1	-	-	289	mA
High Power Mode Power Class 2 module					
Power consumption[4]	P_2	-	-	1.5	W
Instantaneous peak current at hot plug[2,3,5]	Icc_ip_2	-	-	600	mA
Sustained peak current at hot plug[2,3]	Icc_sp_2	-	-	495	mA
Steady state current	Icc_2	-	-	433	mA
High Power Mode Power Class 3 module					
Power consumption[4]	P_3	-	-	2.0	W
Instantaneous peak current at hot plug[2,3,5]	Icc_ip_3	-	-	800	mA
Sustained peak current at hot plug[2,3]	Icc_sp_3	-	-	660	mA
Steady state current	Icc_3	-	-	577	mA
High Power Mode Power Class 4 module					
Power consumption[4]	P_4	-	-	3.5	W
Instantaneous peak current at hot plug[2,3,5]	Icc_ip_4	-	-	1400	mA
Sustained peak current at hot plug[2,3]	Icc_sp_4	-	-	1155	mA
Steady state current	Icc_4	-	-	1010	mA
High Power Mode Power Class 5 module					
Power consumption[4]	P_5	-	-	5	W
Instantaneous peak current at hot plug[2,3,5]	Icc_ip_5	-	-	1600	mA
Sustained peak current at hot plug[2,3]	Icc_sp_5	-	-	1320	mA
Steady state current	Icc_5	-	-	1443	mA
High Power Mode Power Class 8 module					
Power consumption[4,6]	P_8	-	-	>5	W
Instantaneous peak current at hot plug[2,3,5]	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current at hot plug[2,3]	Icc_sp_8	-	-	P_8/3.03	A
Steady state current[5]	Icc_8	-	-		mA

1: Measured at VccT and VccR at the input to the connector on the host board reference to Vee. Droop is any temporary drop in voltage of the power supply such as that caused by plugging in another module or when enabling another module to High Power Mode.
2: The requirements for current apply to the current through each inductor of Figure A-8-10.
3: The maximum currents are the allowed currents for each power supply VccT or VccR, therefore the total module peak currents can be twice this value. The instantaneous peak current is allowed to exceed the specified maximum current capacity of the connector contact for a short period, see Figure 6-16-.
4: Maximum module power consumption shall not exceed 1.0 W from 500ms after power up until High Power mode operation is enabled. The module must stay within its advertised power class for all supply voltages.
5: Not to exceed the sustained peak limit for more than 50 us; may exceed this limit for shorter durations.
6: Maximum module power consumption is advertised in SFF-8472, Page 02h, Byte 66 or CMIS, Page 00h, Byte 201.

4

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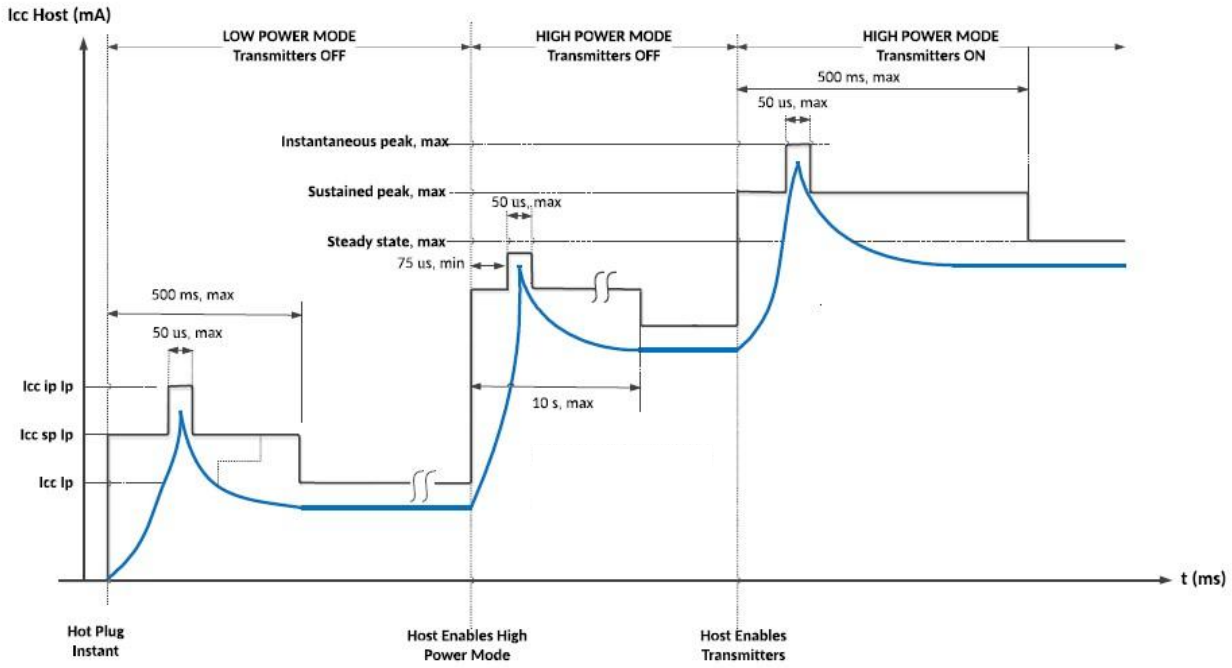

Figure 6-1 Instantaneous and Sustained Peak Current for VccT or VccR

6.2 ESD

The SFP+ module and host SFI contacts (High Speed Contacts) shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.
The SFP+ module and all host contacts with exception of the SFI contacts (High Speed Contacts) shall withstand 2 kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The SFP+ module shall meet ESD requirements given in EN61000-4-2, criterion B test specification such that units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case.

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7. Electrical Specification

7.1 Introduction

This specification has several enhancements over the classic SFP interface (INF-8074i), but the SFP+ host can be designed to also support most legacy SFP modules. Pin functions were also updated for modules using CMIS memory specification. SFP+ 2-wire interface electrical and timing specifications are defined in Section 0, and the SFP+ 2-wire interface management and register map are defined by SFF-8472 or CMIS.

7.2 Host Connector Definition

The SFP+ host connector is a 0.8 mm pitch 20 position improved connector or stacked connector with equivalent electrical performance.
The host card edge connectors are specified by SFF-8071 for SFPs up to 56Gbps and SFF-TA-1031 for SFP-112.

7.2.1 Host PCB and Module Contact Assignments for SFP/SFP+ managed by SFF-8472

Host PCB contact assignment is shown in Figure 7-17- and contact definitions are given in Table 7-1. SFP+ module contacts mate with the host in the order of ground, power, followed by signal as illustrated by Figure 7-2 and the contact sequence order listed in Table 7-1.

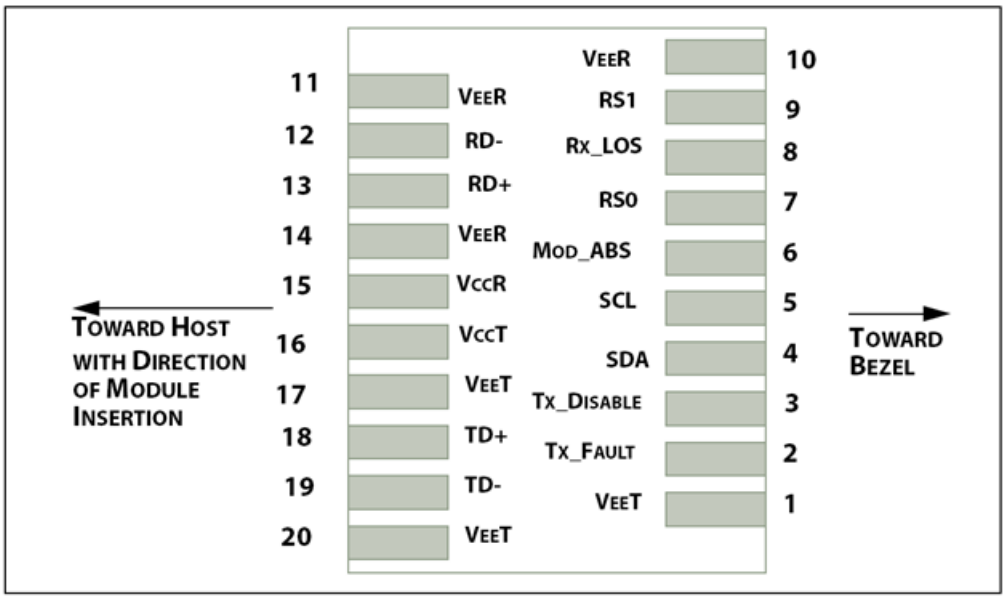

Figure 7-1 Host PCB SFP/SFP+ pad assignment top view

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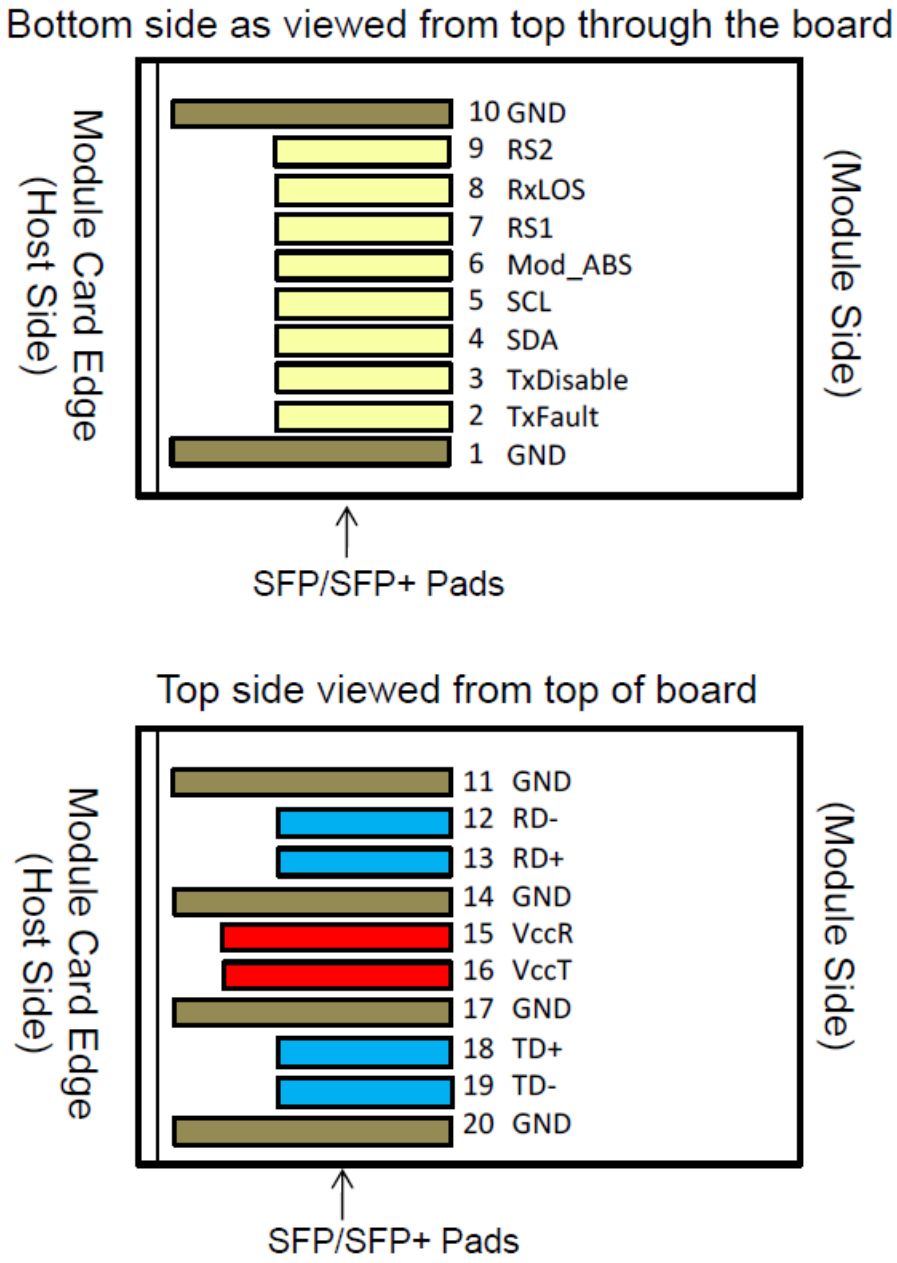

Figure 7-2 SFP+ Module Contact Assignment

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Table 7-1 SFP+ Module and Host Electrical Contact Definition

Contact	Logic[1]	Symbol	Power Sequence	Name/Description
case		Case[2]		Module case
1		VeeT[3]	1st	Module Transmitter Ground
2	LVTTL-O	Tx_Fault[4]	3rd	Module Transmitter Fault
3	LVTTL-I	Tx_Disable[5]	3rd	Transmitter Disable; Turns off transmitter laser output
4	LVTTL-I/O	SDA[6]	3rd	2-wire Serial Interface Data (Same as MOD-DEF2 in INF-8074i)
5	LVTTL-I/O	SCL[6]	3rd	2-wire Serial Interface Clock (Same as MOD-DEF1 in INF-8074i)
6		Mod_ABS[7]	3rd	Module Absent, connected to VeeT or VeeR in the module
7	LVTTL-I	RS0[8]	3rd	Rate Select 0, optionally controls SFP+ module receiver.
8	LVTTL-O	Rx_LOS[4]	3rd	Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect)
9	LVTTL-I	RS1[8]	3rd	Rate Select 1, optionally controls SFP+ module transmitter
10		VeeR[3]	1st	Module Receiver Ground
11		VeeR[3]	1st	Module Receiver Ground
12	CML-O	RD-	3rd	Receiver Inverted Data Output
13	CML-O	RD+	3rd	Receiver Non-Inverted Data Output
14		VeeR[3]	1st	Module Receiver Ground
15		VccR	2nd	Module Receiver 3.3 V Supply
16		VccT	2nd	Module Transmitter 3.3 V Supply
17		VeeT[3]	1st	Module Transmitter Ground
18	CML-I	TD+	3rd	Transmitter Non-Inverted Data Input
19	CML-I	TD-	3rd	Transmitter Inverted Data Input
20		VeeT[3]	1st	Module Transmitter Ground

1. Labeling as inputs (I) and outputs (O) are from the perspective of the module
2. The case makes electrical contact to the cage before any of the board edge contacts are made.
3. The module signal ground contacts, VeeR and VeeT, should be isolated from the module case.
4. This contact is an open collector/drain output contact and shall be pulled up on the host. Pull ups can be connected to one of several power supplies, however the host board design shall ensure that no module contact has voltage exceeding module VccT/R + 0.5 V.
5. Tx_Disable is an input contact with a 4.7 kΩ to 10 kΩ pullup to VccT inside the module.
6. See 0
7. See 0
8. For SFF-8431 rate select definition see 0. (If implementing SFF-8079 contacts 7 and 9 in SFF-8431 are used for AS0 and AS1 respectively).

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7.2.2 Host PCB and Module Contact Assignments for SFP112/SFP224 managed by CMIS

Host PCB contact assignment is shown in Figure 7-3**Figure 7-** and contact definitions are given in Table 7-2. SFP112/224 module contacts mate with the host in the order of ground, power, followed by signal as illustrated by Figure 7-4**Figure 7-** and the contact sequence order listed in Table 7-2.

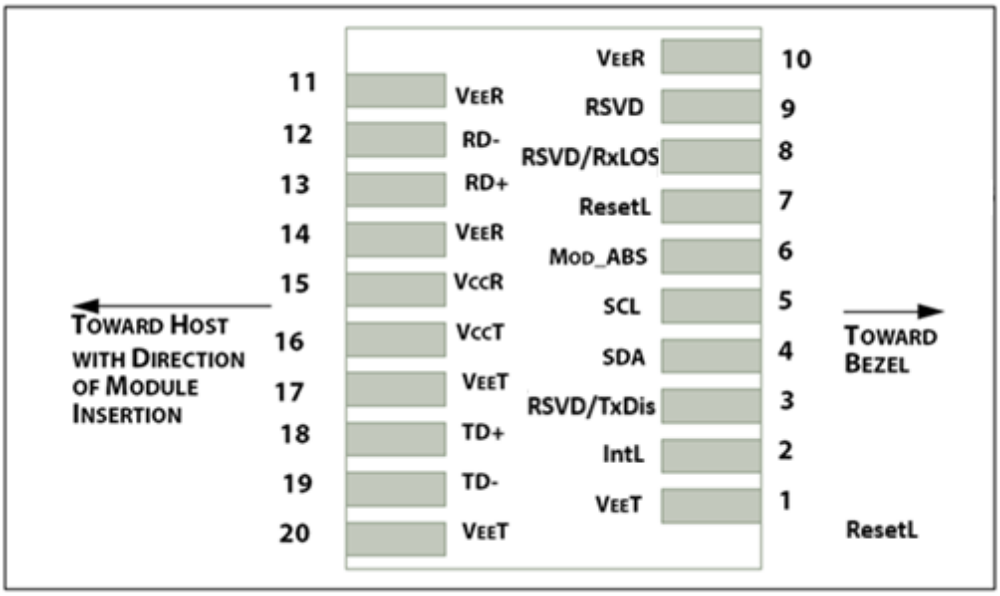

Figure 7-3 Host PCB SFP112/SFP224 pad assignment top view

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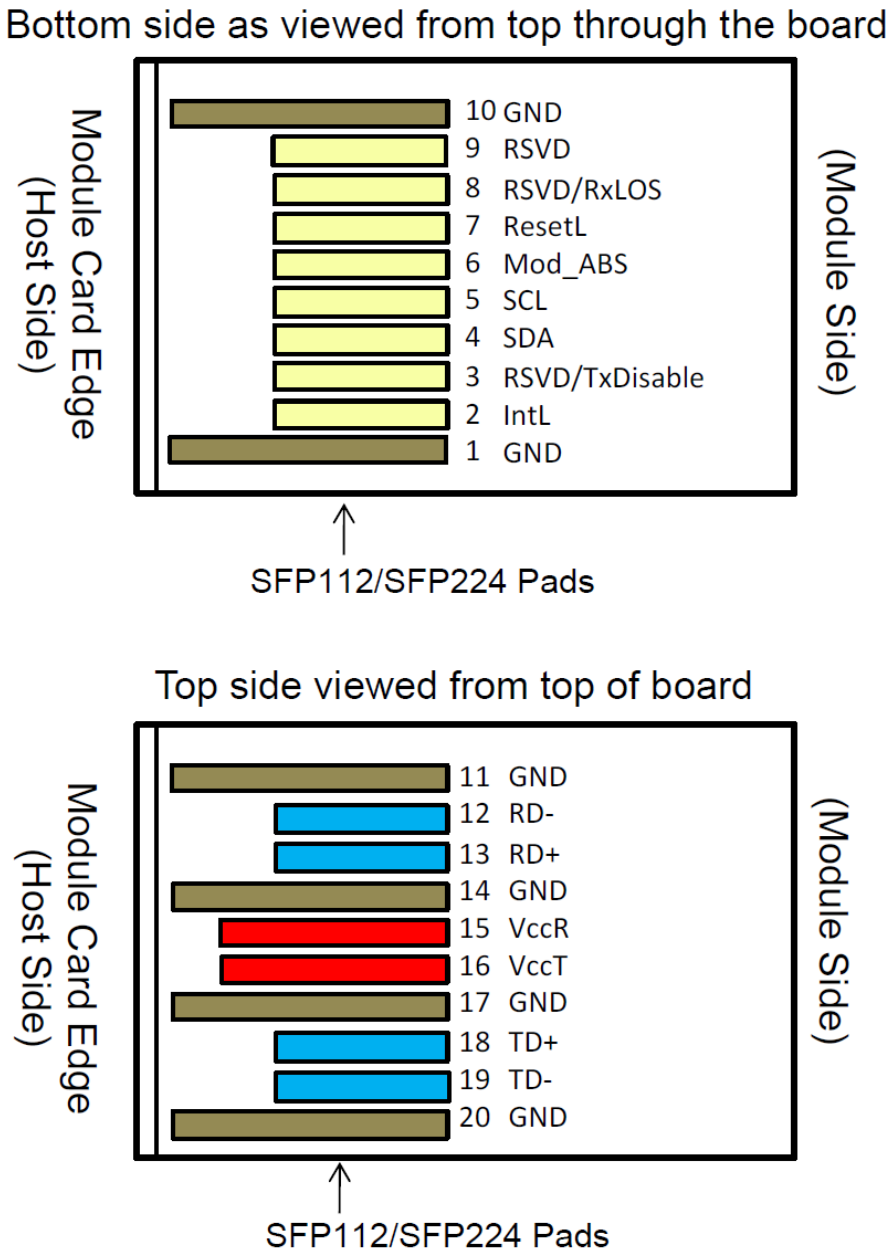

Figure 7-4 SFP112/SFP224 Module Contact Assignment

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Table 7-2 SFP112/SFP224 Module and Host Electrical Contact Definition

Contact	Logic[1]	Symbol	Power Sequence	Name/Description
case		Case[2]		Module case
1		VeeT[3]	1st	Module Transmitter Ground
2	LVTTL-O	INTL	3rd	Module Fault
3	LVTTL-I	RSVD/Tx_Dis[5]	3rd	Reserved or Transmitter Disable
4	LVTTL-I/O	SDA[6]	3rd	2-wire Serial Interface Data (Same as MOD-DEF2 in INF-8074i)
5	LVTTL-I/O	SCL[6]	3rd	2-wire Serial Interface Clock (Same as MOD-DEF1 in INF-8074i)
6		Mod_ABS[7]	3rd	Module Absent, connected to VeeT or VeeR in the module
7	LVTTL-I	ResetL	3rd	Module Reset
8	LVTTL-O	RSVD/Rx_LOS[4]	3rd	Reserved or Receiver Loss of Signal Indication
9	LVTTL-I	RSVD	3rd	
10		VeeR[3]	1st	Module Receiver Ground
11		VeeR[3]	1st	Module Receiver Ground
12	CML-O	RD-	3rd	Receiver Inverted Data Output
13	CML-O	RD+	3rd	Receiver Non-Inverted Data Output
14		VeeR[3]	1st	Module Receiver Ground
15		VccR	2nd	Module Receiver 3.3 V Supply
16		VccT	2nd	Module Transmitter 3.3 V Supply
17		VeeT[3]	1st	Module Transmitter Ground
18	CML-I	TD+	3rd	Transmitter Non-Inverted Data Input
19	CML-I	TD-	3rd	Transmitter Inverted Data Input
20		VeeT[3]	1st	Module Transmitter Ground

1. Labeling as inputs (I) and outputs (O) are from the perspective of the module
2. The case makes electrical contact to the cage before any of the board-edge contacts are made.
3. The module signal ground contacts, VeeR and VeeT, should be isolated from the module case.
4. This dual function is controlled by register 129, page 05h in the CMIS memory map, The control is defined in CMIS-FF Implementation Agreement. When used as an RxLOS indicator, this contact is an open collector/drain output contact and shall be pulled up on the host.
5. The dual function is controlled by register 129, page 05h in the CMIS memory map. The control is defined by CMIS-FF Implementation Agreement. When used as a Tx_Disable, it is an input contact with a 4.7 kΩ to 10 kΩ pullup to VccT inside the module.
6. See 0
7. See 0

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8.

8. SFP+ 2-Wire Interface

8.1 Introduction

The SFP+ management interface is a 2-wire interface, similar to I2C. SFP+ management memory map is specified by SFF-8472. Management memory map for SFP112 and SFP224 is specified by CMIS. Nomenclature for all registers more than 1 bit long is MSB...LSB (MSB transmitted first).

8.2 2-Wire Interface Electrical Specifications

The SFP+ 2-wire interface specifications are given in Table 8-1. These specifications ensure compatibility between host controllers and SFP+ SCL/SDA lines and compatibility with I2C. All voltages are referenced to VeeT.

Table 8-1 2-wire Interface Electrical Specification

Parameter	Symbol	Max	Max	Unit	Conditions
Host 2-wire Vcc	Vcc_Host_2w[1]	3.14	3.46	V	
SCL and SDA	VOL[3]	0.0	0.40	V	Rp2w[2] pulled toVcc_Host_2w
	VOH[3]	Vcc_Host_2w - 0.5	Vcc_Host_2w + 0.3	V	Rp2w[2] pulled to Vcc_Host_2w
SCL and SDA	VIL[3]	-0.3	VccT * 0.3	V	
	VIH[3]	VccT * 0.7	VccT + 0.5	V	
Input current on the SCL/SDA contacts	Il	-10	10	uA	
Capacitance on SCL/SDA I/O contact	Ci[4]		14	pF	
Total bus capacitance for SCL/SDA	Cb[5]		100	pF	For 400 kHz, 3.0 kΩ Rp2w, max For 100 kHz, 8.0 kΩ Rp2w, max For 1000 kHz, see Figure 8-1
			290	pF	At 400 kHz, 1.1 kΩ Rp2w, max At 100 kHz, 2.75 kΩ Rp2w, max For 1000 kHz, see Figure 8-1

Note 1: The Host 2-wire Vcc is the voltage used for resistive pull ups for the 2-wire interface
Note 2: Rp2w is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to any one of several power supplies, however the host board design shall ensure that no module contact has voltage exceeding module VccT/R + 0.5 V nor requires the module to sink more than 3.0 mA current.
Note 3: These voltages are measured on the other side of the connector to the device under test.
Note 4: Ci is the capacitance looking into the module SCL and SDA contacts
Note 5: Cb is the total bus capacitance on the SCL or SDA bus.

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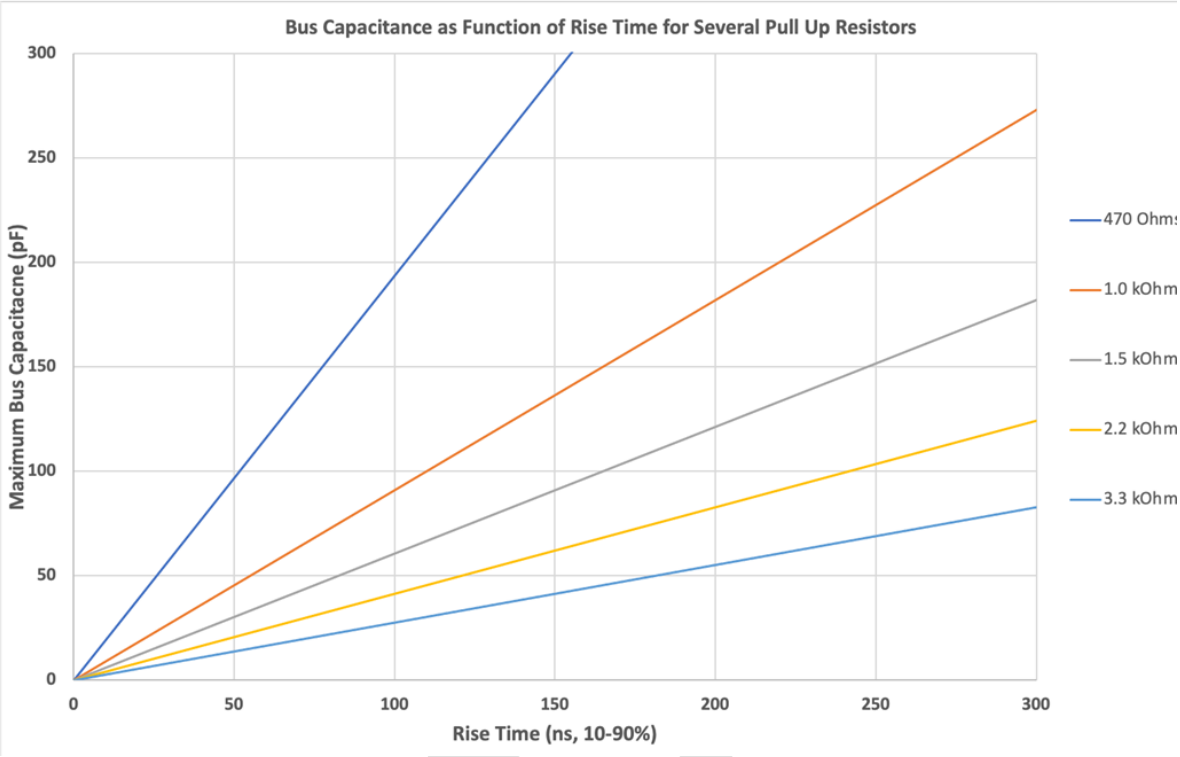

Figure 8-1 SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

8.3 SFP+ 2-Wire Timing Diagram

SFP+ 2-wire bus timing is shown in Figure 8-2Figure 8-Figure 12 and the detail of clock stretching is shown in Figure 8-3Figure 8-Figure 13. SFP+ 2-wire timing specifications are given in Table 8-2Table 8.
The 2-wire serial interface addresses of the SFP+ module are 1010000x (A0h) and 1010001x (A2h).

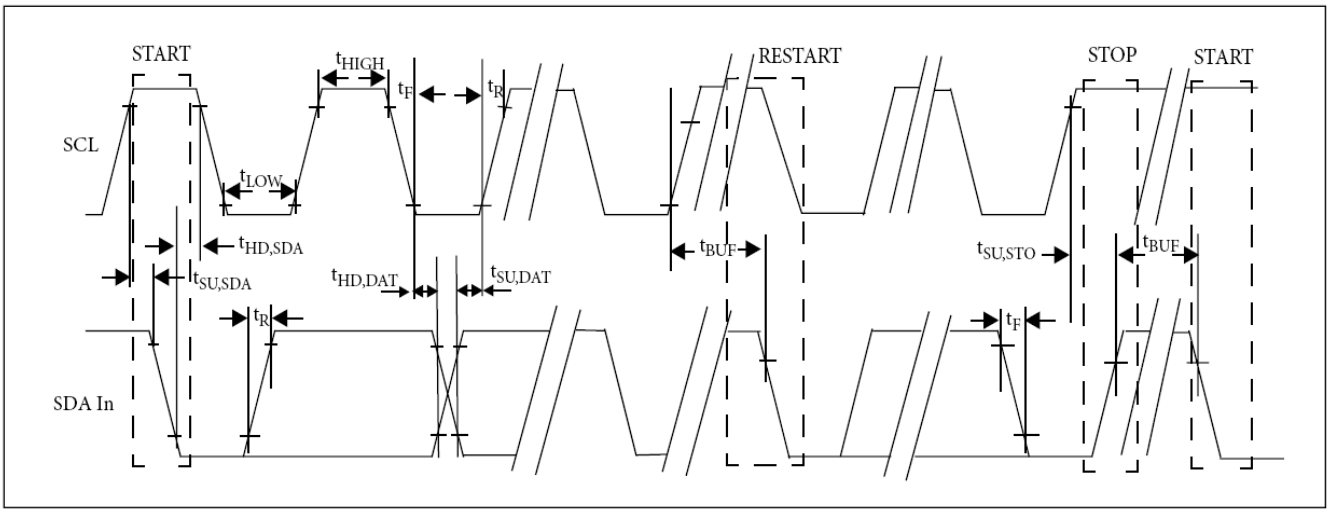

Figure 8-2 2-Wire Timing Diagram

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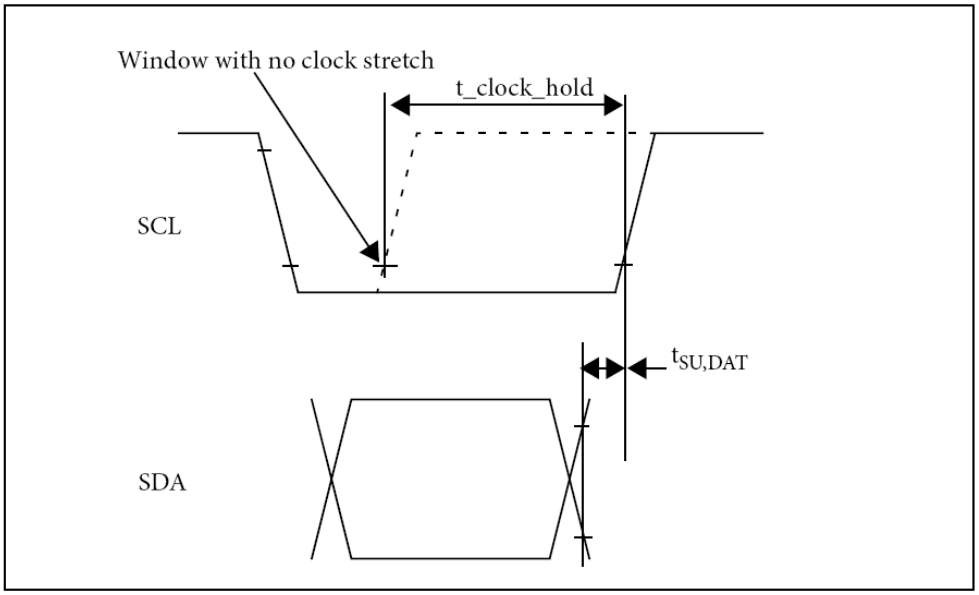

Figure 8-3 Detail of Clock Stretching

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Table 8-2 SFP+ 2-Wire Timing and Memory Transaction Timing Specifications

		Fast Mode (SCL 100/400 kHz)		Fast Mode+ (SCL 1 MHz)			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Clock Frequency	fSCL	0	400	0	1000	kHz	Module shall operate with fSCL up to 100 kHz without requiring clock stretching. The module may clock stretch with fSCL greater than 100 kHz and up to 1 MHz.
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		20		µs	Between STOP and START and between ACK and Restart
START Hold Time	tHD.STA	0.6		0.26		µs	
START Set-up Time	tSU.STA	0.6		0.26		µs	
Data in Hold Time	tHD.DAT	0		0		µs	
Data in Set-up Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300/ 1000		120	ns	From (VIL, MAX-0.15) to (VIH, MIN +0.15)
Input Fall Time	tF		300		120	ns	From (VIH, MIN + 0.15) to (VIL, MAX - 0.15)
STOP Set-up Time	tSU.STO	0.6		0.26		µs	
STOP Hold-up Time	tHD_STO	0.6		0.26		µs	
Clock Holdoff Time (Clock Stretching)	T_clock_ hold		500		500	µs	Maximum time the module may hold SCL low before completing a read or write operation
Aborted sequence – bus release	Deselect_ Abort		2		2	ms	Delay from a host de-asserting ModSelL (at any point in a 2-wire interface sequence) to the module releasing SCL and SDA
ModSelL Setup Time[1]	tSU. ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host-initiated 2-wire interface sequence.
ModSelL Hold Time[1]	tHD. ModSelL	0.01[2] 0.5[3]		2		ms	ModSelL Hold Time is the delay from completion of 2-wire interface sequence to ModSelL rising edge.
Complete single or sequential write to non-volatile registers	tWR		40[2] 80[3]		80	ms	Time to complete a single or sequential write of up to four bytes to non-volatile registers.
Accept a single or sequential write to volatile memory	tNACK		10		10	ms	Time to complete a single or sequential write to volatile registers.
Time to complete a change of memory page or bank	tBPC		10		10	ms	Time to complete a change of memory page or bank.
Endurance (Write Cycles)		10k		10k		cycles	Module Case Temperature = 70 ºC

Note 1: Meeting the setup and hold times specifications are required for all modules. In CMIS transceivers, once the module has initialized the management interface, management registers can be read to determine alternate ModSelL set up and hold times. See CMIS 8.4.5, Durations Advertisement.
Note 2: For transceivers implementing SFF-8472 to complete a Write up to 4 bytes
Note 3: For transceivers implementing CMIS or to complete a Write up to 8 bytes

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1 **8.4**

2 ## 8.4 Device Addressing and Operation

Serial Clock (SCL)	The host supplied SCL input to SFP+ transceivers is used to positively edge clock data into each SFP+ device and negative edge clock data out of each device. The SCL line may be pulled low by an SFP+ module during clock stretching.
Serial Data (SDA)	The SDA contact is bi-directional for serial data transfer. This contact is open-drain or open-collector driven and may be wire-ORed with other open-drain or open collector devices with different device addresses, provided the total bus capacitance meets the requirement of Table 8-1and the Serial Clock (SCL) is also wire-ORed.
Controller/Target	SFP+ transceivers operate only as target devices. The host must provide a bus controller for SCL and initiate all read/write communication.
Device Address	Each SFP+ is hard wired at the device addresses A0h and A2h. See SFF-8472 for memory structure within each transceiver.
Clock and Data Transitions	The SDA contact is normally pulled high with an external device. Data on the SDA contact may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the SFP+ in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.
START Condition	A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.
STOP Condition	A low-to-high transition of SDA with SCL high is a STOP condition.
Acknowledge	After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host shall be acknowledged by SFP+ transceivers. Read data bytes transmitted by SFP+ transceivers shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.
Non-acknowledge (NACK)	When a target is unable to receive or transmit, because, e.g., it is performing a higher priority function, the data line shall be left high by the target. A NACK is generated when the target leaves the data line high during the ACK clock pulse. The controller can then generate either a STOP condition to abort the transfer or a repeated START condition to start a new transfer. When in a transfer, a controller-receiver must signal the end of data to the target-transmitter by not generating an acknowledge on the last byte clocked out of the target. A NACK is generated when the controller leaves the data line High during the ACK clock pulse. The target-transmitter must release the data line to permit the controller to generate a STOP or repeated START condition.
Memory (Management Interface) Reset	After an interruption in protocol, power loss or system reset the SFP+ management interface can be reset. Memory reset is intended only to reset the SFP+ transceiver management interface (to correct a hung bus). No other transceiver functionality is implied. 1. Clock up to 9 cycles. 2. Look for SDA high in each cycle while SCL is high. 3. Create a START condition as SDA is high.
Device Addressing	SFP+ devices require an 8 bit device address word following a start condition to enable a read or write operation. The device addresses to select A0h or A2h are shown in Table 8-34. This is common to all SFP+ devices.

3

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Table 8-3 SFP+ Device Address Word

Address							Address Select	R/W select
A0h	1	0	1	0	0	0	0	x
A2h	1	0	1	0	0	0	1	x
	MSB							LSB
The LSB of the device address word is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low.								

8.5 Read/Write Functionality

The methods for reading from and writing to the two different SFP+ addresses A0h and A2h are described in this section. They are identical for the two different addresses except that the appropriate address is used for each read and write. For simplicity in the figures the address is labelled 101000x where the x is 0 for the A0h address and 1 for the A2h address. Note that the address here is only seven bits. In order to complete the full 8 bit byte a one or zero is added to the end of the address depending on whether a read or a write operation is taking place.

8.5.1 Memory Address Counter (Read and Write Operations)

SFP+ devices maintain two internal data word address counters one for each address. These counters contain the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the transceiver. This address stays valid between operations as long as SFP+ power is maintained. The address 'roll over' during read and write operations is from the last byte of the 256 byte memory page to the first byte of the same page.

8.5.2 Read Operations (Current Address Read)

A current address read operation requires only that the device address read word (10100001 or 10100011) be sent, Figure 8-. Once acknowledged by the SFP+, the current address data word is serially clocked out. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

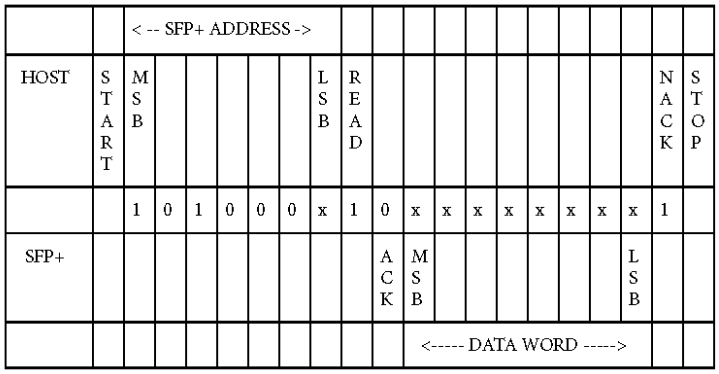

Figure 8-4 Current Address Read Operation

8.5.3 Read Operations (Random Read)

A random read operation requires a 'dummy' write operation to load in the target byte address Figure 8-. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000 or 10100010) and acknowledged by the SFP+. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001 or 10100011). The SFP+ acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

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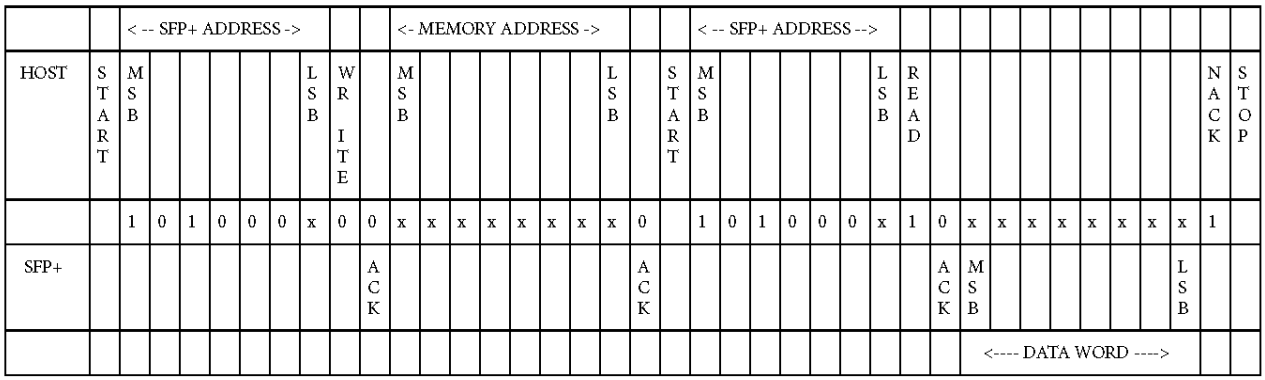

Figure 8-5 Random Read

8.5.4 Read Operations (Sequential Read)

Sequential reads are initiated by either a current word address read Figure 8-68- or a random address read Figure 8-78-. To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the SFP+ receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

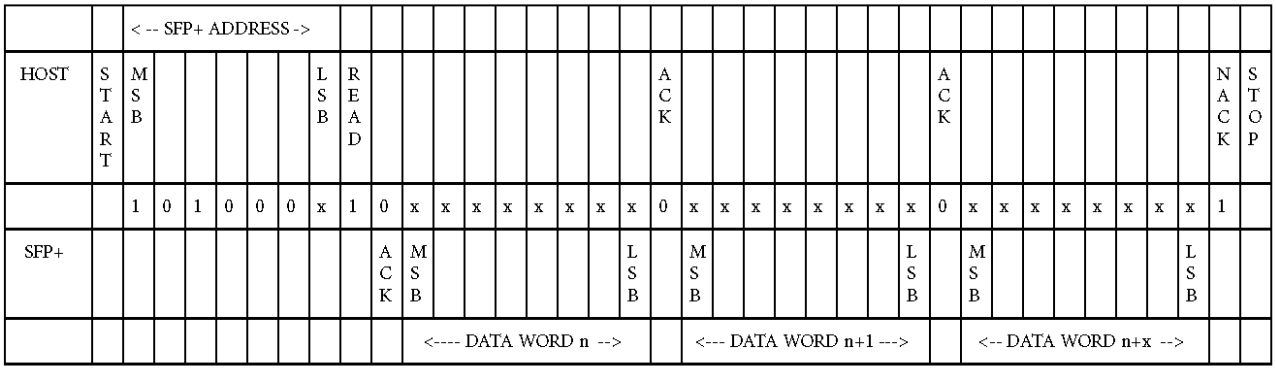

Figure 8-6 Sequential Address Read Starting at Current Word Address

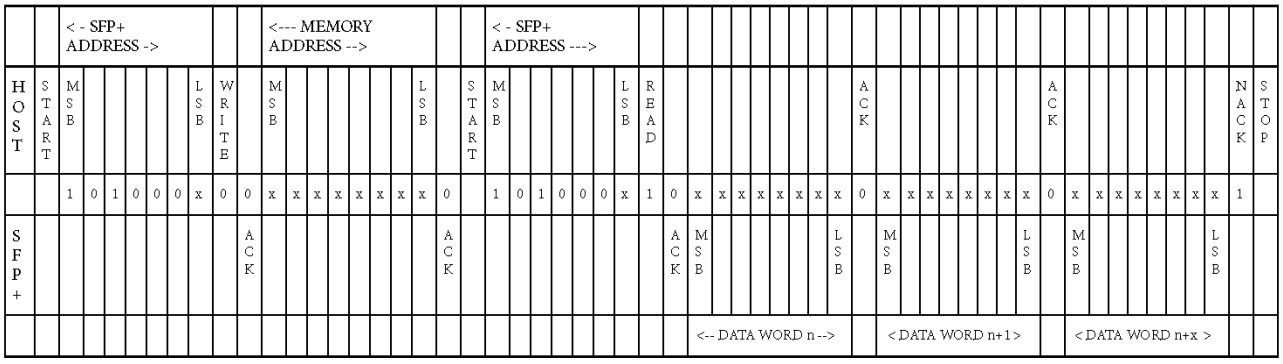

Figure 8-7 Sequential Address Read Starting with Random Read

8.5.5 Write Operations (Byte Write)

A write operation requires an 8-bit data word address following the device address write word (10100000 or 10100010) and acknowledgement Figure 8-88-. Upon receipt of this address, the SFP+ shall again respond with a zero (ACK) to acknowledge and then clock in the first 8 bit data word. Following the receipt of the 8 bit data word, the SFP+ shall output a zero (ACK) and the host controller must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per

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the I2C specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the SFP+ enters an internally timed write cycle, tWR, to internal memory. The SFP+ disables its management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that I2C 'Combined Format' using repeated START conditions is not supported on SFP+ write commands.

		< -- SFP+ ADDRESS -->									<-- MEMORY ADDRESS ->									<----- DATA WORD ---->									
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	x	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
SFP+										ACK									ACK									ACK	

Figure 8-8 SFP+ Write Byte Operation

8.5.6 Write Operations (Sequential Write)

SFP+ shall support up to an 8 sequential byte write without repeatedly sending SFP+ address and memory address information. A 'sequential' write is initiated the same way as a single byte write, but the host controller does not send a stop condition after the first word is clocked in. Instead, after the SFP+ acknowledges receipt of the first data word, the host can transmit up to seven more data words. The SFP+ shall send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that I2C 'combined format' using repeated START conditions is not supported on SFP+ write commands.

		<--- SFP+ ADDRESS --->									<--- MEMORY ADDRESS -->									<--DATA WORD 1 -->									<--- DATA WORD 2 -->									<------ DATA WORD 3 ------>									<------ DATA WORD 4 ------>									
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		MSB							LSB		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	x	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
SFP+										ACK									ACK									ACK									ACK									ACK									ACK	

Figure 8-9 Sequential Write Operation

8.5.7 Write Operations (Acknowledge Polling)

Once the SFP+ internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the SFP+ respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

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A. Test Methodology and Measurement (Normative)

A.1 Power Supply Testing Methodology

This section defines power supply noise output as given in 6.1.1 and 6.1.2, and power supply noise tolerance as in 6.1.3.

The reference power supply filter shown in Figure A-8-10 is provided for module testing, including power supply tolerance testing. This filter will meet the noise filtering requirements in most host systems. Other filtering implementations or local regulation may be used to meet the power noise output requirements described in 6.1.1 and 6.1.2.

For each Vcc, the sum of the equivalent series resistances of the 1.0 µH inductor, the 22 µF capacitor and the damping resistor is 0.5 Ω. This resistance is desirable in actual host filters as well as in the reference filter; however, any voltage drop across a filter network on the host is counted against the host VccT and VccR accuracy specification in Table 6-2.

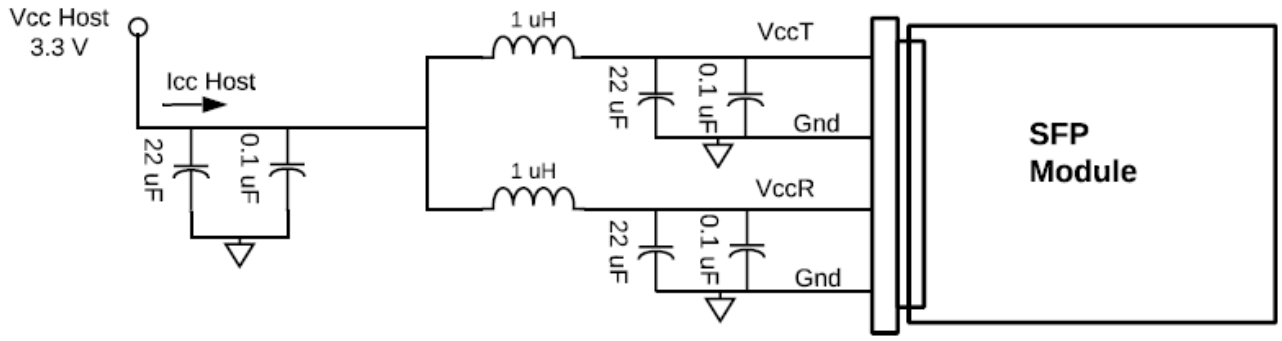

Figure A-8-10 Module Compliance Board Power Supply Filters

A.1.1 Host Power Supply Noise Output

The noise output of a Vcc supply of a host is defined with a resistive load that draws the maximum rated power for the advertised power class, connected between one Vcc contact and Vee, in place of the SFP+ module. This may be implemented using constant current sink circuits attached to each host supply filter output. When the noise on VccT is being measured, VccR is left open circuit, and vice versa. The AC voltage spectrum is measured at the module side of the SFP+ connector. The noise power spectrum is divided by the truncated response of the reference filter and then integrated from 10 Hz to 10 MHz and converted to a voltage. This function is illustrated in the equation below and Figure A-8-11. The specification limit is given in 6.1.1. The test is performed with all other portions of the host board/system active. Hosts with multiple SFP+ modules shall test ports one at a time, with active SFP+ in all the remaining ports.

$$H(f) = a \times (log10(f))^4 + b \times (log10(f))^3 + c \times (log10(f))^2 + d \times (log10(f)) + e$$

The frequency response of the truncated function is illustrated in Figure A-8-11 and the coefficients a, b, c, d, and e for the 5 frequency bands are defined in Table A-41.. The figure shows the original function as specified in SFF-8431 and the scaled function with inductor value of 1 µH.

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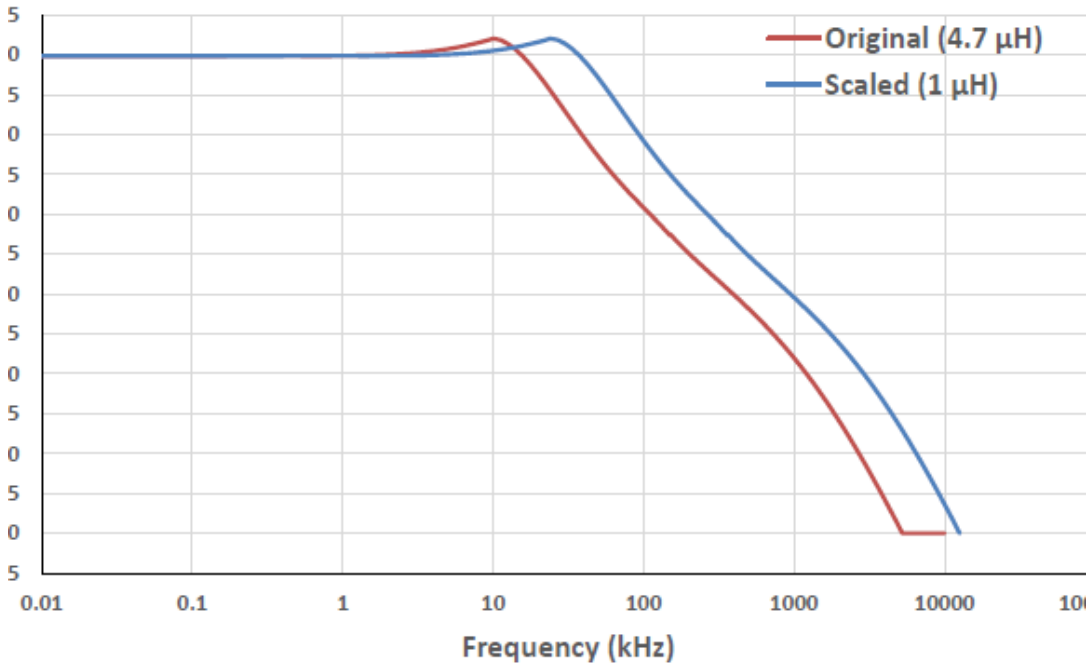

Figure A-8-11 Truncated Transfer Response for Host Board Power Supply Noise Output measurement

Table A-4 Truncated Filter Response Coefficients

Frequency (f)	a	b	c	d	e
10 Hz ≤ f < 240.2 Hz	0	0	0	0	-0.1
240.2 Hz ≤ f < 24.03 kHz	0.3784	-3.6045	12.694	-19.556	11.002
24.03 kHz ≤ f < 360.4 kHz	-22.67038	430.392	-3053.779	9574.26	-11175.98
360.4 kHz ≤ f ≤ 12.6 MHz	3.692166	-91.467	838.80	-3400.38	5139.285
Note: Note: This table differs from SFF-8431 Table 32 in two ways: the frequency ranges differ because the inductor value in this specification is 1 µH, not 4.7 µH as in SFF-8431; and the sign of the value -91.467 in Column b differs, correcting an error.					

NOTES: As a lightly loaded power supply might generate more noise than a fully loaded supply, the host implementer may wish to assess the host power supply noise output at less than maximum current draw also. Because a small measured noise signal at high frequencies is multiplied up to give the inferred noise at virtual point X, care should be taken over the noise floor of the spectrum analyzer. Other measurement methods could be used, e.g. a measurement at a point inside the host, with appropriate consideration to any difference between the reference filter and the host's actual filter.

A.1.2 SFP+ Module Power Supply Noise Output

The module noise voltage output is defined in the frequency band 10 Hz to 10 MHz at point X in Figure A-8-12.

The module must pass module power supply noise output test in all operating modes. This test ensures the module will not couple excessive noise from inside the module back onto the host board. A power meter technique, or a spectrum analyzer technique with integration of the spectrum, may be used. The maximum allowed noise amplitude is given in 6.1.2.

A.1.3 Module Power Supply Tolerance Testing

In this test, a swept sinusoidal tone is applied at point X of Figure A-8-12 with the tolerance signal amplitude and frequency range given in 6.1.3. The AC tolerance signal is created by a circuit such as a low impedance buffer

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amplifier between the power supply and point X. The impedance of the PSU and sine wave generator is less than 0.5 Ω. The amplitude of the sine wave is calibrated at each frequency at point X with the module replaced with a 12 Ω load between Vcc and Vee.

NOTES -- It may be desirable to remove the 0.1 µF capacitors on the host side of the reference filters for this test, to reduce the power needed by the sine wave generator. The calibration of the sine wave is not expected to be significantly different if the module were in place rather than the test resistor.

Alternatively, the test may be performed separately for VccT and VccR with the other supply filter connected directly to the power supply. It is not necessary to show compliance with both separate and common Vcc modulation.

This test applies at minimum and maximum DC setpoint levels. Note that the DC level is inset to the limits in SFF-8419 Low Speed Module Electrical Specifications by the peak of the sinusoidal voltage at the input to the module (which is frequency dependent).

The source frequency is varied over the range specified by 6.1.3 to determine if any frequency causes a parameter to fall out of the specification limit. In all cases, the parameters measured shall pass the optical standards with the tone present over all frequencies specified. Parameters of interest for the transmit may include UJ, Qsq and TDP see [IEEE 802.3]. For the receive side, they include stressed sensitivity, overload, RN and Rx_LOS functions.

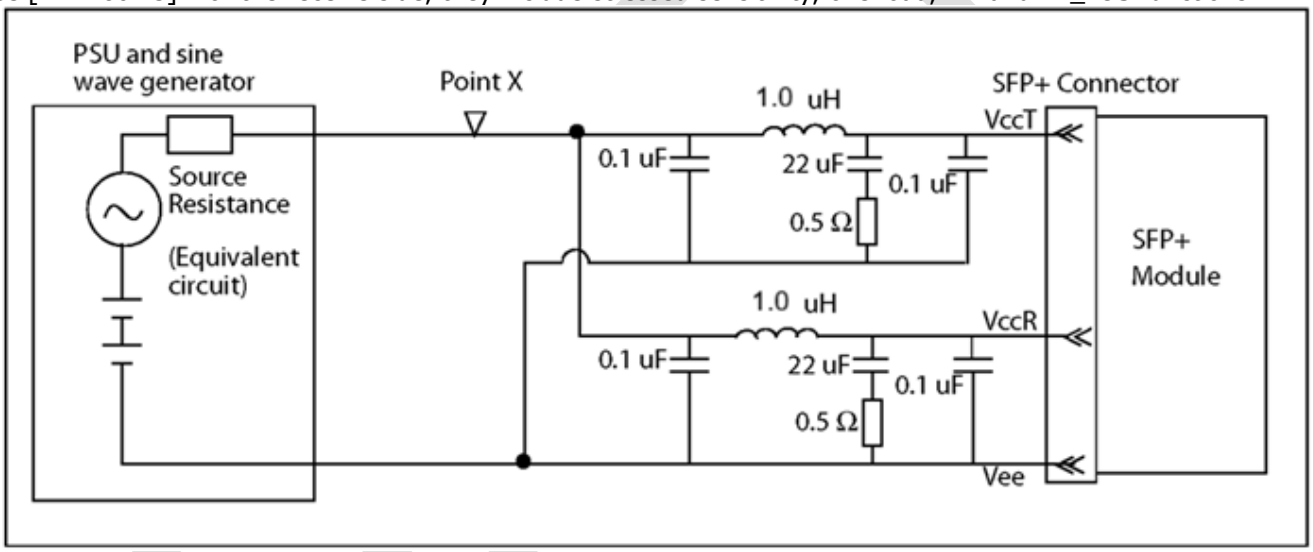

Figure A-8-12 Power Supply Noise Tolerance Test Setup

The AC voltage at node X is defined with reference to Vee. The DC voltage specification including ripple, droop and noise below 100 kHz is met at both VccT and VccR (at the SFP+ connector).

END OF DOCUMENT

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