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New Project Proposal: Reopen SFF-TA-1002

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New Project Proposal: SFF-TA-1002 R1.6

- Reopen specification for PCIe 7.0 support for Straight, RA, straddle and PCIe 6.0 support for Orthogonal. Address feedback received since last revision.
- Editor(s): Anthony Constantine
- Supporters
  1. Amphenol
  2. Foxconn
  3. Lotes
  4. Meta
  5. Micron
  6. Microsoft

New Project Proposal: SFF-TA-1002 R1.6

- Changes:
  - For straight, right angle, and straddle connector, add PCIe 7.0 electricals and mechanical changes to support if necessary w/o breaking backwards compatibility.
  - For orthogonal connector, add PCIe 6.0 electricals and mechanical changes to support if necessary w/o breaking backwards compatibility.
  - Address feedback on dimensioning (if needed).
  - Address feedback on current rating profiles (if needed).
- IP Declaration (if applicable):
  - No known new IP with these changes
- General timeline for project completion
  - Draft and review ballot tbd.
  - Approval ballot before September.

PCIe 7.0: edits

- Add electrical parameter values
- Do we need to make mechanical change (per FIT feedback)?
  - Assuming change is backwards compatible
  - Assuming change doesn't create higher DPM for loop tolerance.
  - Right-angle and Straight connectors may need to be separated due to length deltas.

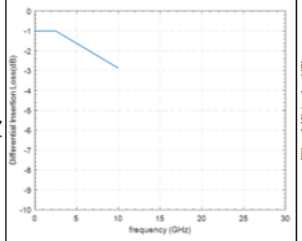
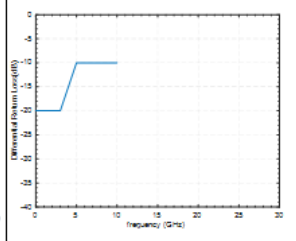
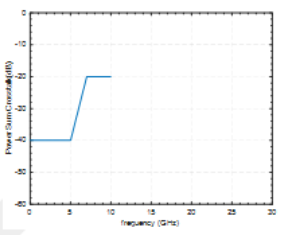
TABLE 6-7. STRAIGHT, RIGHT ANGLE AND STRADDLE MOUNT CONNECTOR SIGNAL INTEGRITY REQUIREMENTS (PCIe APPLICATIONS)

Line Rate	Insertion Loss	Return Loss	Power Sum Near End Crosstalk	Power Sum Far End Crosstalk	Intrapair Skew
8 GT/s NRZ (PCIe 3.0)	See 32GT/s NRZ values from Table 6-6				
16 GT/s NRZ (PCIe 4.0)	See 32GT/s NRZ values from Table 6-6				
32 GT/s NRZ (PCIe 5.0)	See 32GT/s NRZ values from Table 6-6				
64 GT/s PAM4 (PCIe 6.0)	≥(-0.1–0.040625*f)dB (0.01≤f≤16 GHz) ≥(1.75-0.15625*f)dB (16<f≤24 GHz)	≤(-25+0.625*f)dB (0.01≤f≤24 GHz) $iRL^{1,4}$ ≤ -28 dB	≤(-65+0.625*f)dB (0.01≤f≤24 GHz) $ccICN_{NEXT}^{2}$ ≤ 149uV	≤(-70+3.75*f)dB (0.01≤f≤4 GHz) ≤(-58+0.75*f)dB (4≤f≤24 GHz) Straight: $ccICN_{FEXT}^{3}$ ≤ 110uV Right Angle and Straddle mount: $ccICN_{FEXT}^{3}$ ≤ 125uV	≤0.2 ps[5]
128 GT/s PAM4 (PCIe 7.0)					

PCIe 6.0: edits

- Add electrical parameter values
- Additional editorial cleanup to match Straight/RA/Straddle table?
- Any mechanical changes needed?

TABLE 6-8. ORTHOGONAL (SMT AND PRESS FIT) CONNECTOR SIGNAL INTEGRITY REQUIREMENTS ONLY

	Insertion Loss	Return Loss	Power Sum Near End Crosstalk	Power Sum Far End Crosstalk	Intra-pair Skew
Line Rate 16GT/s NRZ					5ps Max
Line Rate 32 GT/s NRZ	-0.8–0.1375*f dB (0≤f≤16 GHz) 3–0.375*f dB (16≤f≤24 GHz)	-20+f dB (0≤f≤4 GHz) -18.2+0.55*f dB (4≤f≤16 GHz) -27+1.1*f dB (16≤f≤20 GHz) -5 dB (20≤f≤24 GHz)	-50+1.25*f dB (0≤f≤8 GHz) -40 dB (8≤f≤16 GHz) -53.3+0.83*f dB (16≤f≤24 GHz)	-50+1.25*f dB (0≤f≤8 GHz) -40 dB (8≤f≤16 GHz) -60+1.25*f dB (16≤f≤24 GHz)	2 ps Max
Line 64 GT/s PAM4					
Procedure	EIA 364-101 The measured differential S parameter shall be referenced to an 85Ω differential impedance.	EIA 364-108 The measured differential S parameter shall be referenced to an 85Ω differential impedance.	EIA 364-90 The measured differential S parameter shall be referenced to an 85Ω differential impedance.	EIA 364-90 The measured differential S parameter shall be referenced to an 85Ω differential impedance.	Intra-pair skew shall be achieved through EIPS measurement method documented in Appendix E

External Feedback on dimensioning

- Looking at Figure 5-4, the width of the second receptacle is dimensioned with a reference dimension, width of (10.225). From where is this dimension derived?

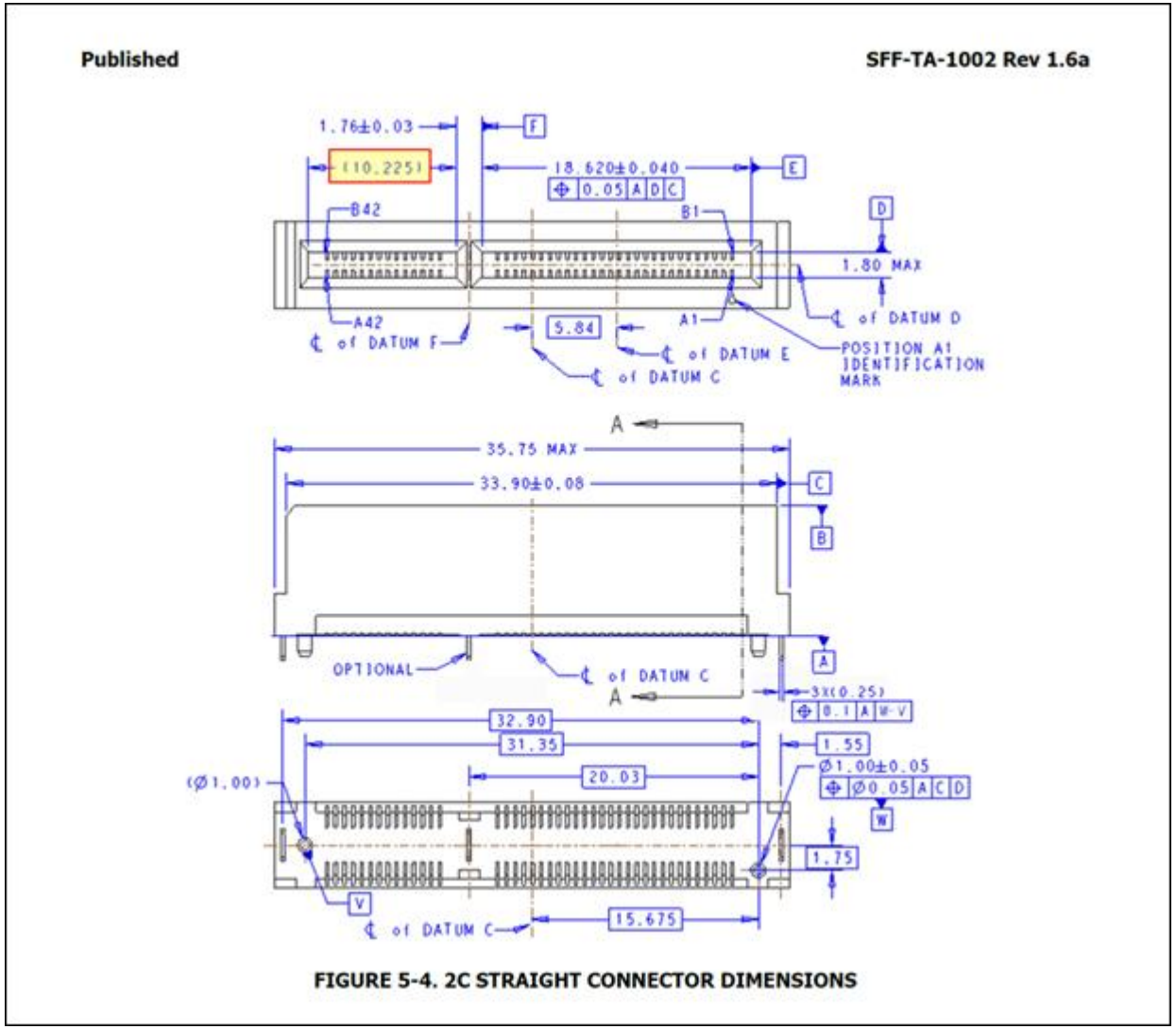


FIGURE 5-4. 2C STRAIGHT CONNECTOR DIMENSIONS

Feedback received:

- Concern received on the test profiles. Are they needed?
  - Maybe okay with the static profile testing since the RMS is not supposed to exceed static value (1.1A/pin).

TABLE 6-3. CONNECTOR ELECTRICAL CURRENT TRANSIENT SUPPORT.

Current Transient Duration "T"	Peak Transient Current
T ≤ 100 microseconds	3 A
100 microseconds < T ≤ 1 second	(3.948 - 0.206 x ln(T)) A
T > 1 second	1.1 A[1]

Notes:
1. This is the static current supported by the connector.

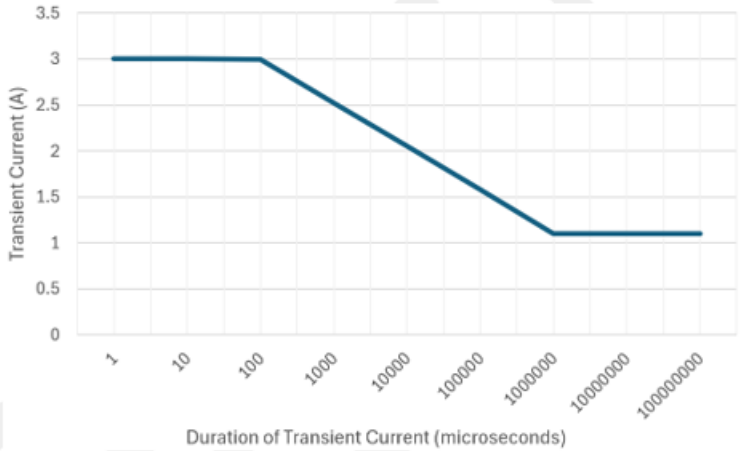


FIGURE 6-1. CONNECTOR ELECTRICAL CURRENT TRANSIENT SUPPORT.

TABLE 6-4. CONNECTOR ELECTRICAL AND OPERATING TEMPERATURE RATINGS.

Parameter	Value	Unit	Comment
Voltage Rating per pin	29	V	Refer to Table 6-5 for testing requirements
Current Rating per pin	Test all 3 profiles a. 3A @100us + 0A @650us b. 2A @10ms + 0A @23ms c. 1.1A	A	Tested per EIA 364-70, Method 3, 30 °C temperature rise. Up to a maximum of 6 adjacent pins per side, 12 pins total
Temperature Rating	-40 to 85	°C	

Feedback received:

- ccICN calculations may need to be revisited as part of these changes.

Thank You

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