SFF-TA-1039

Specification for

PCIe OptiLink Hardware and Electrical Specifications

Rev 0.0.3 October 1, 2025

SECRETARIAT: SFF TWG
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ABSTRACT: This specification defines the contact pads, the electrical, power supply, ESD and thermal characteristics of the PCIe front panel pluggable (FPP) 4x, 8x, and 16x module or cable plug called OptiLink addressing compute and AI scale-up networks. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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FOREWORD

The development work on this specification was done by the PCI-SIG, an industry group and given to the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, as well as since SFF's transition to SNIA in 2016, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TA TWG, the signup for membership can be found at https://www.snia.org/join.

REVISION HISTORY

Rev 0.0.1 - March 28, 2025	Initial release
Rev 0.0.2 - May 1, 2025	2nd release incorporating comments informally
Rev 0.0.3 – October 1, 2025	Incorporating comments from the 1st SFF ballot.

CONTENTS

FIGURES

TABLES

1. Scope

This specification defines electrical requirements for the 4x/8x/16x PCIe™ [1] OptiLink modules and cables addressing compute and AI scale-up networks. The scope includes electrical contacts for the host connector; status, control and management interface signals; power supply requirements; and ESD.

High speed electrical specifications is based on PCI Express 64 GT/s [4] or 128 GT/s [6], and the connector pinout based on PCI Express CopprLink [3], and the multi-lane high speed mechanical specifications for 4x/8x/16x connector/cage specified by SFF-TA-1032 [7]. The 16x OptiLink connector/cage is similar to INF-TA-1003[2] [1], but only SFF-TA-1032 connector/cage is compatible with Optilink module.

2. References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:

[1] INF-TA-1003 400 Gb/s (16 x 25 Gb/s) Pluggable Transceiver, 2018
[2] IEEE Std 802.3-2022 clause 52 Figure 52-2
[3] PCI Express CopprLink 1.0 External Cable Specification for PCI Express 5.0 and 6.0, April 2024
[4] PCI Express Base Specifications Revisions 6.3, January 2024
[5] PCI Express Base Specifications Revisions 6.4, June 2025
[6] PCI Express Base Specifications Revisions 7.0, June 2025
[7] SFF-TA-1032 Multi-Lane External High Speed Cable System, Rev 1.0, March 2025
[8] SFF-8679 QSFP+ 4X Hardware and Electrical Specification, Rev 1.8.4, January 2025
[9] NXP UM10204, I2C-bus specification and user manual, Rev 7.0, October 2021
[10] MIPI Alliance I3C Basic Specification, Rev 1.1.1, June 2021.
[11] OIF Common Management Interface (CMIS), Rev. 5.3, September 2024
https://www.oiforum.com/wp-content/uploads/OIF-CMIS-05.3.pdf
[12] OIF Common Electrical (I/O) (CEI), Rev. 5.2, January 2024
https://www.oiforum.com/wp-content/uploads/OIF-CEI-05.2.pdf
[13] Formfactor Specific Hardware Management CMIS-FF, Rev. 1.0 September 2024
https://www.oiforum.com/wp-content/uploads/OIF-CMIS-FF-01.0.pdf
[14] JEDEC JESD8C.01 Interface Standard for Nominal 3.0/3.3 V Supply Digital Integrated Circuit (LVCMOS)
[15] Human Body Model per ANSI/ESDA/JEDEC JS-001
[16] EN6100-4-2 (IEC immunity standard on ESD), criterion B test specifications
[17] "Measuring PSNR/PSRR/PSMR to meet QSFP/OSFP high-speed Requirements", Steve Sandler, Bob Tarasewicz, Pavel Zivny, Tony Ambrose, DesignCon 2023.
[18] "Power Integrity Testing Requirements Introduce Extreme Interconnect Measures", Steve Sandler, Signal Integrity Journal, February 2023
https://www.signalintegrityjournal.com/articles/2981-power-integrity-testing-requirements-introduce-extreme-interconnect-measures.

[1] PCEe is registered trademarks of PCI-SIG.
[2] Although 16x PCIe OptiLink connector/cage is similar to INF-TA-1003 the formfactors are not compatible.

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

Other standards may be obtained from the organizations listed below:

Standard	Organization	Website
ASME	American Society of Mechanical Engineers (ASME)	https://www.asme.org
Electronic Industries Alliance (EIA)	Electronic Components Industry Association (ECIA)	https://www.ecianow.org
IEEE	Institute of Electrical and Electronics Engineers (IEEE)	https://www.ieee.org
InfiniBand	InfiniBand Trade Association (IBTA)	https://www.infinibandta.org
JEDEC	Joint Electron Deice Engineering Council (JEDEC)	https://www.jedec.org
OIF	Optical Internetworking Forum (OIF)	https://www.oiforum.com
PCIe	PCI-SIG	https://pcisig.com
SAS and other ANSI standards	International Committee for Information Technology Standards (INCITS)	https://www.incits.org

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS: Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a. red (i.e., one of the following colors):
    A. crimson; or
    B. pink;
b. blue; or
c. green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1. top;
2. middle; and
3. bottom.

Lists are associated with an introductory paragraph or phrase and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

DIMENSIONING CONVENTIONS: The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be implemented as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Where the term is used for a signal on a connector contact, the function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies to the restricted designation, then the restricted bit, byte, word, or field shall be treated as a value whose definition is not in scope of this document, and is not interpreted by this specification.

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

ACC: Active Copper Cable, a cable assembly with driver and analog equalizer
AEC: Active Electrical Cable, a cable assembly with repeater/retimer on both end
ANSI: American National Standards Institute
AOC: Active Optical Cable
ASIC: Application specific integrated circuit
CDR: Clock and data recovery
CML: Current mode logic
DC: Direct current
EIA: Electronic Industries Alliance
EMI: Electromagnetic interference
EMLB: Early Mate Late Break
ESD: Electrostatic discharge
FC: Fibre Channel

FPP: Front Panel Pluggable
Gb/s: Gigabits per second
GBd: Gigabaud per second
GT/s Gigatransfer per second (same as GBd)
IEC: International Electrotechnical Commission
IEEE: Institute of Electrical and Electronics Engineers
ISO: International Organization for Standardization
ITU: International Telecommunications Union
I2C: A two-wire serial communication protocol using a serial data line (SDA) and a serial clock line (SCL)
I3C: An improved faster two-wire serial communication protocol using a serial data line (SDA) and a serial clock line (SCL)
JEDEC: Joint Electron Device Engineering Council
LVCMOS: Low voltage complementary metal oxide semiconductor
LVTTL: Low voltage transistor-transistor logic
MDI: Media dependent interface
MPO: Multi-fiber Push Pull connector
NEBS: Network Equipment Building System
PCB: Printed circuit board
PCI: Peripheral Component Interconnect (legacy interface)
PCIe: Peripheral Component Interconnect Express (Modern interface based on high-speed SerDes)
PCB: Printed circuit board
PET: Differentia [p/n] PCI Express Transmitter Lanes
PER: Differential [p/n] PCI Express Receiver Lanes
PERST#: A discrete functional reset to the endpoint device as defined by the PCI Express Base specification.
PRPE: Bidirectional signal (PResence/PESTI) used to indicate the attachment of a cable assembly and a module to a port.
Repeater: A high-speed CDR circuit that is not protocol aware and uses the recovered clock to retransmit the incoming data
Retimer: A PCIe physical layer that include a CDR that is protocol aware
RX: Receiver Transmitter (this document uses PER for consistency with PCI Express)
SerDes: Serializer-Deserializer
TIA: Telecommunications Industry Association
TX: Transmitter (this document uses PET for consistency with PCI Express)
TWI: Two Wire Interface such as I2C.

3.3 Definitions

Connector: Each half of an interface that, when joined together, establishes electrical contact and mechanical retention between two components. In this specification, the term connector does not apply to any specific gender; it is used to describe the receptacle, the plug or the card edge, or the union of receptacle to plug or card edge. Other common terms include connector interface, mating interface, and separable interface.

Contact mating sequence: A term used to describe the order of electrical contact established/ terminated during mating/un-mating. Other terms include contact sequencing, contact positioning, mate first/break last, EMLB (early mate late break) staggered contacts, and long pin/short pin.

Module: In this specification, module may refer to a plug assembly at the end of a copper (electrical) cable (passive or active) or a loopback.

Plug: A term used to describe the connector that contains the penetrating contacts of the connector interface as shown in Figure 3-1. Plugs typically contain stationary contacts. Other common terms include male, pin connector, and card edge.

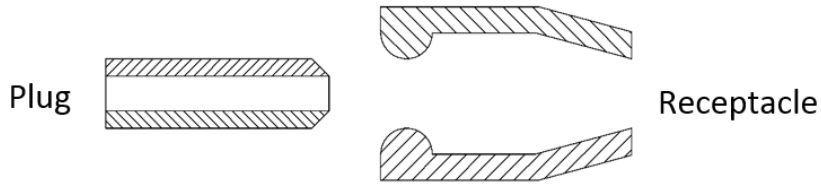

Figure 3-1 Plug and Receptacle Definition

Receptacle: A term used to describe the connector that contains the contacts that accept the plug contacts as shown in Figure 3-1. Receptacles typically contain spring contacts. Other common terms include female and socket connector.

Wipe: The distance a contact travels on the surface of its mating contact during the mating cycle as shown in Figure 3-2.

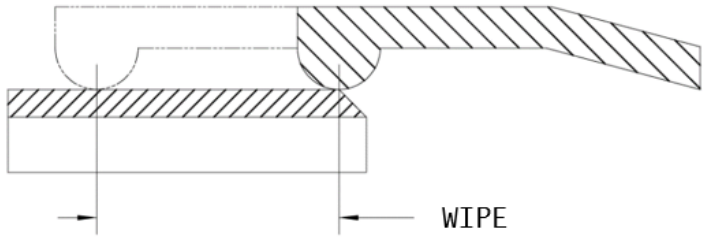

Figure 3-2 Wipe for a Continuous Contact

4. General Description

4.1 Configuration Overview/Descriptions

This specification covers the following items:

- Electrical specifications for 4x/8x/16x PCIe OptiLink (SFF-TA-1039) modules and cables including host connector contact assignments.
- Descriptions for data, control, status and management interface signals.
- Power supply requirements.
- Electrostatic discharge (ESD) tolerance requirements.
- Color coding and labeling.
- Fiber positions for optical interfaces.
- Environmental and thermal requirements (case temperatures).
- Timing requirements.

The high speed signaling for PCIe OptiLink module and cables are defined in PCI Express Gen 6.0 [4] and PCI Express Gen 7 [6], this specification expect to also be compatible with PCI Gen 5.0 if the connector is compatible with SFF-TA-1032 [7]. PCIe OptiLink modules and cables pinout are compatible with PCIe CopprLink [3]. Example modules and cables compatible with these specifications are listed in Table 4-1**Error! Reference source not found.**.

Table 4-1: Example uses of PCIe OptiLink Formfactors

4x PCIe OptiLink	PCI Express Gen 7.0 4x, PCI Express Gen 6.0 4x
8x PCIe OptiLink	PCI Express Gen 7.0 8x, PCI Express Gen 6.0 8x
16x PCIe OptiLink	PCI Express Gen 7.0 16x, PCI Express Gen 6.0 16x

The Application Reference Model in Figure 4-1 shows the high-speed data interface between an PCIe Host and the module/cable. Only one lane of the interface is shown for simplicity. PCIe OptiLink implementation can be modules with parallel MPO connectors or cable assemblies with module attached (i.e., AOC, AEC, or ACC).

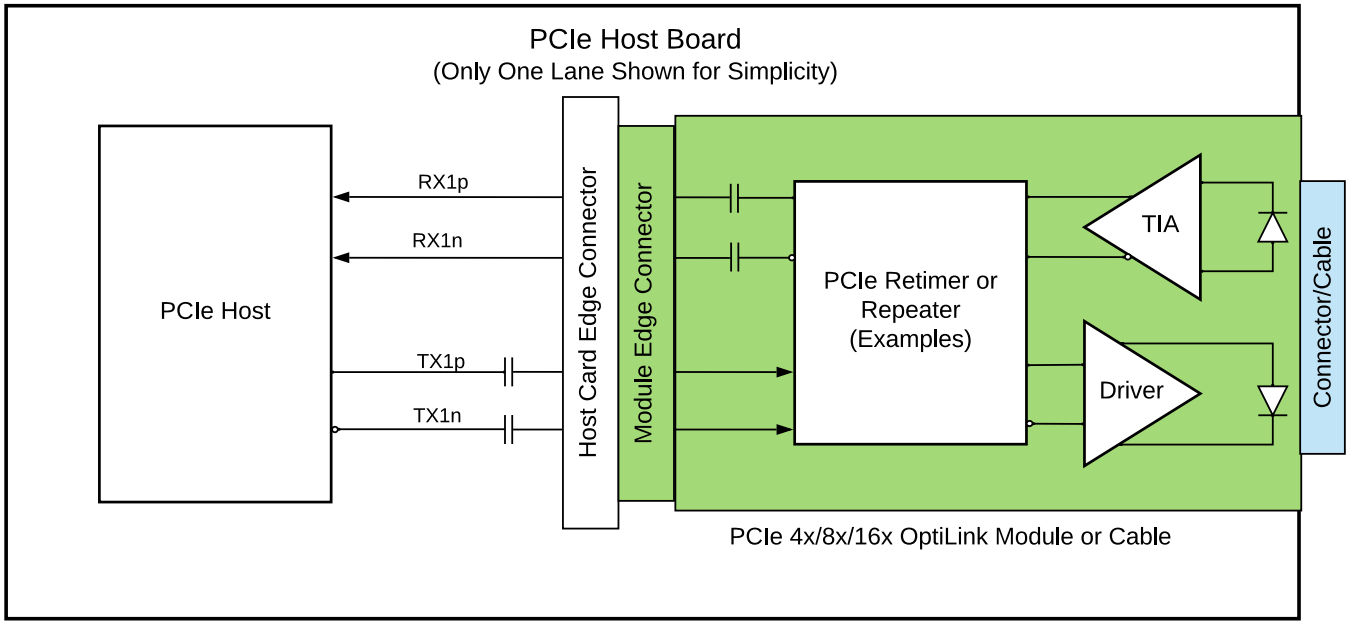

Figure 4-1: Application reference model

4.2 PCIe Compatibility

SFF-TA-1039 supports all of the CopprLink Side-band and FlexIOs, see Table 4-2. Order Sets (OS) have been in PCIe 64 GT/s [5] 128 GT/s [7], similar OS mechanisam maybe defined for SFF-TA-1039 side-bands but this is outside of the scope of this specifications.

Table 4-2: PCI Side-band Compatibility

PCI Signals	CopprLink / OptiLink Side-band Signals	PCI Express Revision 6.4/7.0 In-band Signals using Order-sets
PERST# (Reset end-point)	Direct Wiring (x4, x8, x16)	OS can be defined but may not meet NRC reset requirements
PRPE (Presence/PESTI is Bi-Di Management)	Direct Wiring (x4, x8, x16)	Defined for CEM Presence but could be extended to cables
2WCL/2WDA (I2C for remote device management)	Direct Wiring (x4, x8, x16)	NA
FLEXIO1 (USB2p, PCIe x1 Txp, or GPIO TX or RX)	Direct Wiring (x4, x8, x16)	NA
FLEXIO2 (USB2n, PCIe x1 Txn, or GPIO TX or RX)	Direct Wiring (x4, x8, x16)	NA
FLEXIO3 (100 MHz REFCLK or PCIe x1 RXp GPIO TX or RX)	Direct Wiring (x4, x8, x16)	NA
FLEXIO4 (100 MHz REFCLK or PCIe x1 RXp or GPIO TX or RX)	Direct Wiring (x4, x8, x16)	NA
FLEXIO5 (PCIe x1 RXp or GPIO TX or RX)	Direct Wiring (x16)	NA
FLEXIO6 (PCIe x1 RXp or GPIO TX or RX)	Direct Wiring (x16)	NA
FLEXIO7 (USB 2.0p or GPIO TX or RX)	Direct Wiring (x16)	NA
FLEXIO8 (USB 2.0n or GPIO TX or RX)	Direct Wiring (x16)	NA

5. Compliance boards and reference points for active modules

PCIe OptiLink uses MCB (Module Compliance Board) to measure AOC/AEC/ACC cable module end and uses HCB (Host Compliance Board) to measure the host. PCIe OptiLink modules and hosts electrical interfaces using compliance boards and test points as shown in Figure 5-1.

Reference test points are described in Table 5-1, PCIe OptiLink uses more complete test points consistent with SNIA SFF-8679 [8] and OIF CEI VSR [12] necessary for an active module. These compliance boards are intended to connect the module under test (DUT) to test equipment for verification of compliance to the appropriate standard. The electrical parameters of the compliance boards are specified by the appropriate standard.

Editor's note: There is an ongoing effort to define electrical compliance parameters for PCIe Optilink module in the PCI SIG.

The Module Compliance Board and Host Compliance Board can be plugged together for calibration of compliance signals and to check the electrical parameters of the compliance boards.

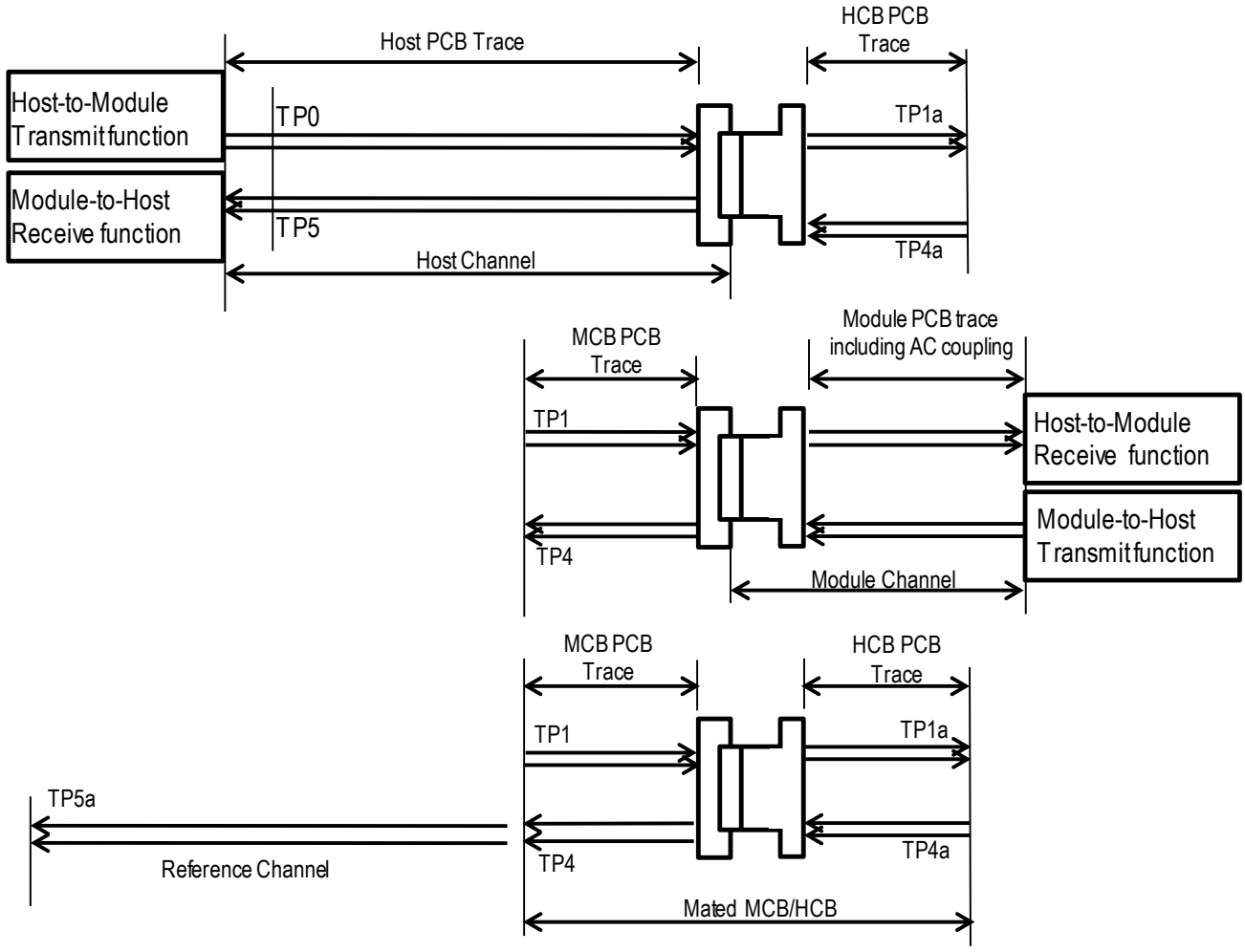

Figure 5-1: Reference Points and Compliance Boards

Table 5-1: Compliance Test Points

Reference Test Points	Description	Relationship to Current PCIe Specifications
TP0	Host ASIC transmitter output at ASIC package ball.	Defined in the PCI Express Base as the ASIC ball.
TP1	Input to Module Compliance Board. Used to test module input.	TP1 in this specification is identical to PCIe CopprLink test shown in Figure 4-1 and 4-2 Specifications [3] and PCIe Gen6/Gen7 Base Specifications [4]/[6]. Also used in the SFF-TA-1039.
TP1a	Host ASIC transmitter output through the host board and host card edge connector at the output of the Host Compliance Board. Also used to calibrate module input compliance signals.	Not currently defined by PCIe specifications but used in the SFF-TA-1039.
TP2[3]	Copper or optical medial dependent output MDI (not currently used by SFF-TA-1039), see	PCIe CopprLink [3] TP2 is equivalent to TP5a test point in this specification.
TP3[4]	Copper or optical medial dependent input MDI (not currently used by SFF-TA-1039)	Not used by PCIe Gen6/Gen7 Base Specifications [4]/[6].
TP4	Input to Module Compliance Board. Used to test module output.	Defined by the PCIe CopprLink but is called TP2. Also used in the SFF-TA-1039.
TP4a	Input to Host Compliance Board. Used to test host input.	Not currently defined by any PCIe specifications but used by the SFF-TA-1039.
TP5	Input at the host ASIC ball.	TP5 in the PCI Express Base specifications is for replica channel input, which has no relationship to TP5 definition in this specification.
TP5a	Far end module output through a reference channel.	PCIe CopprLink [3] TP2 is equivalent to TP5a test point in this specification.

[3] In this specification TP2 is reserved for potential future optical MDI output. TP2 definition in this specification is consistent with OIF definition and is not the same as TP2 definition in CopprLink, where CopprLink TP2 definition is the same as TP4 definition per this specification.

[4] TP3 not used by PCI Express Base Specifications. In this specificationTP3 is reserved for potential future optical MDI output.

6. Electrical Specification

This chapter contains pad definition data for the module. The pad definition data is generic for high speed datacom applications such as PCI Express and Ethernet. Reference points for high-speed electrical measurements are defined in Table 5-1 and illustrated in Figure 5-1. Reference points for all other electrical signals are at comparable points at the host card edge connector.

6.1 Electrical Connector

The module contains a printed circuit board that mates with the electrical connector. The pads are designed for a sequenced mating:

Connected first, disconnected last:	- ground contacts
Connected second, disconnected second:	- power contacts
Connected third, disconnected first:	- signal contacts

For EMI protection the data signals to the connector should be shut off or held to a logic state when the module is absent. Standard board layout practices such as connections to Vcc and GND with vias, the use of short and equal-length differential signal lines, and the use of strip-lines and 42.5 Ω terminations are recommended. The chassis ground (case common) of the module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

6.1.1 x4 Connector and Pad Definition

Pad definition for the x4 connector is the same CopprLink x4 [3] but with additional details such as plug sequence and power to support active module. Figure 6-5 shows the signal symbols and pad numbering for the module edge connector. The diagram shows the module PCB edge as a top and bottom view, where bottom is nearer the host PCB. There are 44 pads intended for high-speed signals, low speed signals, power and ground connections. Color green identifies ground pads, color red identifies power pads, color orange identifies low speed signal/control pads, and color blue identifies high speed I/O pads. Table 6-1 provides more information about each of the 44 pads.

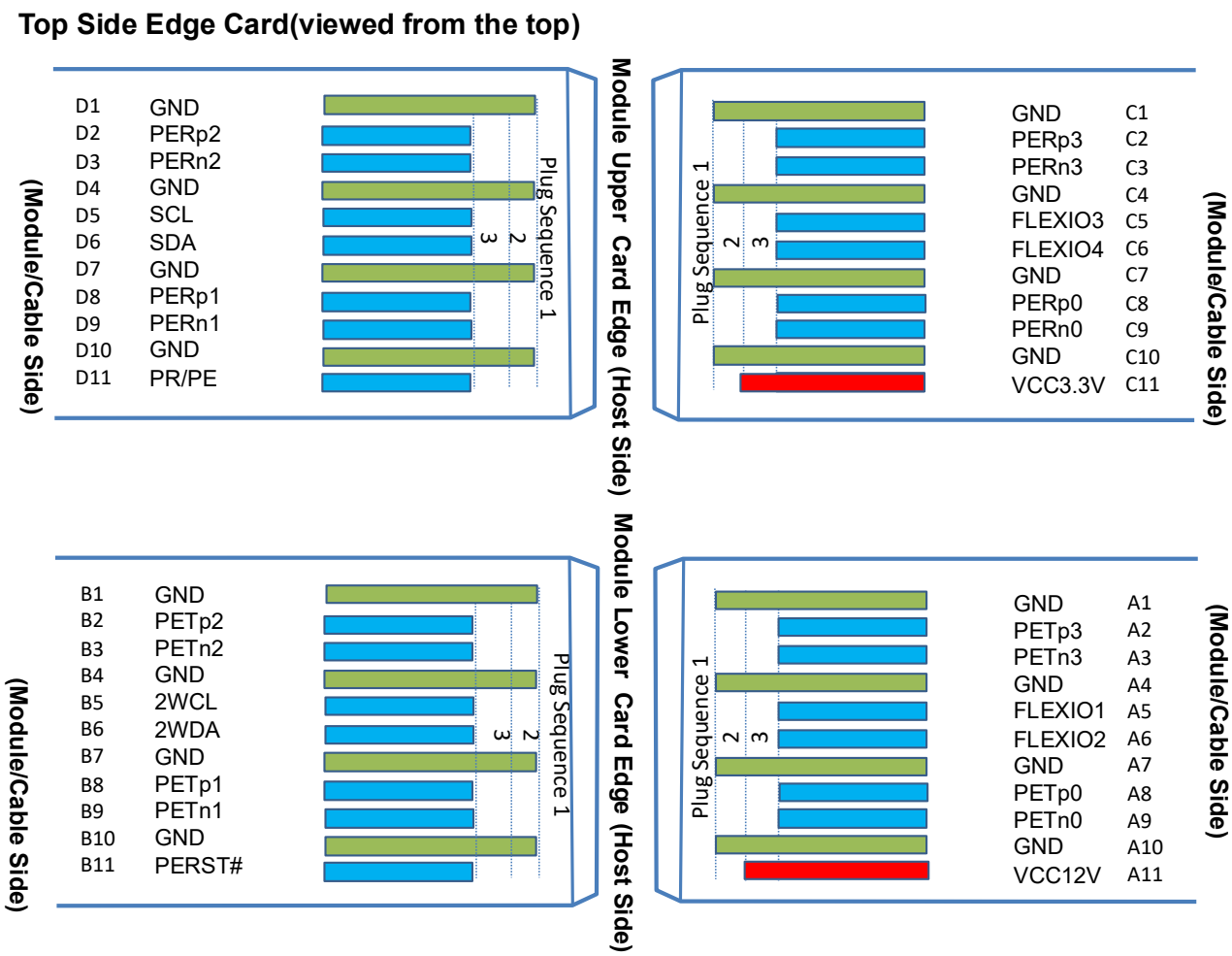

Figure 6-1: PCIe OptiLink x4 Module/Cable Pads

Table 6-1: PCIe OptiLink x4 Module/Cable Pads Definition

Pad	Logic	Symbol	Description	Plug Sequence	Note
A1		GND	Ground	1	1
A2	CML-I	PETp3	Transmitter Non-Inverted Data Input	3	
A3	CML-I	PETn3	Transmitter Inverted Data Input	3	
A4		GND	Ground	1	1
A5	CML-I/O or LVCMOS-I/O	FLEXIO1	FlexIO use case: USB2p or PCIe x1 TXp GPIO TX or RX	3	
A6	CML-I/O or LVCMOS-I/O	FLEXIO2	FlexIO use case: USB2n or PCIe x1 TXn GPIO TX or RX	3	
A7		GND	Ground	1	1
A8	CML-I	PETp0	Transmitter Non-Inverted Data Input	3	
A9	CML-I	PETn0	Transmitter Inverted Data Input	3	
A10		GND	Ground	1	1
A11		VCC12V	VCC +12.0 V Power supply	2	2

B1		GND	Ground	1	1
B2	CML-I	PETp2	Transmitter Non-Inverted Data Input	3	
B3	CML-I	PETn2	Transmitter Inverted Data Input	3	
B4		GND	Ground	1	1
B5	LVCMOS-I	2WCL	Remote two-wire interface management bus clock	3	
B6	LVCMOS-I/O	2WDA	Remote Two-wire interface management bus data	3	
B7		GND	Ground	1	1
B8	CML-I	PETp1	Transmitter Non-Inverted Data Input	3	
B9	CML-I	PETn1	Transmitter Inverted Data Input	3	
B10		GND	Ground	1	1
B11	LVCMOS-I/O	PERST#	Through connected to reset the end point device	3	3
C1		GND	Ground	1	1
C2	CML-O	PERp3	Receiver Non-Inverted Data Input	3	
C3	CML-O	PERn3	Receiver Inverted Data Input	3	
C4		GND	Ground	1	1
C5	CML-I/O or LVCMOS-I/O	FLEXIO3	FlexIO use case: PCIe x1 RXp GPIO TX or RX	3	3
C6	CML-I/O or LVCMOS-I/O	FLEXIO4	FlexIO use case: PCIe x1 RXn GPIO TX or RX	3	3
C7		GND	Ground	1	1
C8	CML-O	PERp0	Receiver Non-Inverted Data Input	3	
C9	CML-O	PERn0	Receiver Inverted Data Input	3	
C10		GND	Ground	1	1
C11		VCC3.3V	VCC +3.3 V Power supply	2	2
D1		GND	Ground	1	1
D2	CML-O	PERp2	Receiver Non-Inverted Data Input	3	
D3	CML-O	PERn2	Receiver Inverted Data Input	3	
D4		GND	Ground	1	1
D5	LVCMOS-I	SCL	Local two-wire interface management bus clock	3	
D6	LVCMOS-I/O	SDA	Local Two-wire interface management bus data	3	
D7		GND	Ground	1	1
D8	CML-O	PERp1	Receiver Non-Inverted Data Input	3	
D9	CML-O	PERn1	Receiver Inverted Data Input	3	
D10		GND	Ground	1	1
D11	LVCMOS-I/O	PRPE	Bidirectional signal (Presence/PESTI)	3	3

Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. For PCIe x4, each connector GND contact is rated for a maximum current of 500 mA.
Note 2: VCC3.3V is applied 1st and module power classes 1 operate from VCC3.3V only. VCC12V is applied after VCC3.3V reaches steady state (see Figure 6-14) and before module transitioned out of ModuleLowPwr. VCC3.3V and VCC12V contacts each have a steady state current rating of 3000 mA.
Note 3: For detail of FLEXIO's, 2WSCL, 2WSDL, PRPE, and PERST# see [3].

6.1.2 PCIe x4 Example Circuits

PCIe X4 OptiLink application reference model and example host RC and host NRC schematics are shown in Figure 6-2.

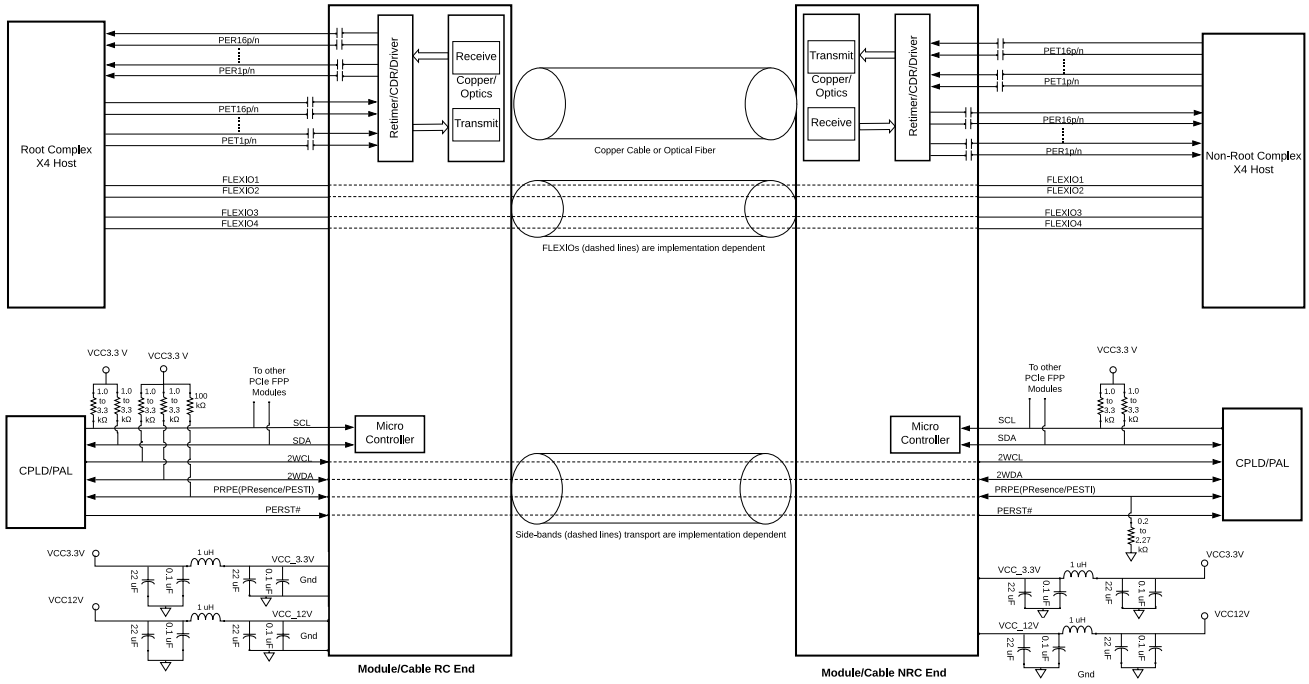

Figure 6-2: PCIe X4 Application Reference Model

6.1.3 X8 Connector and Pad Definition

Pad definition for the x8 connector is the same CopprLink x8 [3] but with additional details such as plug sequence and power to support active module. Figure 6-3 shows the signal symbols and pad numbering for the module edge connector. The diagram shows the module PCB edge as a top and bottom view, where bottom is nearer the host PCB. There are 68 pads intended for high-speed signals, low speed signals, power and ground connections. Color green identifies ground pads, color red identifies power pads, color orange identifies low speed signal/control pads, and color blue identifies high speed I/O pads. Table 6-2 provides more information about each of the 68 pads.

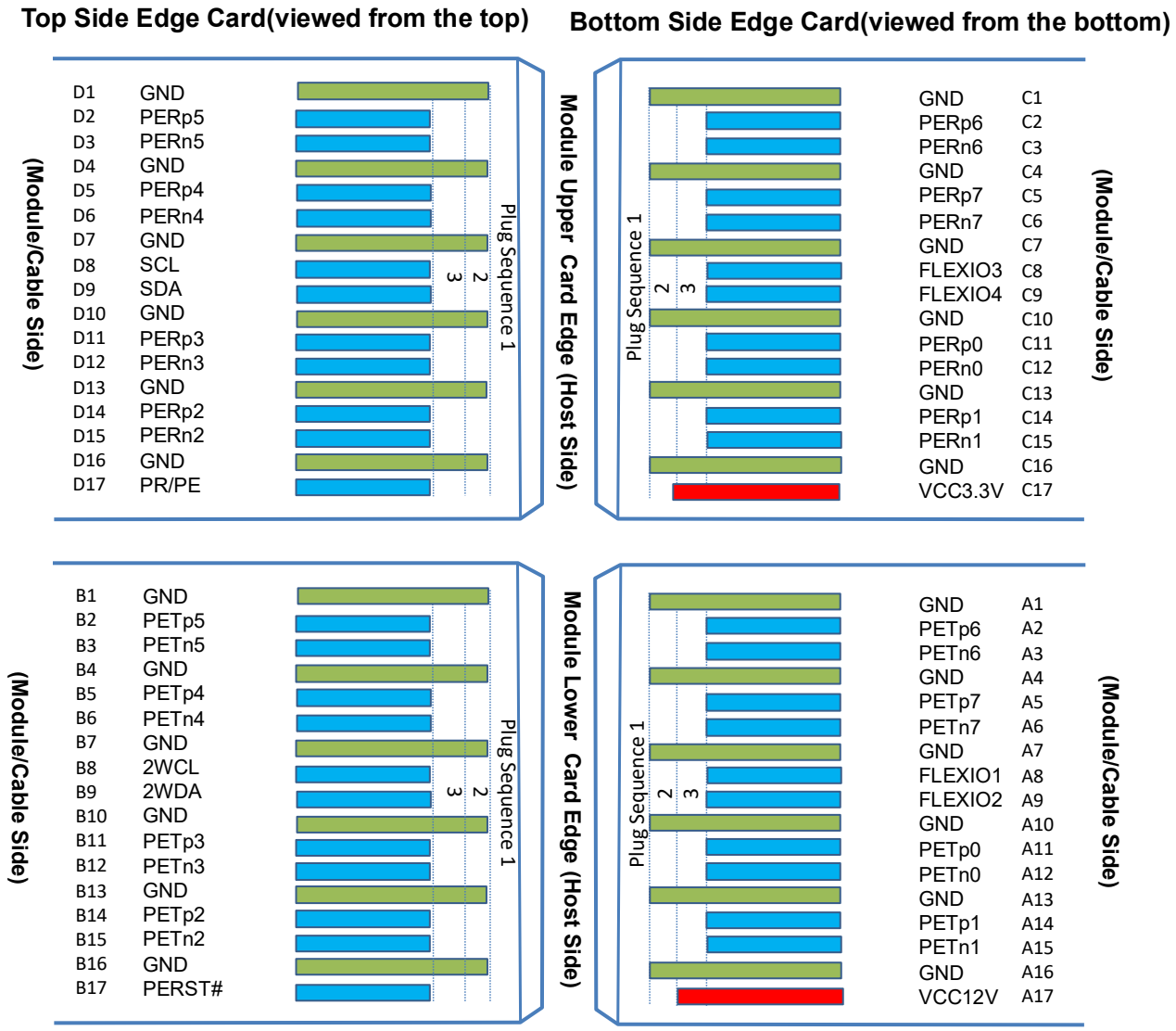

Figure 6-3: PCIe OptiLink x8 Module/Cable Pads

Table 6-2: PCIe OptiLink x8 Module/Cable Pads Definition

Pad	Logic	Symbol	Description	Plug Sequence	Note
A1		GND	Ground	1	1
A2	CML-I	PETp6	Transmitter Non-Inverted Data Input	3	
A3	CML-I	PETn6	Transmitter Inverted Data Input	3	
A4		GND	Ground	1	1
A5	CML-I	PETp7	Transmitter Non-Inverted Data Input	3	
A6	CML-I	PETn7	Transmitter Inverted Data Input	3	
A7		GND	Ground	1	1
A8	CML-I/O or LVCMOS-I/O	FLEXIO1	FlexIO use case: USB2p or PCIe x1 TXp GPIO TX or RX	3	
A9	CML-I/O or LVCMOS-I/O	FLEXIO2	FlexIO use case: USB2n or PCIe x1 TXn GPIO TX or RX	3	
A10		GND	Ground	1	1
A11	CML-I	PETp0	Transmitter Non-Inverted Data Input	3	

A12	CML-I	PETn0	Transmitter Inverted Data Input	3	
A13		GND	Ground	1	1
A14	CML-I	PETp1	Transmitter Non-Inverted Data Input	3	
A15	CML-I	PETn1	Transmitter Inverted Data Input	3	
A16		GND	Ground	1	1
A17		VCC12V	VCC +12.0 V Power supply	2	
B1		GND	Ground	1	1
B2	CML-I	PETp5	Transmitter Non-Inverted Data Input	3	
B3	CML-I	PETn5	Transmitter Inverted Data Input	3	
B4		GND	Ground	1	1
B5	CML-I	PETp4	Transmitter Non-Inverted Data Input	3	
B6	CML-I	PETn4	Transmitter Inverted Data Input	3	
B7		GND	Ground	1	1
B8	LVCMOS-I	2WCL	Remote two-wire interface management bus clock	3	3
B9	LVCMOS-I/O	2WDA	Remote Two-wire interface management bus data	3	3
B10		GND	Ground	1	1
B11	CML-I	PETp3	Transmitter Non-Inverted Data Input	3	
B12	CML-I	PETn3	Transmitter Inverted Data Input	3	
B13		GND	Ground	1	1
B14	CML-I	PETp2	Transmitter Non-Inverted Data Input	3	3
B15	CML-I	PETn2	Transmitter Inverted Data Input	3	3
B16		GND	Ground	1	1
B17	LVCMOS-I/O	PERST#	Through connected to reset the end point device	3	3
B17	CML-I	PETp7	Transmitter Non-Inverted Data Input	3	
C1		GND	Ground	1	1
C2	CML-O	PERp6	Receiver Non-Inverted Data Input	3	
C3	CML-O	PERn6	Receiver Inverted Data Input	3	
C4		GND	Ground	1	1
C5	CML-O	PERp7	Receiver Non-Inverted Data Input	3	
C6	CML-O	PERn7	Receiver Inverted Data Input	3	
C7		GND	Ground	1	1
C8	CML-I/O or LVCMOS-I/O	FLEXIO3	FlexIO use case: PCIe x1 RXp GPIO TX or RX	3	3
C9	CML-I/O or LVCMOS-I/O	FLEXIO4	FlexIO use case: PCIe x1 RXn GPIO TX or RX	3	3
C10		GND	Ground	1	1
C11	CML-O	PERp0	Receiver Non-Inverted Data Input	3	
C12	CML-O	PERn0	Receiver Inverted Data Input	3	
C13		GND	Ground	1	1
C14	CML-O	PERp1	Receiver Non-Inverted Data Input	3	3
C15	CML-O	PERn1	Receiver Inverted Data Input	3	3
C16		GND	Ground	1	1
C17		VCC3.3V	VCC +3.3 V Power supply	2	2
D1		GND	Ground	1	1
D2	CML-O	PERp5	Receiver Non-Inverted Data Input	3	
D3	CML-O	PERn5	Receiver Inverted Data Input	3	
D4		GND	Ground	1	1
D5	CML-O	PERp4	Receiver Non-Inverted Data Input	3	
D6	CML-O	PERn4	Receiver Inverted Data Input	3	
D7		GND	Ground	1	1
D8	LVCMOS-I	2WCL	Remote two-wire interface management bus clock	3	
D9	LVCMOS-I/O	2WDA	Remote Two-wire interface management bus data	3	

D10		GND	Ground	1	1
D11	CML-O	PERp3	Receiver Non-Inverted Data Input	3	
D12	CML-O	PERn3	Receiver Inverted Data Input	3	
D13		GND	Ground	1	1
D14	CML-O	PERp2	Receiver Non-Inverted Data Input	3	
D15	CML-O	PERn2	Receiver Inverted Data Input	3	
D16		GND	Ground	1	1
D17	LVCMOS-I/O	PRPE	Bidirectional signal (Presence/PESTI)	3	3

Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. For PCIe x8, each connector GND contact is rated for a maximum current of 500 mA.
Note 2: VCC3.3V is applied 1st and module power classes 1 operate from VCC3.3V only. VCC12V is applied after VCC3.3V reaches steady state (see Figure 6-14) and before module transitioned out of ModuleLowPwr. VCC3.3V and VCC12V contacts each have a steady state current rating of 3000 mA.
Note 3: For detail of FLEXIO's, 2WSCL, 2WSDL, PRPE, and PERST# see [3].

6.1.4 PCIe x8 Example Circuits

PCIe X4 OptiLink application reference model and example host RC and host NRC schematics are shown in Figure 6-4.

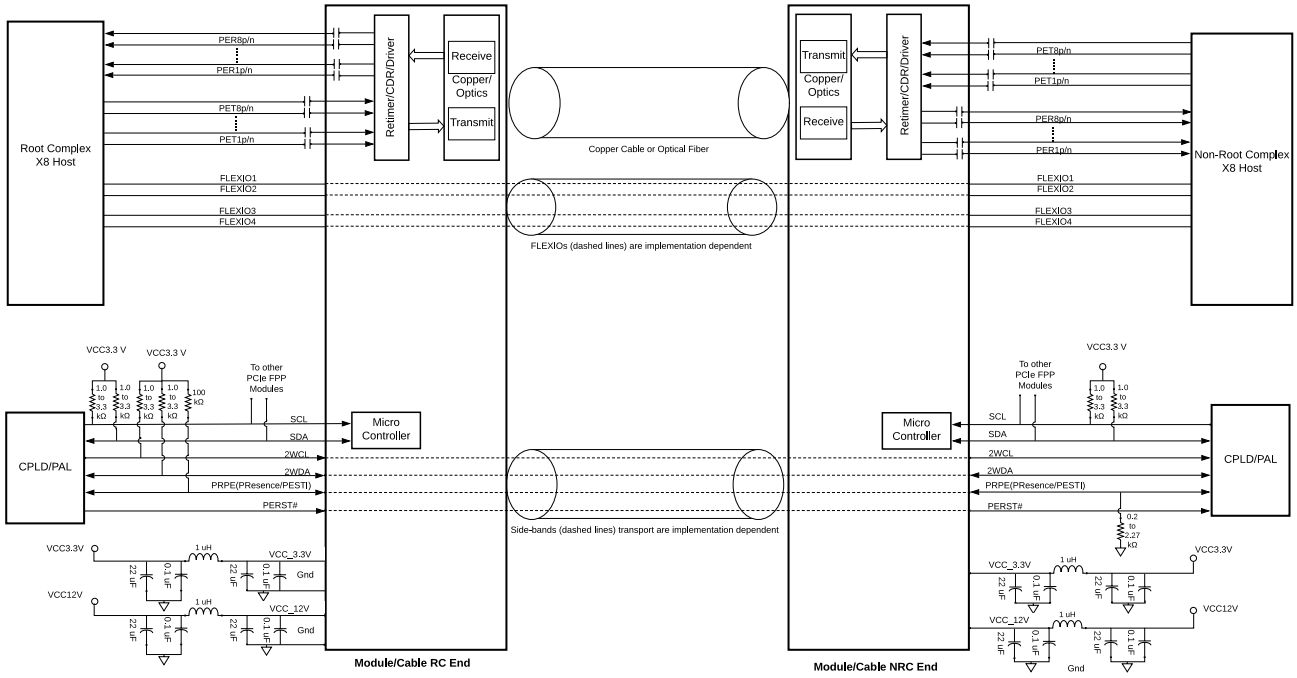

Figure 6-4: PCIe X8 Application Reference Model

6.1.5 x16 Connector and Pad Definition

Pad definition for the x16 connector is the same CopprLink x16 [3] but with additional details such as plug sequence and power to support active module. Figure 6-5 shows the signal symbols and pad numbering for the module edge connector. The diagram shows the module PCB edge as a top and bottom view, where bottom is nearer the host PCB. There are 120 pads intended for high-speed signals, low speed signals, power and ground connections. Color green identifies ground pads, color red identifies power pads, color orange identifies low speed signal/control pads, and color blue identifies high speed I/O pads. Table 6-3 provides more information about each of the 120 pads.

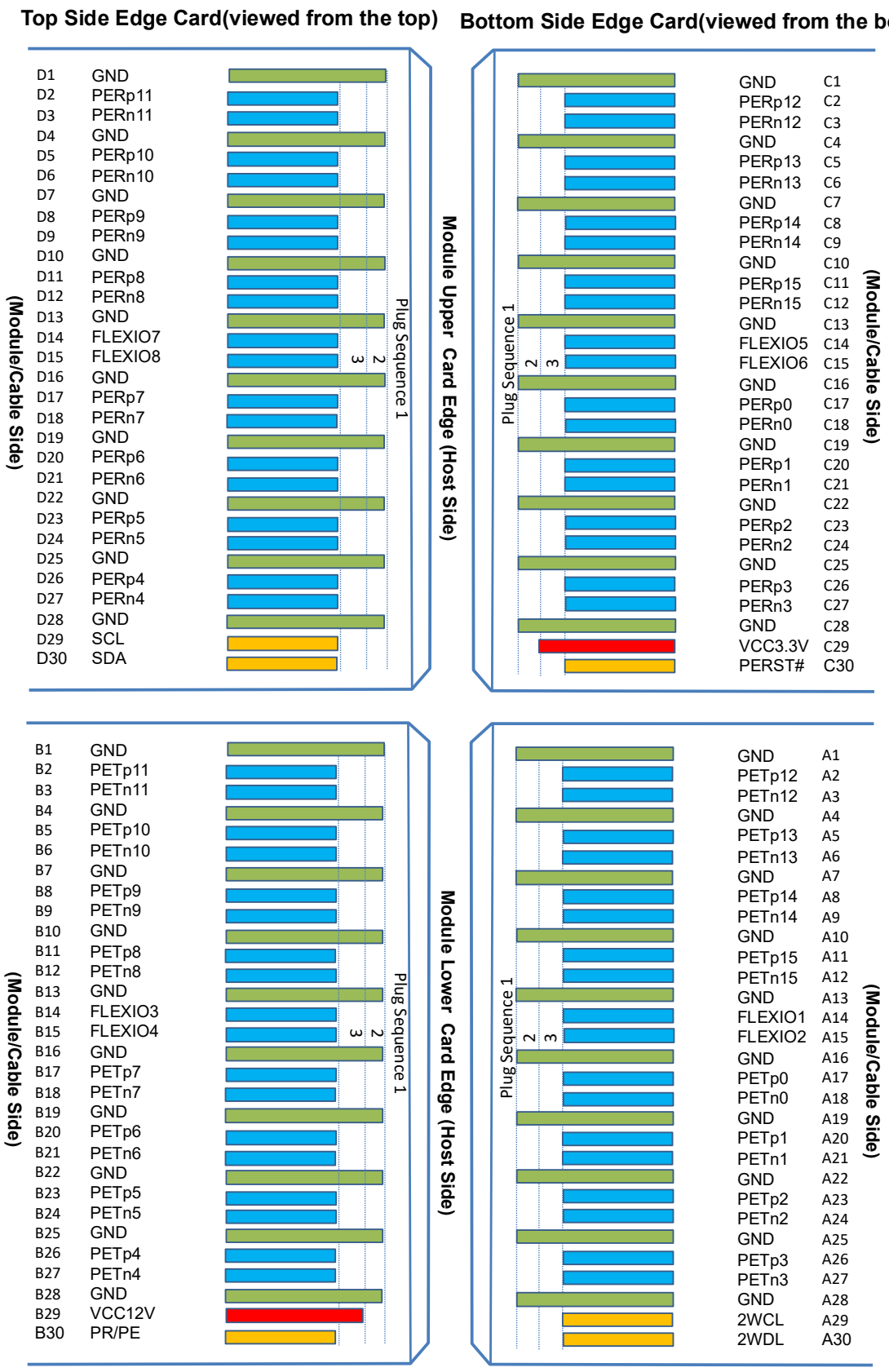

Figure 6-5: PCIe OptiLink x16 Module/Cable Pads

Table 6-3: PCIe OptiLink x16 Module/Cable Pads Definition

Pad	Logic	Symbol	Description	Plug Sequence	Note
A1		GND	Ground	1	1
A2	CML-I	PETp12	Transmitter Non-Inverted Data Input	3	
A3	CML-I	PETn12	Transmitter Inverted Data Input	3	
A4		GND	Ground	1	1
A5	CML-I	PETp13	Transmitter Non-Inverted Data Input	3	
A6	CML-I	PETn13	Transmitter Inverted Data Input	3	
A7		GND	Ground	1	1
A8	CML-I	PETp14	Transmitter Non-Inverted Data Input	3	
A9	CML-I	PETn14	Transmitter Inverted Data Input	3	
A10		GND	Ground	1	1
A11	CML-I	PETp15	Transmitter Non-Inverted Data Input	3	
A12	CML-I	PETn15	Transmitter Inverted Data Input	3	
A13		GND	Ground	1	1
A14	CML-I/O or LVCMOS-I/O	FLEXIO1	FlexIO use case: USB2p or PCIe x1 TXp GPIO TX or RX	3	
A15	CML-I/O or LVCMOS-I/O	FLEXIO2	FlexIO use case: USB2n or PCIe x1 TXn GPIO TX or RX	3	
A16		GND	Ground	1	1
A17	CML-I	PETp0	Transmitter Non-Inverted Data Input	3	
A18	CML-I	PETn0	Transmitter Inverted Data Input	3	
A19		GND	Ground	1	1
A20	CML-I	PETp1	Transmitter Non-Inverted Data Input	3	
A21	CML-I	PETn1	Transmitter Inverted Data Input	3	
A22		GND	Ground	1	1
A23	CML-I	PETp2	Transmitter Non-Inverted Data Input	3	
A24	CML-I	PETn2	Transmitter Inverted Data Input	3	
A25		GND	Ground	1	1
A26	CML-I	PETp3	Transmitter Non-Inverted Data Input	3	
A27	CML-I	PETn3	Transmitter Inverted Data Input	3	
A28		GND	Ground	1	
A29	LVCMOS-I	2WCL	Remote two-wire interface management bus clock	3	3
A30	LVCMOS-I/O	2WDA	Remote Two-wire interface management bus data	3	3
B1		GND	Ground	1	1
B2	CML-I	PETp11	Transmitter Non-Inverted Data Input	3	
B3	CML-I	PETn11	Transmitter Inverted Data Input	3	
B4		GND	Ground	1	1
B5	CML-I	PETp10	Transmitter Non-Inverted Data Input	3	
B6	CML-I	PETn10	Transmitter Inverted Data Input	3	
B7		GND	Ground	1	1
B8	CML-I	PETp9	Transmitter Non-Inverted Data Input	3	
B9	CML-I	PETn9	Transmitter Inverted Data Input	3	
B10		GND	Ground	1	1
B11	CML-I	PETp8	Transmitter Non-Inverted Data Input	3	
B12	CML-I	PETn8	Transmitter Inverted Data Input	3	
B13		GND	Ground	1	1
B14	CML-I/O or LVCMOS-I/O	FLEXIO3	FlexIO use case: 100 MHz REFCLK or PCIe x1 RXp GPIO TX or RX	3	3
B15	CML-I/O or	FLEXIO4	FlexIO use case: 100 MHz REFCLK or PCIe x1 RXn	3	3

	LVCMOS-I/O		GPIO TX or RX		
B16		GND	Ground	1	1
B17	CML-I	PETp7	Transmitter Non-Inverted Data Input	3	
B17	CML-I	PETp7	Transmitter Non-Inverted Data Input	3	
B18	CML-I	PETn7	Transmitter Inverted Data Input	3	
B19		GND	Ground	1	1
B20	CML-I	PETp6	Transmitter Non-Inverted Data Input	3	
B21	CML-I	PETn6	Transmitter Inverted Data Input	3	
B22		GND	Ground	1	1
B23	CML-I	PETp5	Transmitter Non-Inverted Data Input	3	
B24	CML-I	PETn5	Transmitter Inverted Data Input	3	
B25		GND	Ground	1	1
V26	CML-I	PETp4	Transmitter Non-Inverted Data Input	3	
B27	CML-I	PETn4	Transmitter Inverted Data Input	3	
B28		GND	Ground	1	1
B29		VCC12V	VCC +12.0 V Power supply	2	2
B30	LVCMOS-I/O	PRPE	Bidirectional signal (Presence/PESTI)	3	3
C1		GND	Ground	1	1
C2	CML-O	PERp12	Receiver Non-Inverted Data Input	3	
C3	CML-O	PERn12	Receiver Inverted Data Input	3	
C4		GND	Ground	1	1
C5	CML-O	PERp13	Receiver Non-Inverted Data Input	3	
C6	CML-O	PERn13	Receiver Inverted Data Input	3	
C7		GND	Ground	1	1
C8	CML-O	PERp14	Receiver Non-Inverted Data Input	3	
C9	CML-O	PERn14	Receiver Inverted Data Input	3	
C10		GND	Ground	1	1
C11	CML-O	PERp15	Receiver Non-Inverted Data Input	3	
C12	CML-O	PERn15	Receiver Inverted Data Input	3	
C13		GND	Ground	1	1
C14	CML-I/O or LVCMOS-I/O	FLEXIO5	FlexIO use case: PCIe x1 RXp GPIO TX or RX	3	3
C15	CML-I/O or LVCMOS-I/O	FLEXIO6	FlexIO use case: PCIe x1 RXn GPIO TX or RX	3	3
C16		GND	Ground	1	1
C17	CML-O	PERp0	Receiver Non-Inverted Data Input	3	
C18	CML-O	PERn0	Receiver Inverted Data Input	3	
C19		GND	Ground	1	1
C20	CML-O	PERp1	Receiver Non-Inverted Data Input	3	
C21	CML-O	PERn1	Receiver Inverted Data Input	3	
C22		GND	Ground	1	1
C23	CML-O	PERp2	Receiver Non-Inverted Data Input	3	
C24	CML-O	PERn2	Receiver Inverted Data Input	3	
C25		GND	Ground	1	1
C26	CML-O	PERp3	Receiver Non-Inverted Data Input	3	
C27	CML-O	PERn3	Receiver Inverted Data Input	3	
C28		GND	Ground	1	1
C29		VCC3.3V	VCC +3.3 V Power supply	2	2
C30	LVCMOS-I/O	PERST#	Through connected to reset the end point device	3	3
D1		GND	Ground	1	1
D2	CML-O	PERp11	Receiver Non-Inverted Data Input	3	
D3	CML-O	PERn11	Receiver Inverted Data Input	3	

D4		GND	Ground	1	1
D5	CML-O	PERp10	Receiver Non-Inverted Data Input	3	
D6	CML-O	PERn10	Receiver Inverted Data Input	3	
D7		GND	Ground	1	1
D8	CML-O	PERp9	Receiver Non-Inverted Data Input	3	
D9	CML-O	PERn9	Receiver Inverted Data Input	3	
D10		GND	Ground	1	1
D11	CML-O	PERp8	Receiver Non-Inverted Data Input	3	
D12	CML-O	PERn8	Receiver Inverted Data Input	3	
D13		GND	Ground	1	1
D14	CML-I/O or LVCMOS-I/O	FLEXIO7	FlexIO use case: USB2p or GPIO TX or RX	3	3
D15	CML-I/O or LVCMOS-I/O	FLEXIO8	FlexIO use case: USB2n or GPIO TX or RX	3	3
D16		GND	Ground	1	1
D17	CML-O	PERp7	Receiver Non-Inverted Data Input	3	
D18	CML-O	PERn7	Receiver Inverted Data Input	3	
D19		GND	Ground	1	1
D20	CML-O	PERp6	Receiver Non-Inverted Data Input	3	
D21	CML-O	PERn6	Receiver Inverted Data Input	3	
D22		GND	Ground	1	1
D23	CML-O	PERp5	Receiver Non-Inverted Data Input	3	
D24	CML-O	PERn5	Receiver Inverted Data Input	3	
D25		GND	Ground	1	1
D26	CML-O	PERp4	Receiver Non-Inverted Data Input	3	
D27	CML-O	PERn4	Receiver Inverted Data Input	3	
D28		GND	Ground	1	1
D29	LVCMOS-I	2WCL	Local two-wire interface management bus clock	3	
D30	LVCMOS-I/O	2WDA	Local Two-wire interface management bus data	3	

Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. For PCIe x16, each connector GND contact is rated for a maximum current of 500 mA.
Note 2: VCC3.3V is applied 1st and module power classes 1 operate from VCC3.3V only. VCC12V is applied after VCC3.3V reaches steady state (see Figure 6-14) and before module transitioned out of ModuleLowPwr. VCC3.3V and VCC12V contacts each have a steady state current rating of 3000 mA.
Note 3: For detail of FLEXIO's, 2WSCL, 2WSDL, PRPE, and PERST# see [3].

6.1.6 PCIe x16 Example Circuits

PCIe X4 OptiLink application reference model and example host RC and host NRC schematics are shown in Figure 6-6.

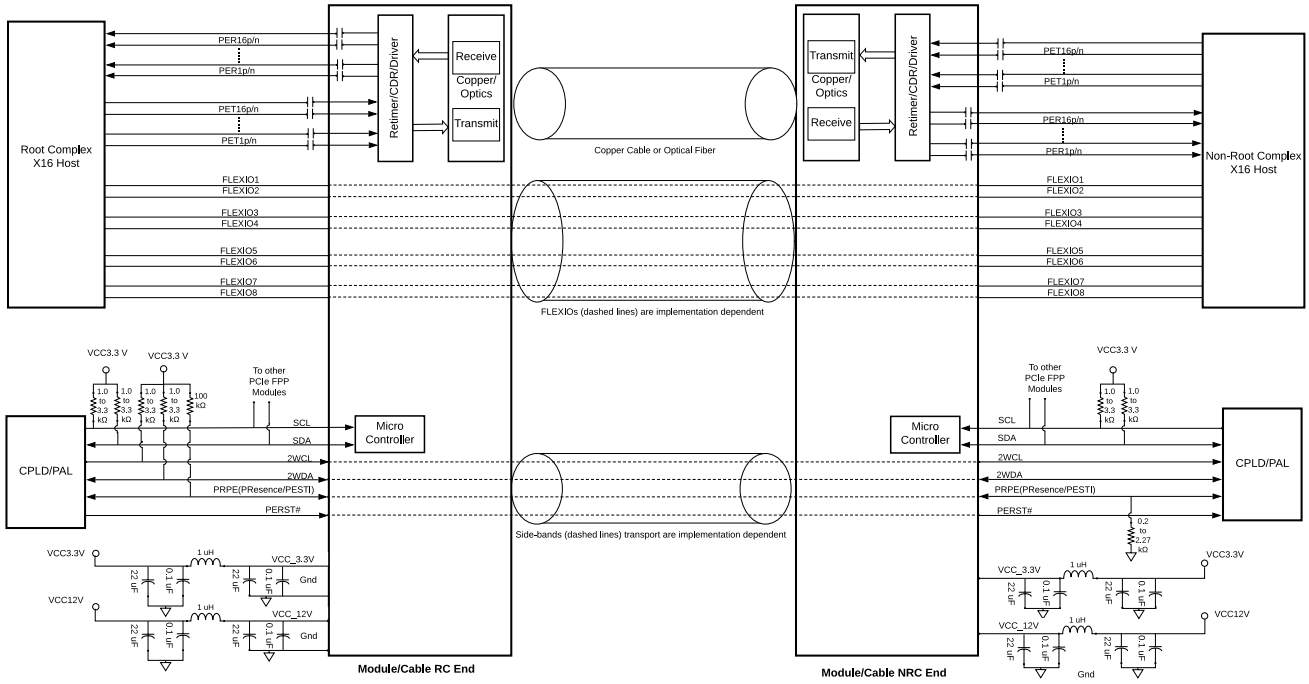

Figure 6-6: PCIe X16 Application Reference Model

6.2 FlexIOs

For full description of FlexIO see CopprLink [3].

6.3 Low Speed Signal Descriptions

OIF CMIS [11] operation require the following Management Signaling Layers (MSL) signals as defined in the OIF CMIS-FF[13]:

- LowPwrRequestHW, see 6.3.1
- CMIS Interrupt, see 6.3.2
- CMIS Reset, see 6.3.5

6.3.1 LowPwrRequestHW

SFF-TA-1039 has no dedicated hardware pin for the LPMode signal. As per CMIS-FF [13] the module therefore behaves as if the LowPwrRequestHW signal was constantly ASSERTED.

6.3.2 IntLs

IntLs has the same function as the classic IntL in SFF-8679 [8], but is a soft interrupt that is carried on the SDA line. When the IntLs signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntLs signal is deasserted "High" after all set interrupt flags are read.

Operation of IntLs, after the bus has been idle for 200 μS the target pulls SDA low for 100 μS to signal IntLs. Figure 6-7 show IntLs operation examples; a. Show applying IntLs after the bus has been idle, b. Show aborting IntLs due to bus activity, c. Show another example of IntLs aborting due to bus activity. If the host starts a request at the same time by also pulling SDA low, the target must release the SDA line at the falling edge of SCL. The

target repeats the 100 μS low period every 200 μS until the host clears the interrupt condition. For soft timing of IntLs see Table 6-6.

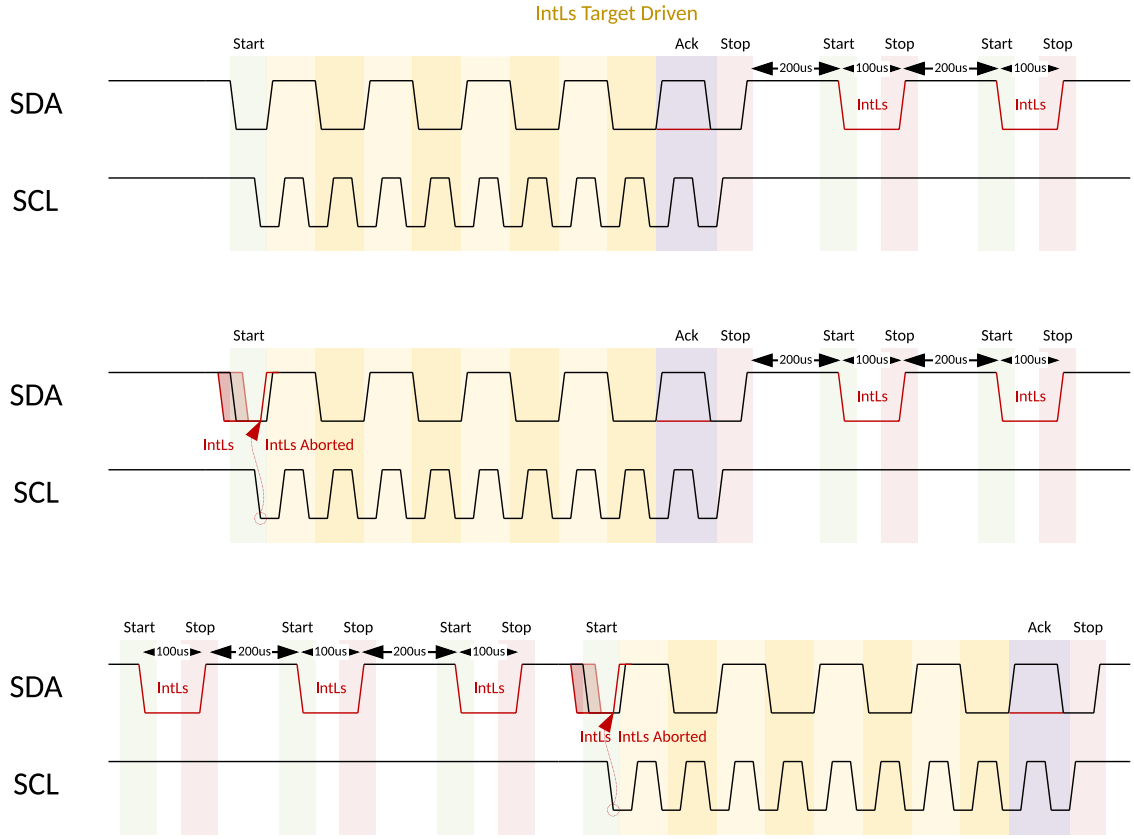

Figure 6-7: IntLs Operation

6.3.3 PRPE

Bidirectional signal (PResence/PESTI) used to indicate the attachment of a CopprLink or SFF-TA-1039 cable assembly or a module to a port.

Optional use as PESTI (see Chapter 12 of PCI Express Base [6]). If PESTI is not supported, the Root-Complex and Non-Root-Complex must support a Presence Indicator with the Root-Complex having a 100kΩ (+/- 5%) pull-up to 3.3V and the Non-Root-Complex with a 2.27kΩ or less (must be greater than 200 ohms) pull-down following power-up. PESTI is permitted to be utilized to indirectly tunnel physical presence status of hot-plug capable downstream targets. A device may request a re-start of the discovery process by asserting and releasing BREAK at any time. If the NRC side of the cable is not plugged in before NRC power is turned on, then the 50 μS low period after power-on that indicates Presence may be missed by the RC side. To address this potential hot plug issue, if the Target doesn't not receive a Discovery Request within in 250 ms then the Target will initiate another 50 μS break event.

6.3.4 PERST#

Active low, push-pull at source. A discrete functional reset to the endpoint device as defined by the PCI Express Base Specification [6].

6.3.5 ResetLs

ResetLs has the same function as the classic Reset in SFF-8679 [8], but is a soft reset that is carried on the SDA line. Host pulls SDA low for 200 μS to signal a ResetLs, when bus has been idle for 200 μS, see Figure 6-8. This must only happen when the host has idled the bus. A low level on the ResetLs signal initiates a complete module reset, returning all user module settings to their default state. For soft timing of ResetLs see Table 6-6.

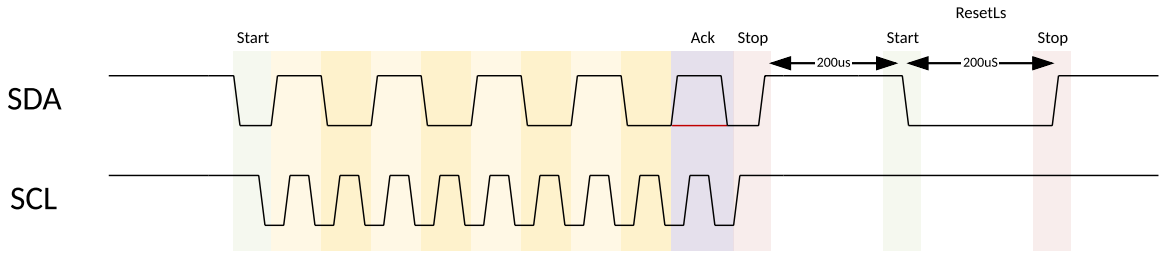

Figure 6-8: RestLs Operation

6.3.6 SCL/SDA

Local management bus (Clock/Data: SCL/SDA) interface between the host and the cable using I2C protocol. A memory device should be connected on each side of the cable assembly via VCC3p3V and the local management bus. The memory device must be compliant with the CMIS, supporting 8-bit addressing and access to 256 bytes of available space to support identification and management functions. Local bus must not traverse the cable assembly

6.3.7 Pass-Through 2WCL/2WDA

Management bus (Clock/Data: 2WCL/2WDA) for Pass-Through two wire interface [3]. The Root-Complex and Non-Root Complex must provide isolation on the bias for these pins until local power is good to avoid backfeed/leakage. Remote bus must traverse the cable assembly.

OptiLink only supports point-to-point (non-bused configuration) 2WCL/2WDL topology from RC host to NRC host. Figure 6-9 show architecture of pass-through 2WCL/2WDA. The 2WCL/2WDA maximum board, cable, and load capacitances are given in Table 6-4.

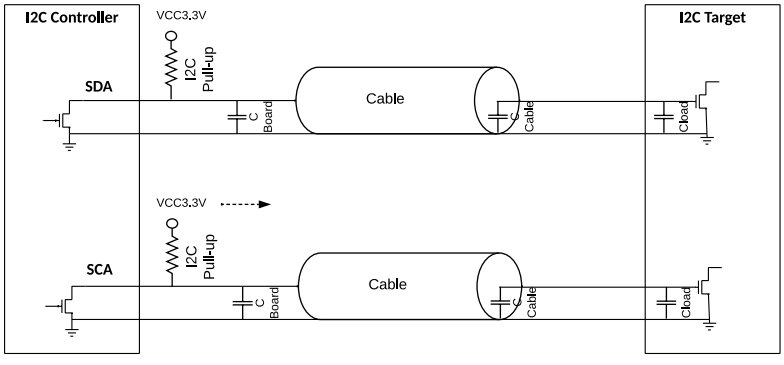

Figure 6-9: Architecture of Pass-Through TWI

6.4 Low Speed Signal Electrical Specifications

TWI bus composed of the initiator and the target devices, the initiator controls the bus and the target device respond to the initiator requests.

6.4.1 Low Speed Signaling

Low speed signaling other than the SCL/2WCL and SDA/2WDL interfaces are based on Low Voltage (LVCMOS) operating at VCC3.3V. Hosts shall use a pull-up resistor connected to VCC3.3V host on each of the TWI interface SCL/2WCL (clock), SDA/2WDL (data), and all low speed status outputs (see Table 6-4). The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

The low speed electrical specifications are given in Table 6-4, where some of the parameters are more stringent than JEDEC JESD8C [13]. Implementations compliant to this specification ensures compatibility between TWI host bus initiator and the TWI target device.

Table 6-4- Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL (max)=3 mA for Fast Mode, 20 mA for Fast Mode+
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	Capacitance of SCL, 2WCL, SDA, and 2WDL in this specification are higher than [9] to account for connector and trace capacitances.
Total bus capacitive load for SCL and SDA	Cb		550	pF	Maximum bus capacitance for Fast-Mode (400 kHz), see [9]. For allowed range of bus capacitance and pullup resistors, see Figure 6-11 and Figure 6-12.
			400	pF	Maximum bus capacitance for Fast-Mode+ (1 MHz), see [9]. For allowed range of bus capacitance and pullup resistors, see [9] and Figure 6-11 and Figure 6-12.
2WCL and 2WDA	VOL	0	0.4	V	IOL (max)=3 mA for Fast Mode, 20 mA for 1 MHz Fast Mode+ For I3C Basic bus (12.5 MHz) capacitance is reduced to 50 pF, see 6.
2WCL and 2WDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance of 2WCL and 2WDA cable assembly at RC	C_{cable}		475	pF	Maximum capacitance for Fast-Mode (400 kHz), see [9]. Capacitance of 2WCL and 2WDA in this specification are lower than [9] to account for board capacitance of Cboard=50 pF and one I2C load Cload=25 pF at the NRC end.

			350	pF	Maximum capacitance for Fast-Mode+ (1 MHz), see [9]. Capacitance of 2WCL and 2WDA in this specification are lower than [9] to account for board capacitance of Cboard=50 pF and one I2C load Cload=25 pF at the NRC end.
Total bus capacitive load for 2WCL and 2WDA	Cb		550	pF	Maximum bus capacitance for Fast-Mode (400 kHz), see [9]. For allowed range of bus capacitance and pullup resistors, see and Figure 6-11 and Figure 6-12. For detail how to support I3C Basic on 2WCL/2WDL (12.5 MHz) see [10].
			400	pF	Maximum bus capacitance for Fast-Mode+ (1 MHz), see [9]. For allowed range of bus capacitance and pullup resistors, see and Figure 6-11 and Figure 6-12. For detail how to support I3C Basic on 2WCL/2WDL (12.5 MHz) see [10].

6.5 Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. The PCIe OptiLink memory map are based on "Common Management Interface Specification (CMIS)" [11]. Some timing requirements are critical, especially for a multi-lanes device, so the interface speed may optionally be increased. Byte 00h on the Lower Page or Address 128 Page 00h is used to indicate the use of CMIS. PCIe OptiLink ports support both PCIe OptiLink module and PCIe CopprLink [3], but PCIe CopprLink do not support CMIS Reset or IntL.

In some applications, muxing or demuxing may occur in the module. In this specification, all references to lane numbers are based on the electrical connector interface lanes, unless otherwise indicated. In cases where a status or control aspect is applicable only to lanes after muxing or demuxing has occurred, the status or control is intended to apply to all lanes in the mux group, unless otherwise indicated.

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at VCC3.3V, [13]. Hosts shall use a pull-up resistor connected to VCC3.3V on the TWI interface SCL/2WCL (clock) and SDA/2WDL (Data) signals. Detailed electrical specifications are given in 6.3. Timing specifications for management functionality involving electrical low speed signals are found are given in Table 6-7.

Nomenclature for all registers more than 1 bit long is MSB-LSB.

6.5.1 Management Interface Timing Specification

The timing parameters for the TWI interface (TWI) to the PCIe OptiLink module memory transaction timings are shown in Figure 6-10 and specified in Table 6-5 and is compatible with I2C [9]. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. The total bus capacitance in conjunction with the SCL/SDA and 2WCL/2WDL pull resistor determines the speed TWI could operate, 6.5.2 provide pull up resistor for bus capacitance and speed. This clause closely follows the QSFP+ SFF-8679 specification [8]. This specification also defines tBUF timing, tWR timing, tNACK timing, tBPC timing.

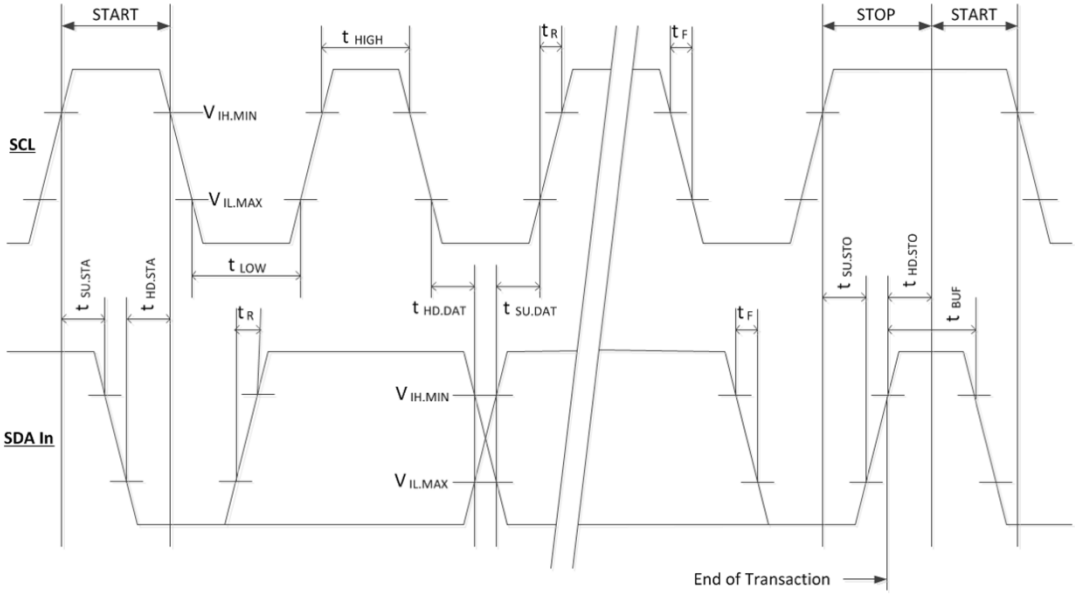

Figure 6-10: TWI Timing Diagram

6.5.2 TWI(I2C) Bus Pull Up Resistor

The maximum SCL/SDA pull resistors is based on the total bus capacitance, operating voltage, and the bus speed. Analysis is based on I2C specifications [9] with some exception, the ViH/ViH in PCIe OptiLink are based on [0.75/0.25]*VCC3.3V instead of [0.7/0.3]*VCC3.3V as specified in the I2C specifications. PCIe OptiLink maximum bus capacitance and pull up resistor will be slightly lower than the I2C specifications. Figure 6-5 show maximum bus capacitance as function of rise time for several pull up resistors. Figure 6-12 show maximum pull up resistor Rp for Fast-mode and Fast-mode plus as function of total bus capacitance to meet the maximum rise time for Fast-mode and Fast-mode plus. In Figure 6-10 minimum Rp is limited to 1100 Ω due to Fast Mode driver capable of only sourcing (I_{OL}) ≤ 3 mA and the figure also doesn't show Rp for greater than 400 pF bus capacitance in case of Fast Mode+ with (I_{OL}) ≤ 20 mA due to excessive power dissipation (Fast-mode plus specifications allow up to 550 pF total bus capacitance [9]).

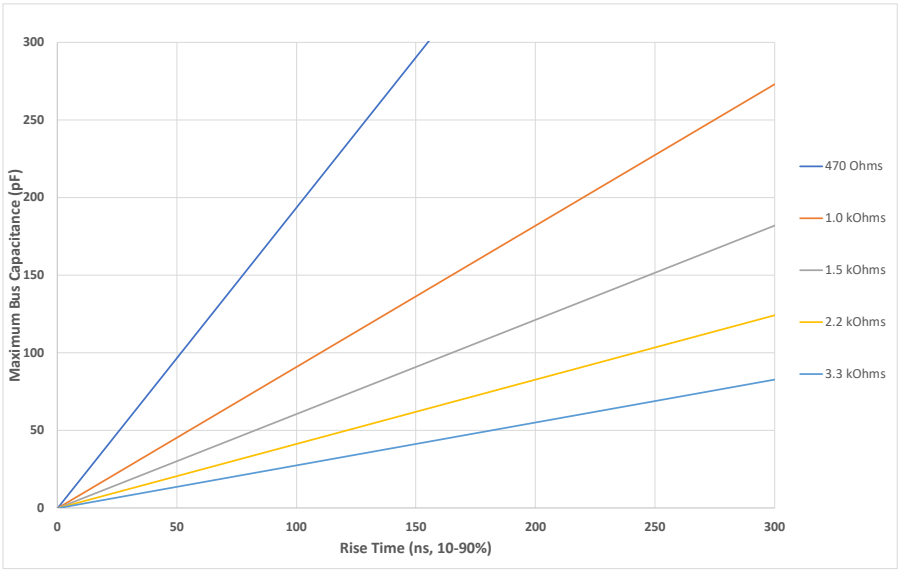

Figure 6-11: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

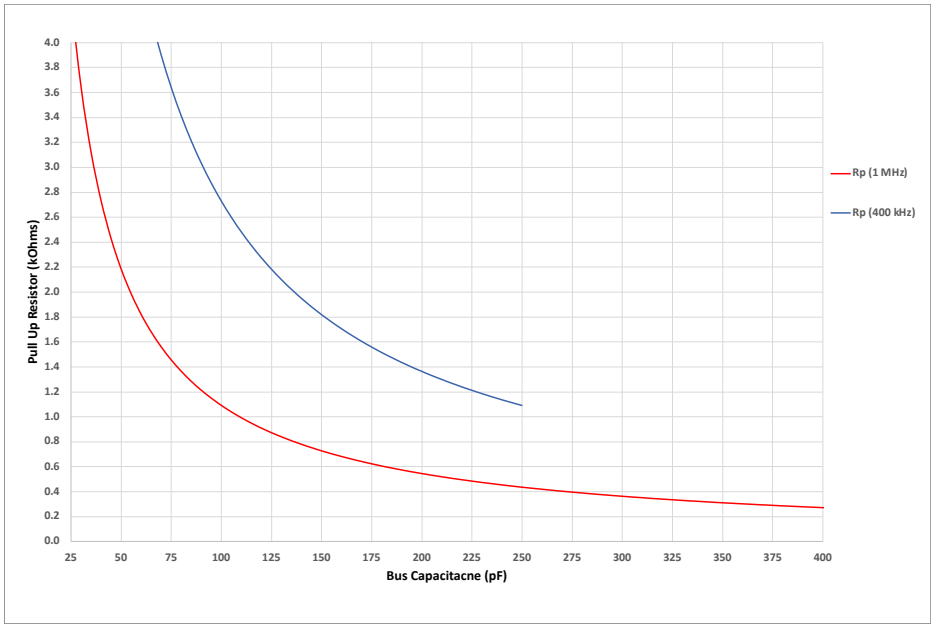

Figure 6-12: TWI Pull Up Resistor as Function of Total Bus Capacitance

Table 6-5- Management Interface timing parameters

TWI Modes		Fast Mode (400 kHz)		Fast Mode+ (1 MHz)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		20		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	t_R		300		120	ns	Maximum pullup resistor Rp (assuming ViH/ViH [0.75/0.25]*VCC), see Figure 6-12
Input Fall Time	t_F		300		120	ns	
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		µs	
Aborted sequence – bus release	Deselect _Abort		2		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the PCIe OptiLink module releasing SCL and SDA
TWI Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500		500	µs	Time the PCIe OptiLink module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to non-volatile registers	tWR		80		80	ms	Time to complete a Single or Sequential Write to non-volatile registers.
Accept a single or sequential write to volatile memory	tNACK		10		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50k		50k		cycles	Module Case Temperature = 70 ºC
Note 1: CMIS management registers can be read to determine alternate ModSelL set up and hold times. See CMIS 8.4.5, Durations Advertising.							

The TWI serial interface address of the PCIe OptiLink module is 1010000X (A0h).

6.5.3 Timing for soft control and status functions

Timing for PCIe OptiLink soft control status functions are described in Table 6-6. Squelch and disable timings are defined in Table 6-7.

1 **Table 6-6: Timing for PCIe OptiLink soft control and status functions**

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1], hot plug or rising edge of reset until until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.
ResetLs Assert Time	t_reset_init	200		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntLs Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntLs.
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[2] operation of associated flag. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
RxLOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntLs asserted [3].
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntLs asserted [3].
RxLOS Deassert Time (optional fast mode)	toff_f_LOS		3	ms	Optional fast mode is advertised via the CMIS. Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high.
TX Disable Assert Time	ton_TxDis		100	ms	Time from Tx Disable bit set to 1 until output falls below 10% of nominal.
TX Disable Assert Time (optional fast mode)	ton_f_TxDis		3	ms	Optional fast mode is advertised via CMIS. Time from TxDis signal high to the optical output reaching the disabled level.
TX Disable Deassert Time	toff_TxDis		400	ms	Time from Tx Disable bit cleared to 1 until output rises above 90% of nominal [4].
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntLs asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntLs asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b) [5] until associated IntLs assertion is inhibited.
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b) [5] until associated IntLs operation resumes
ResetLs Pulse Duration	t_reset_pulse	180	220	µs	Duration of time when SDA is pulled low by host to indicate a Reset signal to the module
ResetLs Repeat Time	t_reset_repeat	180	220	µs	Duration of time when SDA is high during a repeated Reset condition
IntLs Pulse Duration	t_intl_pulse	80	120	µs	Duration of time when SDA is pulled low by the module to indicate an interrupt to the host
IntLs Repeat Time	t_intl_repeat	180	220	µs	Duration of time when SDA is high during a repeated interrupt condition
Data Path Tx Turn On Max Duration[6]	DataPathTxTurnOn_MaxDuration				see CMIS memory P01h: B168
Data Path Tx Turn Off Max Duration[6]	DataPathTxTurnOff_MaxDuration				see CMIS memory P01h: B168
Data Path Deinit Max Duration[6]	DataPathDeinit_MaxDuration				see CMIS memory P01h: B144
Data Path Init Max Duration[6]	DataPathInit_MaxDuration				see CMIS memory P01h: B144
Module Pwr Up Max	ModulePwrUp_MaxDuration				see CMIS memory P01h: B167

Duration[7]		
Module Pwr Dn Max Duration[7]	ModulePwrDn_MaxDuration	see CMIS memory P01h: B167

Notes: 1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6-10.
2. Measured from low to high SDA edge of the Stop condition of the read transaction.
3. Rx LOS condition is defined at the optical input by the relevant standard.
4. Tx Squelch Deassert time is longer than SFF-8679 [8].
5. Measured from low to high SDA edge of the Stop condition of the write transaction.
6. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntLs for the state changes, unless the module advertises a less than 1 ms duration in which case there is no defined measurement.
7. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntLs for the state changes.

1
2
3

Table 6-7: I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached, see 6.6.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached, see 6.6.2.
Tx Squelch Deassert Time	toff_Txsq	1.5	s	Tx squelch deassert is system and implementation dependent, see also 6.6.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence[1] until optical output falls below 10% of nominal.
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal, see notes 2 and 3.
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see notes 2, and 3.
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see notes 2 and 3.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.

Notes:
1. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.
2. CMIS 4.0 and beyond the listed values are superseded by the advertised DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times in P01h.168.
3. Listed values place a limit on the DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times (P01h.168) that can be advertised by such modules (for CMIS 4.0 and beyond).

4
5

6.6 High Speed Electrical Specification

For detailed PCIe OptiLink electrical specifications for operation at 64 GT/s see [4] and for operation at 128 GT/s see [6].

Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations of the following subsections 6.6.1 and 6.6.2 may be used.

6.6.1 Receive PER(n)(p/n)

PERp(n)/PERn(n) are PCIe OptiLink module receiver data output lanes. PERp(n)/PERn(n) are AC-coupled 85 Ohm differential lines that should be terminated with 85 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the PCIE OPTILINK modules and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or as defined by the relevant standard, or whichever is less.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output lane(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output lane as shown in Table 6-8. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the TWI serial interface. Rx Squelch Disable is an optional function.

6.6.2 Transmit PET(n)(p/n)

PETp(n)/PETn(n) are PCIe OptiLink module transmitter data input lanes. They are AC-coupled 85 Ω differential lines with 85 Ω differential terminations inside the PCIe OptiLink optical module. The AC coupling is implemented inside the PCIe OptiLink module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter Tx Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input lane becoming less than the TX Squelch Levels specified in Table 6-8 when terminated in to 85 Ω differential, then the transmitter optical output associated with that electrical input lane shall be squelched and the associated TxLOS flag set. If multiple electrical input lanes are associated with the same optical output lane, the loss of any of the incoming electrical input lanes causes the optical output lane to be squelched.

Table 6-8- TX Squelch Levels

Data Rate	Levels [2]	Unit
PCIe Gen5	70	mV [1]
PCIe Gen6	70	mV [1]
PCIe Gen7	50	mV [1]
1. Differential peak-peak. 2. *Editor's Note: Squelch levels are consistent with the OIF CEI 5.2 clauses 13, 16, and 25 but need confirmation if these levels are applicable to PCI Express.*		

For implementations, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended. For implementations, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended. In modules, where

Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the TWI serial interface. Tx Squelch and Tx Squelch Disable are optional functions.

6.7 Power Requirements

The PCIe OptiLink module paddle card power supply has two designated pads VCC3.3V and VCC12V in the connector.

A host board together with the PCIe OptiLink module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion or module state transitions.

All power supply requirements in Table 6-10 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

6.7.1 Power Classes and Maximum Power Consumption

There are two power modes: Low Power Mode and High Power Mode, and total of eight power classes, Class 1 - Class 8. Module power classes are defined in Table 6-9 and module power specifications are provided in Table 6-10.

Since a wide range of module power classes exist, to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to accommodate only low power consumption modules, it is recommended that host systems designed to accommodate only low power consumption modules also implement the state machine defined in the CMIS [11] and identify the power class of the module before allowing the module to go into High Power Mode, where power class 8 requires reading CMIS (Page00, Byte 201) to determine actual power consumption. This is to avoid exceeding the host system power supply limits and cooling capacity when a module exceeding the power class supported by the system is inserted.

Table 6-9- Module Power Classes

Power Class	Max Power (W)	Module Supply	CMIS Register
1	1.5	VCC3.3V	Direct readout of Page 00h Byte 200[000xxxxx]
2	3.5	VCC3.3V & VCC12V	Direct readout of Page 00h Byte 200[001xxxxx]
3	7.0	VCC3.3V & VCC12V	Direct readout of Page 00h Byte 200[010xxxxx]
4	8.0	VCC3.3V & VCC12V	Direct readout of Page 00h Byte 200[011xxxxx]
5	10	VCC3.3V & VCC12V	Direct readout of Page 00h Byte 200[100xxxxx]
6	12	VCC3.3V & VCC12V	Direct readout of Page 00h Byte 200[101xxxxx]
7	14	VCC3.3V & VCC12V	Direct readout of Page 00h Byte 200[110xxxxx]
8 [1]	>14	VCC3.3V & VCC12V	Direct readout of Page 00h Byte 200[111xxxxx]
Note: 1. When a module reports power class 8 the host must read CMIS Page 00h Byte 201 to determine module power dissipation. Please see CMIS Byte 201 register definition for more information.			

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements. Utilization of the maximum PCIe OptiLink power rating requires thermal design and validation at the system level to ensure the maximum module temperature is not exceeded, see SFF-TA-1032 Connector Performance [7]. A recommended design practice for host supporting power class 8 (>14 W) is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.

6.7.2 Host Board Power Supply Filtering

The specification of the host power supply filtering network is beyond the scope of this specification, particularly because of the wide range of module Power Classes. During power transient events, the host should ensure that any neighboring modules sharing the same supply stay within their specified supply voltage limits. The host should also ensure that the intrinsic noise of the power rail is filtered in order to guarantee the correct operation of the optical modules. An example reference power supply filter is shown in Figure 6-13.

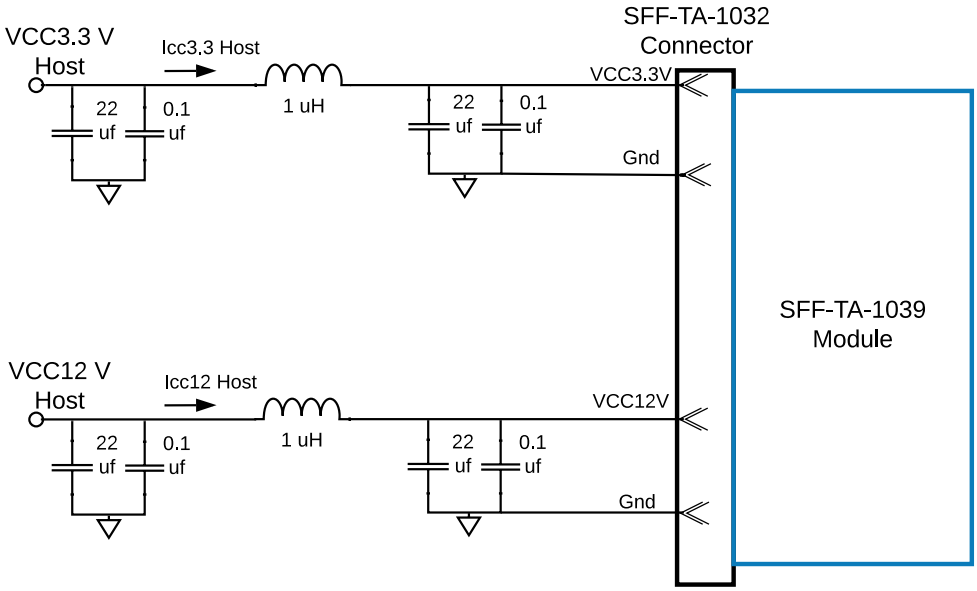

Figure 6-13: Reference Power Supply Filter for Module Testing

Any voltage drops across a filter network on the host is counted against the host DC set point accuracy specification. System designers should choose components with appropriate DCR and ESR, to minimize the voltage drop and the amount of noise coupled to the module. Hosts supporting higher power classes modules may require additional design considerations, in order to minimize the voltage drop and the amount of noise coupled to the module.

The specifications for the PCIe OptiLink power supply are shown in Table 6-10. The limits in Table 6-10 apply to the combined current that flows through all inductors in the power supply filter (represents host Icc3.3 and Icc12 current in Figure 6-13). Inrush current shall be measured with the appropriate equipment, such as current probes or shunt resistors. The test equipment shall provide enough bandwidth, vertical resolution, SNR and memory depth, in order to capture properly all the power events.

6.7.3 Module Power Supply Specification

PCIe OptiLink has no dedicate hardware pin for the LPMode signal. As per CMIS 5.3 [11] the PCIe OptiLink module therefore behaves as if the LowPwrRequestHW signal is constantly ASSERTED in order to avoid exceeding the host system power capacity. Figure 6-14 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power classes are given in Table 6-10.

The module shall not be affected by the instantaneous variations of the power supply caused by its own current drawing profile during all power transient events. The module shall limit maximum instantaneous slew rate to 175 mV/ms on VCC3.3V and VCC12V power supplies. No traffic hits or TWI errors shall be observed as the result of power supplies variations.

Table 6-10- Power supply specifications, instantaneous, sustained, and steady state current limits

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VCC3.3V including ripple, droop and noise below 100 kHz[1]		3.135	3.3	3.465	V
Power supply voltages VCC12V including ripple, droop and noise below 100 kHz[1]		11.4	12	12.6	V
Module inrush - instantaneous peak duration[2]	T_ip			50	µs
Module inrush - initialization time[2]	T_init			500	ms
Low Power Mode for all modules and Power Class 1 module					
Power Consumption Class	P_1			1.5	W
Instantaneous peak current at hot plug (VCC3.3V)	Icc_ip_1	-	-	600	mA
Sustained peak current at hot plug (VCC3.3V)	Icc_sp_1	-	-	495	mA
Steady state current (VCC3.3V)	Icc_1_3.3V	See Note 3			mA
High Power Mode Power Class 2 module					
Power Consumption Class	P_2			3.5	W
Instantaneous peak current (VCC3.3V)	Icc_ip_2_3.3 V	-	-	P_2_3.3/2.5	mA
Instantaneous peak current (VCC12V)	Icc_ip_2_12 V	-	-	P_2_12/9.1	mA
Sustained peak current (VCC3.3V)	Icc_sp_2_3.3 V	-	-	P_2_3.3/3.03	
Sustained peak current (VCC12V)	Icc_sp_2_12 V	-	-	P_2_12/11.02	
Steady state current (VCC3.3V and VCC12V)	Icc_2_3.3V/12V	See Note 3			mA
High Power Mode Power Class 3 module					
Power Consumption Class	P_3			7	W
Instantaneous peak current (VCC3.3V)	Icc_ip_3_3.3V	-	-	P_3_3.3/2.5	mA
Instantaneous peak current (VCC12V)	Icc_ip_3_12V	-	-	P_3_12/9.1	mA
Sustained peak current (VCC3.3V)	Icc_sp_3_3.3V	-	-	P_3_3.3/3.03	
Sustained peak current (VCC12V)	Icc_sp_3_12V	-	-	P_3_12/11.02	
Steady state current (VCC3.3V and VCC12V)	Icc_3_3.3V/12V	See Note 3			mA
High Power Mode Power Class 4 module					
Power Consumption Class	P_4			8	W
Instantaneous peak current (VCC3.3V)	Icc_ip_4_3.3V	-	-	P_4_3.3/2.5	mA
Instantaneous peak current (VCC12V)	Icc_ip_4_12V	-	-	P_4_12/9.1	mA
Sustained peak current (VCC3.3V)	Icc_sp_4_3.3V	-	-	P_4_3.3/3.03	
Sustained peak current (VCC12V)	Icc_sp_4_12V	-	-	P_4_12/11.02	
Steady state current (VCC3.3V and VCC12V)	Icc_4_3.3V/12V	See Note 3			mA
High Power Mode Power Class 5 module					
Power Consumption Class	P_5			10	W
Instantaneous peak current (VCC3.3V)	Icc_ip_5_3.3V	-	-	P_5_3.3/2.5	A
Instantaneous peak current (VCC12V)	Icc_ip_5_12V	-	-	P_5_12/9.1	A
Sustained peak current (VCC3.3V)	Icc_sp_5_3.3V	-	-	P_5_3.3/3.03	A
Sustained peak current (VCC12V)	Icc_sp_5_12V	-	-	P_5_12/11.02	A
Steady state current (VCC3.3V and VCC12V)	Icc_5_3.3V/12V	See Note 3			A
High Power Mode Power Class 6 module					
Power Consumption Class	P_6			12	W
Instantaneous peak current (VCC3.3V)	Icc_ip_6_3.3V	-	-	P_6_3.3/2.5	A
Instantaneous peak current (VCC12V)	Icc_ip_6_12V	-	-	P_6_12/9.1	A
Sustained peak current (VCC3.3V)	Icc_sp_6_3.3V	-	-	P_6_3.3/3.03	A
Sustained peak current (VCC12V)	Icc_sp_6_12V	-	-	P_6_12/11.02	A
Steady state current (VCC3.3V and VCC12V)	Icc_6_3.3/12V	See Note 3			mA
High Power Mode Power Class 7 module					
Power Consumption Class	P_7			14	W
Instantaneous peak current (VCC3.3V)	Icc_ip_7_3.3V	-	-	P_7_3.3/2.5	A
Instantaneous peak current (VCC12V)	Icc_ip_7_12V	-	-	P_7_12/9.1	A

Sustained peak current (VCC3.3V)	Icc_sp_7_3.3V	-	-	P_7_3.3/3.03	A
Sustained peak current (VCC12V)	Icc_sp_7_12V	-	-	P_7_12/11.02	A
Steady state current (VCC3.3V and VCC12V)	Icc_7_3.3V/12V	See Note 3			mA
High Power Mode Power Class 8 module					
Power Consumption Class	P_8 [4]			>14	W
Instantaneous peak current (VCC3.3V)	Icc_ip_8_3.3V	-	-	P_8_3.3/2.5	A
Instantaneous peak current (VCC12V)	Icc_ip_8_12V	-	-	P_8_12/9.1	A
Sustained peak current (VCC3.3V)	Icc_sp_8_3.3V	-	-	P_8_3.3/3.03	A
Sustained peak current (VCC12V)	Icc_sp_8_12V	-	-	P_8_12/11.02	A
Steady state current (VCC3.3V)	Icc_8_3.3V	-	-	3	A
Steady state current (VCC12V)	Icc_8_12V	-	-	3	A
Notes: 1. Measured at VCC3.3V and VCC12V 2. T_ip and T_init are test conditions for measuring inrush current and not characteristics of the module 3. Any combination of Icc_x_3.3V and Icc_x_12V currents that meets the declared power class is acceptable. 4. P_8 is the module power dissipation reported by CMIS Byte 201.					

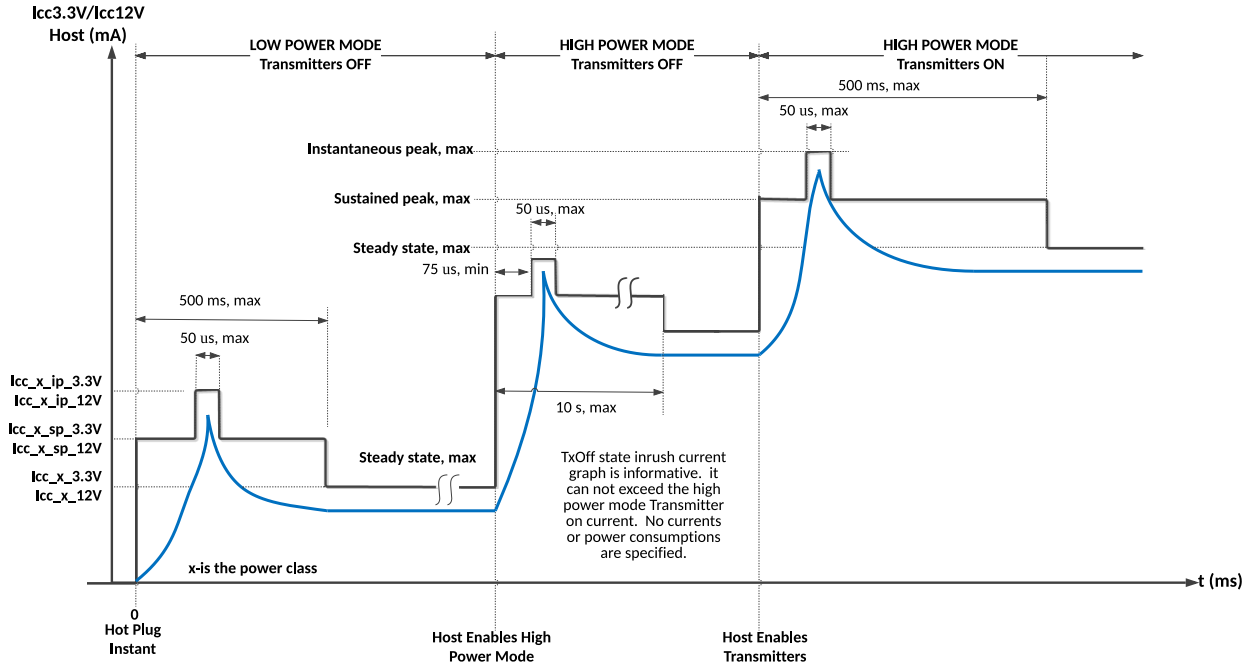

Figure 6-14: Instantaneous and sustained peak currents for Icc3.3V/Icc12V Host (see Table 6-10)

6.7.4 Host and Module Output Noise

Host output noise limit, module output noise limit, and module input noise tolerance limit are given in Table 6-11.

Table 6-11- Host and Module Output Noise and Tolerance Specifications

Parameter	Symbol	Min	Nom	Max	Unit
Host VCC3.3V RMS noise output 40 Hz-10 MHz (eN_Host)[1]				25	mV
Module VCC3.3V RMS noise output 40 Hz - 10 MHz [2]				150	mA
Module VCC3.3V sinusoidal power supply noise tolerance 40 Hz - 10 MHz (p-p) [2, 3]	$PSNR_{mod}$			66	mV
Host VCC12V RMS noise output 40 Hz-10 MHz (eN_Host)[1]				100	mV
Module VCC12V RMS noise output 40 Hz - 10 MHz [2]				150	mA
Module VCC12V sinusoidal power supply noise tolerance 40 Hz - 10 MHz (p-p) [2, 3]	$PSNR_{mod}$			240	mV

1. Host must be tested for all supported power classes.
2. Module must be test at low and high power modes.
3. Recommended test frequencies:
   40, 50, 60, 70, 80, 90 Hz
   100, 200, 300, 400, 500, 600, 700, 800, 900 Hz
   1, 2, 3, 4, 5, 6, 7, 8, 9 kHz
   10, 20, 30, 40, 50, 60, 70, 80, 90 kHz
   100, 200, 300, 400, 500, 600, 700, 800, 900 kHz
   1, 2, 3, 4, 5, 6, 7, 8, 9, 10 MHz.

6.7.5 Host Board Power Supply Noise Output

The host noise output on VCC3.3V and VCC12V supplies are defined with resistive loads that draws the maximum rated power supported by the host power class, see Figure 6-15. The resistive loads are connected in place of the module between VCC3.3V and VCC12V and the Vee. When the noise is measured on the two voltage rails VCC3.3V and VCC12V, the noise is measured independently on each rail, and the voltage rails not being tested are left open circuit. Host power supply limits are given in Table 6-9. The noise power spectrum is measured for each of the 2 rails then integrated from 40 Hz to 10 MHz and converted to a voltage, eN_Host, with limit specified in Table 6-11 for each of the rails.

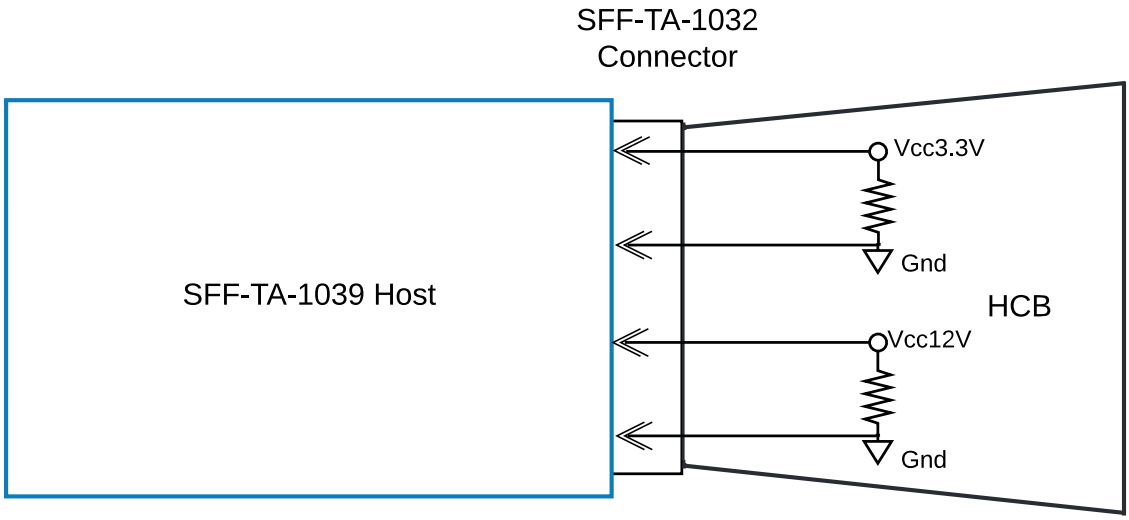

Figure 6-15: Host Noise Output Measurement

6.7.6 Module Power Supply Noise Output

The PCIe OptiLink modules (SFF-TA-1039), when plugged into a reference module compliance board shall generate noise current less than the value in Table 6-11. The module must pass module power supply noise output current test in all operating modes. This test ensures the module will not couple excessive noise from in- side the module back onto the host board. This improved test method uses a current probe with a scope capable of integrating the current noise from 40 Hz to 10 MHz.

Rogowski probes are recommended because they will minimize added interconnect inductance, example of such probes are Tektronix TRCP series, Keysight N7042A or similar. Hall-effect current probes may also be acceptable if added interconnect is negligible, example of such probes are Tektronix TCP, Keysight N1147B.

The RMS module noise current output for each of the rails is defined in the frequency band from 40 Hz to 10 MHz. Module noise current output shall be measured with a current probe at point X, see Figure 6-16 (capacitors are removed for noise measurement) and must meet limits given in Table 6-11 for each of the rails. The leads from point X or Y to the system power supply must be kept as short as possible to minimize the impact of added lead inductance. The module must pass module power supply noise output test in all operating modes. This test ensures the module will not couple excessive noise from inside the module back onto the host board.

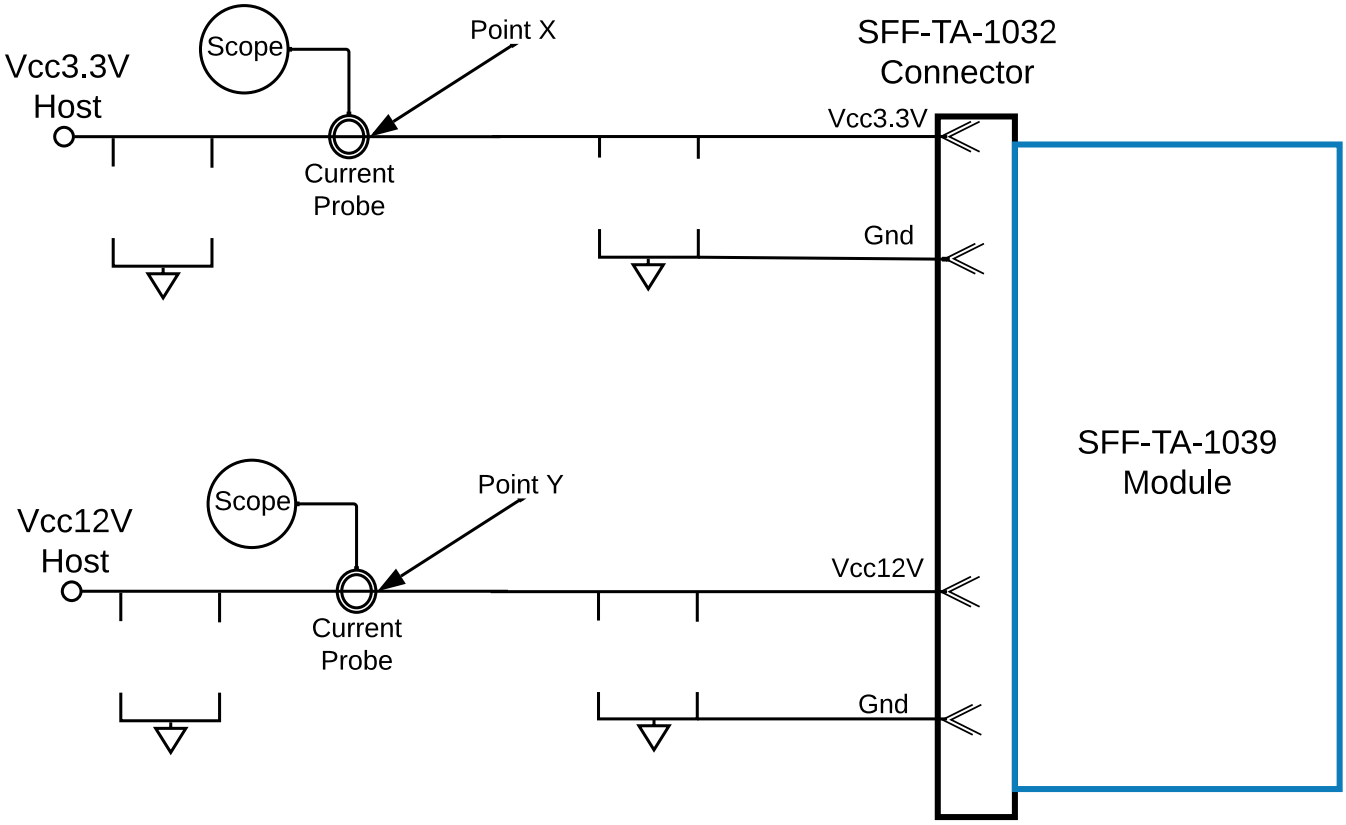

Figure 6-16: Module Noise Output Measurement

6.7.7 Module Power Supply Noise Tolerance

The PCIe OptiLink modules (SFF-TA-1039) shall meet all requirements and operate within the design specifications in the presence of a reference noise waveform described in Table 6-11 superimposed on the DC voltage. The reference noise waveform consists of a sinusoidal 40 Hz to 10 MHz noise generated by Osc1 and added to VCC3.3V or VCC12V PSU, see Figure 6-17. This emulates the worst-case noise that the module must tolerate and operate within the design specifications. The reference noise is generated by Osc1 and amplified by the Power OpAmp then added to VCC3.3V or VCC12V PSU through a Bias-T, see Figure 6-17 (capacitors are removed for noise

measurement). Example of suitable Power OpAmp1/OpAmp2 are Analog Devices ADA4870 (EOL and may not be available) and LT1210, and TI THS3491. With power supply filter components removed, point X or Y measures the noise voltage applied to the module. To facilitate power supply tolerance testing at frequencies < ~100 kHz due to Power OpAmp interaction with PSU and low frequency response of the Bias-T, it is recommended to use noise source Osc2 modulating PSU sense line to generate sinusoidal noise directly on the PSU output, see Figure 6-18 (capacitors are removed for noise measurement). Osc2 amplitude level is adjusted while observing point X or Y amplitudes level as defined in Table 6-11 or module in low power and high-power modes. To modulate the PSU sense lines, the PSU must have high speed sense tracking. An example of PSU with high-speed sense tracking are TI TPSM5D1806 and Keysight N6700 with N6781/N6782 plugins.

For modules without or with limited input stage power filtering one may measure the applied noise to the module by measuring point X or Y directly while the module is active and either in low or high-power modes. To compensate for input stage power filtering in the module, the DUT module is replaced with a resistive load drawing equivalent current of a module configured in low power mode, the DUT module is then replaced with a resistive load drawing equivalent current of a module configured in high power mode. Osc1 is adjusted to produce maximum PSNR level as defined in Table 6-11 at point X or Y with resistive loads drawing the same power as the module in low and high-power modes. The resistive loads are then replaced with the DUT module with the same Osc1 amplitude settings that produced the max PSNR with the resistive loads.

Notes: The user is responsible for the calibration and the validation of the setup across the whole frequency range. An appropriate probing technique is required for noise measurement at point X and Y, see [17] and [18]. Depending on the measurement setup, a ground loop isolator may be required. For modules with limited or no decoupling directly connected to host PSU, the PSNR can be directly measured at point X or Y with module plugged into the host for module operating in low power and high power modes. Osc1 adjusted to provide maximum PSNR at point X or Y for a given module in low power and full power modes.

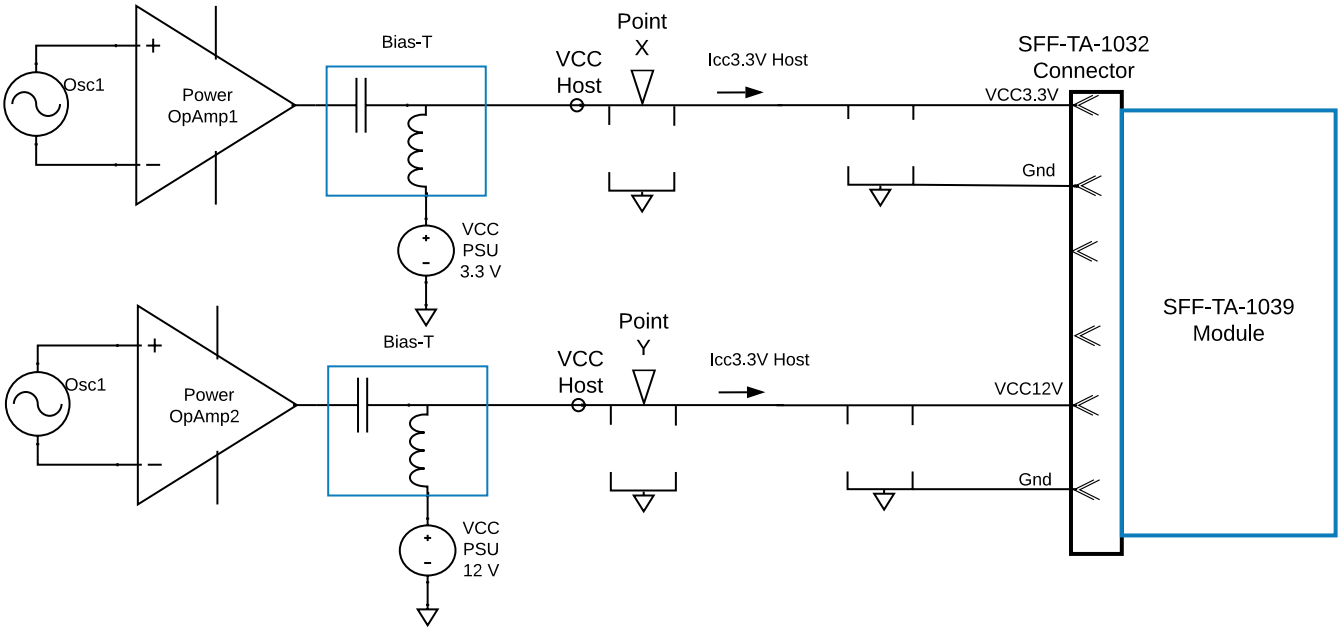

Figure 6-17: Module High Frequency Noise Tolerance

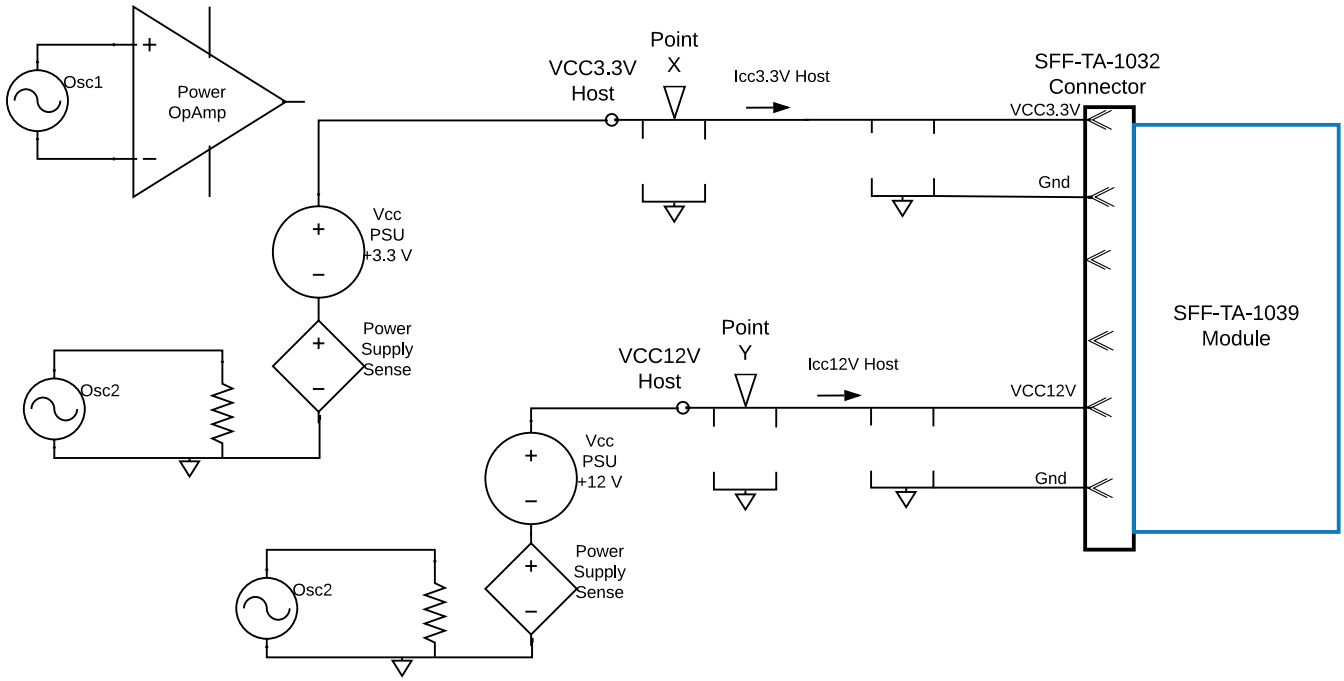

Figure 6-18: Module Low Frequency Noise Tolerance

6.7.8 Module Power Supply Noise Tolerance with Commercial Injector Probe

Module Power Supply Noise Tolerance implementation of 6.7.7 can be replaced with commercially produced injector probes, an example of such broadband injector probe is Picotest P2124A, Figure 6-19 (capacitors are removed for noise measurement) [17]. Injector probe combines a power rail voltage (input voltage) with a modulation signal and injects the noisy bus voltage into the module being tested for noise immunity (PSNR). The form factor of injector probe is such that it can be positioned at the card edge, eliminating power cables and the inductance that can limit the modulation amplitude and bandwidth. This modulation scheme supports the full 40 Hz-10 MHz range without having to change setups at ~100 kHz.

The probe-based implementation supports the requirements by getting close enough to the module under test to allow modulating up to 10 MHz with little attenuation. The DC input power supply voltage at the host can be held constant using a supplied remote sense filter. The remote sense filter allows the user to switch between different operating modes (high power, low power etc.) while keeping the operating point stable across every power state transition. With the appropriate PSU unit and remote filtering, the injector probe will compensate for any additional voltage drop due to the modulator and the interconnects.

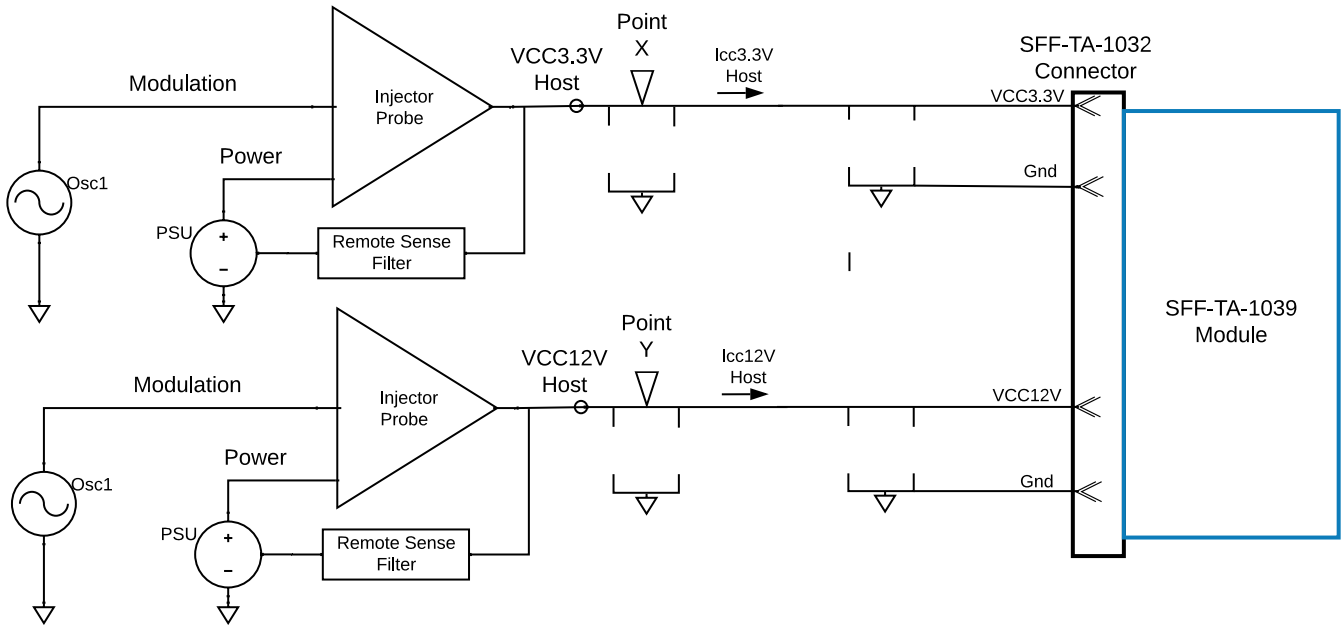

Figure 6-19: Broadband Noise Tolerance Injection Probe Setup

Injection Probe Setup Guideline, see [17] and [18]

- Injection probe may have sense line for optional remote sense.
- The modulated RF signal can be any 50 Ohm generator.
- Usage of a remote sense filter to adjust the power supply voltage level is recommended.
- Benchtop power supply with greater than 12.6 V output range with sufficient current capabilities and with sense line.

6.8 Clocking Considerations

6.8.1 Data Path Description

Within a module, host electrical and module media lanes are grouped together into a logical concept called a data path. A data path is intended to represent a group of lanes over which a block of data is distributed that will be powered up or down and initialized together. Some examples include a X4 to X4 module implementation, where the data path would include four host electrical lanes and four module media lanes, or a X16 to X16 module implementation, where the data path would include sixteen host electrical lanes and sixteen module media lanes.

6.8.2 Tx Clocking Considerations

Within a given Tx data path (x4, x8, or x16) the host is responsible for ensuring that all electrical lanes delivered to the module are frequency synchronous (sourced from the same clock domain). If a module supports multiple Tx data paths (2 instances of x4 in x8 module, 4 instances of x4 in x16 module, or 2 instances of x8 in x16 module) running concurrently, the different Tx data paths can either all be in a single clock domain or separate clock domain. The module advertises which of these two modes it supports via the management registers.

If the module supports multiple Tx data paths running concurrently in a single clock domain, the module shall ensure that active Tx data paths continue to operate undisturbed even as other Tx data paths (and their associated Tx input lanes) are enabled/disabled by the host.

6.8.3 Rx Clocking Considerations

Within a given Rx data path (x4, x8, or x16) all lanes received on the module media interface are required to be frequency synchronous (sourced from the same clock domain). If a module supports multiple Rx data paths running concurrently, the module shall allow the different Rx data paths to be asynchronous from each other (sourced from separate clock domains).

6.9 ESD

Where ESD performance is not otherwise specified, e.g., in the Ethernet specification, the PCIe OptiLink modules shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case. All the PCIe OptiLink (SFF-TA-1039) modules and host pads including high speed signal pads shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JS-001 [15] and IEC EN61000-4-2 [16].