New Project Proposal

ULP Gen7 PCIe Connector SFF-TA-1041

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TE Connectivity
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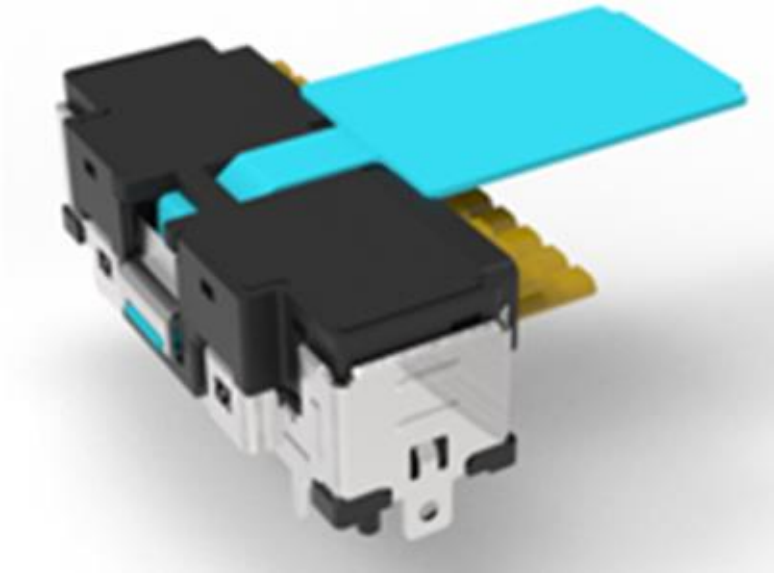
Rev 4.0

New Project Proposal: ULP Gen7 PCIe Connector

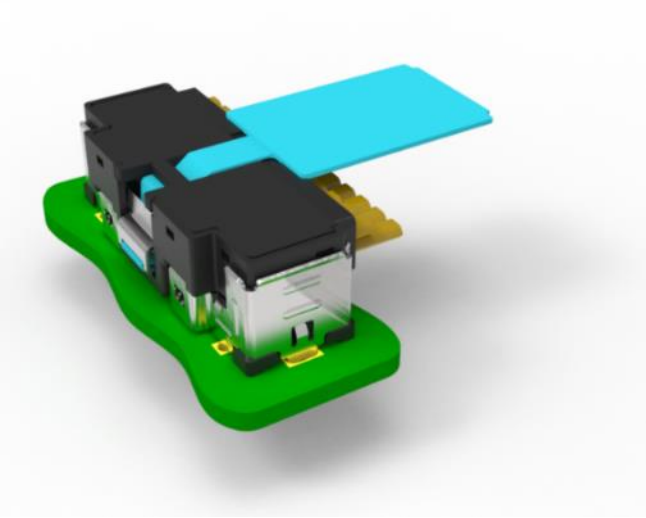
- Purpose of the new SFF project is to define a new PCIe Gen7 connector
  - A new form factor offers the superior SI performance for PCIe Gen7 and addresses the need for low-profile application without sacrificing the board space
  - SMT style receptacle with 85ohm nominal impedance
  - 2pcs connector cabling solution to remove the PCB paddle card from the assembly
  - Consolidated 18DP of high-speed and 16 sidebands into one solution to support PCIe applications. The intention is to support x8 but not limit the scope of this project to solely x8 applications.
- Editor: Olaotan Elenitoba-Johnson(TE Connectivity)
- Supporters:
  1. TE Connectivity (Dan Gorenc)
  2. Molex (Egide Murisa)
  3. Juniper Networks (Jeffery Maki)
  4. ACES (Mick Felton)
  5. FIT (Alex An & Terry Little)
  6. Nvidia (David Herring)

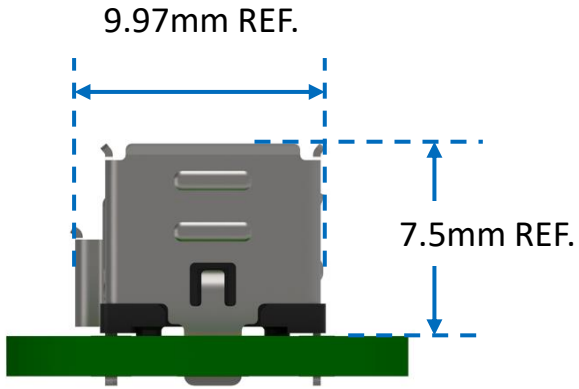
Overview

Form Factor				
Pitch	2.0mm pair to pair pitch			
Cable Plug Type	Straight	Right-Angled	Angled Exit	Lateral Exit
Board Connector Type	Vertical			
Differential Pairs	x8 (18DP+16SB), x16 is under development			
Cable AWG Supported	29-34AWG			
Electrical Specification				
Target Speed	PCIe Gen 7 and beyond			
Impedance	85Ω			

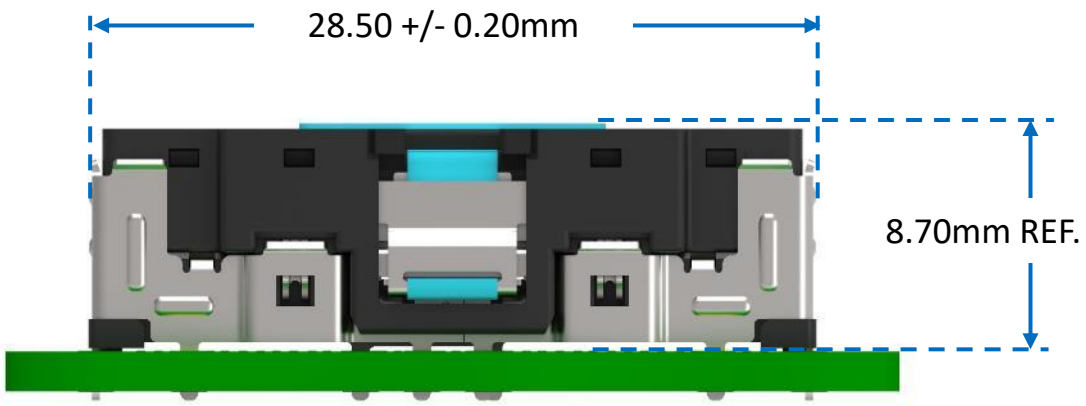


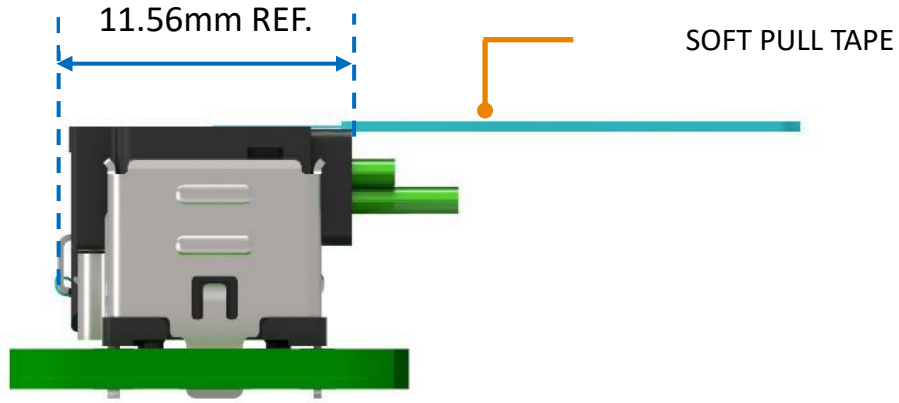
Overview of Connector Applications





THE DIMENSIONS ARE SHOWN FOR RECEPTACLE ONLY

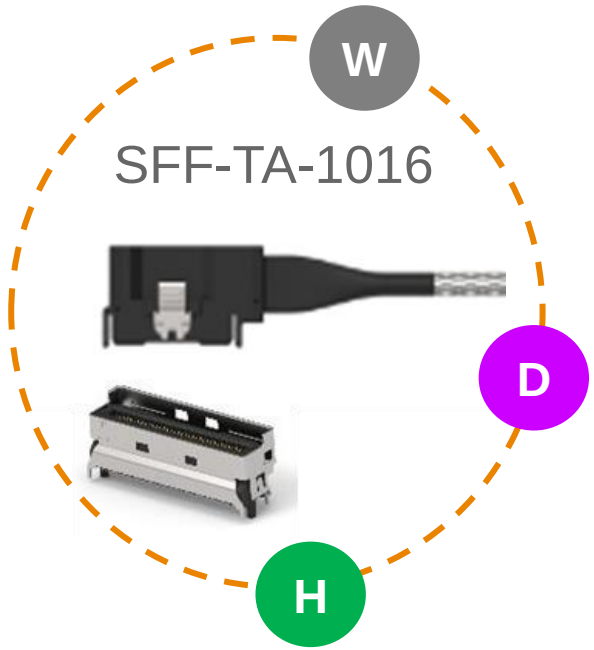


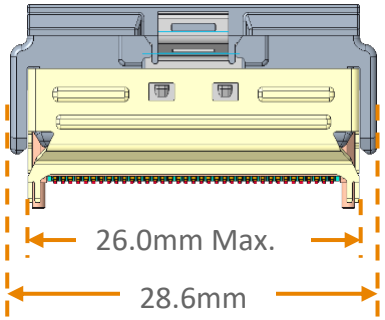


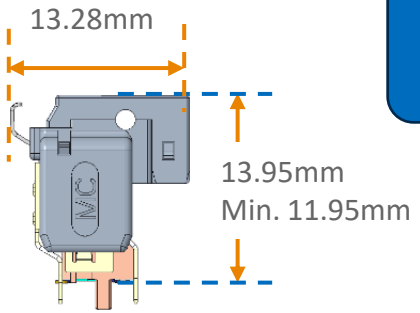
THE DIMENSIONS ARE SHOWN FOR MATING WITH RA CABLE PLUG

Mating Height and Connector Outline Dimension Comparison between x8 SFF-TA-1016 and x8 ULP Gen7

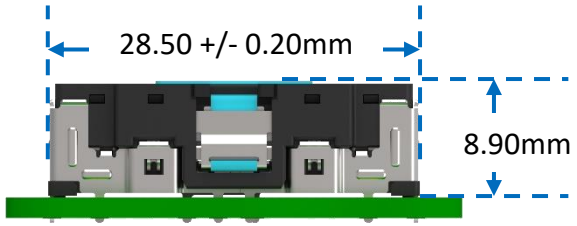
Total number of position
- 74 pins for x8 PCIe
- 16DP + 20SE

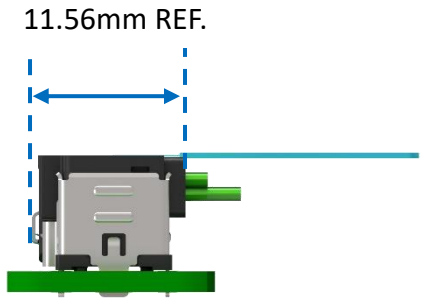




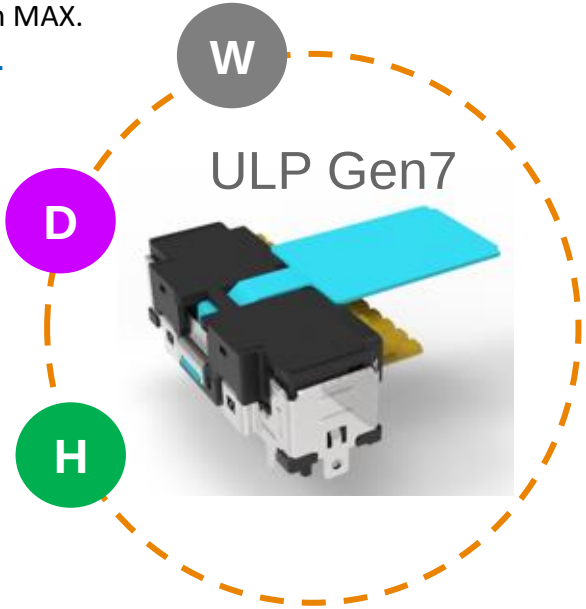


VS





Total number of position
- 18DP + 16SE for x8 PCIe



Mated Connector Outline Dimension
- 28.6mm x 13.28mm x 11.95mm min. (W x D x H)

Mated Connector Outline Dimension
- 28.5mm x 11.56mm x 8.9mm max. (W x D x H)

ULP Gen7 addresses the need for ultra low-profile application without sacrificing the board space

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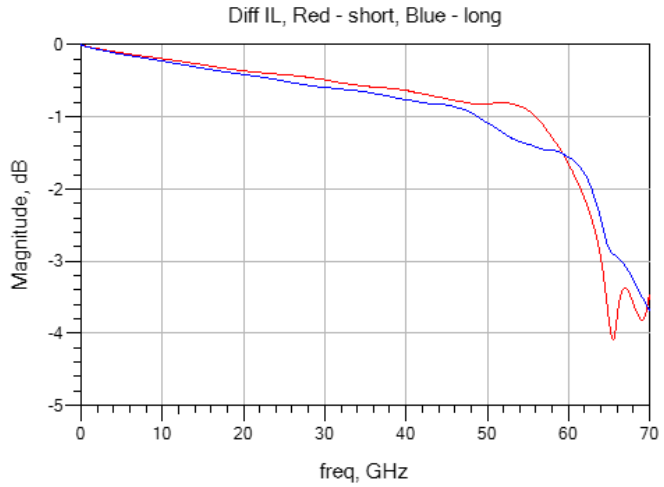
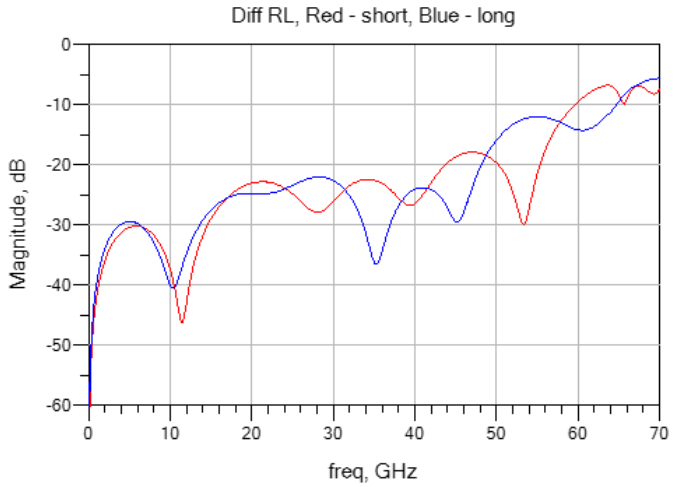
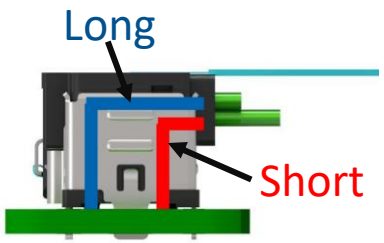
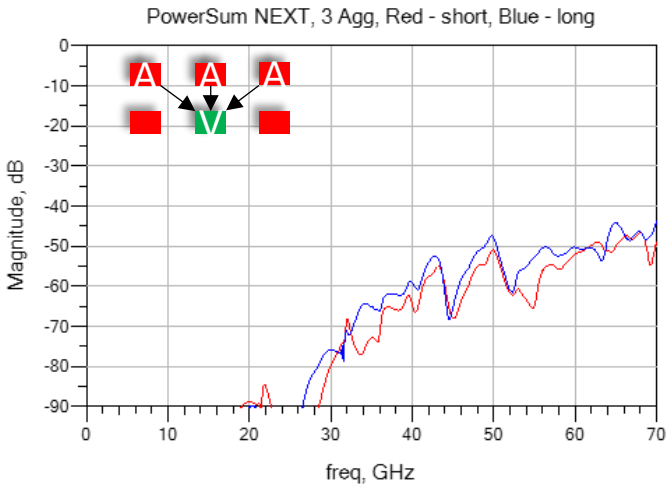
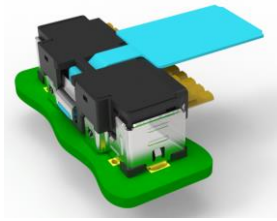
TE PCIe 7.0 Mated Connector with Cable Termination SI











Model includes Host FP + VT Rcpt + RA Plug + Cable Term + 2mm of Bulk Cable

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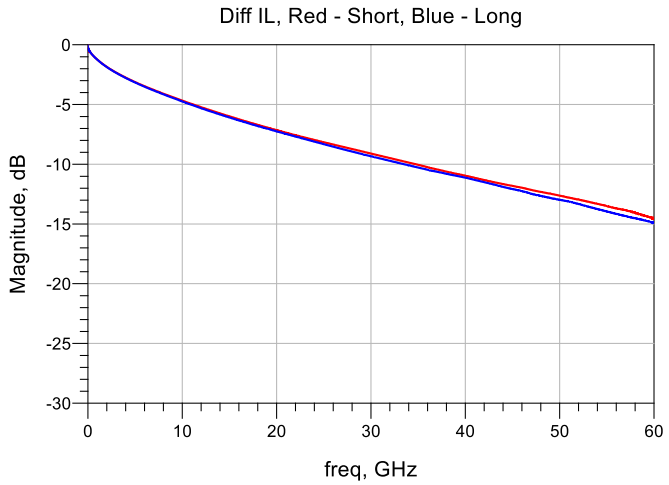
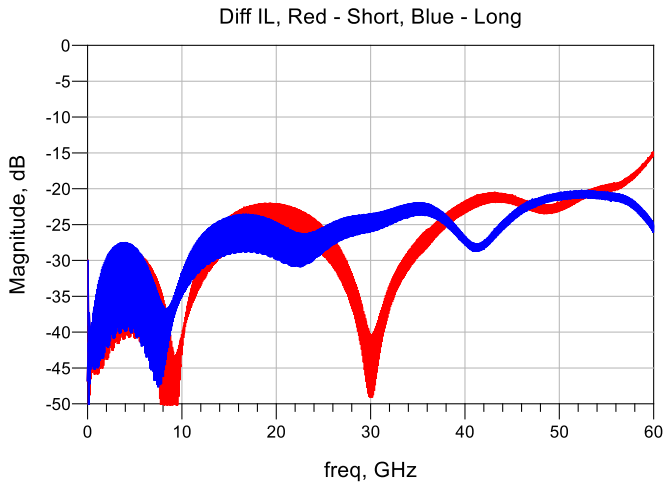
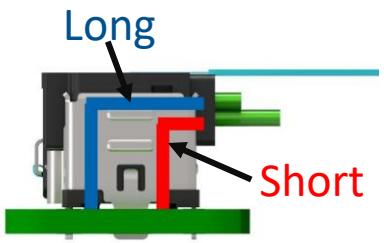
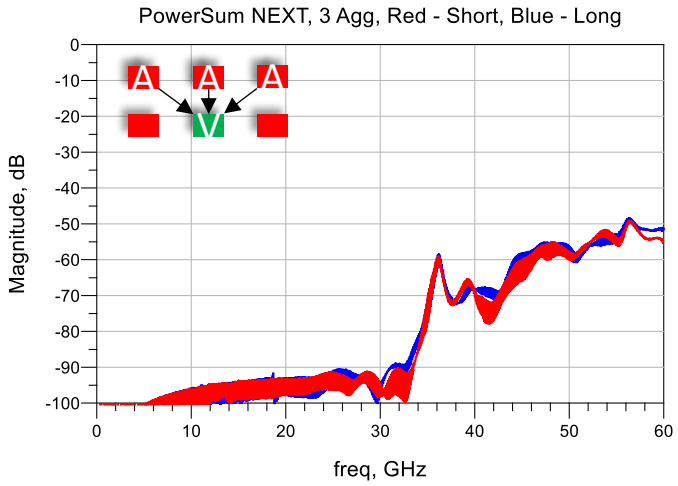
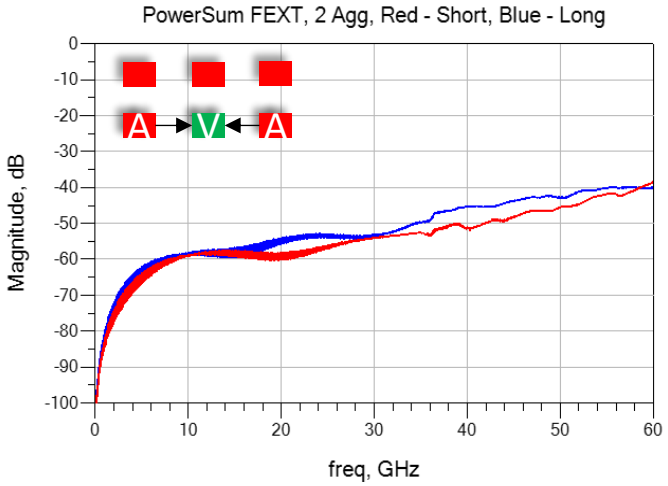
TE PCIe 7.0 1meter 30AWG CA SI Simulation Results

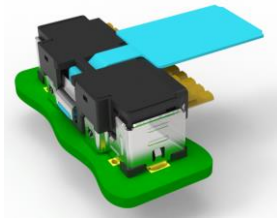












Model includes Host FP + VT Rcpt + RA Plug + 1m 30AWG Bulk Cable + RA Plug + VT Rcpt + Host FP

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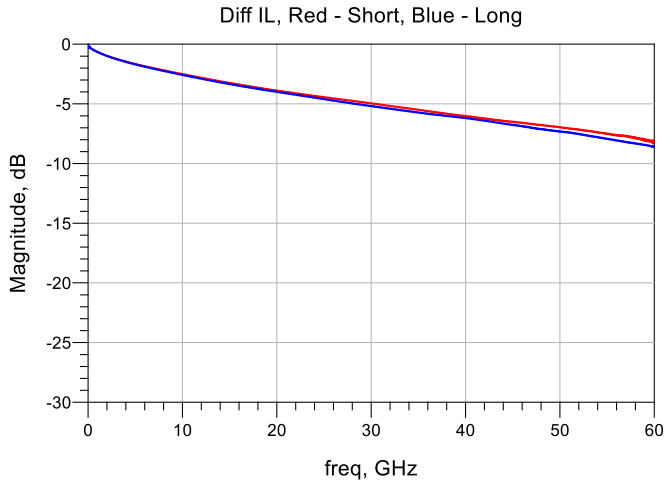
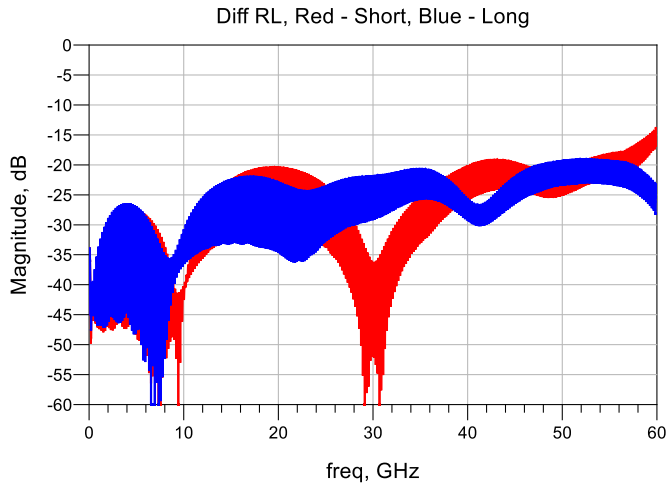
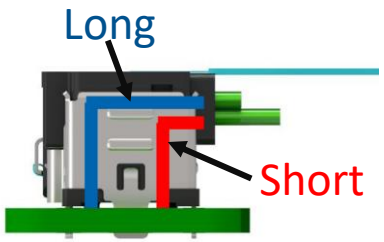
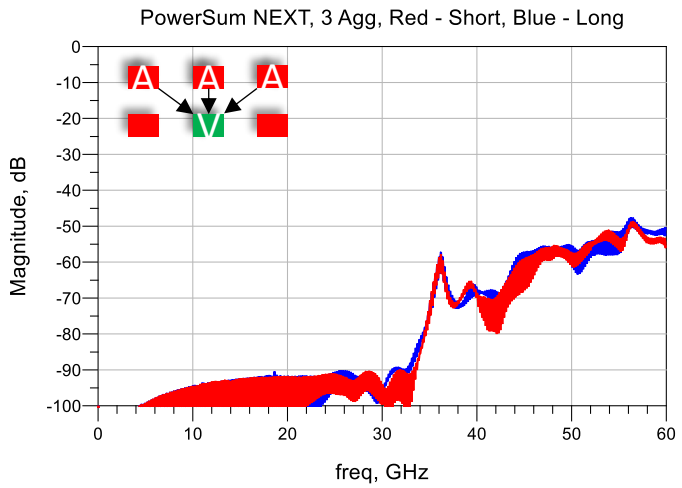
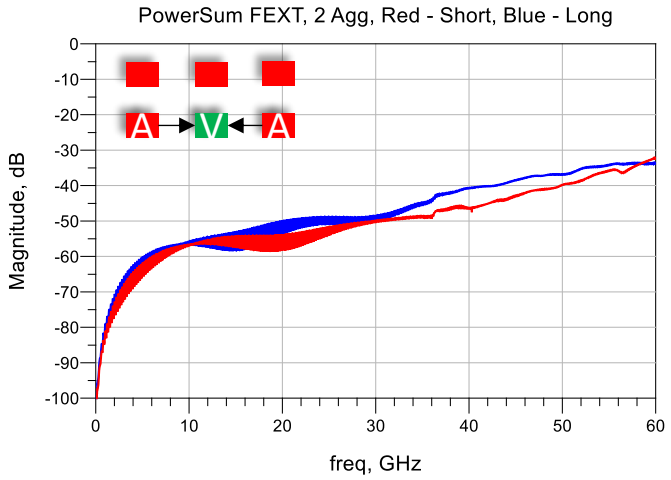
TE PCIe 7.0 0.5meter 30AWG CA SI Simulation Results

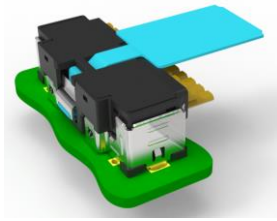












Model includes Host FP + VT Rcpt + RA Plug + 0.5m 30AWG Bulk Cable + RA Plug + VT Rcpt + Host FP

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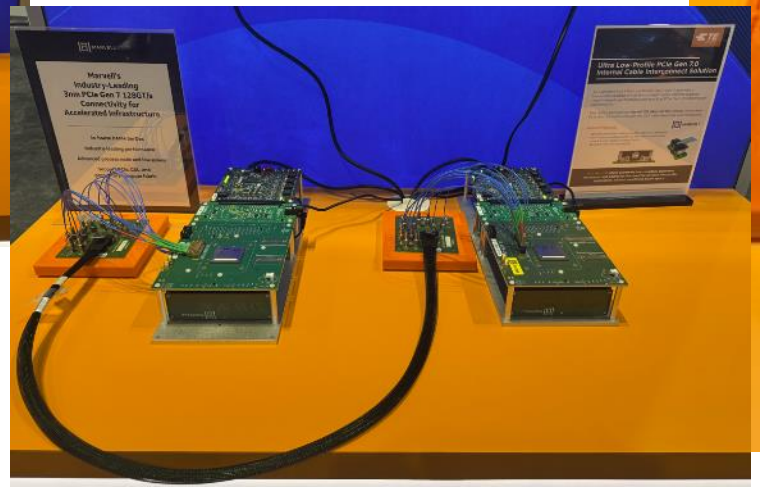
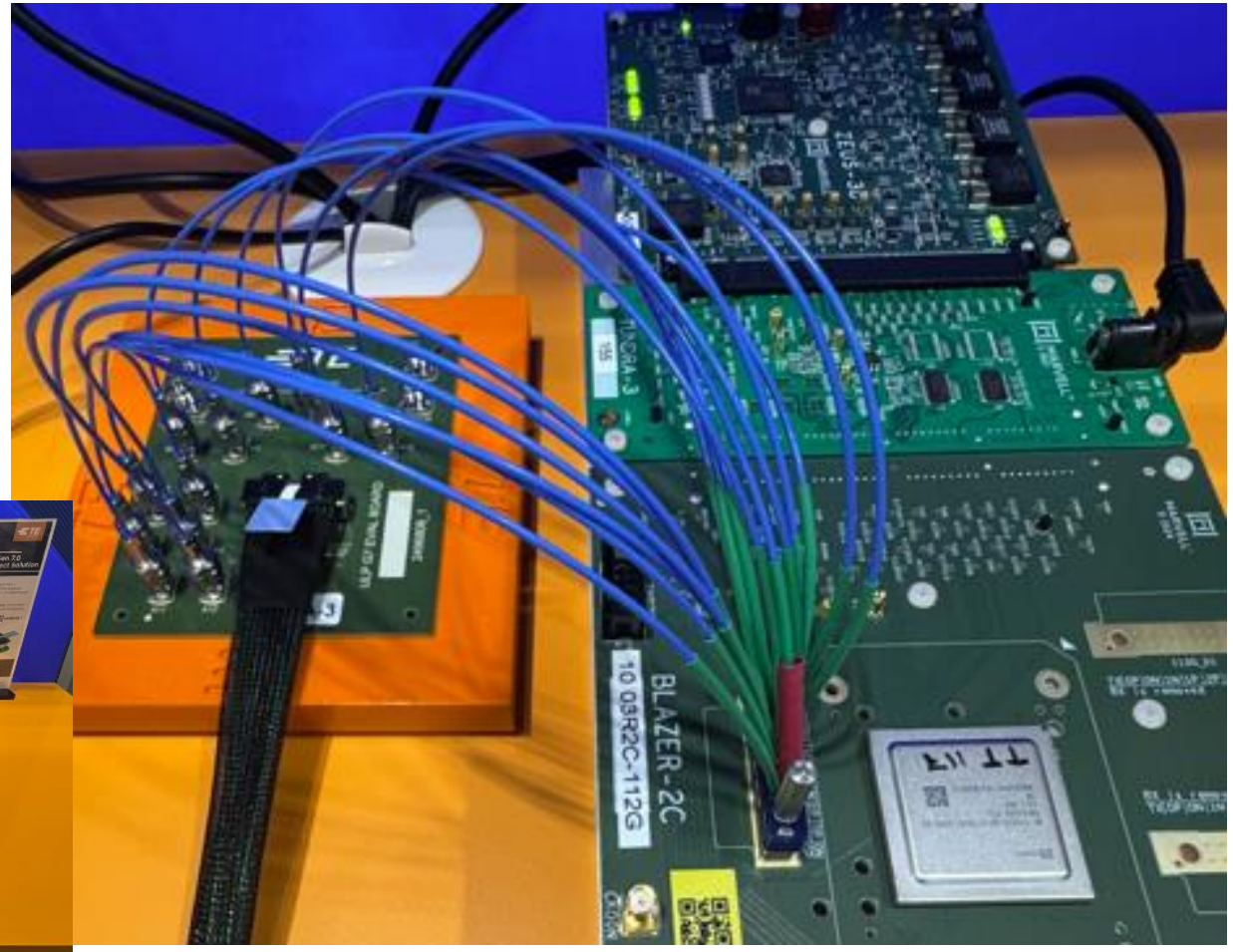
Initial Prototypes Tooled, Tested & Demo’ed at DesignCon 2025





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Summary

- PCIe Gen 7 at 128Gtps justifies a fresh look at achieving performance objectives
- This project proposal enables an industry standard approach to address the higher data rate while also:
  - Addresses the challenging thermal management environment on host design by providing lower profile mated solution (enhanced heat sink on host device above the interconnect)
  - Smaller overall host envelope than existing solutions
  - Superior signal integrity performance already demonstrated in first prototypes
- This project arms the industry with a standardized next gen internal cabled interconnect addressing needs not currently being met

