SNIA
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Technology Affiliate

SFF-9639

Request for Open

1/24/2025

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Overview

- SFF-9639, Table 5-1 uses pin/signal E16 as part of the header for the table
- E16 is incorrectly called out as E16=0, SFF-TA-1001 calls for E16=1 when referring to PCIe
- E16=0 is reserved for Gen-Z devices, which is not relevant to the table title “PCIE DUAL PORT USAGE”

Reference

- E16 is in the header to emphasize how to dual port PCIe
- Both SFF-TA-1001 & U.2 (Quad PCIe) use the dual port pin

5. PCIe Dual Port Lane Usage

For PCIe Dual Port mode, both Quad PCIe and SFF-TA-1001 redefine some of the PCIe lanes to explicitly be a second port with the secondary port starting the lane numbering at 0. The below table describes the Port and Lane numbering change when in dual port mode.

TABLE 5-1 PCIE DUAL PORT LANE USAGE

SFF-TA-1001 Dual Port S15=0, E16=0	Quad PCIe Dual Port S15=1, E16=0	PCIe Lane	
		E25 = Open	E25 = 0
S[2-6]	E[10-14]	PortA Lane0	
S[17-21]	S[17-21]	PortA Lane1	
S[9-13]	S[23-27]	PortA Lane2	PortB Lane0
S[23-27]	E[17-21]	PortA Lane3	PortB Lane1

Note: Single lane (x1) port usage shall use Lane0.

On Thu, Jan 12, 2023 at 2:48 PM Kaler, Paul (Future Server Architecture) <paul.kaler@hpe.com> wrote:

> Hi Jason,
>
> That appears to be a typo in 9639, should be open or “1” to indicate a PCIe interface device.

From: SFF-TA-1001

4.2.2 Host Port Type 1 Pin Operation

The Host Port Type 1 (HPT1) pin shall be an open drain output from the host to the device to determine which type of host protocol the device is mated to. An SFF-TA-1001 compliant host (or slot) shall either assert this pin low or allow for the signal to float high.

The device shall have the necessary input pull-up resistor (meeting signal parameters described in section 4.4) to ensure the proper value is read for Quad PCIe and shall read this pin at power-on to determine PCIe lane configuration.

TABLE 4-6 HOST PORT TYPE PINS

Host Port Type 1 (E16)	Definition
Open	PCIe host interface
Gnd	See table 4-4

Proposal

- Open SFF-9639 Rev 2.1 and make the E16 signal changes to table 5-1
- Correct all signals designating “1” to “Open”

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TABLE 5-1 PCIE DUAL PORT LANE USAGE

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S[17-21]	S[17-21]	PortA Lane1	
S[9-13]	S[23-27]	PortA Lane2	PortB Lane0
S[23-27]	E[17-21]	PortA Lane3	PortB Lane1

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