SNIA
SFF TWG
Technology Affiliate

New Project Proposal: SFF-TA-1039 PCIe FPP Hardware and Electrical Specifications

Presented: December 13, 2024

Presenter: Ali Ghiasi [Molex] [aghiasi@gmail.com]

Supporters: Tom Palkert – Samtec
Jason Stuhlsatz – Broadcom
Ali Ghiasi – Molex

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- A brief description summarizing the scope of the changes to be made to an existing document OR the scope of work for a new document
  - INF-1003 (2018) specifications was developed for 16x25 Gb/s applications and included both electrical specifications and mechanical specifications. SFF-TA-1032 is defining the mechanical specification extending CDFP style connector to 4x128, 8x128, and 16x128 Gb/s (PAM4) operation. The industry also needs a complementary electrical specifications to SFF-TA-1032 to build PCIe FPP modules. This SFF project will define hardware and electrical specifications for the 4x128, 8x128, and 16x128 Gb/s (PAM4) FPP module compatible with PCIe CopprLink.
- Editor(s): Ali Ghiasi
- Supporters: Minimum 3 member companies required (can include editor's company)
  1. Tom Palkert - Samtec
  2. Jason Stuhlsatz - Broadcom
  3. Ali Ghiasi – Molex

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- SFF-TA-1039 will define hardware and electrical requirements to complement SFF-TA-1032 mechanical specifications
- SFF-TA-1039 normative specifications will consist of the following:
  - Electrical connector pinout compatible with PCIe CopprLink 1.0 (2024)
  - Low speed signal definition and timing
  - High speed electrical signals
  - Compliance points
  - Optical port definition and mapping
  - Power requirements
  - ESD.
- SFF-TA-1039 informative specifications will consist of following
  - Example reference circuit
  - Example power filter
- IP Declaration (if applicable):
  - The Editor is strongly encouraged to declare any known IP at the time of the New Project Proposal
- Optional: Approve initial ballot on Feb 28th with expected publication Dec-2025.

Thank You

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SNIA SFF TA URL: https://www.snia.org/sff

