SFF-TA-1024

Former Specification for

Test Procedure for SFF-TA-1016 Mated Cable Assembly

Rev 1.0 June 5, 2024

SECRETARIAT: SFF TA TWG

ABSTRACT: This specification formerly defined the test procedure and outlines the steps required to perform high speed signal integrity measurements on SFF-TA-1016 style mated cable assemblies.

REASON FOR EXPIRATION: Canceled

This project was canceled as most of the information in this specification was included in the *CopprLink Internal Cable Specification for PCI Express 5.0 and 6.0* published at https://pcisig.com.

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SFF-TA-1024

Specification for

Test Procedure for SFF-TA-1016 Mated Cable Assembly

Rev 0.0.3 June 23, 2021

SECRETARIAT: SFF TA TWG
This specification is made available for public review at http://www.snia.org/sff/specifications. Comments may be submitted at http://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

The description of the connector in this specification does not assure that the specific component is available from connector suppliers. If such a connector is supplied, it should comply with this specification to achieve interoperability between suppliers.

ABSTRACT: This specification defines the test procedure and outlines the steps required to perform high speed signal integrity measurements on SFF-TA-1016 style mated cable assemblies.

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Foreword

The development work on this specification was done by the SNIA SFF TA TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TA TWG, the signup for membership can be found at http://www.snia.org/sff/join.

Revision History

Rev 0.0.1 January 15, 2021:
- Initial draft

Rev 0.0.2 March 03, 2021:
- Added "Mated Cable Assembly" to the Section 4 heading.
- Removed Section 4.1 through Section 4.4 and renumbered the remaining Section 4 headings accordingly.
- Added "Mated Cable Assembly" to the Section 4.1 heading.
- In Section 5.1.1, fixed typo in Appendix A reference.
- In Section 5.2.5, corrected reference to Appendix C.
- In Section 5.2.8.5, removed erroneous Appendix reference.
- In Section 6.3, edited Equation 6-1 label.
- In Section 6.4, edited Equation 6-2 label, removed Equation 6-3 label, and renumbered all remaining Equations.
- In Section 6.5.1, added hyphen to single-aggressor and edited new Equation 6-3 label.
- In Section 6.5.2, edited new Equation 6-4 label.
- In Section 6.6.1, added hyphen to single-aggressor and edited new Equation 6-5 label.
- In Section 6.6.2, edited new Equation 6-6 label.
- Inserted a new Section 6.7 and renumbered the remaining Section 6 headings accordingly.
- In Section 6.8, edited new Equation labels and updated the formatting of several Equations.
- In Section 6.9, edited new Equation labels, replaced old Figure 6-14 with new Equation 6-15, renumbered the remaining Section 6 Figures, and updated the formatting of several Equations.
- In Section 6.10, edited new Equation labels and updated the formatting of several Equations.
- In Section 7, rotated Table 7-1, Table 7-2, and Table 7-3 in order to enlarge them to increase the text size.
- In Appendix A, rotated Table A-1 3 in order to enlarge the table to increase the text size.
- In Appendix B, Section B.4, added missing steps to Table B-4 and removed all rows after step 43.
- In Appendix B, Section B.5, removed all rows after step 45 in Table B-5.

Rev 0.0.3 June 23, 2021:
- Updated text in Section 1 Scope to add mated connectors test procedures.
- In Section 2.1, added references to SFF-TA-1017 and SFF-TA-1018.
- Inserted a new Section 4 for connector-only compliance test board description and board design.
- Inserted a new Section 5 for connector-only equipment settings, calibration, and verification.
- Inserted a new Section 6 for connector-only electrical measurements and masks and

renumbered the remaining sections, figures, tables, and equations accordingly.
- Updated Equation 9-9, Equation 9-10, and Equation 9-11.
- Inserted a new Appendix A and renamed the remaining appendices.
-

Contents

Figures

Tables

1. Scope

This specification defines the test procedure and outlines the steps required to perform high speed signal integrity measurements on SFF-TA-1016 style mated connectors and separate test procedures and steps required for mated cable assemblies.

2. References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:

- ASME Y14.5 Dimensioning and Tolerancing
- EIA-364-1000 Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Controlled Environment Applications
- REF-TA-1011 Cross Reference to Select SFF Connectors
- SFF-TA-1017 Test Board Specification for SFF-TA-1002 Straight Connector
- SFF-TA-1018 Test Board Specification for SFF-TA-1002 Right Angle Connector

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at http://www.snia.org/sff/specifications. Suggestions for improvement of this specification will be welcome, they should be submitted to http://www.snia.org/feedback.

EDITOR'S NOTE: Delete sources not cited in Section 2.1; e.g. PCIe, SAS, etc. (or add in any missing references)

Copies of PCIe standards may be obtained from PCI-SIG (http://pcisig.com).

Copies of InfiniBand standards may be obtained from the InfiniBand Trade Association (IBTA) (http://www.infinibandta.org).

Copies of IEEE standards may be obtained from the Institute of Electrical and Electronics Engineers (IEEE) (https://www.ieee.org).

Copies of SAS and other ANSI standards may be obtained from the International Committee for Information Technology Standards (INCITS) (http://www.incits.org).

Copies of JEDEC standards may be obtained from the Joint Electron Device Engineering Council (https://www.jedec.org).

Copies of OIF Implementation Agreements may be obtained from the Optical Internetworking Forum (http://www.oiforum.com).

Copies of ASME standards may be obtained from the American Society of Mechanical Engineers (https://www.asme.org).

Copies of Electronic Industries Alliance (EIA) standards may be obtained from the Electronic Components Industry Association (ECIA) (https://www.ecianow.org).

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS
Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE
If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS
Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a. red (i.e., one of the following colors):
    A. crimson; or
    B. pink;
b. blue; or
c. green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1. top;
2. middle; and
3. bottom.

Lists are associated with an introductory paragraph or phrase, and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

DIMENSIONING CONVENTIONS
The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

NUMBERING CONVENTIONS
The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.
EDITOR'S NOTES:
- *Add any abbreviations or definitions specific to the connector being defined. Keywords may not be added.*
- *Remove keywords, acronyms, or definitions that are not relevant to this specification*

3.1 Keywords

May/ may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Defines the signal on a connector contact [when] its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies the restricted designation, then the restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word, or field (e.g., a restricted byte uses the same value as defined for a reserved byte).

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

AWG: American Wire Gauge
dB: decibel, given in dB-volt i.e., 20log10(V2/V1)
DUT: Device Under Test
E-Cal: Electronic calibration
EMLB: Early Mate Late Break
EIPS: Effective Intra-pair Skew
EPPS: Effective Pair-to-Pair Skew
ESD: Electrostatic Discharge
Fmax: stop frequency, maximum operating frequency, and frequency at which insertion loss – return loss of the fixture 5 dB
IDC: Insulation Displacement Contact
IDT: Insulation Displacement Termination
Gbps: Gigabits per second
GT/s: Giga-Transfers per second
HVLP: Hyper Very Low Profile
HVSP: Hyper Very Smooth Profile
LLCR: Low Level Contact Resistance
MCA: Mated Cable Assembly
PCB: Printed Circuit Board
PF: Press Fit
PSFEXT: Power Sum Far End Crosstalk
PSNEXT: Power Sum Near End Crosstalk
PTH: Plated Through Hole
RA: Right Angle
RAR: Right Angle Receptacle
RAND: Reasonable and Non-Discriminatory
RL: Return Loss
SDD11: Input Differential Return Loss
SDD12: Output Differential Return Loss
SDD21: Input Differential Insertion Loss
SDD22: Output Differential Return Loss
SMA: Sub-Miniature version A
SMT: Surface Mount Technology
SOLT: Short, Open, Load, Thru
TDR: Time Domain Reflectometry
TDT: Time Domain Through
TEM: Transverse Electro-Magnetic
TRL: Through, Reflect, Line
VNA: Vector Network Analyzer
VR: Vertical Receptacle
VLC: Vertical Launch Connector
VSP: Very Smooth Profile

3.3 Definitions

Allen Test: Insertion loss and return loss measurement of the primary thru, measurement made after SOLT/E-calibration and prior to TRL/2x Thru calibration to determine the maximum operational frequency of the VNA and fixture equipment set.

Alignment guides: A term used to describe features that pre-align the two halves of a connector interface before electrical contact is established. Other common terms include: guide pins, guide posts, blind mating features, mating features, alignment features, and mating guides.

Basic (dimension): The theoretical exact size, profile, orientation, or location of a feature. It is used as the basis from which permissible variations are established by tolerances in notes or in feature control frames (GD&T).

Cable Assembly: the combination of wire and free connectors

Connector: Each half of an interface that, when joined together, establish electrical contact and mechanical retention between two components. In this specification, the term connector does not apply to any specific gender; it is used to describe the receptacle, the plug or the card edge, or the union of receptacle to plug or card edge. Other common terms include: connector interface, mating interface, and separable interface.

Contact mating sequence: A term used to describe the order of electrical contact established/ terminated during mating/un-mating. Other terms include: contact sequencing, contact positioning, mate first/break last, EMLB (early mate late break) staggered contacts, and long pin/short pin.

Contacts: A term used to describe connector terminals that make electrical connections across a separable interface.

Datum: A point, line, plane, etc. assumed to be exact for the purposes of computation or reference, as established from actual features, and from which the location or geometric relationship of either feature is established.

Device Under Test (DUT): The components within the measurement reference planes.

Free Connector: a connector, typically a plug, permanently attached to wire, creating a cable assembly.

Fixed Connector: a connector, typically a receptacle, permanently attached to the printed circuit board.

Frontshell / Backshell: A term used to describe the metallic part of a module that provides mechanical and shielding continuity between the plug and receptacle. Other terms commonly used are: housing, snout, and metal shroud.

Mated Cable Assembly (MCA): refers to the combination of copper wire, plugs, receptacles and receptacle footprint that comprise the device under test in this specification.

Module: In this specification, module may refer to a plug assembly at the end of a copper (electrical) cable (passive or active), an active optical cable (AOC), an optical transceiver, or a loopback.

Plug: A term used to describe the connector that contains the penetrating contacts of the connector interface as shown in Figure 3-1. Plugs typically contain stationary contacts. Other common terms include male, pin connector, and card edge.

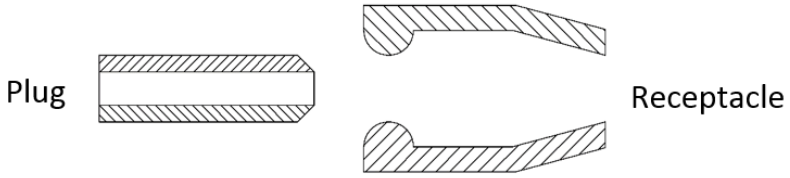


Figure 3-1 Plug and Receptacle Definition

Plated through hole termination: A term used to describe a termination style in which rigid pins extend into or through the PCB. Pins are soldered to keep the connector or cage in place. Other common terms are through hole or PTH.

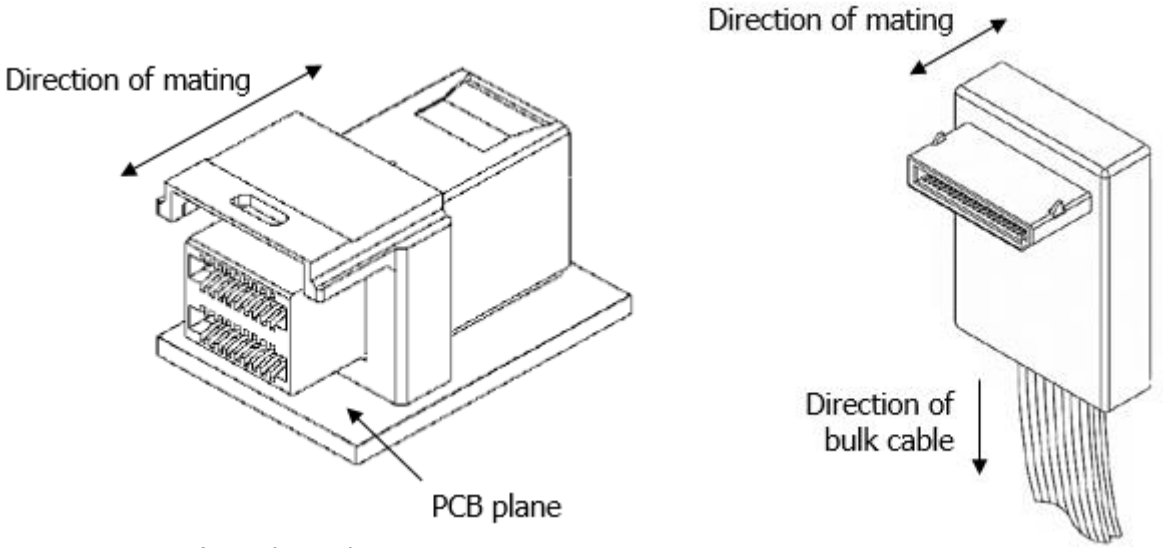
Press fit: A term used to describe a termination style in which collapsible pins penetrate the surface of a PCB. Upon insertion, the pins collapse to fit inside the PCB's plated through holes. The connector or cage is held in place by the interference fit between the collapsed pins and the PCB.

Receptacle: A term used to describe the connector that contains the contacts that accept the plug contacts as shown in Figure 3-1. Receptacles typically contain spring contacts. Other common terms include female and socket connector.

Reference (dimension): A dimension provided for information or convenience. It has no tolerance and is not to be used for inspection or conformance. It can be calculated from other tolerance dimensions or can be found elsewhere on the drawing with a tolerance. If removed, it would have no impact on the defined object or the ability or reproduce it.

Reference Plane: the location within the measurement fixture where user calibration is performed and where the measurement is made.

Right Angle: A term used to describe either a connector design where the mating direction is parallel to the plane of the printed circuit board upon which the connector is mounted or a cable assembly design where the mating direction is perpendicular to the bulk cable.



a) Right angle connector

b) Right angle cable assembly

Figure 3-2 Right Angle Connector and Cable Assembly

Straddle mount: A term used to describe a termination style that uses surface mount termination points

on both sides of a PCB.

Straight: A term used to describe a connector design where the mating direction is parallel to the bulk cable.

Surface mount: A term used to describe a termination style in which solder tails sit on pads on the surface of a PCB and are then soldered to keep the connector or cage in place. Other common terms are surface mount technology or SMT.

Termination: A term used to describe a connector's non-separable attachment point such as a connector contact to a bulk cable/ a cage to a PCB or flex circuit/ bulk cable to a PCB or flex circuit/ solder tail to PCB. Common PCB terminations include: surface mount (SMT), plated through hole termination (PTH), and press fit (PF). Common cable terminations include insulation displacement contact (IDC), insulation displacement termination (IDT), wire slots, solder, welds, crimps, and brazes.

Vertical: A term used to describe a connector design where the mating direction is perpendicular to the printed circuit board upon which the connector is mounted.

Wipe: The distance a contact travels on the surface of its mating contact during the mating cycle as shown in Figure 3-3.

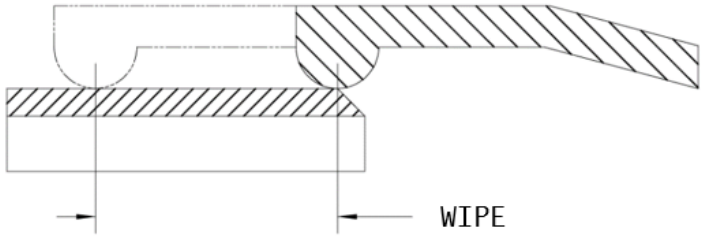


Figure 3-3 Wipe for a Continuous Contact

4. General Connector-only Compliance Test Board Description

The connector-only compliance test board is intended to test the performance of the connector and footprint only. The set-up tests worst-case coupling and other electrical parameters using six differential pairs.

4.1 Connector-only Compliance Board Design

The connector-only test board design shall be such that both the Module Compliance Board (MCB) and Host Compliance Board (HCB) come from the same fabrication panel. The impedance of the copper traces shall be 85 Ohm differential (42.5 Ohm single-ended). Signal launch-off connectors on the test board shall have at a minimum a 40 GHz bandwidth. The coupon accommodations shall be sufficient to accommodate an AFR calibration as well as a spider approach of removing fixture cross-talk. The total coupon size shall be as specified in Table 4-1 and illustrated in Figure 4-1 and Figure 4-?.

Table 4-1 Total Coupon Sizes

Length	
Width	
Thickness	

Insert Vertical Figure here

Insert Vertical Top View Figure here

Insert Vertical Bottom View Figure here

Insert Right Angle Figure here

Insert Right Angle Top View Figure here

Insert Right Angle Bottom View Figure here

4.2 Connector-only Test Board Stack-up

Both the MCB and HCB shall have the same stack-up. The test board stack-up shall consist of 8 layers. The board material shall be Nelco 4000-13SI. The signal trace width is 7.5 mils (0.1905 mm) using ½ ounce copper weight. The board stack-up as illustrated in Figure 4-#.

> **Developer's Note:** The supporting Gerber package includes trace width and impedance details. Should there be any contradiction between the trace width and meeting the impedance requirements as indicated on the Fab drawing for a PCB manufacturer, the impedance requirement shall take precedence.

Insert Figure here

4.3 Vertical and Right Angle Test Card Connector Footprints

The connector footprints shall be as specified in Appendix A of SFF-TA-1016. The signals use 6 mil (0.1524 mm) microvias from the top layer's SMT pads to the second layer. As illustrated in Figure 4-#, microvias are used to move the stripline signals to the top layer with limited signal degradation.
The connector footprints contain a bus on the ground layer to bus the grounds together. This structure

mitigates crosstalk that can happen when transitioning from the stripline layer to the outer layers.

Insert Figure here

4.4 Connector-only Tested Pairs

The test board tests six high-speed pairs using three pairs within row A and three pairs within row B directly across from each other as illustrated in Figure 4-# & Figure 4-#.

Insert Figure here

Insert Figure here

4.5 Vertical and Right Angle Module Compliance Board (MCB)

Enter details about the MCBs here.

Insert Figure here

Insert Figure here

4.6 Vertical and Right Angle Host Compliance Board (HCB)

Enter details about the HCBs here.

Insert Figure here

Insert Figure here

4.7 Vertical and Right Angle Mated Test Set-up

To ensure proper and stable mating during the test of this board the HCB and MCB shall be secured into position once mated as illustrated in Figure 4-# & Figure 4-#.

Insert Figure here

Insert Figure here

When mating the HCB into the connector on the MCB the leading edge shall be fully inserted such that the card bottoms out inside the connector slot on the seating plane. Testing shall be performed at a fully-mated condition where there is a nominal 1.30 mm wipe length on the signal pads and 1.70 mm wipe length on the ground pads. This may require an additional mechanical structure to provide stability and to prevent cables from disturbing the mated interface during measurement. See Appendix # for additional details.

5. Connector-only Equipment Settings, Calibration, & Verification

This section details the equipment settings, the calibration method, and the verifications required for connector-only testing. For the equipment settings, the calibration method, and the verification required for cable assemblies, refer to Section 8.

5.1 AFR Calibration for Connector-only Tests

The test fixture is designed for automatic fixture removal (AFR) calibration with 2x thru traces. The 2x thru

trace is on the connector-only test MCB. After de-embedding the 2x Thru, the reference plane shall be set immediately before the anti-pad to ensure clean calibration.

Developer's Note: This specification references AFR throughout, but it is acceptable to use an AFR equivalent.

Developer's Note: This fixture includes the microvias and microstrip length of 45mils in the electrical characterization.

The traces are short to provide higher metrology grade bandwidth to the test fixture. After the traces are de-embedded with AFR, the resulting device under test (DUT) shall contain a 0.5mm trace before the footprint as illustrated in Figure 5-#.

Insert Figure here

5.2 AFR Measurement Flow for Connector-only Tests

The flowchart below in Figure 5-# provides the steps needed for repeatable and accurate measurements.

Insert Figure here

5.3 VNA Settings for Connector-only Measurements

The vector network analyzer (VNA) should be set to the settings provided in Table 5-# below.

Setting	Value
Averaging	
Step Size	
IF Bandwidth	
Start Frequency	
Stop Frequency	

The VNA system impedance should be set to 50 Ohms.

5.4 End of Cable SOLT Calibration

A standard end of cable SOLT calibration needs to be performed in order to move the reference plane to the end of the test point cables. The SOLT calibration may be done with an eCAL or manually with the standards kit that comes with the VNA.

5.5 Determine Stop Frequency

The Stop Frequency is determined by measuring the 2x Thru after the SOLT Calibration. The resultant IL and RL should be plotted on the same graph to determine the Stop Frequency. The Stop Frequency is determined by the frequency where the IL is not greater than the RL by 5dB. The Stop Frequency depends on board quality. An example of the stop frequency that is good up to 40GHz.

Insert Figure here

5.6 Connector-only Procedure

After the reference plane is moved to the end of the cable, the 2x Thrus may be measured to continue moving the reference plane to immediately before the DUT. There are three 2x Thrus measurements that need to be completed for the proper calibration. The MCB_2x Thru, HCB Layer2_2x Thru, and HCB

Layer7_2xThru need to be measured. Half fixtures are derived from these three 2x Thru measurements and are used to de-embed their respective boards.

- The 2x Thru on the MCB is used to de-embed all pairs both A and B on the MCB board
- The 2x Thru on the HCB Layer 2 is used to de-embed all the A pairs (A17/A18, A20/A21, A23/A24)
- The 2x Thru on the HCB Layer 7 is used to de-embed all the B pairs (B17/B18, B20/B21, B23/B24)

5.7 Connector-only Calibration Verification

The verification of the half fixture should be done by de-embedding the 2x Thru from which the half fixture was created.

5.8 Connector-only TDR Option

A time domain reflectometry (TDR) using a 1x Thru trace to calibrate rise time of the incoming signal at the connector. A TDR may be used to verify any questionable frequency domain-to-time domain transformations due to causality and passivity issues during testing.

Insert Figure here

6. Connector-only Electrical Measurements and Masks

6.1 VNA Port Naming Convention for Connector-only Tests

6.2 Differential Insertion Loss and Return Loss (DDIL\DDRL) for Connector-only Tests

6.3 Connector-only Crosstalk Measurements

6.3.1 Connector-only Power Sum Near-End Cross Talk (PSNEXT)

6.3.2 Connector-only Power Sum Far End Cross Talk (PSFEXT)

7. General Mated Cable Assembly Compliance Test Board Description

7.1 Mated Cable Assembly Compliance Board Design

Test boards are designed to support TRL calibration and 2x thru methods with launch to reference plane lengths equal within ±0.0005” enabling accurate high-speed measurements of the mated cable assembly. Crosstalk spider patterns are used to estimate fixture crosstalk to aid in accurate characterization of cable assembly crosstalk. All boards are designed to achieve 42.5 ± 5% impedance control. Board stacks, materials, line lengths and calibration structures are designed to allow mated cable assembly characterization.

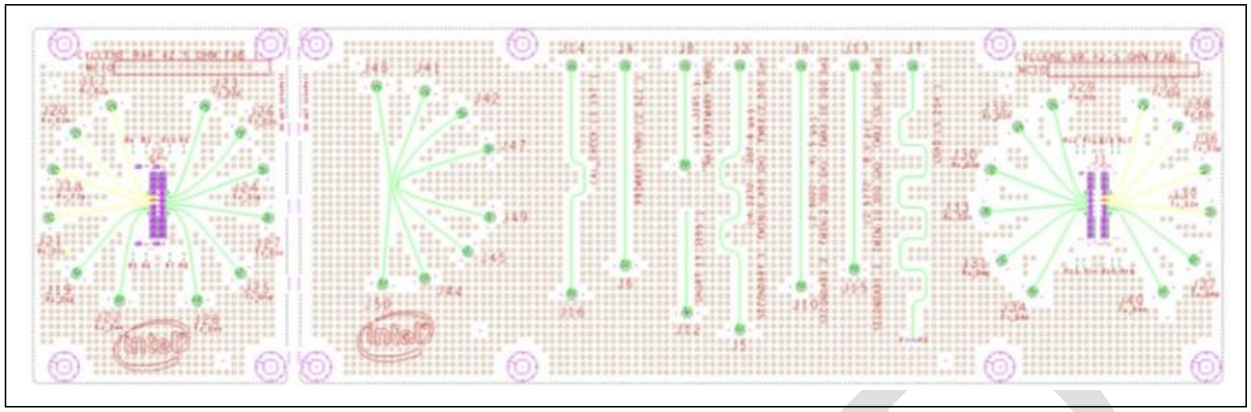


Figure 7-1 Mated Cable Assembly Evaluation Board Set: Cyllene RAR, Cyllene VR

7.2 Calibration Standards

TRL calibration standards, one primary through, one short (reflect), three lines (called Secondary 1, 2, and 3) and one load are used as depicted in Figure 7-2. The frequency range for each secondary is written on the silkscreen. Secondary line delay labels are for reference only, use measured secondary delays for calibration. 2X through calibration is enabled using the primary though (2X through).

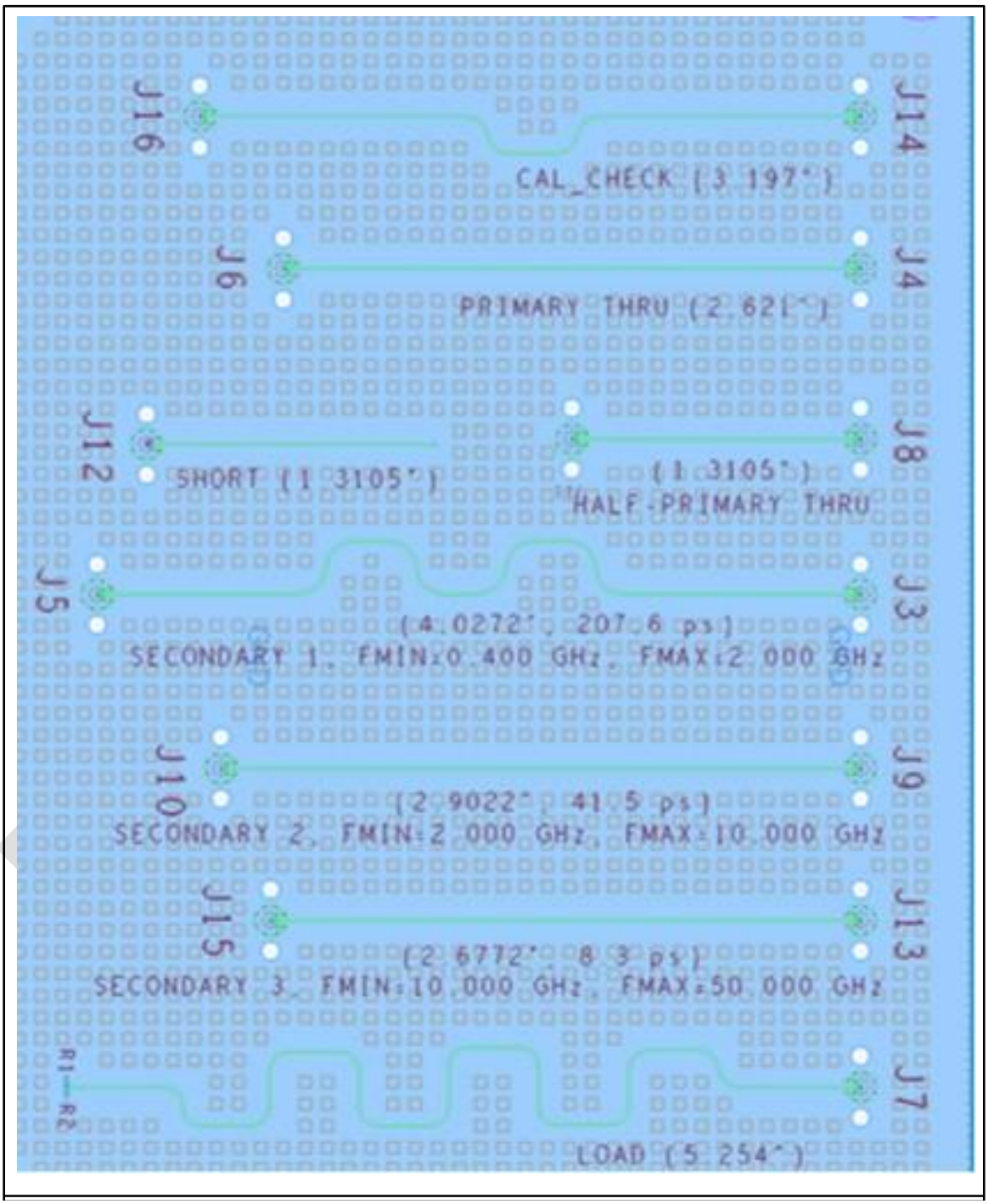


Figure 7-2 Mated Cable Assembly Evaluation TRL Calibration Traces

7.3 Reference Plane Positions

The primary through is designed to position the reference plane 0.050” from the trace/anti-pad transition on the test board.

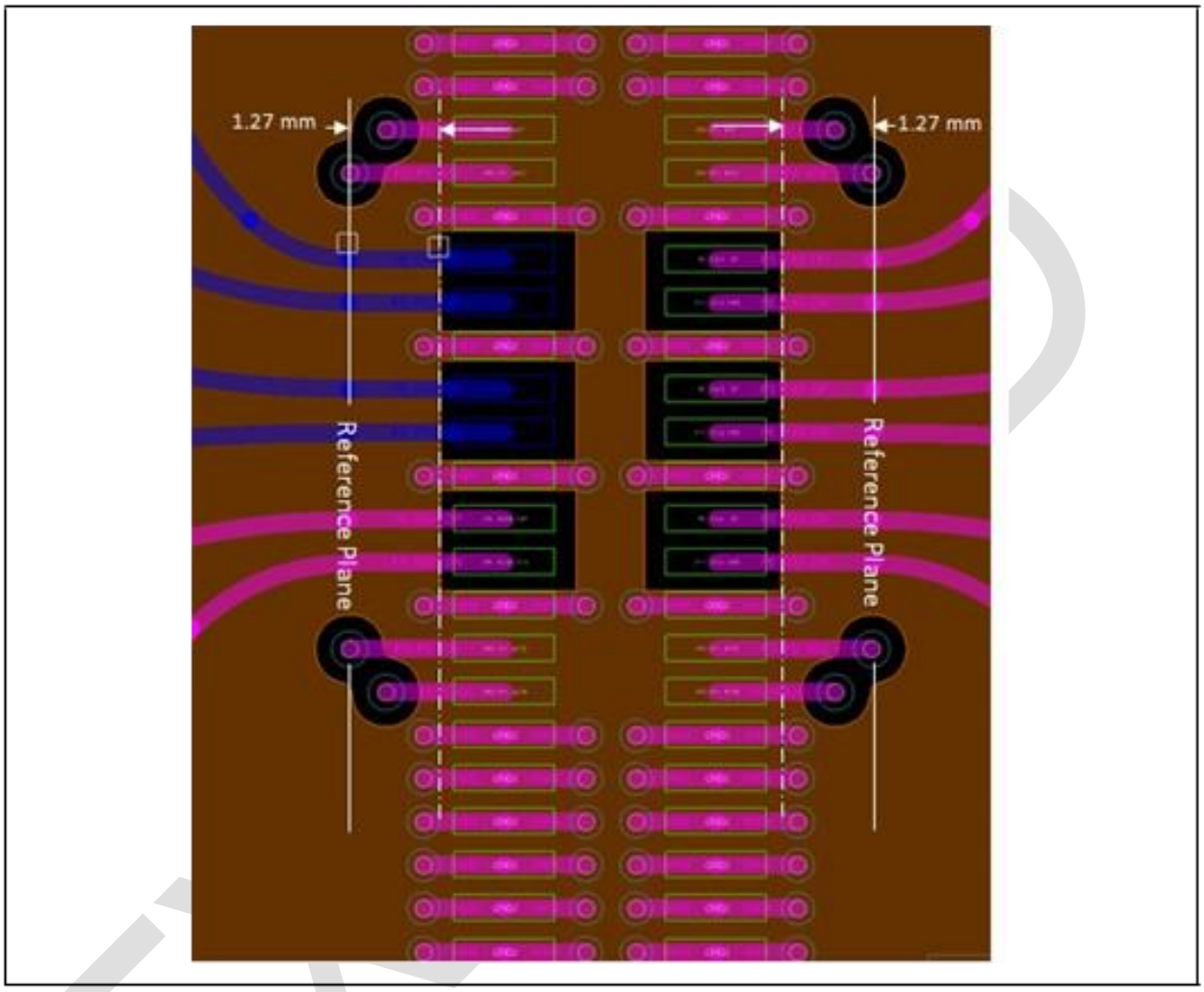


Figure 7-3 Mated Cable Assembly Evaluation Board Reference Plane Location: RAR

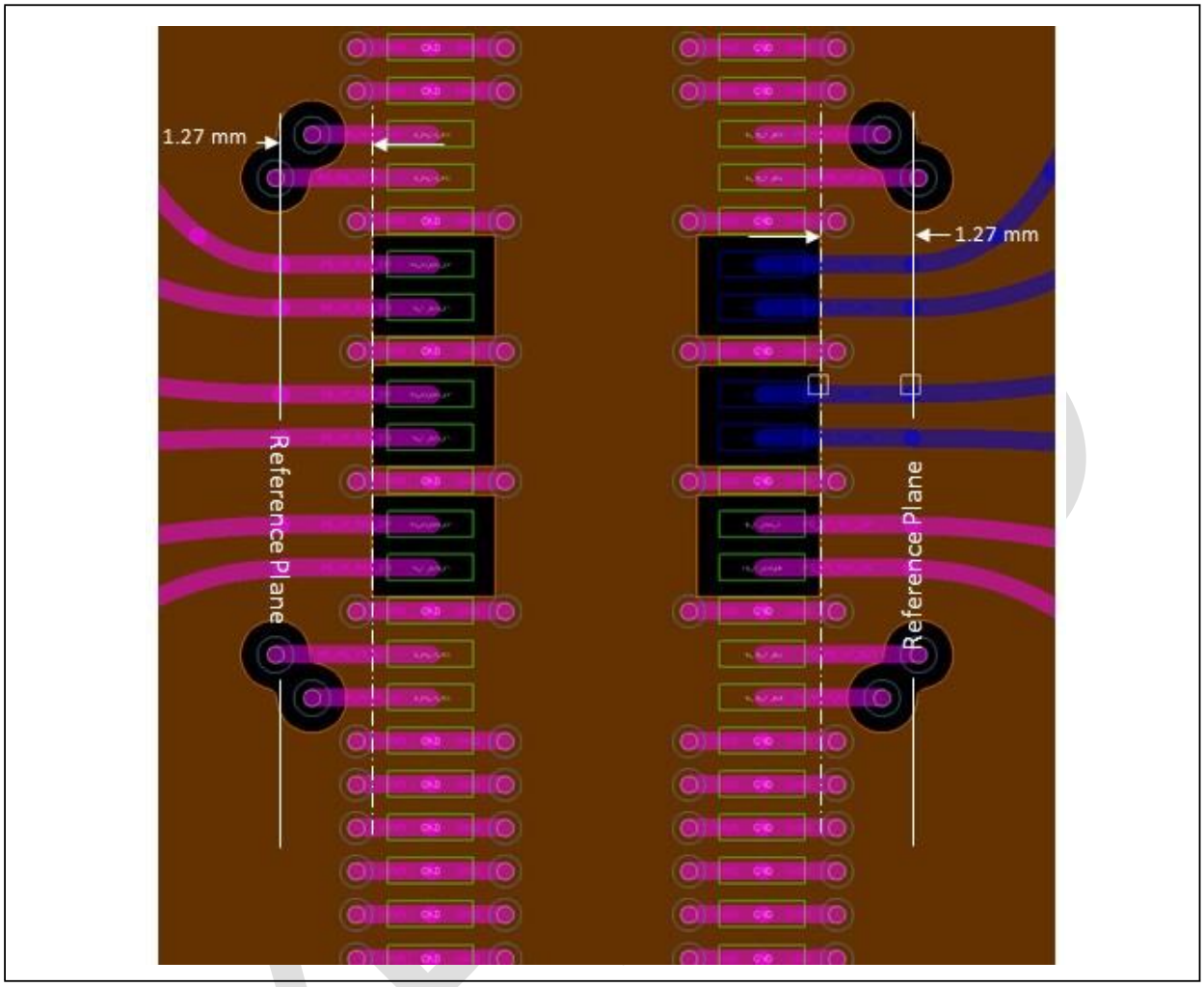


Figure 7-4 Mated Cable Assembly Evaluation Board Reference Plane Location: VR

The fixture FEXT removal structure is based on the four traces with highest potential for fixture crosstalk in the vertical receptacle board.

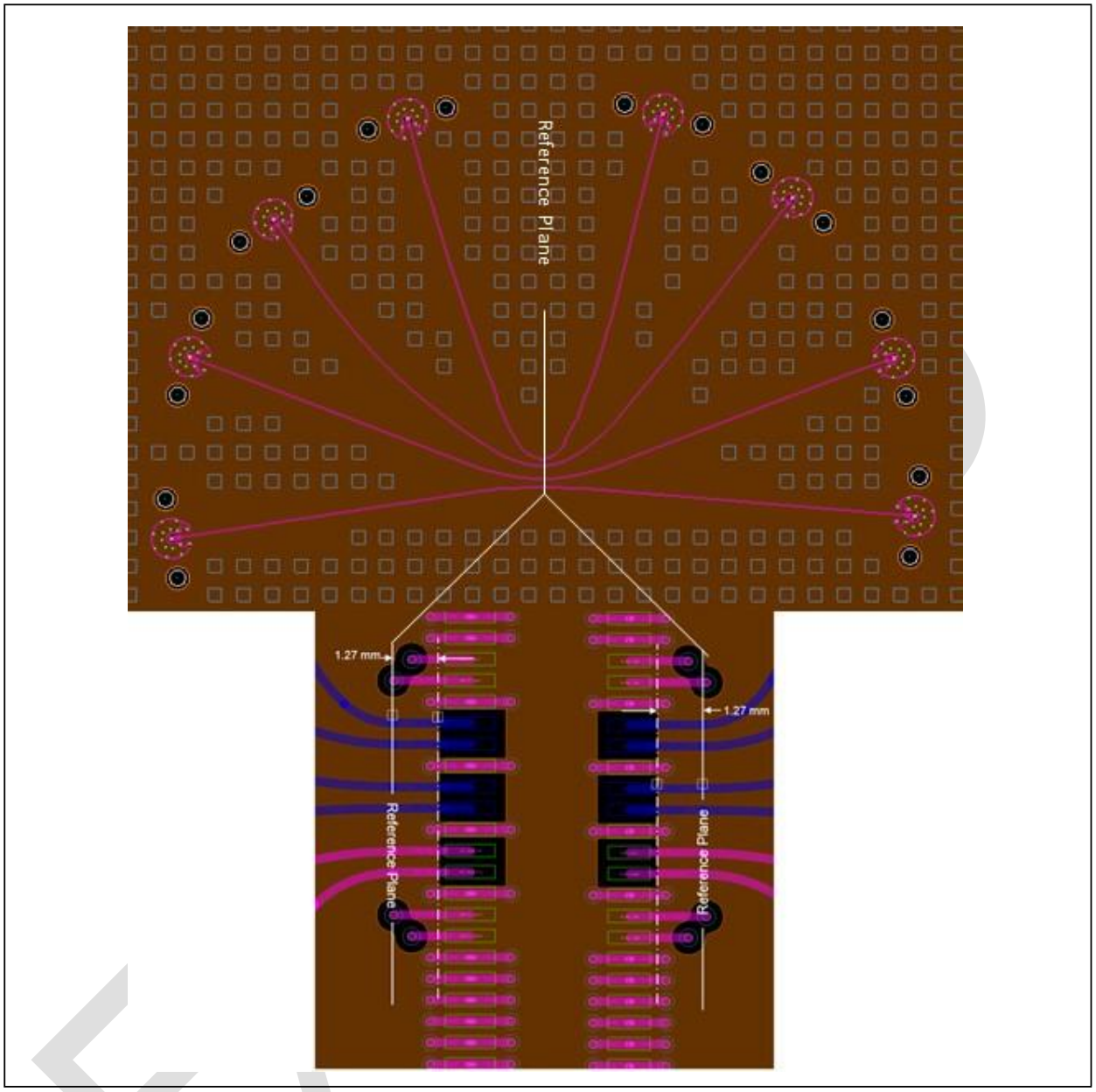


Figure 7-5 Mated Cable Assembly Reference Plane Location in Crosstalk Spider

7.4 Board Stack-up

The VNA setup and test plan used in this procedure are designed to produce S-parameter measurements referenced to a 42.5 ohm single-ended impedance. All test traces are held to a characteristic impedance of 42.5 ohms +/- 5%. The test board is an eight layer stack-up. MEGTRON 6 or TU-883 are used for the laminate material on all layers. The stack-up details for the boards are shown in Figure 7-6.

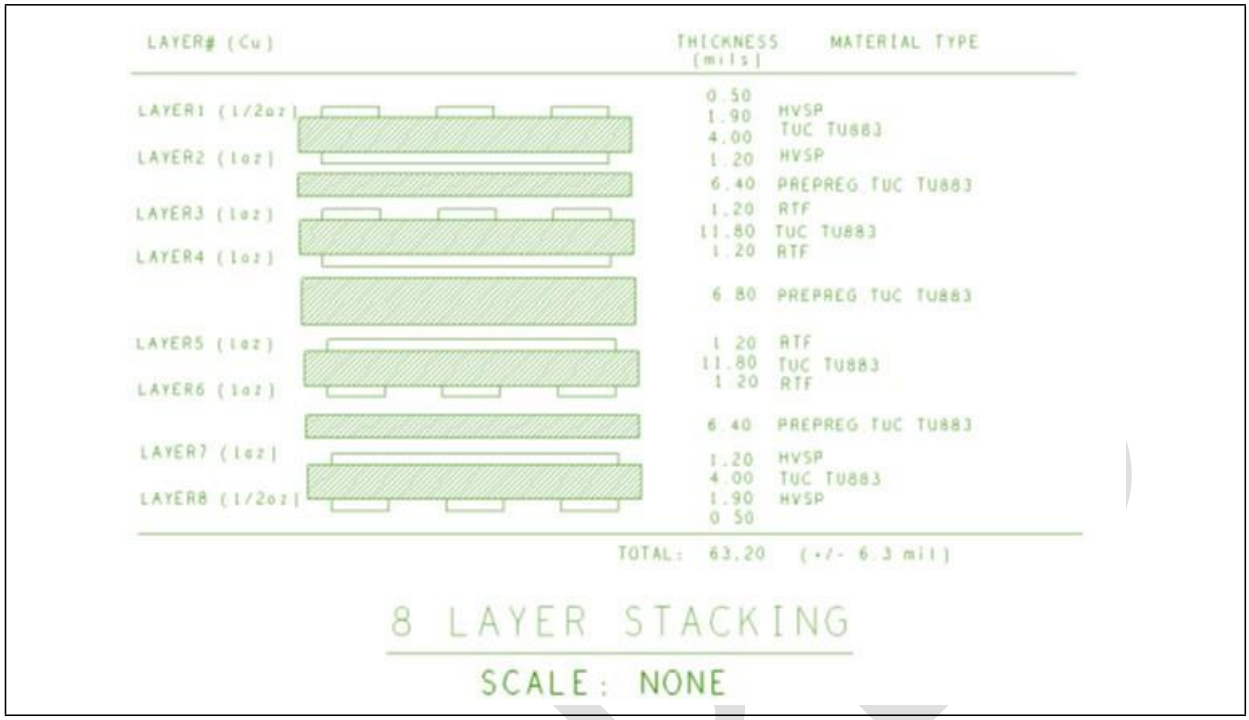


Figure 7-6 The 8-Layer Stack-up for Cyllene RAR & Cyllene VR Test Boards

7.5 Fixed Connector Footprint

Fixed connector surface pad, anti-pad, ground via size, and position have a significant impact on mated cable assembly performance. The following figures illustrate optimal fixed connector footprints for vertical and right angle receptacles.

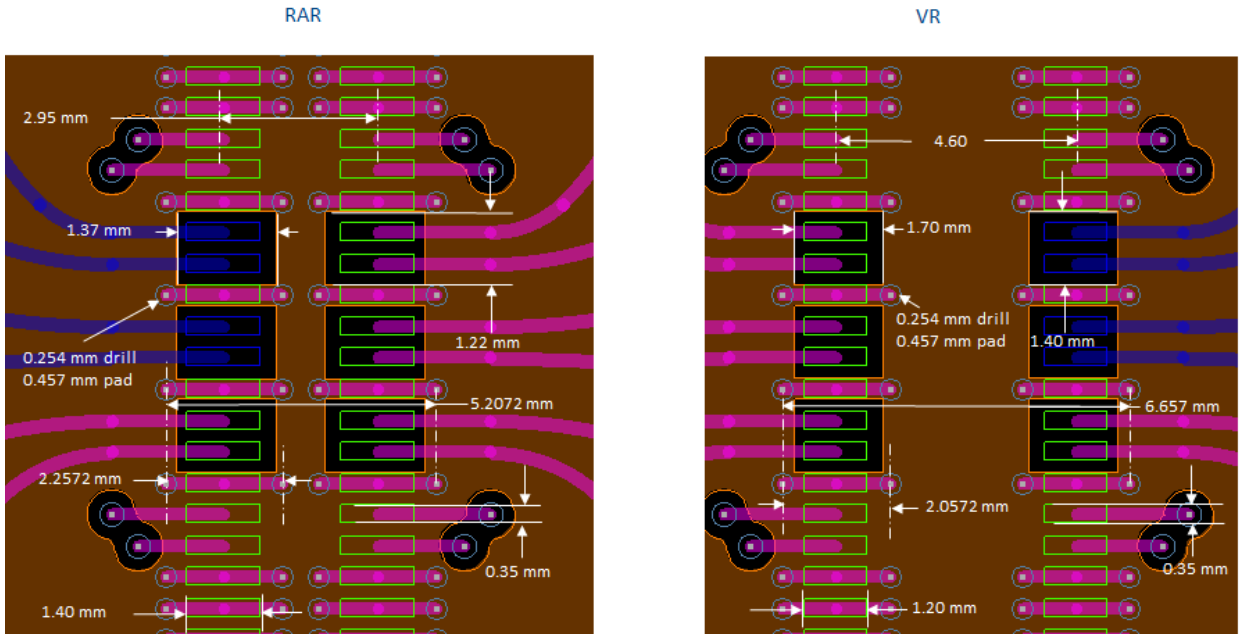


Figure 7-7 Mated Cable Assembly Evaluation Board Footprint Dimensions: RAR, VR

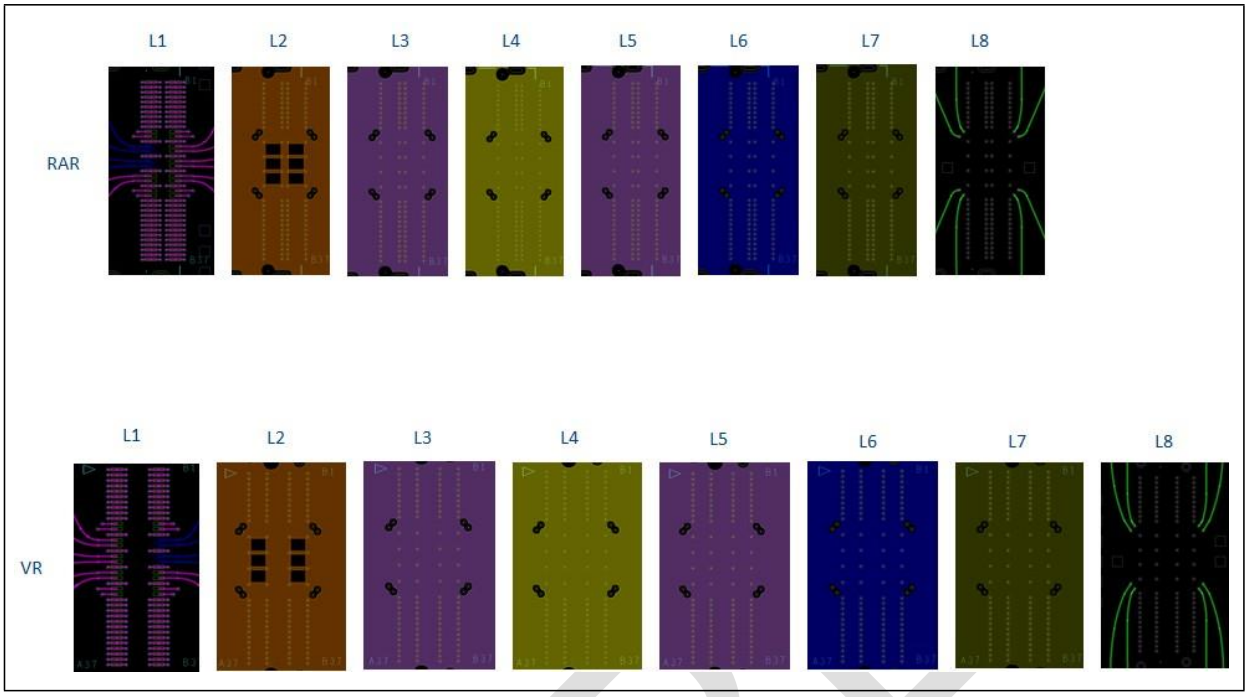


Figure 7-8 Mated Cable Assembly Evaluation Board Stack-up: RAR, VR

7.6 Mated Cable Assembly Test Set-up

The test boards should be attached to a rigid structure to ensure proper and stable mated cable assembly configuration during test. Recommended mated cable assembly configurations are shown in Figure 7-9.

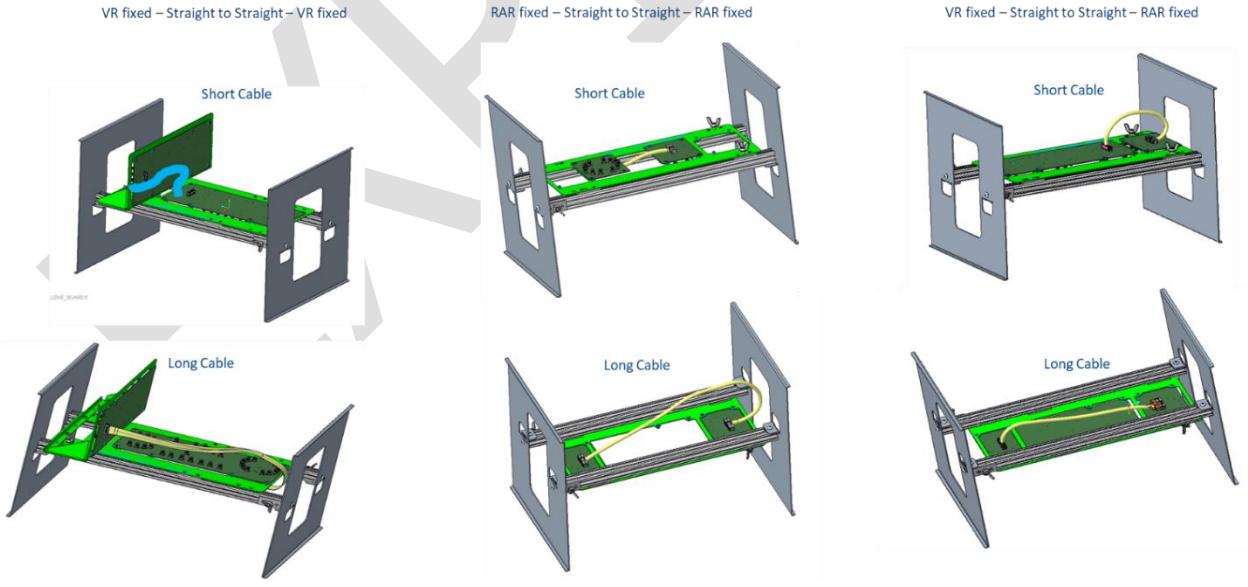


Figure 7-9 Recommended Mated Cable Assembly Configurations

8. Equipment Settings, Calibration, & Verification for Cable

Assemblies

8.1 Overview

8.1.1 Device Under Test (DUT)

Figure 8-1 illustrates the test setup for the VNA measurement, location of the measurement reference planes, and mated cable assembly DUT descriptions.

The vector network analyzer setup used in this test procedure performs single-ended S-parameter measurements that are used to calculate differential response in an 85 ohm characteristic impedance environment.

Test traces on the board are maintained to 42.5 ±2.25 ohms (±5%). Test boards are designed with trace length (L) from the launch connector to the reference plane to within ±0.0005. The bill of materials is listed in Appendix A.

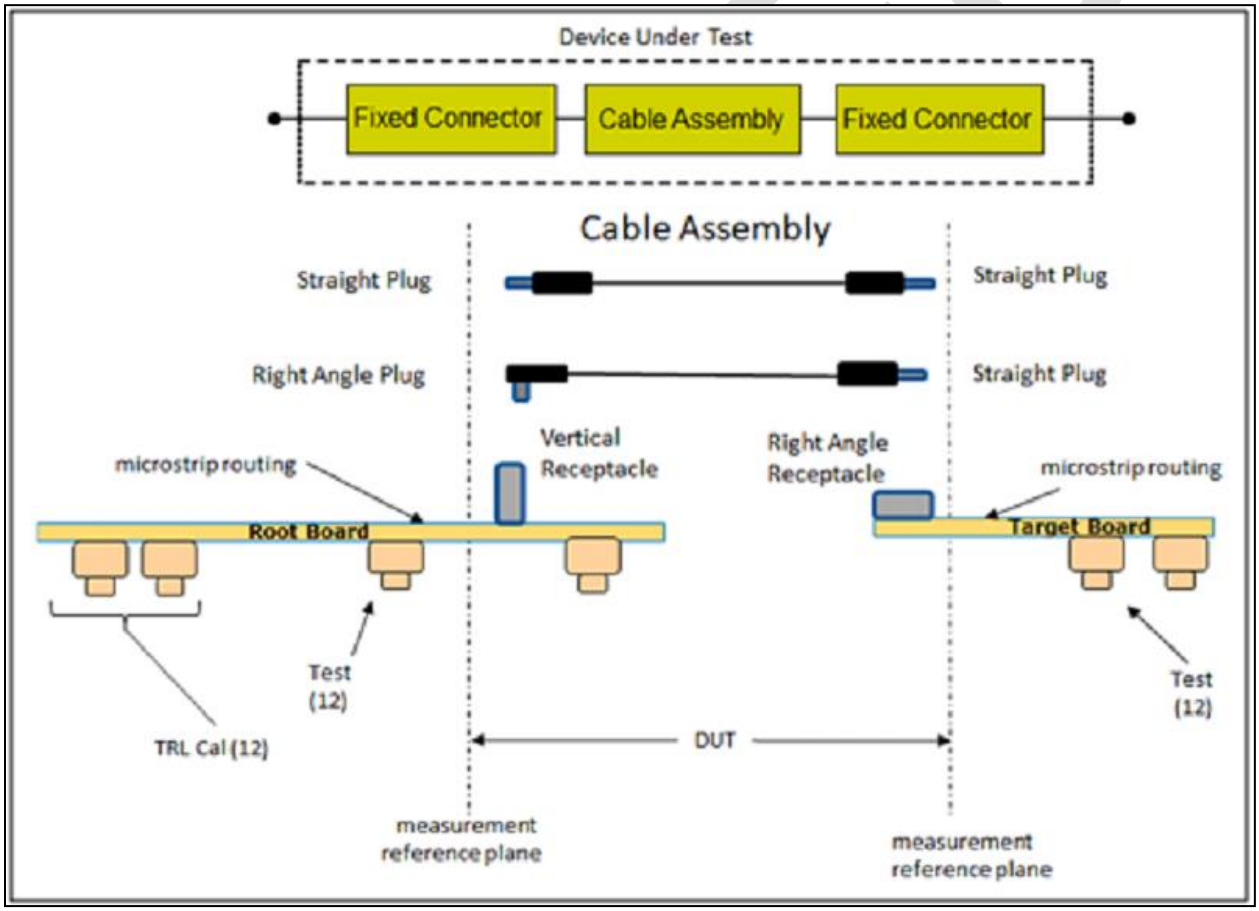


Figure 8-1 Mated Cable Assembly Evaluation Device Under Test, VR-RAR Fixed Connectors

8.1.2 Time and Frequency Domain Measure Test Flow

The test flow in the following figure describes the key steps and responses needed to complete accurate and repeatable time and frequency domain measurements. Key steps such as calibration, rise time verification, de-skew and Cal check should be performed daily, both before and after completing the measurement test plan to ensure stability of the test environment for the duration of the measurement

activity.

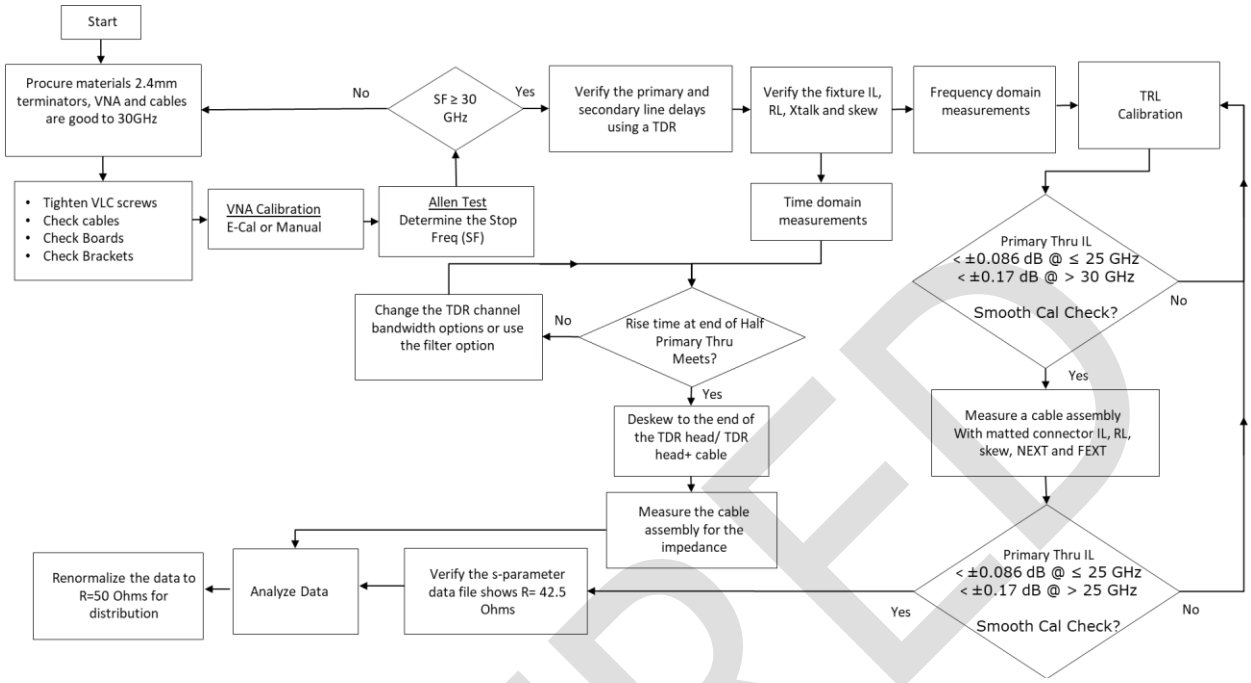


Figure 8-2 Time and Frequency Domain Measurement Test Flow

8.2 VNA Equipment Settings

S-parameter measurements are made using a Vector Network Analyzer (VNA). VNA settings affect the measurement and calibration performance. To improve measurement accuracy and repeatability, use the baseline settings indicated in the following table when running a calibration procedure.

Table 8-1 VNA Equipment Settings

Frequency Range	0.01 GHz: 0.01 GHz: 40 GHz
IF Bandwidth	≤ 1 kHz
Number of averages	Averaging is not recommended
Smoothing	Off

CAUTION: WHEN ATTACHING THE SMA FEMALE/MALE CONNECTORS BETWEEN THE FIXTURE AND THE VNA INSTRUMENT MAKE SURE TO ROTATE THE EXTERNAL BOLT OF THE CONNECTOR AVOIDING THE ROTATION OF THE CABLES/FIXTURE/CALIBRATION DEVICES TO AVOID THE DAMAGE OF THE CENTRAL PIN. MAKE SURE TO TIGHTEN THE CONNECTIONS TO 8 IN-LBS USING A TORQUE WRENCH.

8.2.1 Electronic Calibration (E-Cal)

To carry out the calibration of the equipment using the E-Cal device, the number of points, IF bandwidth, and the start and stop frequencies must be set. With the proper setting of the VNA instrument, go to the calibration menu and choose the option E-Cal, then chose the proper E-Cal device and run the calibration making the proper connections as indicated by the wizard. Once the calibration is finished save the setup.

8.2.2 Manual Calibration

The manual calibration is performed using the calibration kit provided by the manufacturer of the VNA instrument. The calibration routine must be carried out setting the appropriate number of points and ensuring that the start/stop calibration frequencies enclose the stop frequency of the Allen Test.

WARNING: VERIFY THE PROPER MATCHING OF THE CONNECTOR CABLES AND THE CONNECTIONS OF THE MANUAL CALIBRATION DEVICES TO AVOID MECHANICAL DAMAGE.

Under normal conditions the following calibrations are required:

- Reflective Calibration: This calibration includes three different measurements using the devices provided in the calibration kit.
  a. Short Circuit Calibration
  b. Open Circuit Calibration
  c. Broadband load calibration (usually a 50 Ω load)
- Through Calibration: The through calibration is carried out connecting the ports to be calibrated with the cables in short circuit. It is important to take into consideration the extra delay introduced by the through device when the through calibration is carried out.
- Isolation calibration: The isolation calibration is usually omitted.

8.2.3 Stop Frequency, F(max)

The Stop Frequency Test is a useful test procedure to determine the maximum operating frequency (Fmax) of the test set-up including test fixture and VNA. Over the frequency range up to Fmax, the RF components and the VNA should not resonate. The Allen Test is performed using the primary through. There should be at least 5 dB margin between Insertion Loss (IL) and Return Loss (RL) at the highest measured frequency. The following steps are recommended for the Allen Test.

1. Perform SOLT calibration to set the reference plane at the VNA cable ends.
2. Measure primary through on the baseboard
3. Assess IL for significant high Q deviations.
4. Assess frequency of 5 dB difference between insertion loss and return loss.

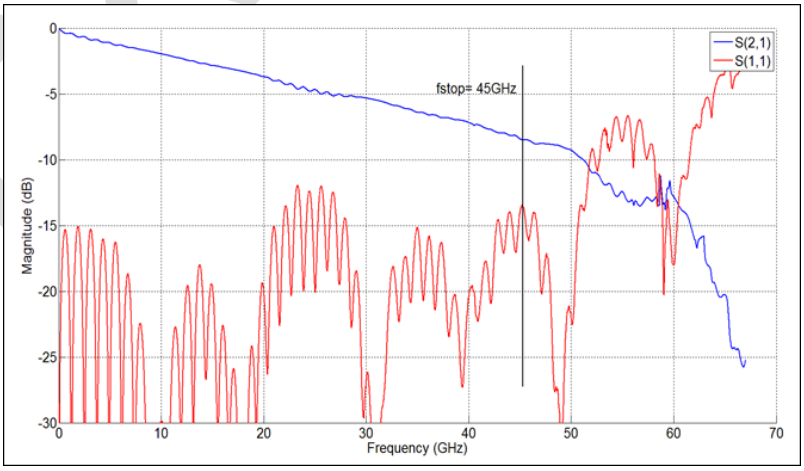


Figure 8-3 Example of Allen Test results to characterize the stop frequency, Fmax

8.2.4 Reference Plane Definition

The VNA must be calibrated to a known standard to characterize the performance of the connector in the test fixture. The intent of the calibration is to eliminate systematic errors in the measurement and improve measurement accuracy.

The precise geometric location at which a vector network analyzer measurement is made is called the reference plane. There are sometimes two different reference planes involved in a connector measurement. If a commercial coaxial calibration kit is used, it will typically establish a reference plane near the end of the test cables. In this case, a secondary calibration is needed to remove the influence of the test fixture and move the reference plane closer to the DUT.

One key property of the reference plane is it is far enough from geometric transitions such as vias that ephemeral modes die out before reaching the reference plane. The footprint is measured as part of the DUT. The recommended reference plane VNA Settings (see Table 8-1) for Measuring Intel UPI 2.0 Cable Assembly position is 50 mils from any geometric transition, e.g., signal trace to connector/via/anti-pad, signal trace to baseboard pad/anti-pad or signal trace to edge finger/anti-pad.

8.2.5 Time Domain Reflectometry Tuning

Impedance measurements are obtained using TDR measurements. Two critical requirements must be tuned before carrying out a TDR measurement:

De-skewing cables ensure the arrival of the TDR pulse at the end of the cables within appropriate delay, minimizing common mode effects in the measurement.

1. Connect the cables to the channels of the TDR instrument and leave them in an open circuit configuration, ρ= 1.

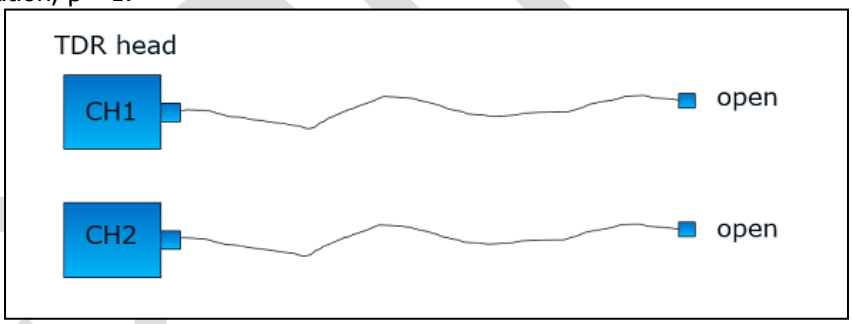


Figure 8-4 Open Circuit Configuration

2. Carry on the settings that were used to get the rise time of 15 psec at the reference plane of the half primary through.
3. Under Setup> TDR configure the individual channels to form the differential channel.

For example, if using C1 and C2 as a differential channel, then set C1 as a rising edge and C2 as a falling edge.

a. Turn ON the TDR step and acquisition for both the channels.
b. Change the units of both the channels to rho (ρ).

Rise time verification: The equipment must have an approximate rise time of the TDT step. TDR modules must enable a 15 ps rise time (20-80%) at the reference plane. To measure the differential impedance, two channels used as excitation (TDR pulse) must be de-skewed (in differential mode). See Appendix D.

8.2.6 Fixture Intra-pair Skew

DUT (Device Under Test) skew is obtained using VNA measurement data. In order to capture the inter-pair skew properly, the following procedures are recommended to estimate fixture skew.

1. Perform SOLT calibration at the VNA cable ends.
2. Measure RL on test boards as shown in the following figure. Note that DUT is not assembled, and the board is open at the pads where DUT is to be placed.
3. Convert RL of a differential pair in FD (frequency-domain) into TDR in TD (time-domain) to obtain the TDR, use a step voltage for the stimulus with the rise time (20-80%) defined for impedance testing.

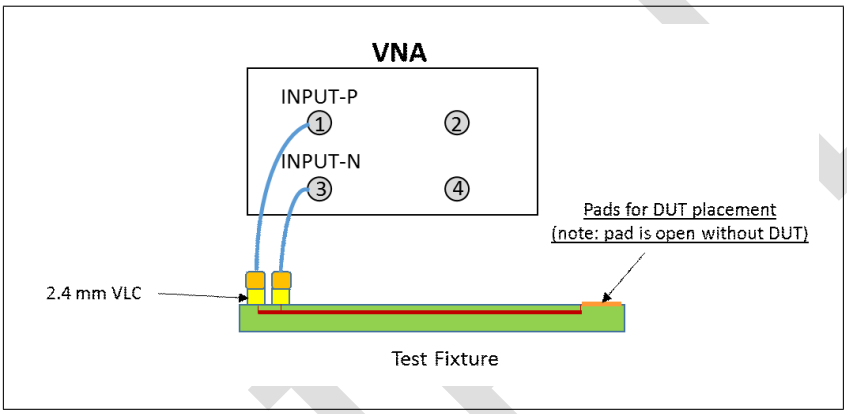


Figure 8-5 RL Measurement from Test Fixtures

4. Measure the fixture skew of fixtures using TDR, DF = [(TP-TN)/2].

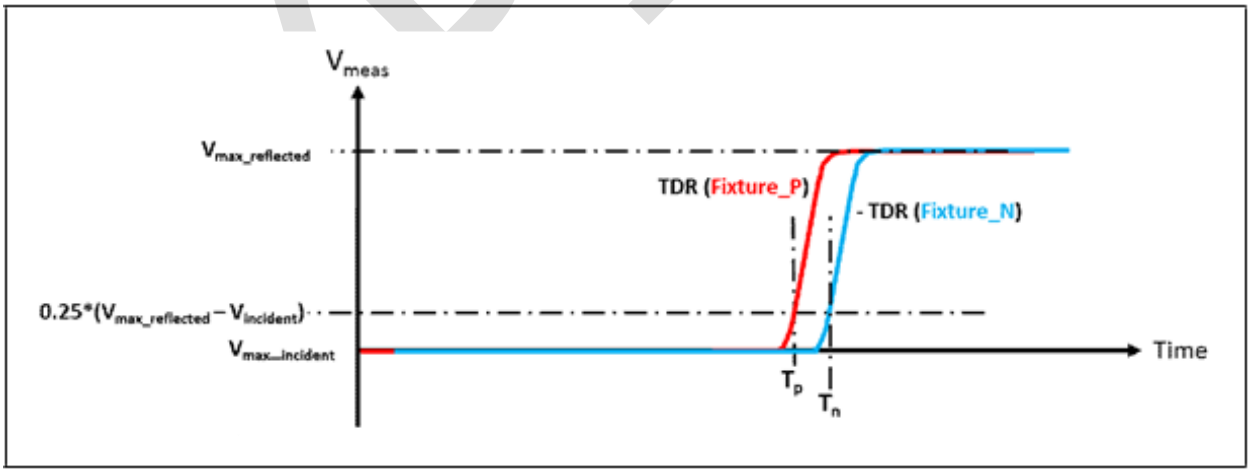


Figure 8-6 TDR Obtained via FD to TD Conversion of RL of a Differential Pair

5. Calculate fixture skew by adding average 'Fixture A' skew and average 'Fixture B' skew while retaining the of Fixture skew values. Note that this addition should be done per differential signal path without mixing different pairs.
6. Round Fixture skew using the following rule: 0 ps to 1 ps = 1 ps, 1 ps to 2 ps = 2 ps; -1 ps to 0 ps = -1 ps, -2 ps to -1 ps = -2 ps.

7. Record fixture skew.

8.2.7 Flight Time

Measure flight time to obtain the actual flight time offset between the primary through and each secondary line for the TRL calibration. The time of flight is measured using a TDT measurement following the procedure shown below:

1. Make sure the TDR instrument is properly compensated at room temperature.
2. Set the screen scale to capture 50 ps/div and leave the acquisition mode to average.
3. Set one channel as the driver and the other the receiver.
4. Capture the primary through and save the waveform as a reference.
5. Connect the channels to Secondary 1 and capture the waveform and measure the flight time difference between Primary Through and the Secondary 1 (reference to 20% of the maximum voltage).
6. Repeat Step 4 for Secondary 2 and 3.
7. Record the flight time offsets of the secondary lines for TRL calibration.
8. Compare to design values.
9. Use measured delay values for TRL calibration.

Table 8-2 CYLLENE Mated Cable Evaluation Board TRL Calibration Launch Position vs TRL Line

Launch Connector Pair	Calibration Line
J_HPRIM_A - J_HPRIM_B	PRIMARY THRU – 2.621”
J_PRIM_A - J_PRIM_B	HALF PRIMARY THRU - 1.3105”
J_SHORT	SHORT - 1.3105”
J_SEC1A - J_SEC1B	SECONDARY 1 - 4.0607” / 207.6 ps / 0.4 GHz - 2.0 GHz
J_SEC2A - J_SEC2B	SECONDARY 2 – 2.9089” / 41.5 ps / 2.0 GHz - 10 GHz
J_SEC3A - J_SEC3B	SECONDARY 3 – 2.6786” / 8.3 ps / 10 GHz - 50 GHz
J_CAL_A - J_CAL_B	CAL CHECK 3.197”
J_LOAD	LOAD 5.242”

8.2.8 Calibration Verification

8.2.8.1 Secondary Line Phase Margin

Verify secondary line phase margin on new boards. The phase plot should be linear over the secondary line frequency range. Secondary line phase margin should be greater than 20 degrees.

8.2.8.2 Calibration Stability

Verify the stability of the calibration using the insertion loss measurement of the primary through before and after completing the test plan. Absolute value of primary through loss |S21| after TRL calibration should be ≤ 0.1 dB up to 18 GHz and ≤ 0.2 dB above 18 GHz.

8.2.8.3 Dynamic Range

Verify the dynamic range is large enough to capture the crosstalk. The noise floor measurement is a crosstalk measurement between two distant traces. The crosstalk reading is the noise floor, which is the lower boundary of the dynamic range the VNA in use can support after the calibration. The noise floor should be less than -50 dB up to 8 GHz and less than -40 dB up to 18 GHz.

8.2.8.4 Check System Reference Impedance

Some tools do not correctly handle S-parameters with reference impedances other than 50 ohms. If using a reference impedance other than 50 ohms, check that the tool correctly recognizes the reference impedance used in the measurement. If using S-parameters to obtain the TDR result, examine the impedance in the time domain to ensure the target impedance is being correctly interpreted by the tool. For example, if measuring 85 ohm connectors, TDR impedance should be around 85 ohms.
Helpful tips:

- Make a copy of the touchstone file.
- Edit the R parameter to change the stated reference impedance.
- Reload the data into the tool.
- Check that the tool recognizes the change by comparing insertion loss plots.
- If the tool recognizes the change, the tool is working correctly.
- If the tool does not recognize the change, the data must be normalized to 50 ohm reference impedance before using the tool.
- The reference impedance is the impedance of the TRL calibration lines on the board, which may not be 50 ohms. The VNA may report a default value of 50 ohms regardless of the TRL line impedance.

WARNING: IF THE VNA DOES NOT REPORT THE CORRECT REFERENCE IMPEDANCE, EDIT THE TOUCHSTONE FILE SO THAT IT ACCURATELY STATES THE CORRECT REFERENCE IMPEDANCE.

- Always distribute data files normalized to 50 ohm reference impedance.
- Use actual measurement data to compare measurement to modeled cable performance

8.2.8.5 TRL Four Port Calibration

A TRL calibration is intended to remove the effect of the fixture moving the reference plane to closest proximity to the fixed connector. The TRL calibration has the advantage that it can be easily tailored to impedances other than 50 ohms and can eliminate the need for de- embedding the test fixture. It has the disadvantage that it is not available on all machines and is not as familiar to many users as other calibration methods.

1. To remove previous data in the memory, reboot the VNA instrument.

WARNING: FAILURE TO REBOOT CAN RESULT IN UNSTABLE/ UNUSABLE TRL CALIBRATION.

2. Set the start and stop frequencies for the TRL calibration in the instrument. Is important to notice that the maximum frequency it is given by the Allen Test described previously.
3. Set frequency step size to 10 MHz, number of averages to three, smoothing off, power to 0 dBm and IF bandwidth to 1 kHz.
4. For a (1,3;2,4) VNA configuration when performing a TRL calibration, set 1-2 and 3-4 as a defined Through and 2-3 and 1-4 as an unknown Through.
5. Load the calibration file in the equipment for Keysight.
6. Open the calibration wizard in the calibration menu and select smart calibration, (when using a Keysight VNA) and select 4 port calibration.
7. Select the calibration file for the Intel UPI connector.
8. Define the ports and run the calibration making the connections on the calibration fixture on

CYLLENE board (as described in Table 8-1 VNA Equipment Settings) following the wizard instructions.

9. Take notes of the delays and save the calibration. See Appendix B "VNA TRL Calibration" for more details.

9. Cable Assembly Frequency Domain Measurement

9.1 Port Naming Convention

Insertion and return loss are multi-port measurements using the port naming convention in the following figure. All differential pairs other than those being measured need to be terminated. Since wide band 42.5 ohm terminators do not exist, adjacent unused measurement ports can be terminated with 50 ohm terminators.

The measured S-parameter should be referenced to 85 ohm differential impedance for compliance check against the cable assembly specification.

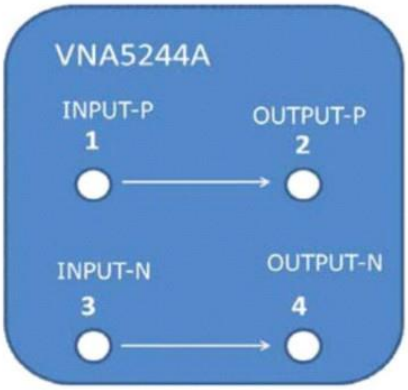


Figure 9-1 VNA Port Naming Convention Example

9.2 Fixed Connector Termination During Measurement

Right Angle Recptacle			
	Terminate Fixed Connector A Side	Terminate Fixed Connector B Side	
1	ground	ground	1
2	ground	ground	2
3	ground	ground	3
4	ground	ground	4
5	ground	ground	5
6	ground	ground	6
7	ground	ground	7
8	ground	ground	8
9	ground	ground	9
10	ground	ground	10
11	42.5 ohm	42.5 ohm	11
12	42.5 ohm	42.5 ohm	12
13	ground	ground	13
14	VLC	VLC	14
15	VLC	VLC	15
16	ground	ground	16
17	VLC	VLC	17
18	VLC	VLC	18
19	ground	ground	19
20	VLC	VLC	20
21	VLC	VLC	21
22	ground	ground	22
23	42.5 ohm	42.5 ohm	23
24	42.5 ohm	42.5 ohm	24
25	ground	ground	25
26	ground	ground	26
27	ground	ground	27
28	ground	ground	28
29	ground	ground	29
30	ground	ground	30
31	ground	ground	31
32	ground	ground	32
33	ground	ground	33
34	ground	ground	34
35	ground	ground	35
36	ground	ground	36
37	ground	ground	37

Vertical Recptacle			
	Terminate Fixed Connector A Side	Terminate Fixed Connector B Side	
1	ground	ground	1
2	ground	ground	2
3	ground	ground	3
4	ground	ground	4
5	ground	ground	5
6	ground	ground	6
7	ground	ground	7
8	ground	ground	8
9	ground	ground	9
10	ground	ground	10
11	42.5 ohm	42.5 ohm	11
12	42.5 ohm	42.5 ohm	12
13	ground	ground	13
14	VLC	VLC	14
15	VLC	VLC	15
16	ground	ground	16
17	VLC	VLC	17
18	VLC	VLC	18
19	ground	ground	19
20	VLC	VLC	20
21	VLC	VLC	21
22	ground	ground	22
23	42.5 ohm	42.5 ohm	23
24	42.5 ohm	42.5 ohm	24
25	ground	ground	25
26	ground	ground	26
27	ground	ground	27
28	ground	ground	28
29	ground	ground	29
30	ground	ground	30
31	ground	ground	31
32	ground	ground	32
33	ground	ground	33
34	ground	ground	34
35	ground	ground	35
36	ground	ground	36
37	ground	ground	37

Figure 9-2 Mated Cable Assembly Evaluation Board Pin Termination: RAR, VR

9.3 Differential Insertion Loss (SDD21)

Differential insertion loss is calculated using the following equation shown below where S is formatted as a complex number.

Calculation of differential insertion loss SDD21 presuming ports 1 and 3 are driven, ports 2 and 4 are outputs is shown in Equation **9-1**.

Equation 9-1 Calculations for SDD21

$$SDD21(dB) = 20\,log_{10}\left[\frac{|S21 + S43 - S23 - S41|}{2}\right]$$

9.4 Differential Return Loss (SDD11 and SDD22)

Differential return loss is calculated using the following equation shown below where S is formatted as a complex number.

Calculation of differential return loss SDD11 presuming ports 1 and 3 are driven, ports 2 and 4 are outputs is shown in Equation 9-2.

Equation 9-2 Calculations for SDD11 and SDD22

$$SDD11(dB) = 20\,log_{10}\left[\frac{|S11 + S33 - S13 - S31|}{2}\right]$$

$$SDD22(dB) = 20\,log_{10}\left[\frac{|S22 + S44 - S24 - S42|}{2}\right]$$

The configuration of the cable assembly to carry out the differential measurements of insertion and return loss are shown in the following figures.

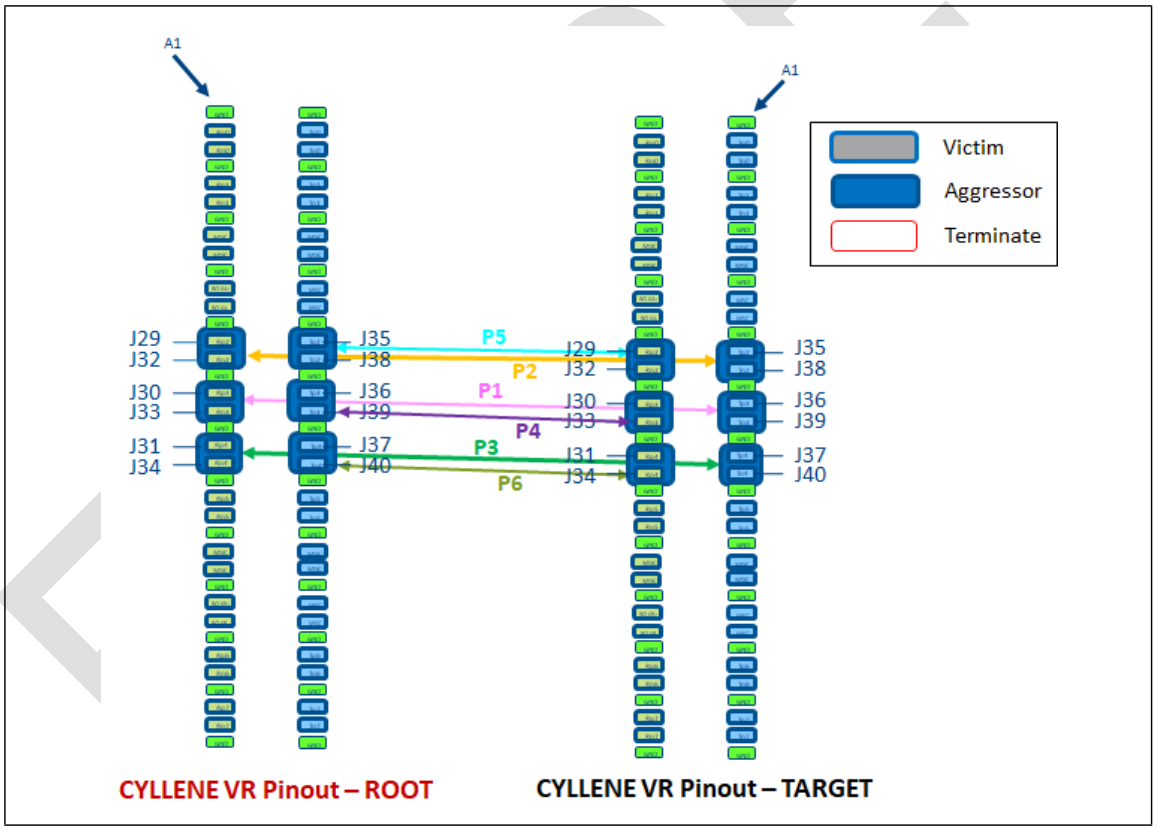


Figure 9-3 Vertical MCIO to Vertical MCIO, Insertion Loss/Return Loss, Tx to Rx Cable

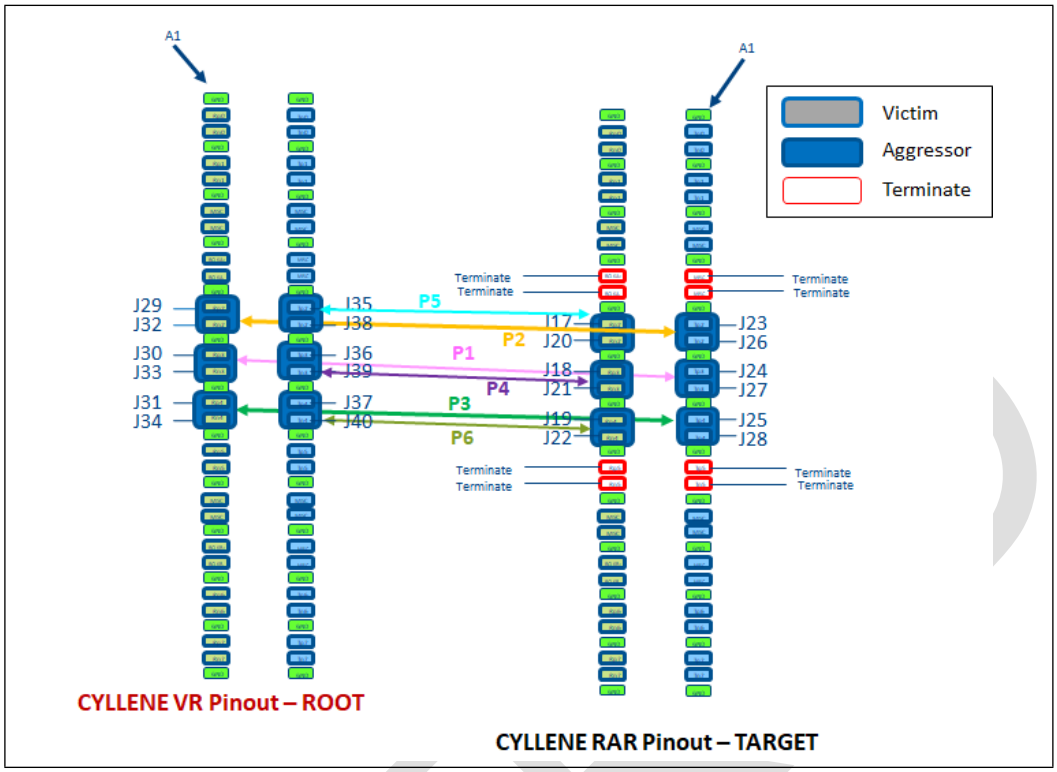


Figure 9-4 Vertical MCIO to RA MCIO Tx to Rx Cable

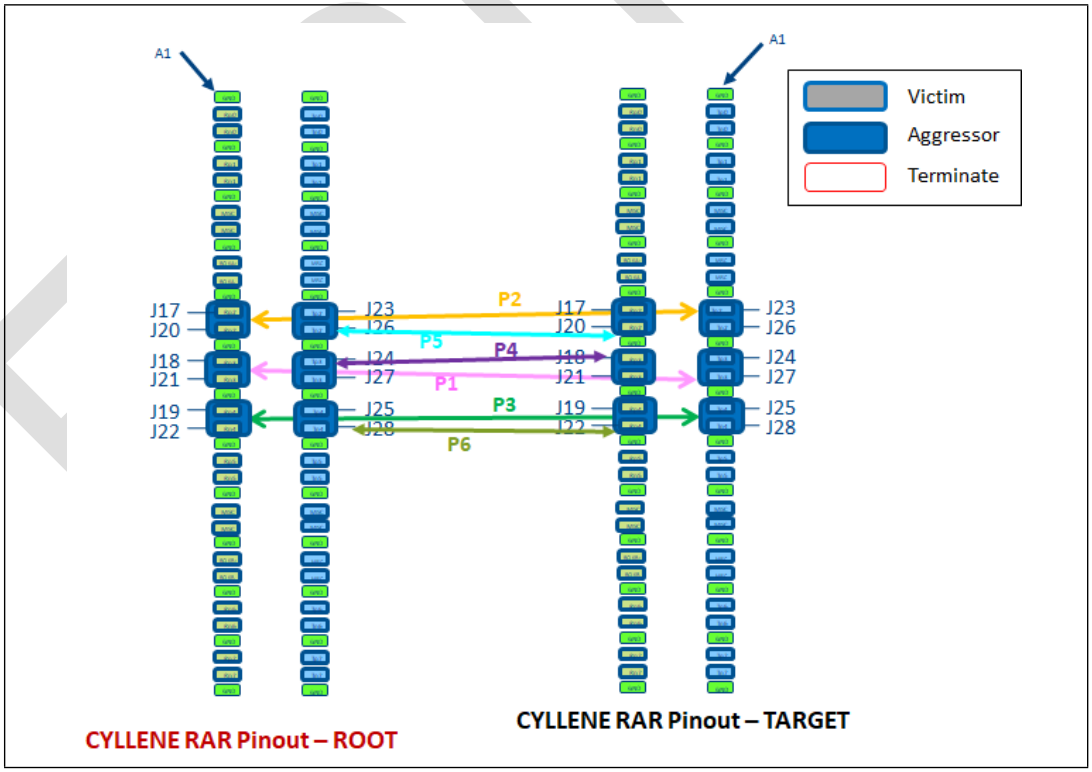


Figure 9-5 Right Angle MCIO to Right Angle MCIO, Insertion Loss/Return Loss, Tx to Rx Cable

9.5 Crosstalk Measurement

Differential power sum crosstalk is calculated using the following equations shown below where S is formatted as a complex number.

9.5.1 Single-aggressor Near-end Crosstalk (DDNEXT)

Differential single-aggressor near end crosstalk (DDNEXT) on the victim differential pair is calculated by the following formula.

Equation 9-3 Calculations for DDNEXT

$$DDNEXT(dB) = 20\,log_{10}\left[\frac{|S21 + S43 - S23 - S41|}{2}\right]$$

9.5.2 Multi-Disturber Near-end Crosstalk (MDNEXT)

Multi-Disturber Near-End Crosstalk (MDNEXT) on the victim differential pair is calculated as a power sum using the following equation shown below where MDNEXT(f) is expressed in dB.

Equation 9-4 Calculations for MDNEXT

$$MDNEXT\ (f) = \ 10\ log_{10}\left(\sum\nolimits_{n} 10^{\frac{DDNEXT(f)}{10}}\right)\ |_{n=1,2,3}$$

The configuration of the cable assembly to carry out the differential measurements of insertion and return loss are shown in the following figures.

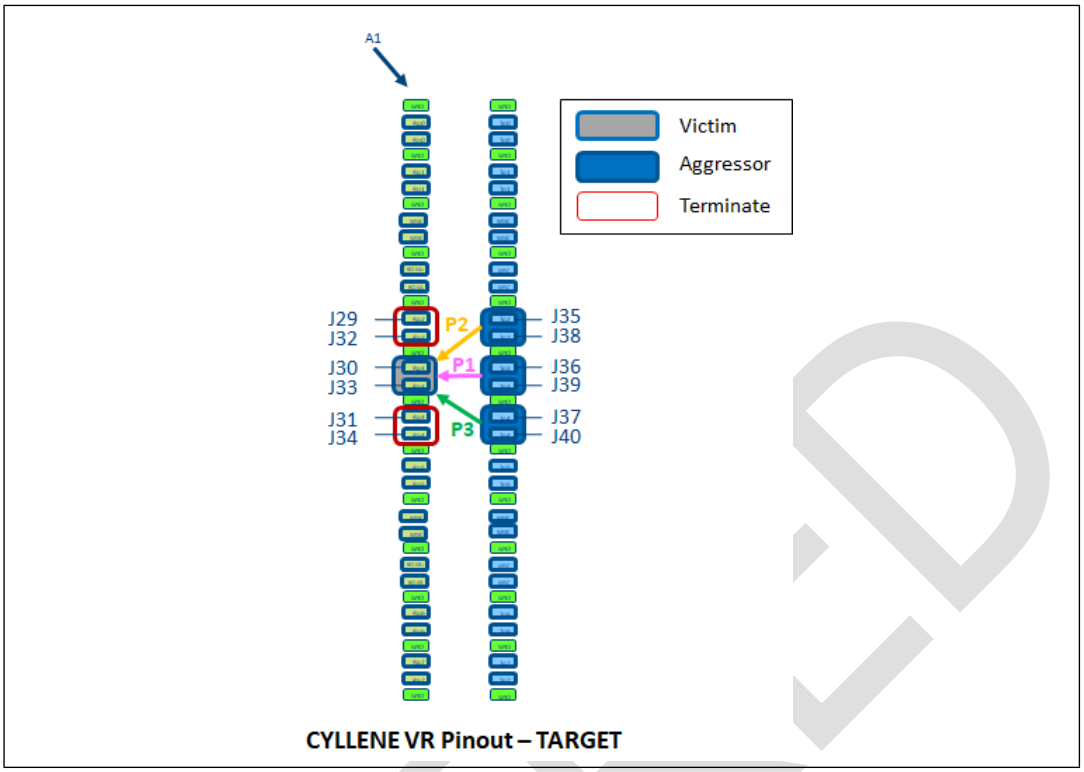


Figure 9-6 Vertical Receptacle, NEXT RX Victim

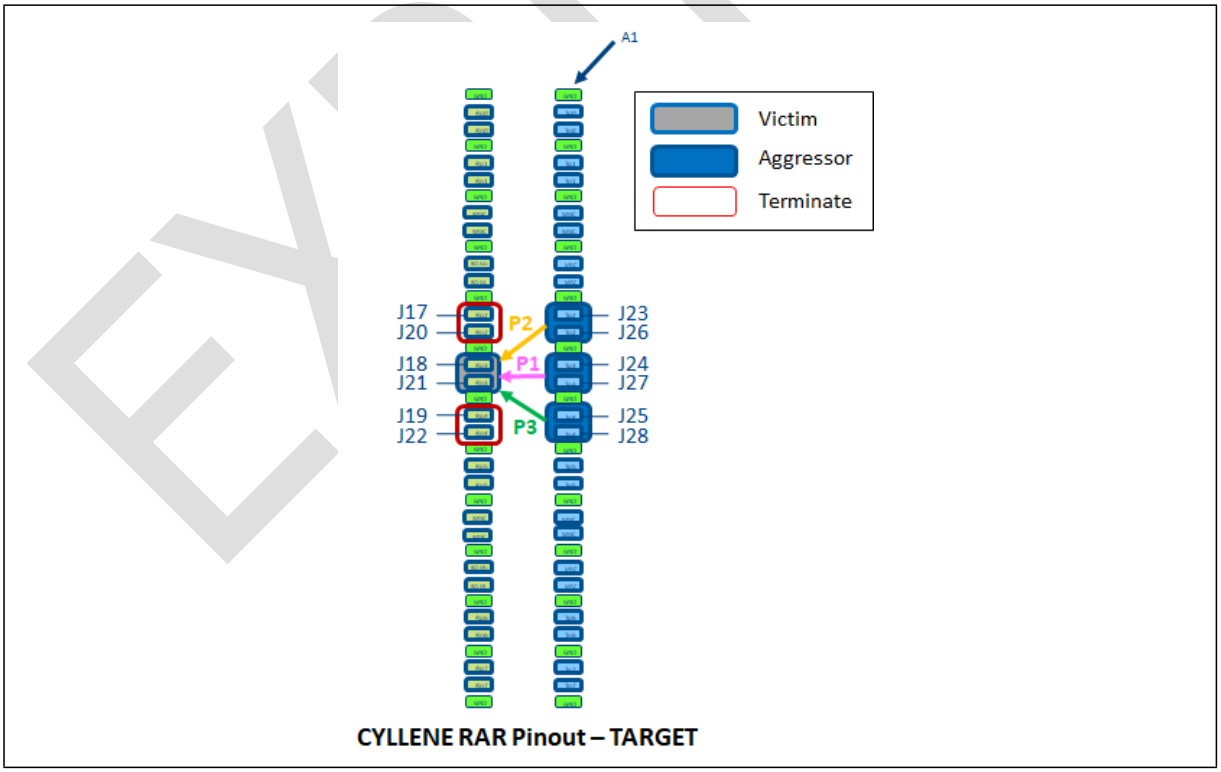


Figure 9-7 Right Angle Receptacle, NEXT RX Victim, Tx to Rx Cable

9.6 Far End Crosstalk

9.6.1 Single-aggressor Far-End Crosstalk (DDFEXT)

Differential single-aggressor far end crosstalk (DDFEXT) on the victim differential pair is calculated by the following formula.

Equation 9-5 Calculations for DDFEXT

$$DDFEXT(dB) = 20log_{10}\left[\frac{|S21 + S43 - S23 - S41|}{2}\right]$$

9.6.2 Multi-Disturber Far-End Crosstalk (MDFEXT)

Multi-Disturber Far-End Crosstalk (MDFEXT) on the victim differential pair is calculated as a power sum using the following equation shown below where MDFEXT(f) is expressed in dB.

Equation 9-6 Calculations for MDFEXT

$$MDFEXT\ (f) = 10\ log_{10}\left(\sum_n 10^{\frac{DDFEXT(f)}{10}}\right)|_{n=1,2,3}$$

The configuration of the cable assembly to carry out the differential measurements of insertion and return loss are shown in the following figures.

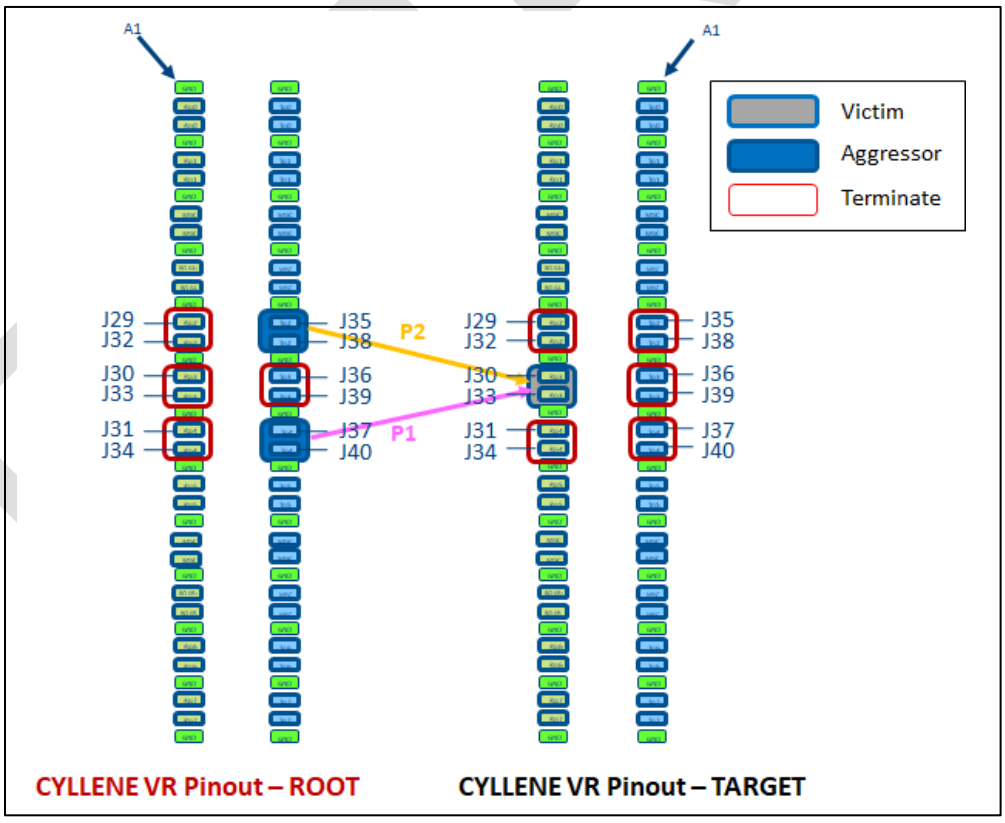


Figure 9-8 Vertical to Vertical, FEXT Rx Victim, Tx to Rx Cable

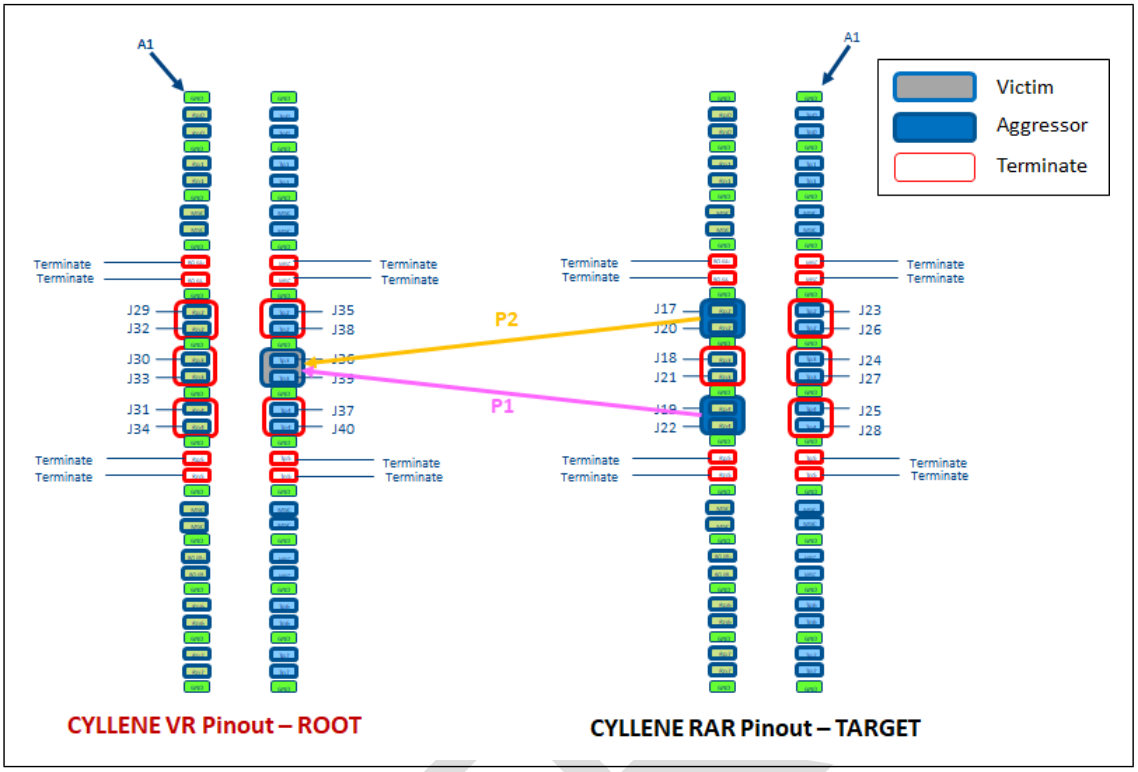


Figure 9-9 Vertical to Right Angle, FEXT Rx Victim, Tx to Rx Cable

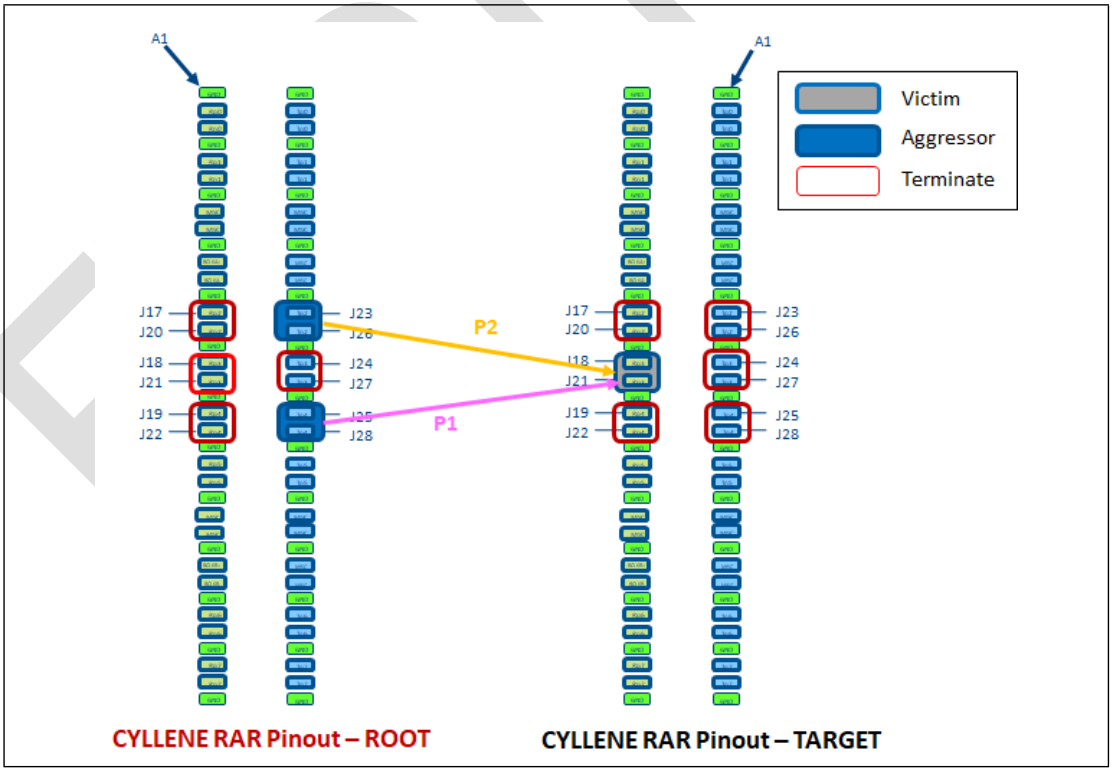


Figure 9-10 Vertical to Right Angle, FEXT Rx Victim, Tx to Rx Cable

9.7 MDFEXT Without Fixture FEXT ($MDFEXT_{woff}$)

Test boards may include fixture FEXT contributions that might be significant to verification assessments. Fixture FEXT may be removed using these steps:

1. Identify the worst case single-aggressor DDFEXT measurement including fixture, $DDFEXT_{wc}$.
2. Identify the insertion loss measurement of the victim position, $SDD21_v$.
3. Identify the fixture FEXT measurement, $FEXT_{spider}$.
4. Subtract fixture FEXT from worse case aggressor ($DDFEXT_{wcawf}$) as shown in Equation 9-7.

Equation 9-7 Calculations for $DDFEXT_{wc}$ Without Fixture FEXT

$$DDFEXT_{wcawf} = 20\,log_{10}\left(\left|DDFEXT_{wc} - \left(SDD21_v\ x\ FEXT_{spider}\right)\right|\right)$$

5. Calculate multi-aggressor FEXT without fixture FEXT ($MDFEXT_{woff}$) as shown in Equation 9-8 where N is the number of lesser aggressors and $MDFEXT_{woff}$ is expressed in dB.

Equation 9-8 Calculations for MDFEXT Without Fixture FEXT

$$MDFEXT_{woff}(f) = 10\,log_{10}\left(10^{\frac{DDFEXT_{wcawf}}{10}} + \sum_n 10^{\frac{DDFEXT_n}{10}}\right)\Big|_{n\,=\,1,2,\ldots N}$$

9.8 Effective Intra-Pair Skew (EIPS)

The effective skew calculation starts from the frequency domain skew, which is captured from the modified mixed-mode insertion loss. The modified mixed-mode insertion loss relates the differential input to the single-ended output while accounting for the coupling within a differential pair properly. The modified mixed-mode insertion loss, S2d1, and S4d1, which relate the differential input to the single-ended outputs within a 4-port system, are depicted in Figure 9-11. The intra-pair skew addition mechanism is illustrated in Figure 9-12.

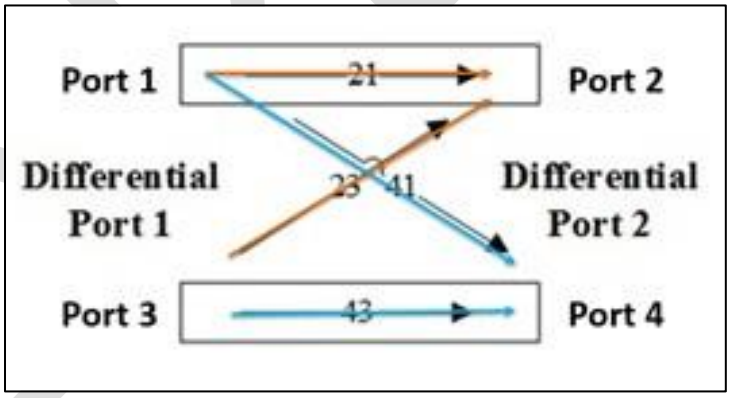


Figure 9-11 Modified Mixed-Mode Insertion Loss, S2d1 and S4d1

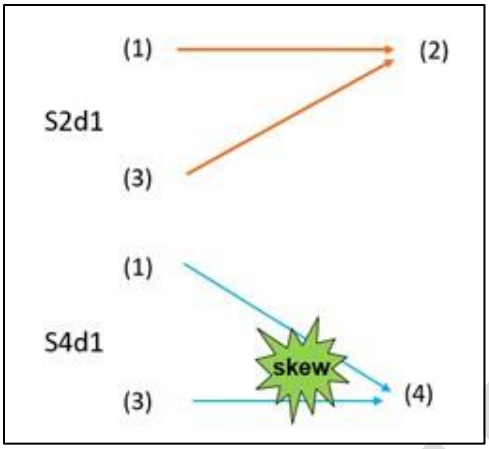


Figure 9-12 Intra-Pair Skew Introduction to a 4-Port System

The modified mixed-mode insertion loss can be represented by the single-ended S-parameter equations.

Equation 9-9 Calculations for S2d1 and S4d1

$$S2d1 = 1/\sqrt{2} \cdot (S21 - S23)$$
$$S4d1 = 1/\sqrt{2} \cdot (S43 - S41)$$

The frequency domain skew, skew(f) is obtained by calculating the difference between two phase delays.

Equation 9-10 Calculations for Skew

$$\Delta t_1 = -unwrap\big(phase(S2d1)\big)/2\pi f$$
$$\Delta t_2 = -unwrap\big(phase(S4d1)\big)/2\pi f$$
$$skew(f) = \Delta t_1 - \Delta t_2$$

The calculated frequency domain skew is multiplied by a weighting function, which is the product of power spectral density of the random binary sequence and skew impact on the normalized mode conversion. EIPS is the weighted frequency domain skew and is integrated over the frequency region up to 1.5×(Nyquist frequency, f_N),

Equation 9-11 Calculations for Effective Intra-pair Skew

$$S43_{0ps} = S43 \times e^{j2\pi f skew}$$
$$S41_{0ps} = S41 \times e^{j2\pi f skew}$$

$$SDD21_{0ps} = \big(S21 + S43_{0ps} - S23 - S41_{0ps}\big)/2$$
$$SCD21_{0ps} = \big(S21 - S23 + S41_{0ps} - S43_{0ps}\big)/2$$

$$|skew(f)| = \frac{unwrap\big(angle(S2d1/S4d1)\big)}{2\pi f}$$

$$ID(f) = \left|20\log_{10}\left|SCD21_{0ps}\right| - 20\log_{10}\left|SDD21_{0ps}\right| - (20\log_{10}|SCD21| - 20\log_{10}|SDD21|)\right|$$

$$W(f) = sinc^2\left(\frac{f}{f_b}\right)\left(\frac{1}{1+\left(\frac{f}{f_t}\right)^4}\right)\left(\frac{1}{1+\left(\frac{f}{f_r}\right)^8}\right)$$

$$EIPS = \frac{\sum_{\substack{f=min \\ Step=10MHz}}^{f=max} (ID(f) \times W(f) \times |skew(f)|)}{\sum_{\substack{f=min \\ Step=10MHz}}^{f=max} (ID(f) \times W(f))}$$

… where f_b = 2×(Nyquist frequency, f_N), f_r = 0.75× f_b, f_{max} = 1.5×(Nyquist frequency, f_N), f_{min} = minimum data provided.

Calculate |Scd21-Sdd21|impacted by $skew_{max}$ in dB. First calculate maximum skew in magnitude over the frequency of interest, up to 1.5×f_N and calculate |Scd21- Sdd21|impacted by $skew_{max}$ in dB from the S-parameter matrix shown below.

Equation 9-12 S-parameter Matrix for Calculationg Maximum Skew

$$\begin{bmatrix} S11 & S12 & S13 & S14e^{j2\pi fskew_{max}} \\ S21 & S22 & S23 & S24 \\ S31 & S32 & S33 & S34e^{j2\pi fskew_{max}} \\ S41e^{j2\pi fskew_{max}} & S42 & S43e^{j2\pi fskew_{max}} & S44 \end{bmatrix}$$

9.9 Effective Pair-to-Pair Skew (EPPS)

The Effective Pair-to-Pair Skew (EPPS) is the flight time delta between two differential pairs. The flight time is captured from phase delay, which is captured from differential insertion loss,

Figure 9-13 2 Differential Pair Port Map

Equation 9-13 Calculations for Pair-to-Pair Skew

$$\Delta flight\_time_1 = -{unwrap(phase(Sdd12))}/{(2\pi f)}$$
$$\Delta flight\_time_2 = -{unwrap(phase(Sdd34))}/{(2\pi f)}$$
$$pair\text{-}to\text{-}pair\ skew(f) = \Delta flight\_time_1(f) - \Delta flight\_time_2(f)$$

… where Sdd12 and Sdd34 are insertion loss which can be calculated from single-ended S-parameters as shown below.

Equation 9-14 Calculations for Insertion Loss, Sdd12 and Sdd34

$$Sdd12 = {}^1/_2 \cdot (S21 - S41 - S23 + S43)$$
$$Sdd34 = {}^1/_2 \cdot (S65 - S85 - S67 + S87)$$

Once frequency domain skew is calculated, the calculated frequency domain skew is multiplied by a weighting function which is the power spectral density of a random binary sequence. Effective Pair-to-Pair Skew (EPPS) is obtained by integrating the weighted frequency domain skew over the frequency region up to 1.5×(Nyquist frequency, f_N).

Equation 9-15 Calculations for Effective Pair-to-Pair Skew

$$EPPS = \int_{f_{min}}^{f_{max}} W(f) \cdot |skew(f)| df$$

$$W(f) = \frac{sinc^2\left({}^{2\pi f}/_{f_N}\right)}{\int_{f_{min}}^{f_{max}} sinc^2\left({}^{2\pi f}/_{f_N}\right) df}$$

… where f_{max} is set at 1.5×(Nyquist frequency, f_N).

9.10 Mated Cable Assembly Skew Measurement

1. Insert cable assembly into the test fixtures for the full channel measurement. The test set up is depicted in the following figure.

Figure 9-14 Skew Measurement Test Set

2. Capture the test set intra-pair skew from IL measurement of each differential pair in the test plan, defined as 'test set skew'. The test set skew is calculated using the equations as shown below and the maximum value over the frequency range is picked.

Equation 9-16 Calculations for Test Set Skew

$$Freq_{skew} = MovingAverage\left(Phase_{delay1} - Phase_{delay2}\right)$$

… for 5 GHz ≤ f ≤ 24 GHz, where …

$$Phase_{delay1} = {}^{unwrap(angle(S2D1))}/_{2\pi f}$$

$$Phase_{delay2} = {}^{unwrap(angle(S4D1))}/_{2\pi f}$$

… and …

$$S2D1 = {}^{1}/_{\sqrt{2}}(S21 - S23)$$

$$S4D1 = {}^{1}/_{\sqrt{2}}(S43 - S41)$$

The window size of the moving average is 100 points.

3. Calculate DUT skew by subtracting absolute value of rounded fixture skew from absolute value of the test set skew.

9.11 Impedance Measurement

9.11.1 Rise Time

Ensure a 15 psec (20-80%) rise time is achieved at the end of the half primary through such that the proper rise time is set at the reference plane.

9.11.2 Instantaneous Impedance

For a given 85 ± Zi Ohm instantaneous impedance specification one would evaluate as follows.

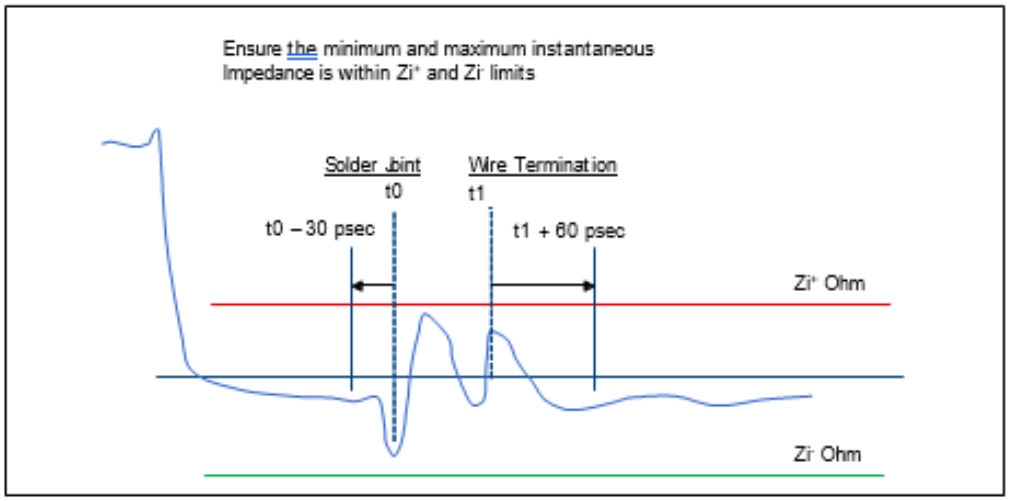


Figure 9-15 Instantaneous Impedance Example

9.11.3 Average Impedance

For a given 85 ± Za Ohm average impedance specification one would evaluate as follows

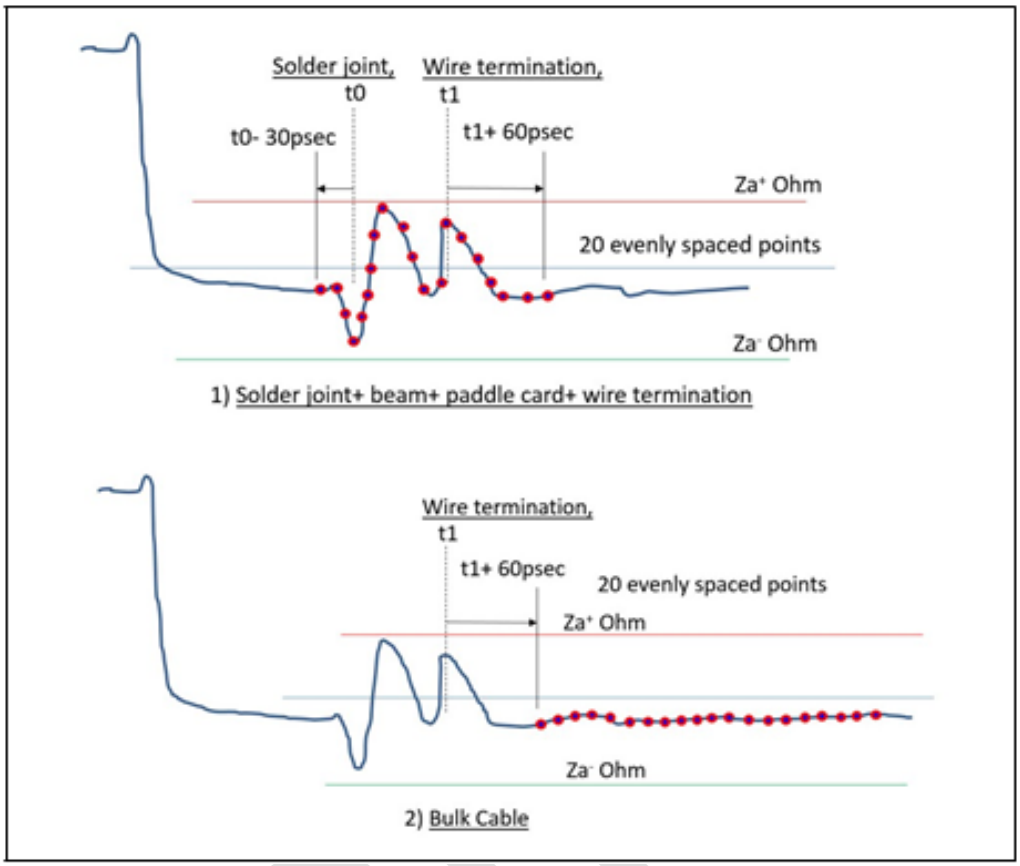


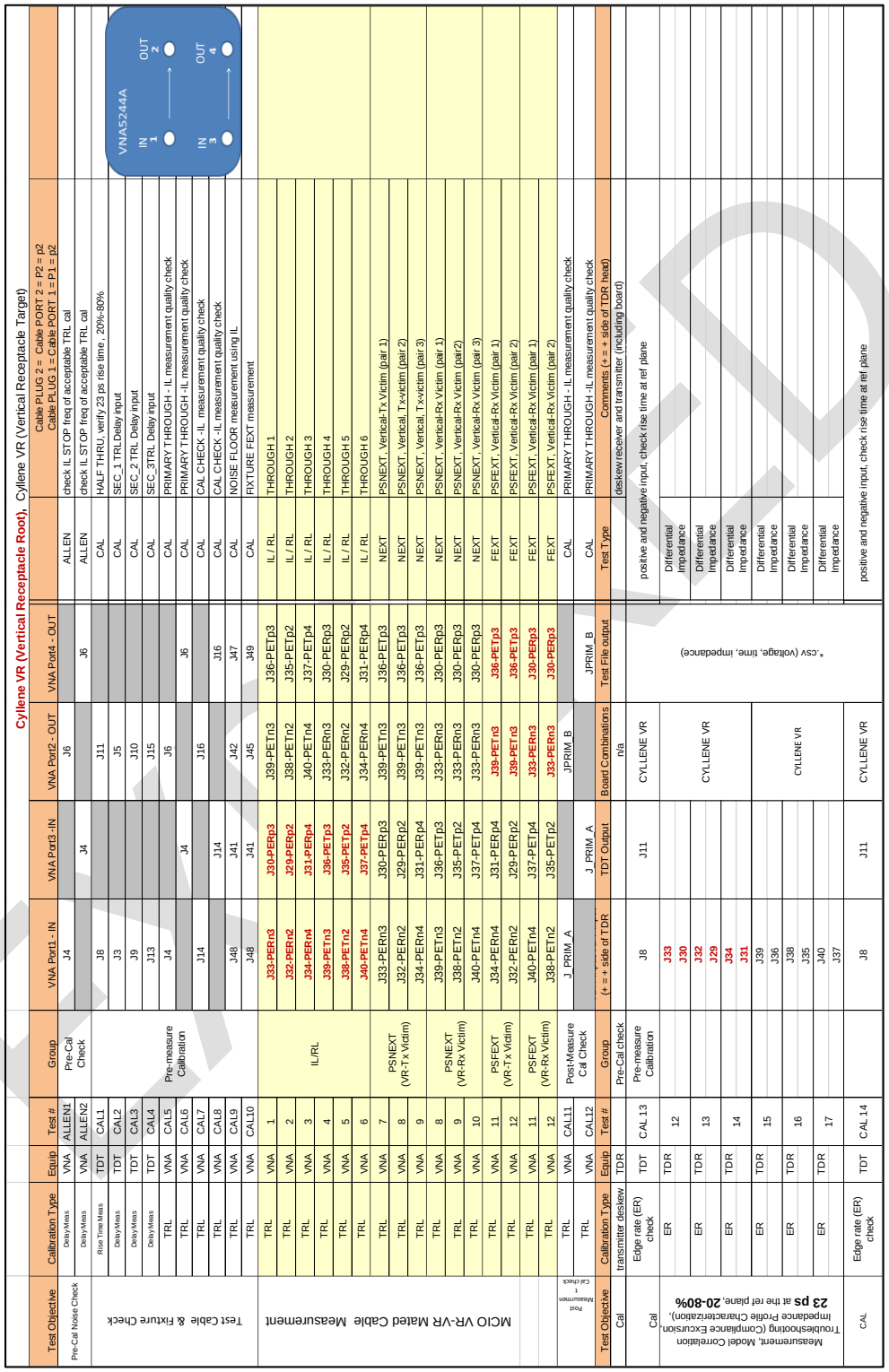
Figure 9-16 Average Impedance Example

10. Cable Assembly Test Plans

10.1 Vertical Receptacle to Vertical Receptacle, MCA Measurement, Rx to Tx

Cable

Table 10-1 VR to VR Test Plan



Cyllene VR (Vertical Receptacle Root), Cyllene VR (Vertical Receptacle Target)

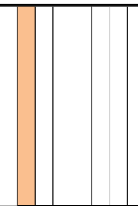
Cable PLUG 2 = Cable PORT 2 = P2 = p2
Cable PLUG 1 = Cable PORT 1 = P1 = p2

Test Objective	Calibration Type	Equip	Test #	Group	VNA Port1 - IN	VNA Port3 -IN	VNA Port2- OUT	VNA Port4 - OUT		Comments (+ = + side of TDR head)
Pre-Cal Noise Check	Delay/Mass	VNA	ALLEN1	Pre-Cal Check	J4		J6		ALLEN	check IL STOP freq of acceptable TRL cal
	Delay/Mass	VNA	ALLEN2			J4		J6	ALLEN	check IL STOP freq of acceptable TRL cal
Test Cable & Fixture Check	Rise Time Meas	TDT	CAL1	Pre-measure Calibration	J8		J11		CAL	HALF THRU, verify 23 ps rise time , 20%-80%
	Delay/Mass	TDT	CAL2		J3		J5		CAL	SEC_1 TRL Delay input
	Delay/Mass	TDT	CAL3		J9		J10		CAL	SEC_2 TRL Delay input
	Delay/Mass	TDT	CAL4		J13		J15		CAL	SEC_3TRL Delay input
	TRL	VNA	CAL5		J4	J6			CAL	PRIMARY THROUGH - IL measurement quality check
	TRL	VNA	CAL6			J4		J6	CAL	PRIMARY THROUGH -IL measurement quality check
	TRL	VNA	CAL7		J14		J16		CAL	CAL CHECK -IL measurement quality check
	TRL	VNA	CAL8			J14		J16	CAL	CAL CHECK -IL measurement quality check
	TRL	VNA	CAL9		J48	J41	J42	J47	CAL	NOISE FLOOR measurement using IL
	TRL	VNA	CAL10		J48	J41	J45	J49	CAL	FIXTURE FEXT measurement
MCIO VR-VR Mated Cable Measurement	TRL	VNA	1	IL/RL	J33-PERn3	J30-PERp3	J39-PETn3	J36-PETp3	IL / RL	THROUGH 1
	TRL	VNA	2		J32-PERn2	J29-PERp2	J38-PETn2	J35-PETp2	IL / RL	THROUGH 2
	TRL	VNA	3		J34-PERn4	J31-PERp4	J40-PETn4	J37-PETp4	IL / RL	THROUGH 3
	TRL	VNA	4		J39-PETn3	J36-PETp3	J33-PERn3	J30-PERp3	IL / RL	THROUGH 4
	TRL	VNA	5		J38-PETn2	J35-PETp2	J32-PERn2	J29-PERp2	IL / RL	THROUGH 5
	TRL	VNA	6		J40-PETn4	J37-PETp4	J34-PERn4	J31-PERp4	IL / RL	THROUGH 6
	TRL	VNA	7	PSNEXT (VR-T x Victim)	J33-PERn3	J30-PERp3	J39-PETn3	J36-PETp3	NEXT	PSNEXT, Vertical-Tx Victim (pair 1)
	TRL	VNA	8		J32-PERn2	J29-PERp2	J39-PETn3	J36-PETp3	NEXT	PSNEXT, Vertical, Tx-victim (pair 2)
	TRL	VNA	9		J34-PERn4	J31-PERp4	J39-PETn3	J36-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 1)
	TRL	VNA	8	PSNEXT (VR-Rx Victim)	J39-PETn3	J36-PETp3	J33-PERn3	J30-PERp3	NEXT	PSNEXT, Vertical-Rx Victim (pair2)
	TRL	VNA	9		J38-PETn2	J35-PETp2	J33-PERn3	J30-PERp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 3)
	TRL	VNA	10		J40-PETn4	J37-PETp4	J33-PERn3	J30-PERp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 3)
	TRL	VNA	11	PSFEXT (VR-T x Victim)	J34-PERn4	J31-PERp4	J39-PETn3	J36-PETp3	FEXT	PSFEXT, Vertical-Rx Victim (pair 1)
	TRL	VNA	12		J32-PERn2	J29-PERp2	J39-PETn3	J36-PETp3	FEXT	PSFEXT, Vertical-Rx Victim (pair 2)
	TRL	VNA	11	PSFEXT (VR-Rx Victim)	J40-PETn4	J37-PETp4	J33-PERn3	J30-PERp3	FEXT	PSFEXT, Vertical-Rx Victim (pair 1)
	TRL	VNA	12		J38-PETn2	J35-PETp2	J33-PERn3	J30-PERp3	FEXT	PSFEXT, Vertical-Rx Victim (pair 2)
Post Measurement (Cal check)	TRL	VNA	CAL11	Post-Measure Cal Check	J_PRIM_A		J_PRIM_B		CAL	PRIMARY THROUGH - IL measurement quality check
	TRL	VNA	CAL12			J_PRIM_A		JPRIM_B	CAL	PRIMARY THROUGH -IL measurement quality check
Test Objective	Calibration Type	Equip	Test #	Group	TDT Output	Board Combinations	Test File output		Test Type	Comments (+ = + side of TDR head)
Cal	transmitter deskew	TDR		Pre-Cal check		n/a				deskew receiver and transmitter (including board)
Measurement, Model Correlation Troubleshooting (Compliance Excursion, Impedance Profile Characterization), **23 ps** at the ref plane, **20-80%**	Edge rate (ER) check	TDT	CAL 13	Pre-measure Calibration	J11	CYLLENE VR	*.csv (voltage, time, impedance)		positive and negative input, check rise time at ref plane	
	ER	TDR	12						Differential Impedance	
					J33					
					J30					
	ER	TDR	13		J32	CYLLENE VR			Differential Impedance	
					J29					
	ER	TDR	14		J34				Differential Impedance	
					J31					
	ER	TDR	15		J39				Differential Impedance	
					J36					
	ER	TDR	16		J38	CYLLENE VR			Differential Impedance	
					J35					
	ER	TDR	17		J40				Differential Impedance	
					J37					
CAL	Edge rate (ER) check	TDT	CAL 14		J8	J11	CYLLENE VR		positive and negative input, check rise time at ref plane	

10.2 Vertical Receptacle to RA Receptacle, MCA Measurement, Rx to Tx Cable

Table 10-2 VR to RA Test Plan

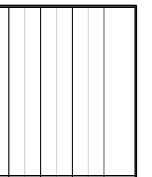
Test Objective	Calibration Type	Equip	Test #	Group	Cyllene VT (Vertical Root), Cyllene RAR (Right Angle Target) VNA Port1 - IN	VNA Port3 -IN	VNA Port2 - OUT	VNA Port4 - OUT	Test Type	Cable PLUG 2 = Cable PORT 2 = P2 = p2 Cable PLUG 1 = Cable PORT 1 = P1 = p2
Pre-Cal Noise Check	Delay Meas	VNA	ALLEN1	Pre-Cal Check	J4	J4	J6	J6	ALLEN	check IL STOP freq of acceptable TRL cal
	Delay Meas	VNA	ALLEN2						ALLEN	check IL STOP freq of acceptable TRL cal
Test Cable & Fixture Check	Rise Time Meas	TDT	CAL1		J8	J4	J11		CAL	HALF THRU, verify 23 ps rise time , 20%-80%
	Delay Meas	TDT	CAL2		J3		J5		CAL	SEC_1 TRLDelay Input
	Delay Meas	TDT	CAL3		J9		J10		CAL	SEC_2 TRL Delay Input
	Delay Meas	TDT	CAL4		J13		J15		CAL	SEC_3TRL Delay Input
	TRL	VNA	CAL5	Pre-measure Calibration	J4	J6	J6	J6	CAL	PRIMARY THROUGH - IL measurement quality check
	TRL	VNA	CAL6			J4	J6	J6	CAL	PRIMARY THROUGH -IL measurement quality check
	TRL	VNA	CAL7		J14		J16		CAL	CAL CHECK -IL measurement quality check
	TRL	VNA	CAL8			J14		J16	CAL	CAL CHECK -IL measurement quality check
	TRL	VNA	CAL9		J48	J41	J42	J47	CAL	NOISE FLOOR measurement using IL
	TRL	VNA	CAL10		J48	J41	J45	J49	CAL	FIXTURE FEXT measurement
MCIO V-RAR Mated Cable Measurement	TRL	VNA	1	IL/RL	J33-PERn3	J30-PERp3	J27-PETn3	J24-PETp3	IL / RL	THROUGH 1
	TRL	VNA	2		J32-PERn2	J29-PERp2	J26-PETn2	J23-PETp2	IL / RL	THROUGH 2
	TRL	VNA	3		J34-PERn4	J31-PERp4	J28-PETn4	J25-PETp4	IL / RL	THROUGH 3
	TRL	VNA	4		J39-PETn3	J36-PETp3	J21-PERn3	J18-PERp3	IL / RL	THROUGH 4
	TRL	VNA	5		J38-PETn2	J35-PETp2	J20-PETn2	J17-PETp2	IL / RL	THROUGH 5
	TRL	VNA	6		J40-PETn4	J37-PETp4	J22-PERn4	J19-PERp4	IL / RL	THROUGH 6
	TRL	VNA	7	PSNEXT (VR-TX Victim)	J33-PERn3	J30-PERp3	J39-PETn3	J36-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 1)
	TRL	VNA	8		J32-PERn2	J29-PERp2	J39-PETn3	J36-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair2)
	TRL	VNA	9		J34-PERn4	J31-PERp4	J39-PETn3	J36-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 3)
	TRL	VNA	10	PSNEXT (RAR-Tx Victim)	J21-PERn3	J18-PERp3	J27-PETn3	J24-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 1)
	TRL	VNA	11		J20-PETn2	J17-PETp2	J27-PETn3	J24-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair2)
	TRL	VNA	12		J22-PERn4	J19-PERp4	J27-PETn3	J24-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 3')
	TRL	VNA	7	PSNEXT (VR-Rx Victim)	J39-PETn3	J36-PETp3	J33-PETn3	J30-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 1)
	TRL	VNA	8		J38-PETn3	J35-PETp3	J33-PETn3	J30-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair2)
	TRL	VNA	9		J40-PETn3	J37-PETp3	J33-PETn3	J30-PETp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 3)
	TRL	VNA	10	PSNEXT (RAR-Rx Victim)	J27-PETn3	J24-PETp3	J21-PERn3	J18-PERp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 1)
	TRL	VNA	11		J26-PETn2	J23-PETp2	J21-PERn3	J18-PERp3	NEXT	PSNEXT, Vertical-Rx Victim (pair2)
	TRL	VNA	12		J28-PETn4	J25-PETp4	J21-PERn3	J18-PERp3	NEXT	PSNEXT, Vertical-Rx Victim (pair 3')
	TRL	VNA	13	PSFEXT (VR-Tx Victim)	J22-PERn4	J19-PERp4	J39-PETn3	J36-PETp3	FEXT	PSFEXT, RA-Rx Victim (pair 1)
	TRL	VNA	14		J20-PETn2	J17-PETp2	J39-PETn3	J36-PETp3	FEXT	PSFEXT, RA-Rx Victim (pair 2)
	TRL	VNA	15	PSFEXT (VR-Rx Victim)	J28-PETn4	J25-PETp4	J33-PERn3	J30-PERp3	FEXT	PSFEXT, RA-Rx Victim (pair 1)
	TRL	VNA	16		J26-PETn2	J23-PETp2	J33-PERn3	J30-PERp3	FEXT	PSFEXT, RA-Rx Victim (pair 2)
	TRL	VNA	13	PSFEXT (RAR-Tx Victim)	J40-PETn3	J37-PETp3	J21-PERn3	J18-PERp3	FEXT	PSFEXT, RA-Rx Victim (pair 1)
	TRL	VNA	14		J38-PETn2	J35-PETp2	J21-PERn3	J18-PERp3	FEXT	PSFEXT, RA-Rx Victim (pair 2)
	TRL	VNA	15	PSFEXT (RAR-Rx Victim)	J34-PERn4	J31-PERp4	J27-PETn3	J24-PETp3	FEXT	PSFEXT, RA-Rx Victim (pair 1)
	TRL	VNA	16		J32-PERn2	J29-PERp2	J27-PETn3	J24-PETp3	FEXT	PSFEXT, RA-Rx Victim (pair 2)
Post Measurement Cal Check	TRL	VNA	CAL11	Post-Measure Cal Check	J4		J6		CAL	PRIMARY THROUGH - IL measurement quality check
	TRL	VNA	CAL12			J4		J6	CAL	PRIMARY THROUGH -IL measurement quality check
Test Objective	Calibration Type	Equip	Test #	Group	(+ = + side of TDR	TDT Output	Board Combinations	Test File output	Test Type	Comments (+ = + side of TDR head)
Cal	transmitter deskew	TDR		Pre-Cal check			n/a			deskew receiver and transmitter (including board)
Measurement, Model Correlation Troubleshooting (Compliance Excursion, Impedance Profile Characterization), **23 ps** at the ref plane, **20-80%**	Edge rate (ER) check	TDT	CAL 13	Pre-measure Calibration	J8	J11	CYLLENE VR	*.csv (voltage, time, impedance)	positive and negative input, check rise time at ref plane	
	ER	TDR	17		J35				Differential Impedance	
	ER	TDR	18		J36		CYLLENE VR		Differential Impedance	
	ER	TDR	19		J34				Differential Impedance	
	ER	TDR	20		J33				Differential Impedance	
	ER	TDR	21		J37		CYLLENE RAR		Differential Impedance	
	ER	TDR	22		J38				Differential Impedance	
CAL	Edge rate (ER) check	TDT	CAL 14		J8	J11	CYLLENE VR		positive and negative input, check rise time at ref plane	



10.3 RA Receptacle to RA Receptacle, MCA Measurement, Rx to Tx Cable

Table 10-3 RA to RA Test Plan

					CYLLENE RAR - ROOT, CYLLENE RAR - TARGET						
Test Objective	Calibration Type	Equip	Test #	Group	VNA Port1 - IN	VNA Port3 -IN	VNA Port2 - OUT	VNA Port4 - OUT	Test Type	Cable PLUG 2 = Cable PORT 2 = P2 = p2 Cable PLUG 1 = Cable PORT 1 = P1 = p2	Notes
Pre-Cal Noise Check	Delay Meas	VNA	ALLEN1	Pre-Cal Check	J4		J6		ALLEN	check IL STOP freq of acceptable TRL cal	
	Delay Meas	VNA	ALLEN2			J4		J6	ALLEN	check IL STOP freq of acceptable TRL cal	
Test Cable & Fixture Check	Rise Time Meas	TDT	CAL1	Pre-measure Calibration	J8		J11		CAL	HALF THRU, verify 23 ps rise time , 20%-80%	
	Delay Meas	TDT	CAL2		J3		J5		CAL	SEC_1 TRLDelay input	
	Delay Meas	TDT	CAL3		J9		J10		CAL	SEC_2 TRL Delay input	
	Delay Meas	TDT	CAL4		J13		J15		CAL	SEC_3TRL Delay input	
	TRL	VNA	CAL5		J4	J4	J6	J6	CAL	PRIMARY THROUGH - IL measurement quality check	
	TRL	VNA	CAL6						CAL	PRIMARY THROUGH -IL measurement quality check	
	TRL	VNA	CAL7		J14	J14	J16	J16	CAL	CAL CHECK -IL measurement quality check	
	TRL	VNA	CAL8						CAL	CAL CHECK -IL measurement quality check	
	TRL	VNA	CAL9		J48	J41	J42	J47	CAL	NOISE FLOOR measurement using IL	
	TRL	VNA	CAL10		J48	J41	J45	J49	CAL	FIXTURE FEXT measurement	
MCIO RAR-RAR cable assembly Frequency domain measurement	TRL	VNA	1	IL/RL	J21 - A18_Rx_3_DN	J18 - A17_Rx_3_DP	J27 - B18_Tx_3_DN	J24 - B17_TX_3_DP	IL / RL	THROUGH 1 (pair 1)	
	TRL	VNA	2		J20 - A15_RX_2_DN	J17 - A15_RX_2_DP	J26 - B15_TX_2_DN	J23 - B14_TX_2_DP	IL / RL	THROUGH 2 (pair 2)	
	TRL	VNA	3		J22 - A21_Rx_4_DN	J19 - A20_Rx_4_DP	J28 - B21_Tx_4_DN	J25 - B20_TX_4_DP	IL / RL	THROUGH 3 (pair 3)	
	TRL	VNA	4		J27 - B18_Tx_3_DN	J24 - B17_TX_3_DP	J21 - A18_Rx_3_DN	J18 - A17_Rx_3_DP	IL / RL	THROUGH 4 (pair 4)	
	TRL	VNA	5		J26 - B15_TX_2_DN	J23 - B14_TX_2_DP	J20 - A15_RX_2_DN	J17 - A15_RX_2_DP	IL / RL	THROUGH 5 (pair 5)	
	TRL	VNA	6		J28 - B21_Tx_4_DN	J25 - B20_TX_4_DP	J22 - A21_Rx_4_DN	J19 - A20_Rx_4_DP	IL / RL	THROUGH6 (pair 6)	
	TRL	VNA	7	PSNEXT (RAR-Rx Victim)	J27 - B18_Tx_3_DN	J24 - B17_TX_3_DP	J21 - A18_Rx_3_DN	J18 - A17_Rx_3_DP	NEXT	PSNEXT,Rx Victim_bottom (pair 1)	
	TRL	VNA	8		J28 - B21_Tx_4_DN	J25 - B20_TX_4_DP	J21 - A18_Rx_3_DN	J18 - A17_Rx_3_DP	NEXT	PSNEXT, Rx Victim_bottom (pair 2)	
	TRL	VNA	9		J26 - B15_TX_2_DN	J23 - B14_TX_2_DP	J21 - A18_Rx_3_DN	J18 - A17_Rx_3_DP	NEXT	PSNEXT, Rx-victim_bottom (pair 3)	
	TRL	VNA	7	PSNEXT (RAR-Tx Victim)	J21 - A18_Rx_3_DN	J18 - A17_Rx_3_DP	J27 - B18_Tx_3_DN	J24 - B17_TX_3_DP	NEXT	PSNEXT, Rx Victim_bottom (pair 1)	
	TRL	VNA	8		J20 - A15_RX_2_DN	J17 - A15_RX_2_DP	J27 - B18_Tx_3_DN	J24 - B17_TX_3_DP	NEXT	PSNEXT, Rx Victim_bottom (pair 2)	
	TRL	VNA	9		J22 - A21_Rx_4_DN	J19 - A20_Rx_4_DP	J27 - B18_Tx_3_DN	J24 - B17_TX_3_DP	NEXT	PSNEXT, Rx-victim_bottom (pair 3)	
	TRL	VNA	10	PSFEXT (RAR-Rx Victim)	J28 - B21_Tx_4_DN	J25 - B20_TX_4_DP	J21 - A18_Rx_3_DN	J18 - A17_Rx_3_DP	FEXT	PSFEXT, Rx Victim_top (pair 1)	
	TRL	VNA	11		J26 - B15_TX_2_DN	J23 - B14_TX_2_DP	J21 - A18_Rx_3_DN	J18 - A17_Rx_3_DP	FEXT	PSFEXT, Rx Victim_top (pair 2)	
	TRL	VNA	10	PSFEXT (RAR-Tx Victim)	J22 - A21_Rx_4_DN	J19 - A20_Rx_4_DP	J27 - B18_Tx_3_DN	J24 - B17_TX_3_DP	FEXT	PSFEXT, Rx Victim_top (pair 1)	
	TRL	VNA	11		J20 - A15_RX_2_DN	J17 - A15_RX_2_DP	J27 - B18_Tx_3_DN	J24 - B17_TX_3_DP	FEXT	PSFEXT, Rx Victim_top (pair 2)	
Post Measurement Cal check	TRL	VNA	CAL11	Post-Measure Cal Check	J4		J6		CAL	PRIMARY THROUGH - IL measurement quality check	
	TRL	VNA	CAL12			J4		J6	CAL	PRIMARY THROUGH -IL measurement quality check	
	Test Objective	Calibration Type	Equip	Test #	Group	TDR Input/TDT Input (+ = + side of TDR head)	TDT Output	Board Combinations	Test File output	Test Type	Comments (+ = + side of TDR head)
MCIO-style Mated cable assembly Time domain measurement 23 ps at the ref plane, 20-80%	TD Skew Check	receiver and transmitter deskew	TDR		Pre-Cal check			n/a	*.csv (voltage, time, impedance)		deskew receiver and transmitter (including board)
	TD Cal Check	Edge rate (ER) check	TDT	CAL 13	Pre-measure Calibration	J8	J11	CYLLENE VR		positive and negative input, check rise time at ref plane	
		ER	TDR	12		J20	CYLLENE RA - ROOT			Differential Impedance	
						J17					
		ER	TDR	13		J21				Differential Impedance	
						J18					
		ER	TDR	14		J22	CYLLENE RA - TARGET			Differential Impedance	
						J19					
		ER	TDR	15		J26				Differential Impedance	
						J23					
		ER	TDR	16		J27				Differential Impedance	
						J24					
		ER	TDR	17		J28				Differential Impedance	
						J25					
	TD Cal Check	Edge rate (ER) check	TDT	CAL 14		J8	J11	CYLLENE VR		positive and negative input, check rise time at ref plane	



Appendix A System Mechanical Specification for Connector-only Testing

A.1 VNA AFR Measurement Templates

A.2 Vertical Connector Mechanical Fixture

A.3 Vertical Connector Test Board Bill of Materials

A.4 Right Angle Connector Mechanical Fixture

A.5 Right Angle Connector Test Board Bill of Materials

Appendix B Cyllene Bill of Materials For Cable Assembly Testing

Table B-1 Cyllene Bill of Materials

Item Typ	Item No	Item Desc	Qty	UM	Location/ID	Mfr Name	Mfr Part
SYSTEM-MOTHERBOARD	K66997-100	PBA,MB,CYLLENE,FAB1,	0	EA	EMPTY LOCATIONS MH-SITES: MH1, MH2, MH3, MH4, MH5, MH6, MH7, MH8, MH9, MH10, MH11, MH12		
SPPRINTEDBOARD	K66996-001	PB,APD,CYLLENE,6.0.010IN,0.006IN,	1	EA			
RESISTOR-DISCRETE		RES_D,0201,88.7OHM,1.00%,1/20W,	1	EA	R1		
RESISTOR-DISCRETE		RES_D,0201,82OHM,1.00%,1/20W,	1	EA	R2		
RESISTOR-DISCRETE	A47430-014	RES D,0402,42.20 OHM,1.00%,1/16W,YES	16	EA	R10, R11, R12, R13, R14, R15, R16, R17, R18, R3, R4, R5, R6, R7, R8, R9		
CONN_RF	H34229-002	Conn_RF,2.4,STD,50.0GHZ,1,VT,CMP,GOLD,MT,1	46	EA	J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J3, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J4, J40, J41, J42, J44, J45, J47, J48, J49, J5, J50, J6, J7, J8, J9	HIROSE ELECTRIC (U.S.A.),INC.*	H2.4-R-SR2-IN(37)
CONN_CARD_EDGE	K64129-002	CONN,CEDG,74P,HSEC,VT,0.600mm,SMT,BK	1	EA	J1	AMPHENOL*	G97V22312HR
CONN_CARD_EDGE	K64130-002	CONN,CEDG,74P,HSEC,RA,0.600mm,SMT,BK	1	EA	J2	AMPHENOL*	G97R22312HR

Appendix C VNA TRL Calibration

C.1 TRL Calibration Crossover Frequencies

The TRL calibration kit designed to remove the test fixture effect from the S-parameter measurement are included in the connector evaluation board design using the standards shown in Table C-1.

Table C-1 TRL Calibration Kit Crossover Frequencies

Frequency Ranges	Description
DC to ≤ 0.4 GHz	Load 1 and Load 2
> 0.4 to ≤ 2.0 GHz	Secondary #1
> 2.0 to ≤ 10.0 GHz	Secondary #2
> 10.0 to ≤ 50.0 GHz	Secondary #3

C.2 TRL Calibration E-cal and Fixture Bandwidth

TRL calibration requires preparation including e-cal, fixture bandwidth assessment and measured secondary delay times. Table C-2 shows the typical steps used to assess fixture bandwidth.

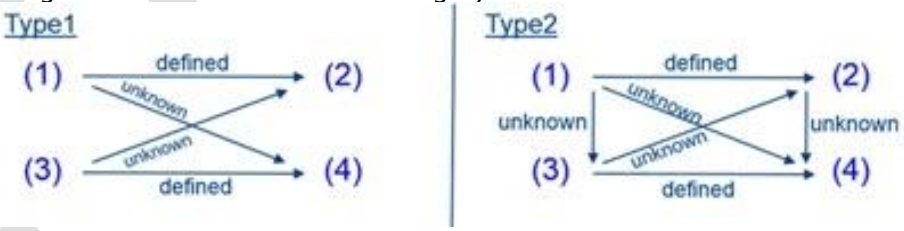
Table C-2 E-cal and Fixture Bandwidth Checks

Step	Description
1	Restart the VNA
2	Set the frequency sweep
3	Set the port power
4	Set Averaging and IF bandwidth
5	Set e-cal calibration (3 defined throughs)
6	Save the calibration
ECAL1	IL, RL measurement of Primary through
ECAL2	IL, RL measurement of Primary through

C.3 Initial TRL Calibration Steps 1 - 22

TRL calibration requires several steps. Table C-3, Table C-4, and Table C-5 show the typical steps used to achieve stable TRL calibration.

Table C-3 Initial TRL Calibration Steps

Step	Description
1	Restart the VNA
2	Recall the e-cal
3	Insert a new cal kit
4	Edit Cal Kit Information
5	TRL Cal Kit Setup: Open
6	TRL Cal Kit Setup: Short
7	TRL Cal Kit Setup: Load
8	TRL Cal Kit Setup: Primary Through
9	TRL Cal Kit Setup: Secondary 1 (use measured delay time)
10	TRL Cal Kit Setup: Secondary 2 (use measured delay time)
11	TRL Cal Kit Setup: Secondary 3 (use measured delay time)
12	TRL class assignment: TRL Through
13	TRL Class assignment: TRL Reflect
14	TRL Class assignment: TRL Line/Match
15	TRL Class assignment: Isolation
16	Set the frequency sweep
17	Set the port power
18	Set Averaging and IF bandwidth
19	TRL Guided Calibration (2 defined throughs + 2 unknown throughs or 2 defined throughs + 4 unknown unknown throughs)  ***Note:*** Choice of 2 + 2 or 2 + 4 depends on VNA firmware. Use Type 1 on initial calibration, use Type 2 to address TRL cal instability.
20	SmartCal (GUIDED Calibration)
21	DUT Connector selection
22	Modify Cal

C.4 Final TRL Calibration Steps Using 2 Defined Throughs + 2 Unknown Throughs

Final TRL calibration steps 23 to 43 and TRL calibration check using 2 defined throughs + 2 unknown throughs are shown in Table C-4.

Table C-4 TRL Calibration Steps 23 to 43 Using 2 Defined Throughs + 2 Unknown Throughs

Step	Description
23	Guided Calibration
24	Guided Calibration Step 1 of 18: Connect Port 1 to Short
25	Guided Calibration Step 2 of 18: Connect Port 2 to Short
26	Guided Calibration Step 3 of 18: Connect Port 1 to Port 2
27	Guided Calibration Step 4 of 18: Connect Port 1 and Port 2 to Secondary 3
28	Guided Calibration Step 5 of 18: Connect Port 1 and Port 2 to Secondary 2
29	Guided Calibration Step 6 of 18: Connect Port 1 and Port 2 to Secondary 1
30	Guided Calibration Step 7 of 18: Connect Port 1 to Load
31	Guided Calibration Step 8 of 18: Connect Port 2 to Load
32	Guided Calibration Step 9 of 18: Connect Port 3 to Short
33	Guided Calibration Step 10 of 18: Connect Port 4 to Short
34	Guided Calibration Step 11 of 18: Connect Port 3 to Port 4
35	Guided Calibration Step 12 of 18: Connect Port 3 and Port 4 to Secondary 3
36	Guided Calibration Step 13 of 18: Connect Port 3 and Port 4 to Secondary 2
37	Guided Calibration Step 14 of 18: Connect Port 3 and Port 4 to Secondary 1
38	Guided Calibration Step 15 of 18: Connect Port 3 to Load
39	Guided Calibration Step 16 of 18: Connect Port 4 to Load
40	Guided Calibration Step 17 of 18: Connect Port 1| Adapter | Port 4
41	Guided Calibration Step 18 of 18: Connect Port 2| Adapter | Port 3 : Quality check, adapter offset of Port 2 and Port 3 = Sec 3 delay +- 6 ps
42	Save the Calibration
43	Check the Calibration

C.5 Final TRL Calibration Steps Using 2 Defined Throughs + 4 Unknown Throughs

Final TRL calibration steps 23 to 45 and TRL calibration check using 2 defined throughs + 4 unknown throughs are shown in Table C-5.

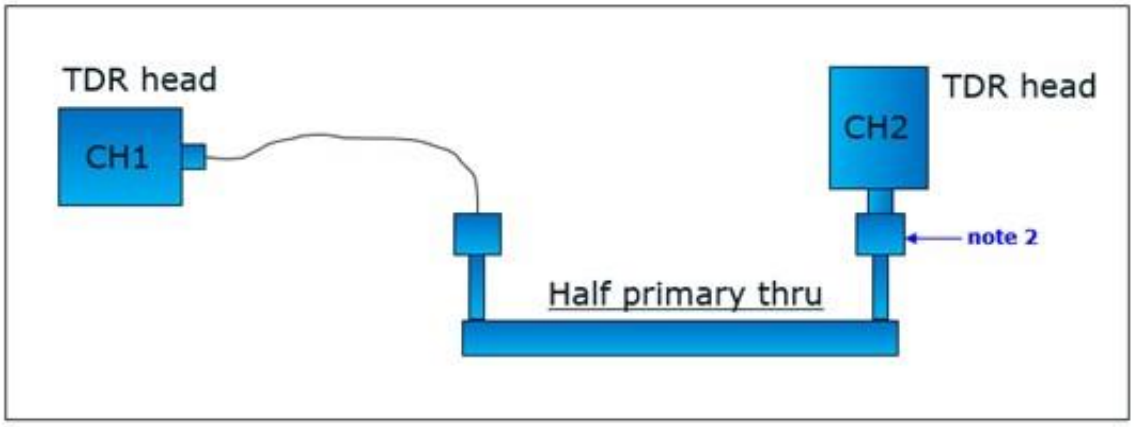
Table C-5 Final TRL Calibration Steps Using 2 Defined Throughs + 4 Unknown Throughs

Step	Description
23	Guided Calibration
24	Guided Calibration Step 1 of 20: Connect Port 1 to Short
25	Guided Calibration Step 2 of 20: Connect Port 2 to Short
26	Guided Calibration Step 3 of 20: Connect Port 1 to Port 2
27	Guided Calibration Step 4 of 20: Connect Port 1 and Port 2 to Secondary 3
28	Guided Calibration Step 5 of 20: Connect Port 1 and Port 2 to Secondary 2
29	Guided Calibration Step 6 of 20: Connect Port 1 and Port 2 to Secondary 1
30	Guided Calibration Step 7 of 20: Connect Port 1 to Load
31	Guided Calibration Step 8 of 20: Connect Port 2 to Load
32	Guided Calibration Step 9 of 20: Connect Port 3 to Short
33	Guided Calibration Step 10 of 20: Connect Port 4 to Short
34	Guided Calibration Step 11 of 20: Connect Port 3 to Port 4
35	Guided Calibration Step 12 of 20: Connect Port 3 and Port 4 to Secondary 3
36	Guided Calibration Step 13 of 20: Connect Port 3 and Port 4 to Secondary 2
37	Guided Calibration Step 14 of 20: Connect Port 3 and Port 4 to Secondary 1
38	Guided Calibration Step 15 of 20: Connect Port 3 to Load
39	Guided Calibration Step 16 of 20: Connect Port 4 to Load
40	Guided Calibration Step 17 of 20: Connect Port 1 | Adapter | Port 3
41	Guided Calibration Step 18 of 20: Connect Port 1 | Adapter | Port 4
42	Guided Calibration Step 19 of 20: Connect Port 2| Adapter | Port 3 : Quality check, adapter offset of Port 2 and Port 3 = Sec 3 delay +- 6 ps
43	Guided Calibration Step 20 of 20: Connect Port 2| Adapter | Port 4 : Quality check, adapter offset of Port 2 and Port 4 = Sec 3 delay +- 6 ps
44	Save the Calibration
45	Check the Calibration

Appendix D Rise Time Measurement

D.1 TDR Head Connections

Connect the CH1 TDR head through a cable to the half primary through and the CH2 TDR head directly to the half primary through.



(Note)
1. **It is okay to switch CH1 and CH2. But for the consistency, we will keep this configuration in this document.**
2. **An adaptor can be used for the connection.**

Figure D-1 TDR Head Connections

D.2 TDR Instrument Default Settings.

Set the TDR instrument to its default settings.

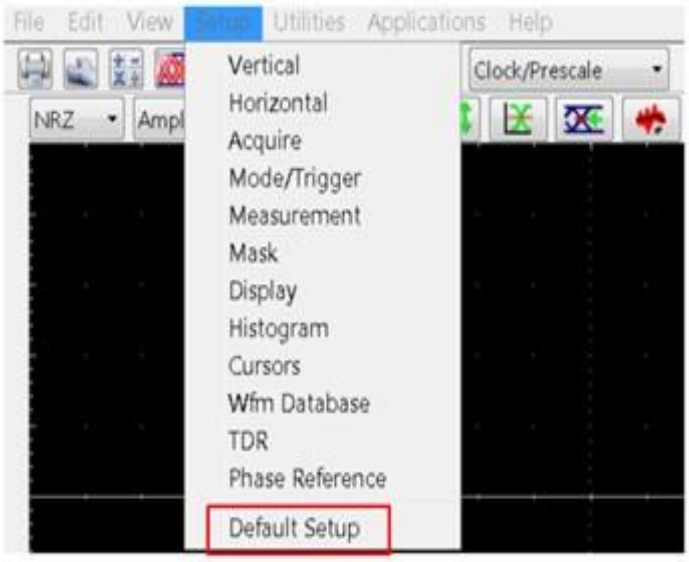


Figure D-2 TDR Instrument Default Settings Screenshot

D.3 TDR Mode Setup.

Change the TDR Mode (Setup> Mode/ Trigger> TDR) and set the rate to 200 kHz.

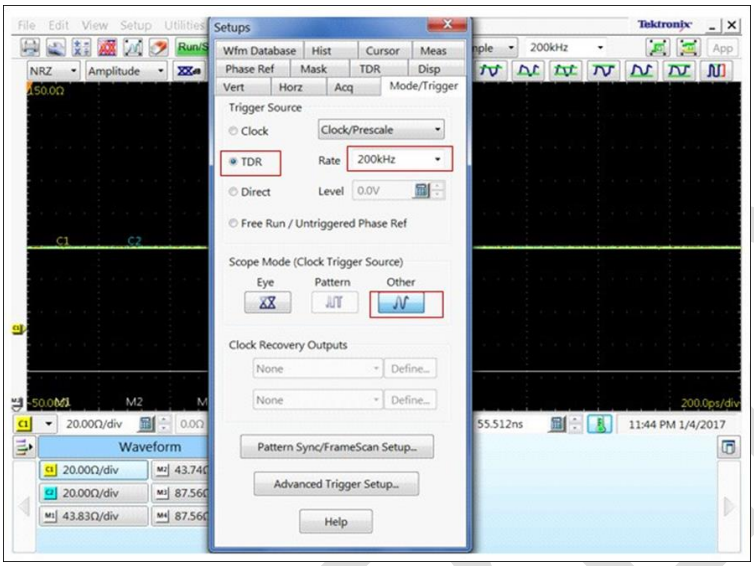


Figure D-3 TDR Mode Setup Screenshot

D.4 Channel Definition

Define the channel.

a. Setup> TDR
b. Configure both the channels to have rising edge.
c. Configure the individual channels TDR step and acquisition as follows:
   => C1: TDR step= ON and ACQ= OFF
   => C2: TDR step= OFF and ACQ= ON
d. Change the units of both the channels to 'voltage (V)'.

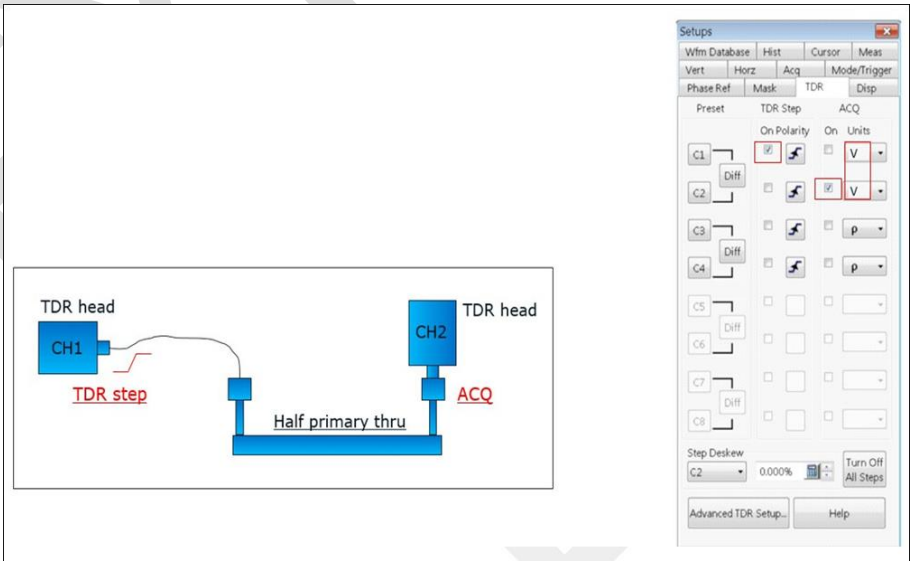


Figure D-4 Channel Definition Setup

D.5 View the Rising Edge

Use the horizontal scale and position to be able to view the rising edge.

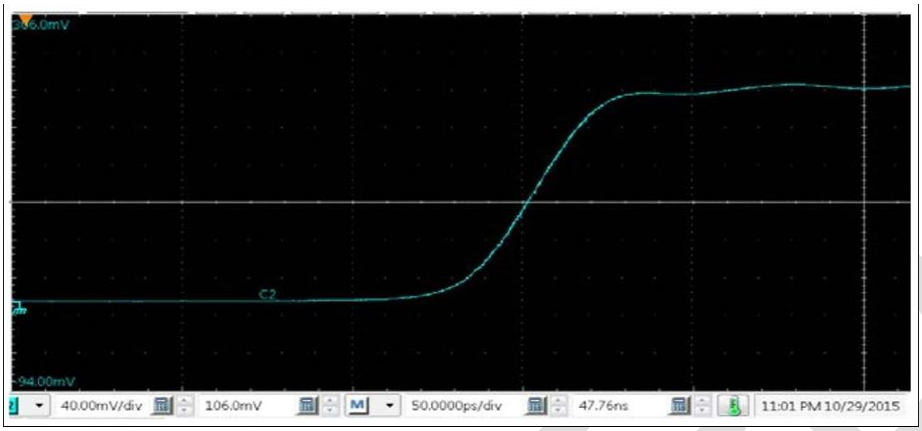


Figure D-5 TDR View of Rising Edge

D.6 Rise Time Measurement Setup.

Perform the following setup steps to enable making a rise time measurement.

a. Setup> Measurement.
b. Select Meas> Pulse- Timing> Rise Time.
c. Set Source1> C2 on Main.
d. Untick Use Wfm Database and click Clear'.
e. Select the signal type as Pulse.
f. Set the RefLevel to relative 80-20%.
g. Turn on statistics and annotations.
h. Turn on the measurement.

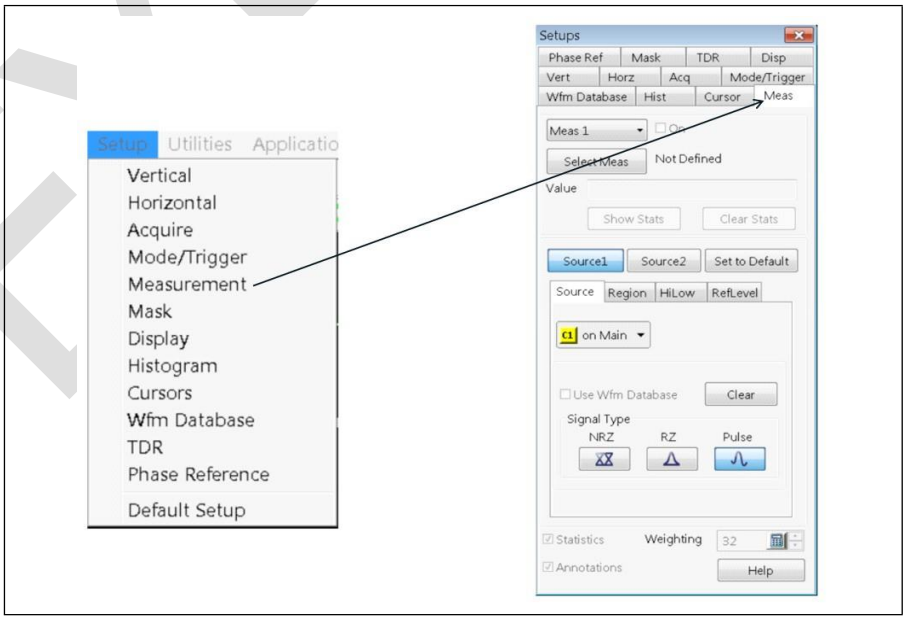


Figure D-6 Screenshot for Setup Steps a. and b.

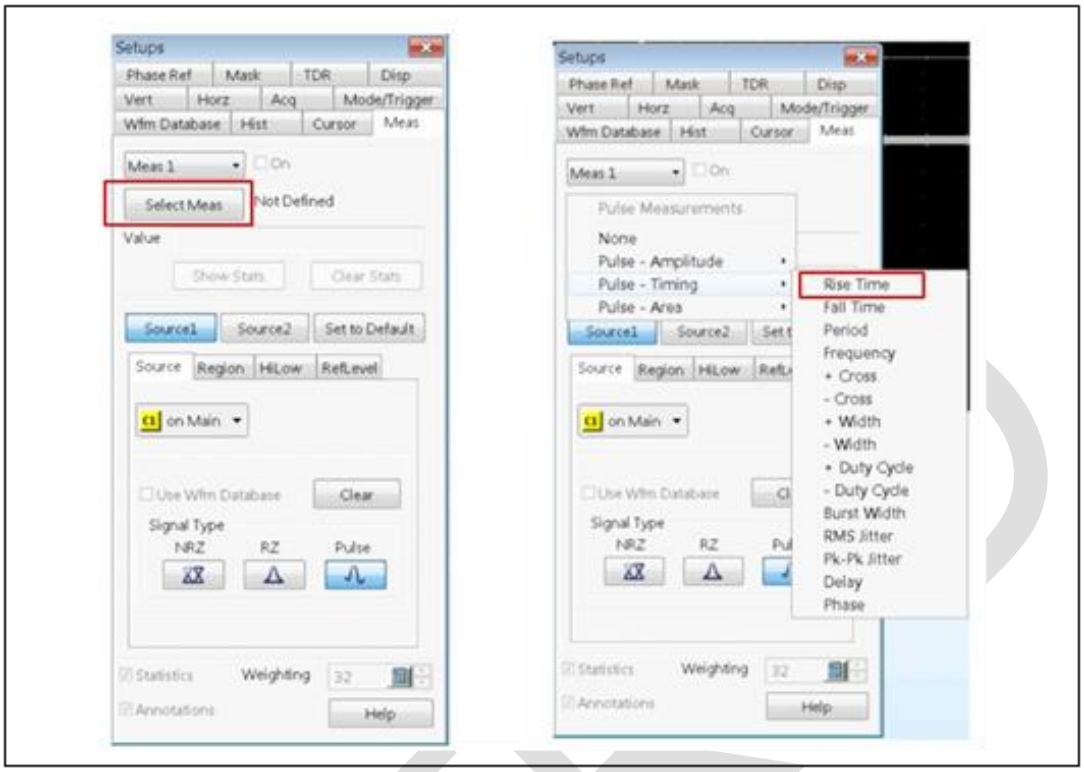


Figure D-7 Screenshot for Setup Steps b. and c.

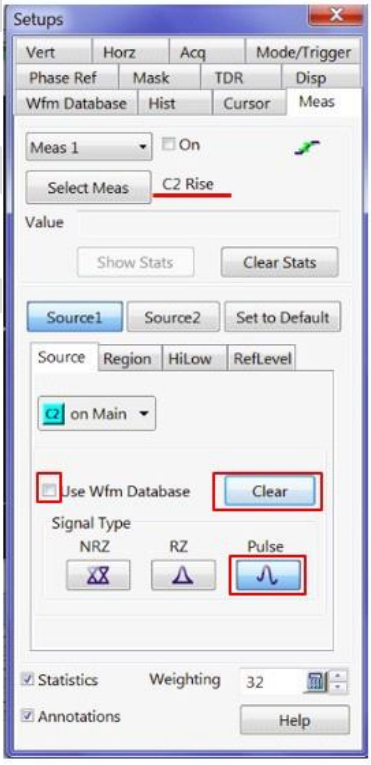


Figure D-8 Screenshot for Setup Steps d. and e.

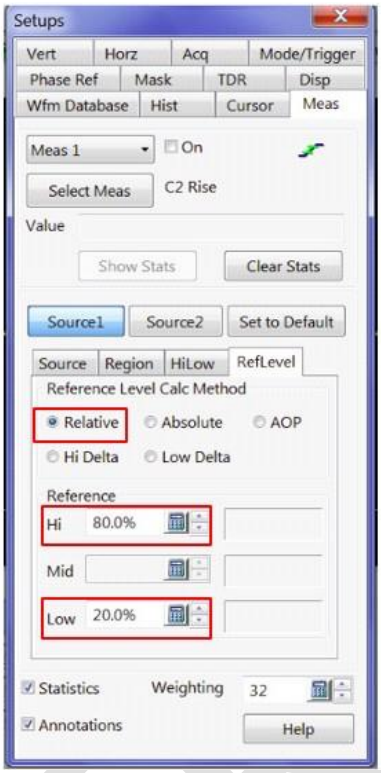


Figure D-9 Screenshot for Setup Step f.

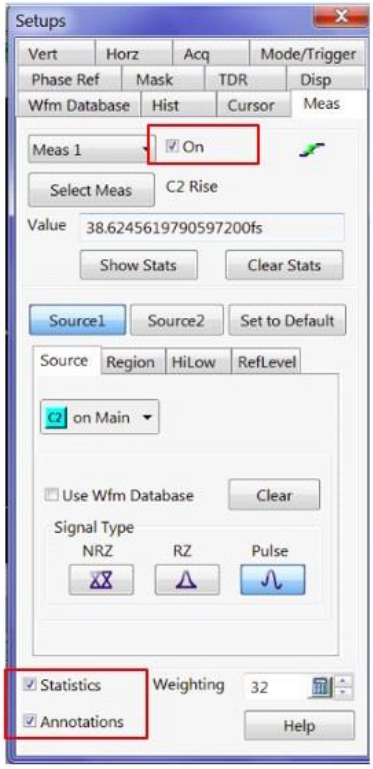


Figure D-10 Screenshot for Setup Steps g. and h.

D.7 Rise Time Adjustments.

D.7.1 Rise Time Adjustment Option 1

a. Setup> Vertical.
b. Select waveform> C1.
c. Check 'ON'.
d. Toggle between the different bandwidth options to set the right rise time.

D.7.2 Rise Time Adjustment Option 2.

- Another option to adjust the rise time is to use a software defined filter to slow the edge.

a. Edit> Define Math.
b. Math Expression: 'Filter(C2)'
c. Set the number of averages to 200.
d. Adjust the filter rise time value to reach the desired rise time by monitoring the M1 rise time measurement value.

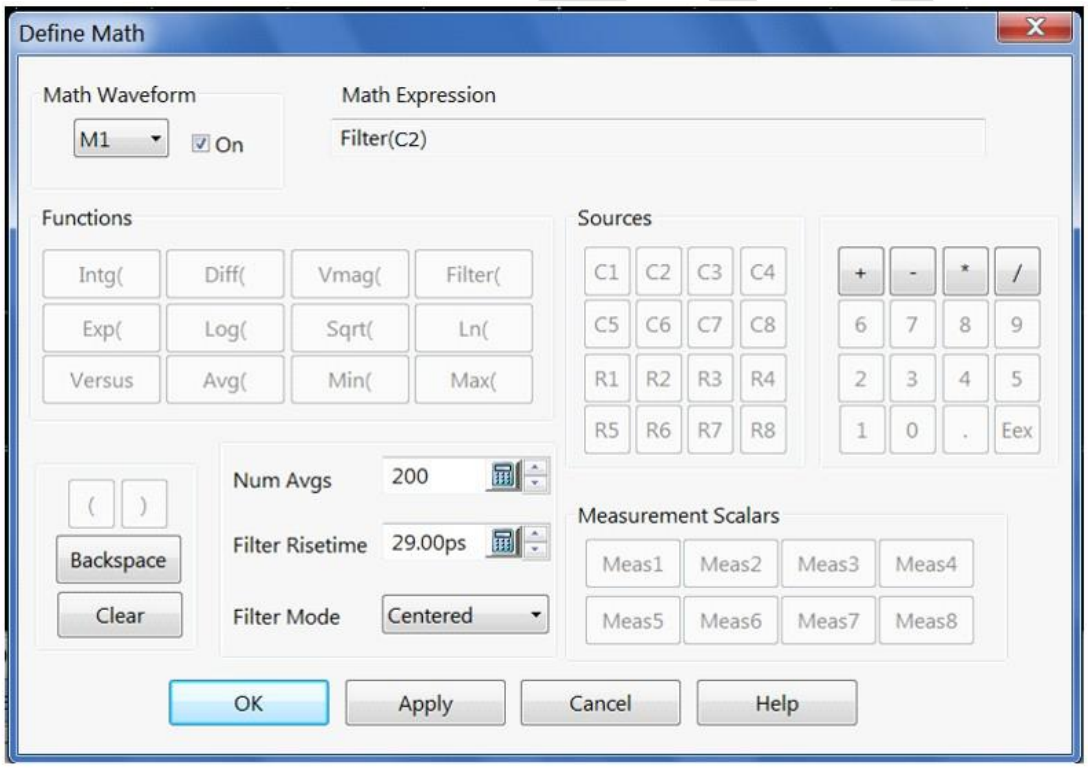


Figure D-11 Screenshot for Option 2 Steps a. and b. and c.

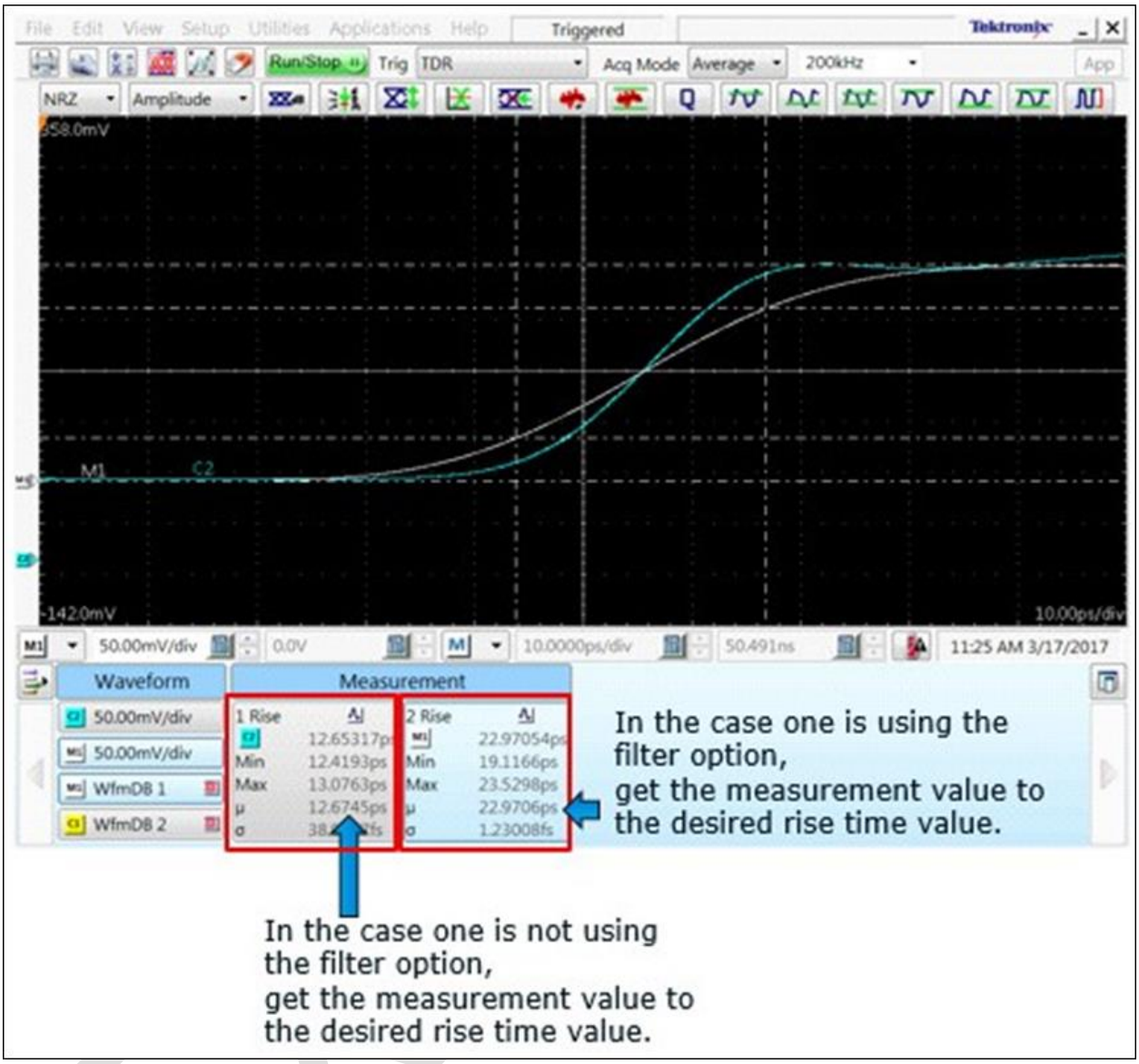


Figure D-12 Screenshot Showing Measured Rise Time