SFF-TA-1034

Specification for

Pluggable Multipurpose Module (PMM)

Rev 1.0a June 18, 2024

SECRETARIAT: SFF TA TWG

This specification is made available for public review at https://www.snia.org/sff/specifications. Comments may be submitted at https://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

This specification provides a common reference for host systems manufacturers, host system integrators, and device suppliers.

The description of the details in this specification does not assure that the specific component is available from device suppliers. If such a device is supplied it shall comply with this specification to achieve interoperability between device suppliers.

ABSTRACT: This specification defines the mechanical attributes, pin list and pin placement, function of the pins, device specific electrical requirements, and specific features of a Pluggable Multipurpose Module for use in Enterprise and Datacenter systems. This specification relies on SFF-TA-1037 for the connector mechanicals.

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Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/sff/join.

Revision History

Rev 1.0 *May 6, 2024:*
- Initial release.

Rev 1.0a *May 13, 2024:*
- Added Figure 4-1 back (did not copy during publishing).
- Fixed PCIe BASE spec reference.

Contents

Figures

Tables

1. Scope

The following specification defines the requirements for a device that is optimized for Enterprise and Datacenter applications.

1.1 Application Specific Criteria

This specification defines the pin list and pin placement, function of the pins, device specific electrical requirements, and specific features of enterprise and datacenter-based devices. This specification relies on SFF-TA-1037 for the connector mechanicals.

2. References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:

- ASME Y14.5-2009 Dimensioning and Tolerancing published by ASME, available at https://www.asme.org.
- MIPI™ Alliance Specification for I3C Basic, Version 1.0 available at https://www.mipi.org.
- Open Compute Project OCP NIC 3.0 Design Specification, revision 1.2.0 available at https://www.opencompute.org/wiki/Server/Mezz.
- PCI Express® (PCIe) Base Specification, revision 6.2, available from https://www.pcisig.com.
- PCI Express® (PCIe) Card Electromechanical Specification, revision 5.1, Version 1.0 available from https://www.pcisig.com.
- SNIA SFF-TA-1002 Card Edge multilane protocol agnostic connector specification available at https://www.snia.org/sff/specifications.
- SNIA SFF-TA-1009 Enterprise and Datacenter Standard Form Factor Pin and Signal Specification https://www.snia.org/sff/specifications.
- SNIA SFF-TA-1037 Connectors for Pluggable Multi-Purpose Module available at https://www.snia.org/sff/specifications.
- ENG-46158 Serial Gigabit Media Independent Interface (SGMII), Revision 1.8 available at https://ia803002.us.archive.org/25/items/sgmii/SGMII.pdf
- System Management Bus (SMBus) Specification, Version 3.1, available from http://smbus.org.
- United Serial Bus (USB) Specification, Version 2.0, available from https://usb.org

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

DIMENSIONING CONVENTIONS: The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May or may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Defines the signal on a connector contact when its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies the restricted designation, then the restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word, or field (e.g., a restricted byte uses the same value as defined for a reserved byte).

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

PMM: Pluggable Multipurpose Module

3.3 Definitions

Card: Refers to the device plugged into a connector

Contact Sequence: The order that a device card edge pin makes physical contact to the host connector.

Device: Refers to the interface target.

Dual Port: When enabled, the device is configured with a PCIe port A and a PCIe port B. This is known as Dual Port mode. When disabled, all lanes form a single PCIe port A. In dual port mode, the two ports must operate independently. Any interaction between the two ports is outside the scope of the specification.

Enclosure: The housing that protects the internal components and acts as a heat sink.

Endpoint: The PCIe interface target logic located on the Device.

Host: Refers to the interface source or initiator.

Root Complex: The initiator source logic located on the Host.

SRIS: Acronym for Separate Reference clock Independent Spread spectrum clocking. This is a PCI Express feature that allows independent reference clocks for host and device. In this implementation, the host does not need to provide the reference clock and each independent source supports Spread Spectrum Clocking (SSC).

SRNS: Acronym for Separate Reference clock with No Spread spectrum clocking. This is a PCI Express feature that allows independent reference clocks for host and device. In this implementation, the host does not need to provide the reference clock and Spread Spectrum Clocking (SSC) is not enabled by either source.

Switch: A logic component located on the Host used to connect between a Root Complex and 1 or more Endpoints.

Thickness: Form factor dimension including PCB thickness, z-height of all components plus mechanicals.

4. General Description

The application environment for the Pluggable Multipurpose Module (PMM) is a cabinet or enclosure connecting to one or more add-in cards. The device connects electrically to the system through a card edge connector as defined in SFF-TA-1037. This form factor is intended for use in enclosures that fit within a 1U or greater space (e.g., 1U refers to 1 standard unit of an IT equipment rack and the IT enclosures that fit in this space). An example of the form factor is shown in Figure 4-1. This specification defines the following features:

- PCIe support for existing and future specifications
  - Supports 5.0 specification (up to 32.0 GT/s signaling).
  - Supports 6.0 specification (up to 64.0 GT/s signaling).
- 1 card edge supporting up to 3 connectors as defined in SFF-TA-1037.
  - A 168-pin receptacle supporting Sixteen (16) Tx and Rx PCIe lanes, up to 200W sustained for power, and sidebands (4C+).
  - An optional power receptacle supporting up to an additional 400W sustained.
  - An optional 108-pin receptacle supporting an additional Sixteen (16) Tx and Rx PCIe lanes.
- 2 device lengths supported:
  - Short: 167 mm
  - Long: 230 mm
- 2 device thicknesses supported:
  - ½U: 18.3 mm
  - 1U: 38.4 mm
- Hot-plug capable connector and pin out but capability dependent on device support/usage.
- Common clock with options for SRIS and SRNS support by both host and device.
- Link Bifurcation control
- Support for sideband management over SMBus, I3C Basic, USB 2.0.
- Connector compatibility with SFF-TA-1008 and OCP NIC 3.0 (with host pin configurability or an interposer).

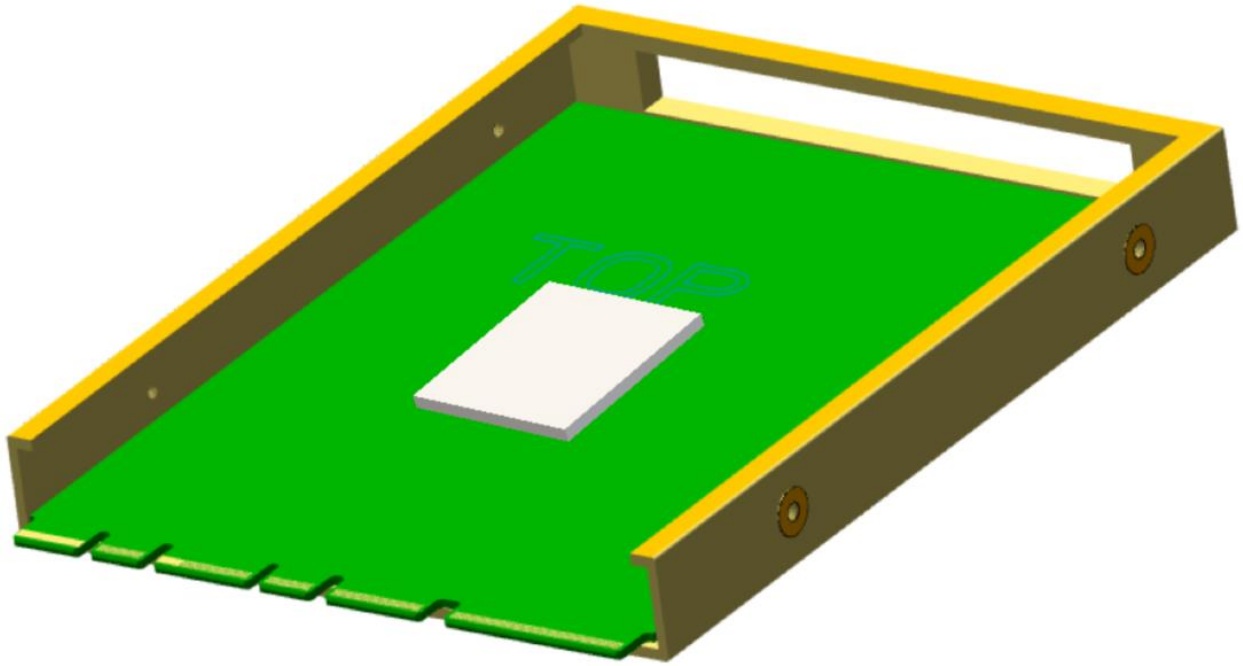

Figure 4-1. Example implementation of the Pluggable Multipurpose Module

5. Mechanical Specification

5.1 Overview

This section specifies the dimensions for the device form factor. The dimensioning convention is per ASME-Y14.5-2009 Dimensioning and Tolerancing. For mating interface details refer to SFF-TA-1037. This specification allows for device implementations that can vary in length and thickness. The following are nominal dimensions for four device variations:

- A 167 mm long x 120 mm wide x 18.30 mm thick form factor
- A 167 mm long x 120 mm wide x 38.40 mm thick form factor
- A 230 mm long x 120 mm wide x 18.30 mm thick form factor
- A 230 mm long x 120 mm wide x 38.40 mm thick form factor

No part of the host chassis of a host enclosure or parts connected to the mounting holes should encroach into any part of the bounding volume of the device form factor dimensions and tolerances as specified in this standard when the device is inserted into the host enclosure. The dimensioning convention is per ASME-Y14.5-2009 Dimensioning and Tolerancing.

The host should ensure the weight of the devices does not cause retention issues.

Unless specified, the default tolerance is +/- 0.15 mm. All dimensions provided in mm.

5.2 Physical Definition: PMM

Table 5-1. PMM Dimensions

Dimensions	Millimeters	Tolerance	Comment
A1a	18.30	+0.2/-0.5	Device Thickness (1/2U)
A1b	38.40	+0.2/-0.5	Device Thickness (1U)
C1a	167	0.55	Short device length
C1b	230	0.55	Long device length

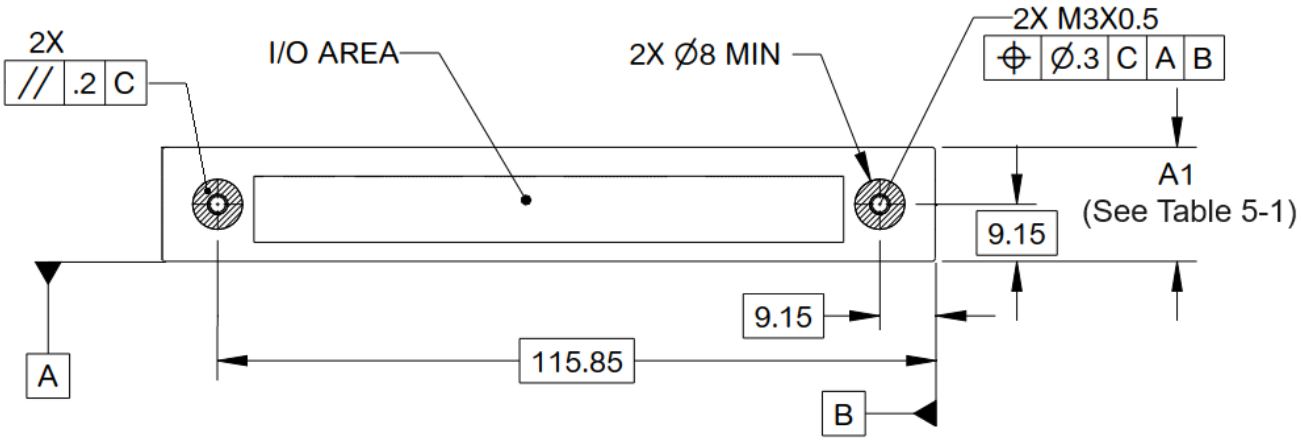

Figure 5-1. Front of PMM

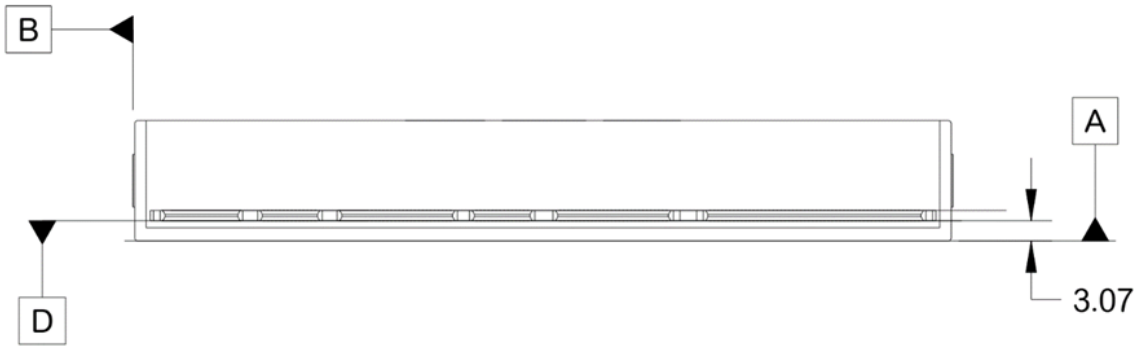

Figure 5-2. Back of PMM (card edge facing)

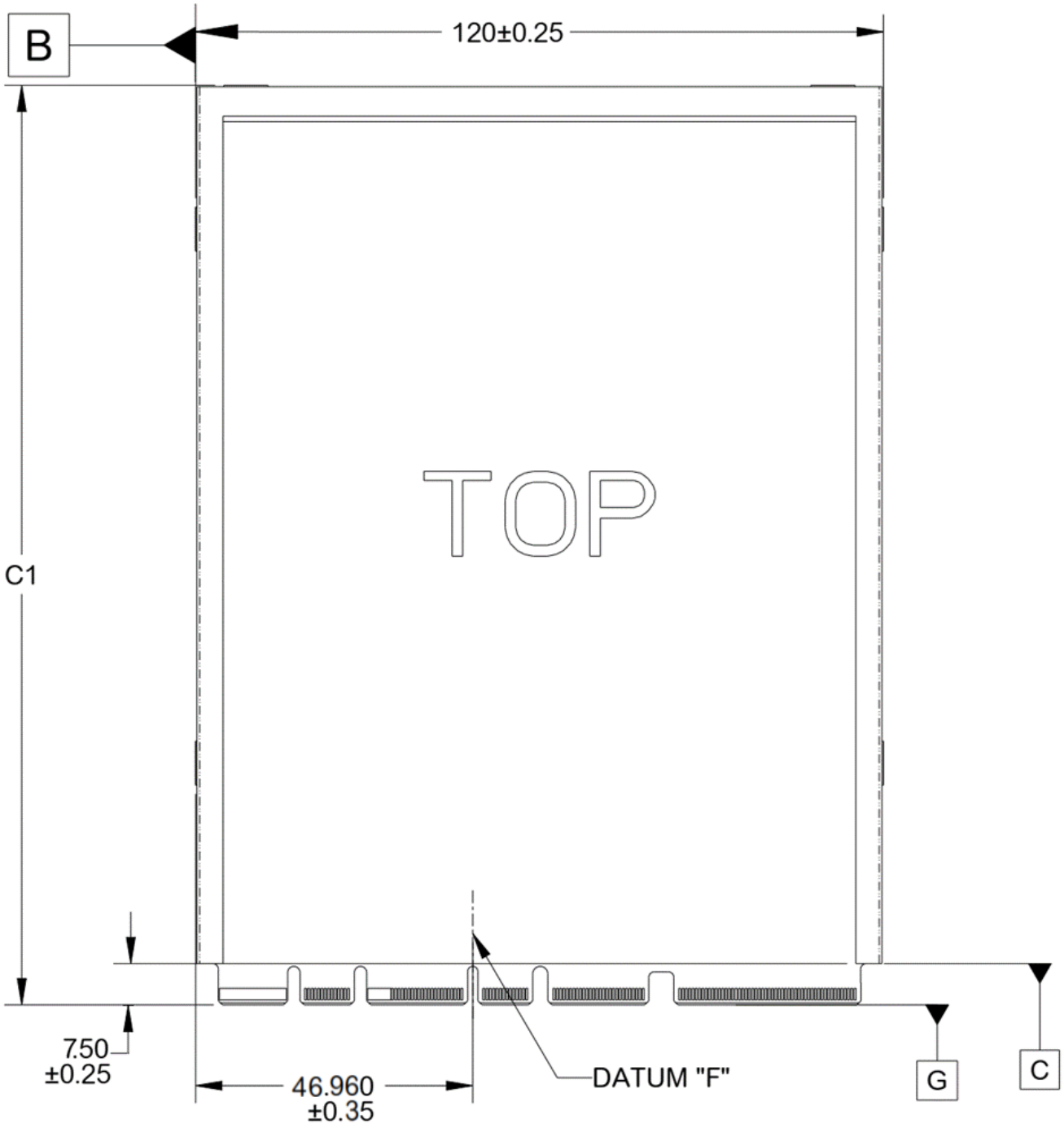

Figure 5-3. Top of PMM

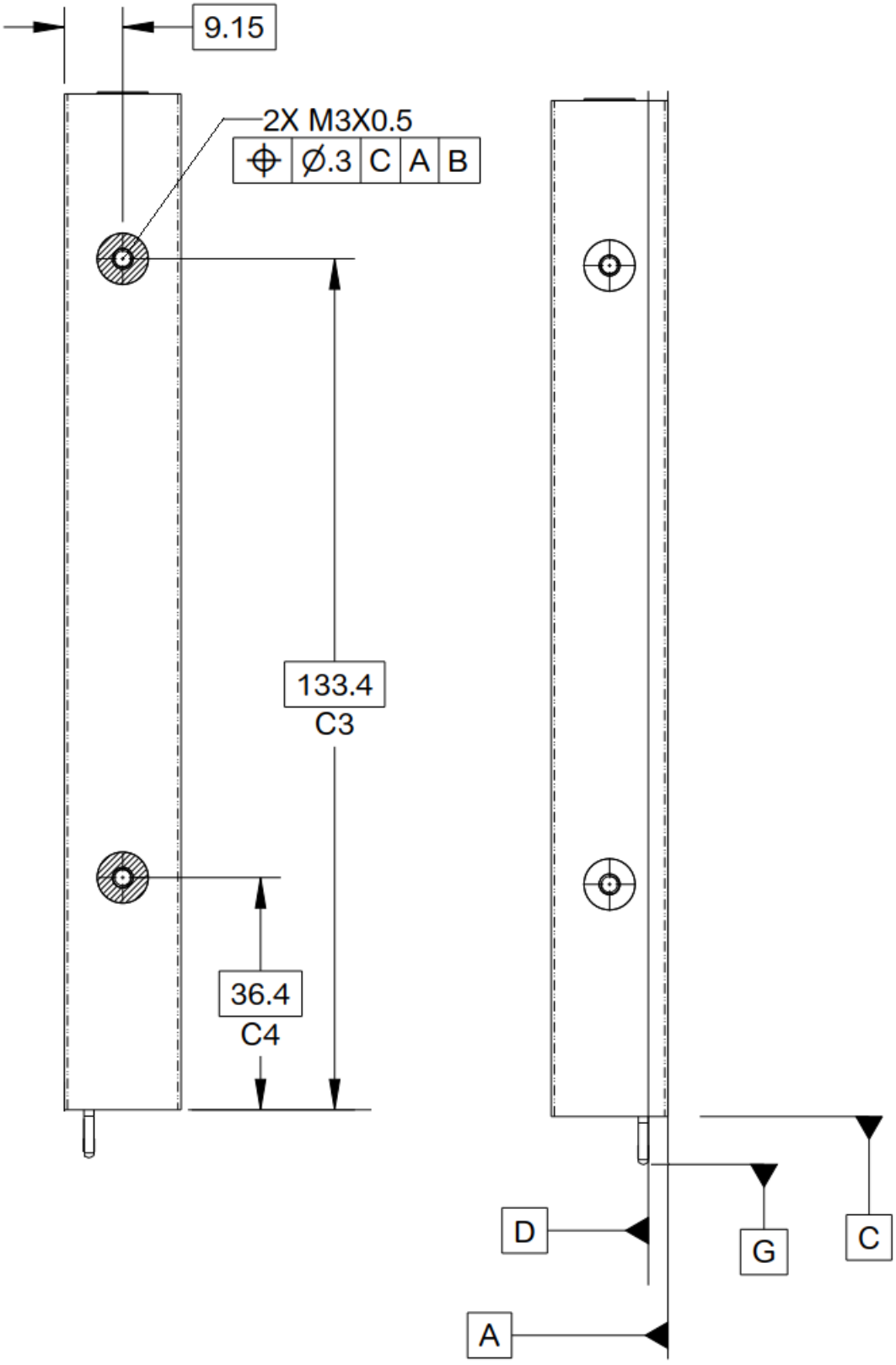

Figure 5-4. Sides of PMM

6. Signal List

This chapter covers the signal summary, definitions, and signal placement for the PMM connectors. Signal directions (I/O) are with respect to the host and the signals are mandatory for the device unless otherwise specified.

Table 6-1. PMM Connector Pin List

Interface	Signal Name	Host I/O	Function
Power and Grounds	12 V	O	+12 V power
	HP_12 V	O	HP_12 V: High power +12 V power
	3.3 Vaux	O	+3.3 V power
	GND	O	Return current path
PCIe	PETp0, PETn0	O	PCIe TX Differential signals defined by the *PCI Express Card Electromechanical Specification*. PETp/n[0..15] are supported with the x16 or x32 connectors. PETp/n[16..31] are supported only with the x32 connector.
	PETp1, PETn1		
	PETp2, PETn2		
	PETp3, PETn3		
	PETp4, PETn4		
	PETp5, PETn5		
	PETp6, PETn6		
	PETp7, PETn7		
	PETp8, PETn8		
	PETp9, PETn9		
	PETp10, PETn10		
	PETp11, PETn11		
	PETp12, PETn12		
	PETp13, PETn13		
	PETp14, PETn14		
	PETp15, PETn15		
	PETp16, PETn16		
	PETp17, PETn17		
	PETp18, PETn18		
	PETp19, PETn19		
	PETp20, PETn20		
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	PETp22, PETn22		
	PETp23, PETn23		
	PETp24, PETn24		
	PETp25, PETn25		
	PETp26, PETn26		
	PETp27, PETn27		
	PETp28, PETn28		
	PETp29, PETn29		
	PETp30, PETn30		
	PETp31, PETn31		
	PERp0, PERn0	I	PCIe RX Differential signals defined by the *PCI Express Card Electromechanical Specification*. PERp/n[0..15] are supported with the x16 or x32 connectors. PERp/n[16..31] are supported only with the x32 connector.
	PERp1, PERn1		
	PERp2, PERn2		
	PERp3, PERn3		
	PERp4, PERn4		
	PERp5, PERn5		
	PERp6, PERn6		
	PERp7, PERn7		
	PERp8, PERn8		

Interface	Signal Name	Host I/O	Function
	PERp9, PERn9		
	PERp10, PERn10		
	PERp11, PERn11		
	PERp12, PERn12		
	PERp13, PERn13		
	PERp14, PERn14		
	PERp15, PERn15		
	PERp16, PERn16		
	PERp17, PERn17		
	PERp18, PERn18		
	PERp19, PERn19		
	PERp20, PERn20		
	PERp21, PERn21		
	PERp22, PERn22		
	PERp23, PERn23		
	PERp24, PERn24		
	PERp25, PERn25		
	PERp26, PERn26		
	PERp27, PERn27		
	PERp28, PERn28		
	PERp29, PERn29		
	PERp30, PERn30		
	PERp31, PERn31		
	REFCLKp0, REFCLKn0	O	PCIe Reference Clock signals defined by the *PCI Express Base Specification*.
	REFCLKp1, REFCLKn1		
	REFCLKp2, REFCLKn2		
	REFCLKp3, REFCLKn3		
	REFCLKOUTp0, REFCLKOUTn0	I	Reserved for Future Use
	PERST0#	O	PE-Reset is a fundamental reset to the device defined as PERST# by the *PCI Express Base Specification*.
	PERST1#		
	PERST2#		
	PERST3#		
	PERST4#		
	PERST5#		
	PERST6#		
	PERST7#		
	PERSTOUT#	I	Reserved for Future Use
Sideband Signals	PRSNTB0#	I	Active low signal. This signal indicates to the host that the device is electrically attached.
	PRSNTB1#	I	Active low signal. This signal is used to detect device presence.
	PRSNTB2#/ PRSNT0#	I	Active low signal. This signal indicates to the host that the device is electrically attached.
	PRSNTB3#/ PRSNT2#	I	Active low signal. This signal is available in the x16 connector as a presence signal to indicate to the host that the device is electrically attached.
	PRSNT3#	I	Active low signal. This signal is available in the x32 connector as a presence signal to indicate to the host that the device is electrically attached.

Interface	Signal Name	Host I/O	Function
	LED	O	LED: Active high signal. This signal is used to drive the amber or amber/blue LED state from the host to the device. This signal is for EDSFF compatibility and is not used by PMM.
	GND/EDSFF_DETECT	I	Active high signal. This signal indicates to the host that an EDSFF device is attached.
	BIF0#, BIF1#, BIF2#	O	Active low signals. The bifurcation signals allow the host to configure the bifurcation support of the device as defined in the *OCP NIC 3.0 Design Specification*.
	AUX_PWR_EN	O	AUX_PWR_EN: Active high signal. Auxiliary power enable is used to indicate the host is in aux power mode as defined in the *OCP NIC 3.0 Design Specification*.
	MAIN_PWR_EN	O	Active high signal. Main power enable is used to indicate the host is in main power mode as defined in the *OCP NIC 3.0 Design Specification*.
	PMM_PWR_GOOD	I	Active high signal. NIC power good is used to indicate that the device has good internal power in aux power mode and main power mode.
	PWRBRK#	O	Open drain active low signal with pull-up on device. PWRBRK# communicates that an emergency power reduction is needed as defined in the *PCI Express Card Electromechanical Specification*.
	M-PESTI_IN	O	Reserved for Future Use
	M-PESTI_OUT	I	Reserved for Future Use
	RFU		Reserved for Future Use
2-wire interface	SMBCLK/I3CCLK	O	SMBCLK: Open Drain with pull-up on host. SMBus Clock. I3CCLK: Active high push-pull and open drain signal. I3C Basic Clock.
	SMBDATA/I3CDATA	I/O	SMBDATA: Open Drain with pull-up on host. SMBus Data. I3CDATA: Active high push-pull and open drain signal. I3C Basic Data.
	SMRST#	O	Active low signal. SMRST# is a reset for the management interface.
	SMBCLKOUT/I3CCLKOUT	I	I3CCLK: Active high push-pull and open drain signal. I3C Basic Clock.
	SMBDATAOUT/I3CDATAOUT	I/O	I3CDATA: Active high push-pull and open drain signal. I3C Basic Data.
802.3 SGMII interface	SGMII_TXp, SGMII_TXn	O	Ethernet management port differential outputs as defined by *ENG-46158 Serial Gigabit Media Independent Interface.*
	SGMII_RXp, SGMII_RXn	I	Ethernet management port differential inputs as defined by *ENG-46158 Serial Gigabit Media Independent Interface.*
USB	USB_DATp, USB_DATn	I/O	USB interface as defined in the *USB 2.0 Specification*.
Scan Chain	CLK	O	Active high signal. Scan Chain clock.
	DATA_OUT	O	Active high signal. Scan Chain data output signal.
	DATA_IN	I	Active high signal. Scan Chain data input signal.

Interface	Signal Name	Host I/O	Function
	LD#	O	Active low signal. Scan Chain shift register load signal.

6.1 Power and Grounds

The PMM connector supports a 12 V power source to power the device up to 200W. It also supports a 3.3 Vaux power source to provide power to manage sideband communication. All power and grounds shall be supported by the implemented connector on the host and the implemented card edge on the device.

The PMM connector also supports an optional high power 12 V power source called HP_12 V that provides an additional 400W of power to the device.

There are no power sequencing requirements between 3.3 Vaux and 12 V/HP_12 V. These voltages are independent from each other.

All devices are limited to 80W until the slot power limit support is set by the host. See the *PCI Express Base Specification* for more information.

6.2 PCIe Signals

6.2.1 High Speed Signals (PERp/n, PETp/n)

A device shall implement a minimum of one (1) PCIe lane. A lane consists of an input and output differential pair. Additional lanes are optional. Refer to the *PCI Express Base Specification* for more details on the functional requirements of the interface signals.

The PET signals (PETp[0..31], PETn[0..31]) on the host shall connect to the PET signals on the connector and the PER signals on the Device Logic. The PER signals (PERp[0..31], PERn[0..31]) on the host shall connect to the PER signals on the connector and the PET signals on the Device Logic. For a high-level wiring diagram, see Figure 6-1.

Lane Polarity Inversion shall be supported on both the host and the device to simplify host and device PCB trace routing constraints.

Lane reversal may be supported on both the host and device. If it is supported, then the transmitting and receiving lanes shall be connected using the same ordering.

PMM follows the same method as OCP NIC 3.0 for determining bifurcation support of a device. *See the Open Compute Project OCP NIC 3.0 Design Specification* for more information.

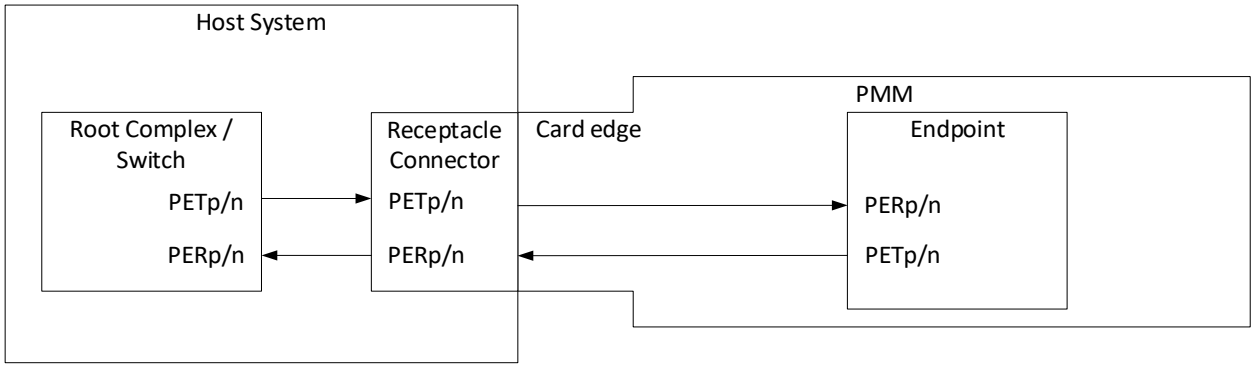


Figure 6-1. PET and PER Signal Connectivity Between Host and Device

6.2.2 Reference Clock (REFCLK[0..3][p/n])

The REFCLKp/REFCLKn signals are used to assist the synchronization of the device's PCI Express interface timing circuits. Refer to the *PCI Express Base Specification* for more details on the functional and tolerance requirements for the reference clock signals.

If SRIS or SRNS is supported by both the system and the device then the reference clock is optional on the host. The reference clock shall be the default configuration on the device. If the reference clock is not detected upon detecting PERST# de-assertion, then the SRIS/SRNS supported device shall switch into SRIS/SRNS mode. The device shall only enter SRNS if the device is configured for this usage through a method outside the scope of this version of the specification.

There are four sets of clock pairs. All devices shall implement REFCLKp0 and REFCLKn0. REFCLKp[1..3] and REFCLKn[1..3] are dependent on device bifurcation support. See Table 6-2 for more details. Note that if x4 bifurcation is needed for a 32 lane PMM device then SRIS/SRNS is required.

It is recommended that the host terminate all reference clocks signals with a pull-down resistor if the clocks are not provided by the host.

6.2.3 PERST[0..7]#

Refer to the *PCI Express Base Specification* for more details on the functional requirements.

All devices and hosts shall implement PERST0#. PERST[1..7] shall be implemented by the host/device depending on bifurcation support. See Table 6-2 for more details.

Table 6-2. REFCLK and PERST# Mapping Based on Bifurcation.

Lane Bifurcation	PET[0..3] PER[0..3]	PET[4..7] PER[4..7]	PET[8..11] PER[8..11]	PET[12..15] PER[12..15]	PET[16..19] PER[16..19]	PET[20..23] PER[20..23]	PET[24..27] PER[24..27]	PET[28..31] PER[28..31]
1, x16	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#	NA	NA	NA	NA
2, x8	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK1 PERST1#	REFCLK1 PERST1#	NA	NA	NA	NA
4, x4	REFCLK0 PERST0#	REFCLK1 PERST1#	REFCLK2 PERST2#	REFCLK3 PERST3#	NA	NA	NA	NA
1, x32	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#
2, x16	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK1 PERST1#	REFCLK1 PERST1#	REFCLK1 PERST1#	REFCLK1 PERST1#
4, x8	REFCLK0 PERST0#	REFCLK0 PERST0#	REFCLK1 PERST1#	REFCLK1 PERST1#	REFCLK2 PERST2#	REFCLK2 PERST2#	REFCLK3 PERST3#	REFCLK3 PERST3#
8, x4	SRIS/SRNS PERST0#	SRIS/SRNS PERST1#	SRIS/SRNS PERST2#	SRIS/SRNS PERST3#	SRIS/SRNS PERST4#	SRIS/SRNS PERST5#	SRIS/SRNS PERST6#	SRIS/SRNS PERST7#

6.2.4 Reference Clock Outputs (REFCLKOUT[p/n])

REFCLKOUTp/REFCLKOUTn are not supported in this revision of the specification so are reserved for future use. These pins shall be electrically not connected on both host and device.

6.2.5 PERSTOUT#

PERSTOUT# is not supported in this revision of the specification so is reserved for future use. These pins shall be electrically not connected on both host and device.

6.3 Sideband Signals

6.3.1 PRSNT[0..3]#

PRSNT[0..2]# signals indicate physical presence of a device plugged into the host connector and the type of connector on the device. All devices supporting the x4 device connector shall implement PRSNT0#. All devices supporting the x8 device connector shall implement PRSNT0# and PRSNT1#. All devices supporting the x16 device connector shall implement PRSNT0#, PRSNT1#, PRSNT2#. The device shall connect each implemented PRSNT[0..2]# signal to ground.

6.3.2 PRSNTB[0..3]#

The PRSNTB[0..3]# are used to detect device presence and provide the host PCIe capability information. The signals shall each be pulled up on the host by a 1 kΩ resistor. If used on the device, the signals shall have a 200 Ω series resistor between the card edge and the PRSNTA# signal and shall float if not used. Refer to the *OCP NIC 3.0 Design Specification* for more details on how to configure these resistors.

These signals are shared with PRSNT[0..2]# and RFU signals. Correct detection and configuration of these signals are the responsibility of the host. Not configuring these signals for the correct usage may result in undefined behavior with the device.

6.3.3 PRSNTA#

The PRSNTA# signal is used to indicate device presence. It is connected to ground on the host and connected to the PRSNTB[0..3]# pins on the device that are used. Refer to the *OCP NIC 3.0 Design Specification* for more details.

6.3.4 GND/EDSFF_DETECT

The GND/EDSFF_DETECT signal indicates an EDSFF device is plugged into the host connector. This signal is optional for the host and is only used if the host chooses to support EDSFF devices in a PMM slot. A PMM device shall connect this pin directly to ground. A host that does not support EDSFF devices shall connect this pin directly to ground. If the host supports EDSFF devices then this pin shall have a pull-up resistor greater than 9 kΩ. If asserted (driven high), then the host should configure its sidebands for EDSFF operation. For more details, see Section 9.2.

6.3.5 BIF[0..2]#

BIF[0..2]# are used by the host to configure the bifurcation support of a device. The signal is actively driven by the host.

6.3.6 AUX_PWR_EN

AUX_PWR_EN is asserted by the host to indicate that the host and device are to be in aux power mode and tells the device aux power mode power rails are allowed to be powered. The signal shall be pulled down on the host using a 10 kΩ resistor.

6.3.7 MAIN_PWR_EN

MAIN_PWR_EN is asserted by the host to indicate that the host and device are to be in main power mode and tells the device main power mode power rails are allowed to be powered. The signal shall be pulled down on the host using a 10 kΩ resistor.

6.3.8 PMM_PWR_GOOD

PMM_PWR_GOOD is asserted by the device to indicate to the host that power is good when the host initiates the aux power mode or main power mode. The signal shall be pulled down on the host using a 100 kΩ resistor.

6.3.9 PWRBRK#

PWRBRK# is an optional signal. See the *PCI Express Card Electromechanical Specification and the PCI Express Base Specification* for details on the functional requirements for PWRBRK# and transitioning into the Emergency Power Reduction State. If PWRBRK# is supported by the host, then the PWRBRK# pin shall be pulled up on the device with a 9 kΩ to 60 kΩ resistor.

This signal is shared with a RFU pin. Correct detection and configuration of this signal is the responsibility of the host. Not configuring the signal for the correct usage may result in undefined behavior with the device.

6.3.10 RFU

Signals documented as RFU are reserved for future use. These pins shall be electrically not connected. These pins shall be electrically not connected on both host and device.

6.4 M-PESTI

6.5 M-PESTI Interface

M-PESTI is not supported in this revision of the specification so are reserved for future use. These pins shall be electrically not connected on both host and device.

6.6 2-Wire Interface

6.6.1 SMBus Interface

The SMBus interface is a sideband management interface. SMBus is a two-wire interface through which various system component chips communicate with each other and with rest of the system. Refer to the *System Management Bus (SMBus) Specification*.

SMBus is an Open Drain interface. The pull-ups for SMBDATA and SMBCLK shall be on the host and powered within the voltage limits defined for Vddsmb in Table 7-3. The device is allowed to have weak pull-up resistors to protect from floating inputs. If present, then the pull-up resistors on the device are recommended to be greater than or equal to 45 kΩ.

The SMBCLK signal provides the clock signaling from the SMBus initiator to the SMBus target to be able to decode the data on the SMBDATA line.

The SMBDATA signal is used to transfer the data packets between the host and the device according to the SMBus protocol.

6.6.2 I3C Basic Interface

The I3C Basic interface is an optional sideband management interface. It is a two-wire interface through which various system component chips communicate with each other and with rest of the system. Refer to the *PCI Express Base Specification* and the *MIPI™ Alliance Specification for I3C Basic Specification* for more information for more details.

Devices that support I3C Basic shall support SMBus and tolerate SMBus voltage signaling for backwards

compatibility.

6.6.3 SMRST#

The SMRST# signal is an external reset signal for the SMBus interface as defined by the System Management Bus (SMBus) Specification and an external reset for the I3C Basic interface if I3C Basic is supported. SMRST# shall be implemented by the device and is optional for the host. It shall not affect the PCIe interface or other non SMBus/I3C Basic circuit related functions. The device shall have a pull-up resistor greater than or equal to 9 kΩ on SMRST#.

If the host asserts SMRST#, then the device shall keep the SMBCLK/I3CCLK and SMBDATA/I3CDATA in a high impedance state and ignore any transitions on SMBCLK/I3CCLK and SMBDATA/I3CDATA. When the host de-asserts SMRST#, the device shall place the SMBus or I3C Basic in the SMBus power-on reset state at 3.3 V.

Cycling 3.3 Vaux shall not be used by the host to reset the SMBus or I3C Basic. Cycling 3.3 Vaux may or may not have an effect on the device's SMBus or I3C Basic interface.

6.6.4 I3C Basic Output Interface

The I3C Basic output interface is an optional sideband management interface however for these signals the device is the initiator instead of target. It is a two-wire interface through which various system component chips communicate with each other and with rest of the system. Refer to the *MIPI™ Alliance Specification for I3C Basic Specification* for more information.

6.7 SGMII Interface

6.7.1 SGMII

SGMII is an optional interface that is used as the primary management interface between the host and device. It's a 4-pin differential interface with 1 differential TX and 1 differential RX. If supported, the host and device shall implement a recovered clock instead of source synchronous clocking. Refer to the *ENG-46158 Serial Gigabit Media Independent Interface Specification* for more details on enumeration, protocol, electricals, and other features.

6.8 USB

6.8.1 USB_DATp, USB_DATn

The USB interface provides an optional sideband interface between host and device. It's a 2-pin differential interface with the device being the endpoint. Refer to the *United Serial Bus (USB) Specification* for more details on enumeration, protocol, electricals, and other features.

6.9 Scan Chain

6.9.1 Scan Chain Interface

The Scan Chain Interface provides status indication between host and device. Refer to the *OCP NIC 3.0 Design Specification* for more details on functional and timing requirements.

The CLK pin shall be pulled up on the device through a 1 kΩ resistor. The DATA_OUT pin shall be pulled down on the device through a 10 kΩ resistor. The LD# pin shall be pulled up on the device through a 10 kΩ resistor.

If the host supports the Scan Chain Interface, the DATA_IN pin shall be pulled up using a 10 kΩ resistor.

If the host does not support Scan Chain Interface, the CLK pin shall be connected to ground and the DATA_OUT

pin shall be pulled down using a 1 kΩ resistor, and the LD# pin shall be pulled up with a 1 kΩ resistor.

6.10 Connector pinout definitions

Table 6-3 shows the signal pinouts for the connector. These pinouts are shown from the host point of view. Hot plug shall be supported by the device. The contact sequence for each pinout is shown to indicate the order in which the pins make contact to the host. For more details, please refer to *SFF-TA-1037 Connectors for Pluggable Multi-Purpose Module.*

Table 6-3. PMM Connector Pinout

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
BH1	2nd mate	HP_12 V/HP_48 V	GND	1st mate	AH1
		Gap	Gap		
BO1	1st mate	PMM_PWR_GOOD	PERST2#	1st mate	AO1
BO2	1st mate	MAIN_PWR_EN	PERST3#	2nd mate	AO2
BO3	1st mate	LD#	M-PESTI_IN	1st mate	AO3
BO4	1st mate	DATA_IN	GND	1st mate	AO4
BO5	1st mate	DATA_OUT	SGMII_RXn	1st mate	AO5
BO6	1st mate	CLK	SGMII_RXp	1st mate	AO6
BO7	1st mate	RFU	GND	1st mate	AO7
BO8	1st mate	RFU	SGMII_TXn	1st mate	AO8
BO9	1st mate	RFU	SGMII_TXp	1st mate	AO9
BO10	1st mate	GND	GND	1st mate	AO10
BO11	2nd mate	REFCLKn2	REFCLKn3	2nd mate	AO11
BO12	2nd mate	REFCLKp2	REFCLKp3	2nd mate	AO12
BO13	1st mate	GND/EDSFF_DETECT	GND	1st mate	AO13
BO14	1st mate	RFU	RFU	1st mate	AO14
		Separator	Separator		
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6

B7	2nd mate	BIF0#	SMBCLK/I3CCLK	2nd mate	A7
B8	2nd mate	BIF1#	SMBDATA/I3CDATA	2nd mate	A8
B9	2nd mate	BIF2#	SMRST#	2nd mate	A9
B10	2nd mate	PERST0#	PRSNTA#	2nd mate	A10
B11	2nd mate	3.3 Vaux	PERST1#	2nd mate	A11
B12	2nd mate	AUX_PWR_EN	PRSNT0#/PRSNTB2#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28
		Key	Key		
B29	1st mate	GND	GND	1st mate	A29
B30	2nd mate	PETn4	PERn4	2nd mate	A30
B31	2nd mate	PETp4	PERp4	2nd mate	A31
B32	1st mate	GND	GND	1st mate	A32
B33	2nd mate	PETn5	PERn5	2nd mate	A33
B34	2nd mate	PETp5	PERp5	2nd mate	A34
B35	1st mate	GND	GND	1st mate	A35
B36	2nd mate	PETn6	PERn6	2nd mate	A36
B37	2nd mate	PETp6	PERp6	2nd mate	A37
B38	1st mate	GND	GND	1st mate	A38
B39	2nd mate	PETn7	PERn7	2nd mate	A39
B40	2nd mate	PETp7	PERp7	2nd mate	A40

B41	1st mate	GND	GND	1st mate	A41
B42	2nd mate	PRSNT1#/PRSNTB0#	PRSNTB1#	2nd mate	A42
		Separator	Separator		
B43	1st mate	GND	GND	1st mate	A43
B44	2nd mate	PETn8	PERn8	2nd mate	A44
B45	2nd mate	PETp8	PERp8	2nd mate	A45
B46	1st mate	GND	GND	1st mate	A46
B47	2nd mate	PETn9	PERn9	2nd mate	A47
B48	2nd mate	PETp9	PERp9	2nd mate	A48
B49	1st mate	GND	GND	1st mate	A49
B50	2nd mate	PETn10	PERn10	2nd mate	A50
B51	2nd mate	PETp10	PERp10	2nd mate	A51
B52	1st mate	GND	GND	1st mate	A52
B53	2nd mate	PETn11	PERn11	2nd mate	A53
B54	2nd mate	PETp11	PERp11	2nd mate	A54
B55	1st mate	GND	GND	1st mate	A55
B56	2nd mate	PETn12	PERn12	2nd mate	A56
B57	2nd mate	PETp12	PERp12	2nd mate	A57
B58	1st mate	GND	GND	1st mate	A58
B59	2nd mate	PETn13	PERn13	2nd mate	A59
B60	2nd mate	PETp13	PERp13	2nd mate	A60
B61	1st mate	GND	GND	1st mate	A61
B62	2nd mate	PETn14	PERn14	2nd mate	A62
B63	2nd mate	PETp14	PERp14	2nd mate	A63
B64	1st mate	GND	GND	1st mate	A64
B65	2nd mate	PETn15	PERn15	2nd mate	A65
B66	2nd mate	PETp15	PERp15	2nd mate	A66
B67	1st mate	GND	GND	1st mate	A67
B68	2nd mate	I3CCLKOUT	USB_DATn	2nd mate	A68
B69	2nd mate	I3CDATOUT	USB_DATp	2nd mate	A69
B70	2nd mate	PRSNT2#/PRSNTB3#	PWRBRK0#	2nd mate	A70
		Gap	Gap		
B71	1st mate	GND	GND	1st mate	A71
B72	2nd mate	PETn16	PERn16	2nd mate	A72

B73	2nd mate	PETp16	PERp16	2nd mate	A73
B74	1st mate	GND	GND	1st mate	A74
B75	2nd mate	PETn17	PERn17	2nd mate	A75
B76	2nd mate	PETp17	PERp17	2nd mate	A76
B77	1st mate	GND	GND	1st mate	A77
B78	2nd mate	PETn18	PERn18	2nd mate	A78
B79	2nd mate	PETp18	PERp18	2nd mate	A79
B80	1st mate	GND	GND	1st mate	A80
B81	2nd mate	PETn19	PERn19	2nd mate	A81
B82	2nd mate	PETp19	PERp19	2nd mate	A82
B83	1st mate	GND	GND	1st mate	A83
B84	2nd mate	PETn20	PERn20	2nd mate	A84
B85	2nd mate	PETp20	PERp20	2nd mate	A85
B86	1st mate	GND	GND	1st mate	A86
B87	2nd mate	PETn21	PERn21	2nd mate	A87
B88	2nd mate	PETp21	PERp21	2nd mate	A88
B89	1st mate	GND	GND	1st mate	A89
B90	2nd mate	PETn22	PERn22	2nd mate	A90
B91	2nd mate	PETp22	PERp22	2nd mate	A91
B92	1st mate	GND	GND	1st mate	A92
B93	2nd mate	PETn23	PERn23	2nd mate	A93
B94	2nd mate	PETp23	PERp23	2nd mate	A94
B95	1st mate	GND	GND	1st mate	A95
B96	2nd mate	PETn24	PERn24	2nd mate	A96
B97	2nd mate	PETp24	PERp24	2nd mate	A97
B98	1st mate	GND	GND	1st mate	A98
B99	2nd mate	PETn25	PERn25	2nd mate	A99
B100	2nd mate	PETp25	PERp25	2nd mate	A100
B101	1st mate	GND	GND	1st mate	A101
B102	2nd mate	PETn26	PERn26	2nd mate	A102
B103	2nd mate	PETp26	PERp26	2nd mate	A103
B104	1st mate	GND	GND	1st mate	A104
B105	2nd mate	PETn27	PERn27	2nd mate	A105
B106	2nd mate	PETp27	PERp27	2nd mate	A106
B107	1st mate	GND	GND	1st mate	A107

B108	2nd mate	PETn28	PERn28	2nd mate	A108
B109	2nd mate	PETp28	PERp28	2nd mate	A109
B110	1st mate	GND	GND	1st mate	A110
B111	2nd mate	PETn29	PERn29	2nd mate	A111
B112	2nd mate	PETp29	PERp29	2nd mate	A112
B113	1st mate	GND	GND	1st mate	A113
B114	2nd mate	PETn30	PERn30	2nd mate	A114
B115	2nd mate	PETp30	PERp30	2nd mate	A115
B116	1st mate	GND	GND	1st mate	A116
B117	2nd mate	PETn31	PERn31	2nd mate	A117
B118	2nd mate	PETp31	PERp31	2nd mate	A118
B119	1st mate	GND	GND	1st mate	A119
B120	2nd mate	REFCLKOUTn	PERST4#	2nd mate	A120
B121	2nd mate	REFCLKOUTp	PERST5#	2nd mate	A121
B122	1st mate	GND	PERST6#	1st mate	A122
B123	2nd mate	M-PESTI_OUT	PERST7#	2nd mate	A123
B124	2nd mate	PRSNT3#	PERSTOUT#	2nd mate	A124

7. Electrical Requirements

This chapter covers the electrical requirements of the PMM devices. Unless otherwise specified, follow the PCI Express Card Electromechanical Specification.

7.1 Power Supply Requirements

Table 7-1 provides the 12 V power supply requirements and Table 7-2 provides the 3.3 Vaux power supply requirements.

Table 7-1. Combined 12 V and HP_12V Power Supply Requirements

Symbol	Parameter	Value	Unit	Comment
12Vtol	12 V supply Tolerance	10.8 to 13.2	V	Includes DC+AC noise up to 20 MHz
12Vpsus	Maximum sustained device power	600	W	Maximum average power over any 1s period. A device shall not consume more power than the slot power limit regardless of other settings (e.g. PSD in NVMe).
12Vpinit	Initial slot power limit	80	W	This is the initial max power the device can draw over any 1s period prior to reading the Slot Power Limit Value in the *PCI Express Base Specification*
12Vslewrate	Maximum slew rate	0.1	A/us	Maximum slew rate for any step current as measured at the connector. This does not include hot plug
12Vinrush	Max inrush current	15	A	Maximum current load presented by the device 12V supply to the host receptacle averaged over any 5us period during the initial power-up ramp to 90% of the device operating voltage.
12Vcap	Max capacitance for inrush	2000	uF	Capacitance system sees during the initial power-up ramp to 90% of the device operating voltage.

Table 7-2. 3.3 Vaux Power Supply Requirements

Symbol	Parameter	Value	Unit	Comment
33Vauxtol	3.3 Vaux supply Tolerance	2.970 to 3.465	V	Includes Ripple.
33VauxIpin	3.3 Vaux pin current	1.1	A	Maximum averaged current value over any 100 us period after the voltage reaches its operating range.
33Vauxcap	Max capacitance for inrush	150	uF	For inrush current limit.

7.2 Timings

PMM follows the power-Up and Power-down sequencing defined by OCP NIC 3.0. Refer to the *OCP NIC 3.0 Design Specification* for more details.

7.3 3.3 V Logic Signal Requirements

The 3.3 V device logic levels for single-ended digital signals are defined in Table 7-3. Inputs and outputs are referenced from the device standpoint.

Table 7-3. DC Specification for 3.3 V Logic Signaling

Symbol	Parameter	Condition	Min	Max	Unit	Notes
Vddsmb	SMBus Operating Voltage		2.97	3.465	V	
Vih	Input High Voltage		2.0	3.465	V	
Vil	Input Low Voltage		-0.3	0.8	V	
Voh	Output High Voltage			3.465	V	
Vol	Output Low Voltage	4.0 mA		0.2	V	
Iin	Input Leakage Current	0 V to 3.3 V	-100	100	µA	2
Iout	Output Leakage Current	0 V to 3.3 V	-100	100	µA	2
Cin	Input Pin Capacitance			30	pF	1
Cout	Output Pin Capacitance			30	pF	1

Notes:

1. Measured at the card edge-finger.
2. The leakage current requirement excludes current related to mandatory termination (e.g., a pull up) on the side-band signals (e.g., SMRST#).

8. PCIe Electrical Requirements

In general, PMM devices are expected to follow requirements as specified in both the *PCI Express Base Specification* and the *PCI Express Card Electromechanical Specification*. This chapter provides device requirements that deviate from the *PCI Express Card Electromechanical Specification*. For details on the connector electricals, please refer to *SFF-TA-1002 Card Edge multilane protocol agnostic connector specification*.

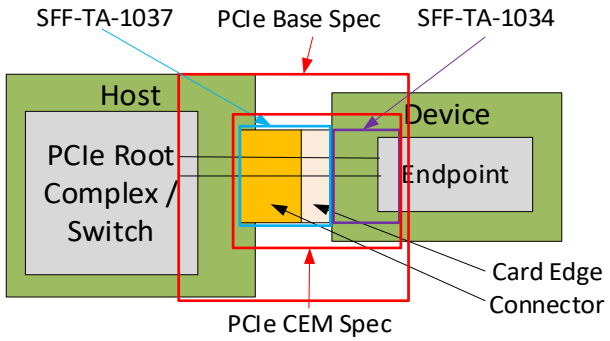


Figure 8-1. PMM Electrical Requirements Coverage

8.1 Signal Integrity Requirements

Table 8-1 summarizes the signal integrity requirements for the device. Additional explanation is provided in the subsequent sections. All measurements are referenced to an 85 Ω differential impedance.

Table 8-1. Summary of Signal Integrity Requirements

Line Rate	Insertion Loss (IL)	Return Loss (RL)	Power Sum Near End Crosstalk (PSNEXT)[1]	Power Sum Far End Crosstalk (PSFEXT)[1]
PCIe 5.0 (32.0 GT/s)	≥ -0.2 - 0.425 * f dB (f = 0 to 16 GHz) ≥ 5 - 0.75 * f dB (f = 16 to 24 GHz)	≤ -10 dB (< 4 GHz) ≤ -7 dB (4 to 24 GHz)	≤ -45 dB (0 to 16 GHz) ≤ -55 + 0.625 * f dB (f = 16 to 24 GHz)	≤ -36 dB (0 to 16 GHz) ≤ -44 + 0.5 * f dB (f = 16 to 24 GHz)
PCIe 6.0 (64.0 GT/s)	≥ -1.5 - 0.28125 * f dB (f = 0 to 16 GHz) ≥ 6 - 0.75 * f dB (f = 16 to 24 GHz)	≤-15dB (< 1.25 GHz) ≤-10dB (1.25 to 24 GHz)	≤ -60 dB (0 to 16 GHz) ≤ -70 + 0.625 * f dB (f = 16 to 24 GHz)	≤ -50 dB (0 to 16 GHz) ≤ -60 + 0.625 * f dB (f = 16 to 24 GHz)

Notes:
1. PSNEXT and PSFEXT are validated through simulation only.
2. In all equations, f is the frequency expressed in GHz.

For Insertion Loss and Return Loss, these measurements are defined as the measurement from where the conductive route exits the gold finger on the card edge to the die TX or RX of the endpoint package. Examples of this include the on die parasitics and ESD structures (but not the driver's output impedance), PCB route for TX or RX loss including vias and coupling capacitors (for TX), package TX and RX insertion loss, and reference plane location. The gold fingers are not included in the loss budget. An example is shown in Figure 8-2.

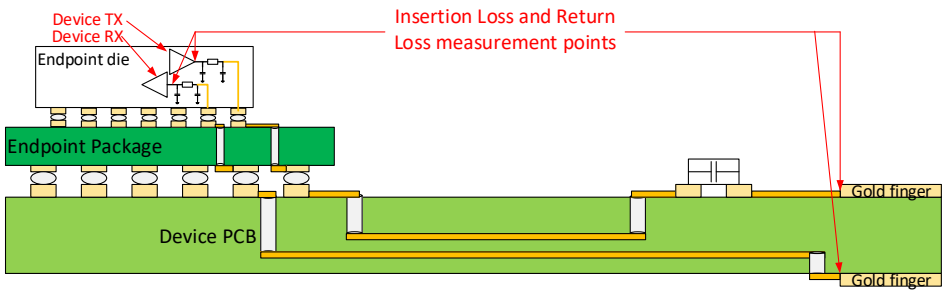


Figure 8-2. Example of Circuit Contributions to Insertion Loss and Return Loss

8.1.1 Insertion Loss (IL)

Insertion Loss at Gen 5.0:

≥ -0.2 - 0.425 * f dB with f = 0 to 16 GHz (-7 dB at f = 16 GHz)
≥ 5 - 0.75 * f dB with f = 16 to 24 GHz (-13 dB at f = 24 GHz)

Insertion Loss at Gen 6.0:

≥ -1.5 - 0.28125 * f dB with f = 0 to 16 GHz (-6 dB at f = 16 GHz)
≥ 6 - 0.75 * f dB with f = 16 to 24 GHz (-12 dB at f = 24 GHz)

8.1.2 Return Loss (RL)

Return Loss at Gen 5.0: ≤ -10 dB at < 4 GHz and ≤ -7 dB between 4 to 24 GHz

Return Loss at Gen 6.0: ≤ -15 dB at < 1.25 GHz and ≤ -10 dB between 1.25 to 24 GHz

8.1.3 Power Sum Near End Crosstalk (PSNEXT)

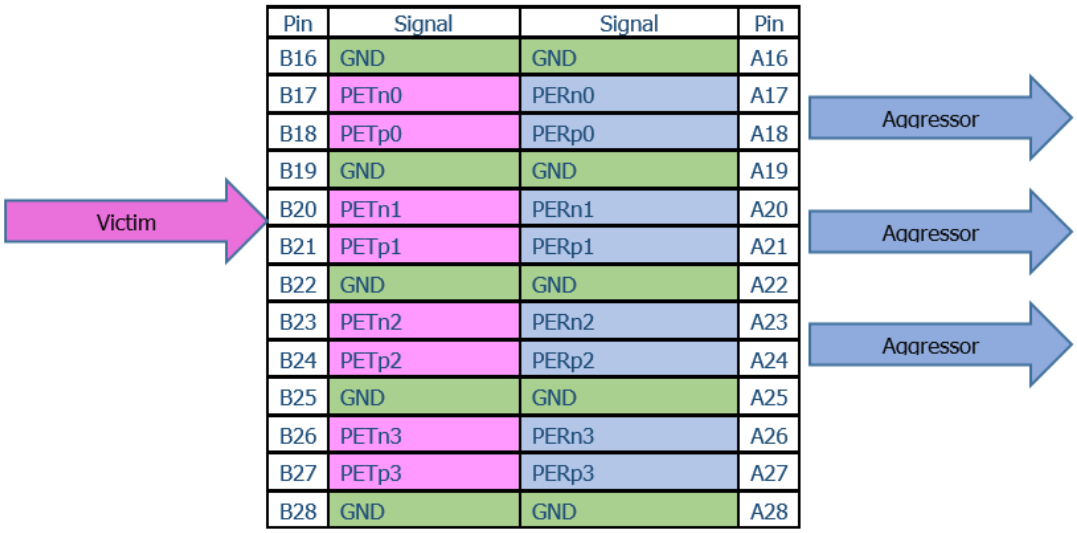
NEXT is defined between TX differential pair and RX differential pair. The power summation of NEXT on one pair TX/RX includes all the contribution of RX/TX pairs from the other side of the card edge. Figure 8-3 shows an example of the 3 worst lanes contributing to PSNEXT however devices should consider the connector pinout, the ASIC pinout, and routing when choosing the lanes for PSNEXT measurements. PSNEXT is measured at where the signal route exits the gold finger. NEXT and PSNEXT shall be referenced to 85 Ω differential impedance.

PSNEXT at Gen 5.0:

≤ -45 dB from 0 to 16 GHz
≤ -55 + 0.625 * f dB with f = 16 to 24 GHz (-43 dB at f = 24 GHz)

PSNEXT at Gen 6.0:

≤ -60 dB (0 to 16 GHz)
≤ -70 + 0.625 * f dB with f = 16 to 24 GHz (-55 dB at f = 24 GHz)



Pin	Signal	Signal	Pin
B16	GND	GND	A16
B17	PETn0	PERn0	A17
B18	PETp0	PERp0	A18
B19	GND	GND	A19
B20	PETn1	PERn1	A20
B21	PETp1	PERp1	A21
B22	GND	GND	A22
B23	PETn2	PERn2	A23
B24	PETp2	PERp2	A24
B25	GND	GND	A25
B26	PETn3	PERn3	A26
B27	PETp3	PERp3	A27
B28	GND	GND	A28

Figure 8-3. Example of PSNEXT Test Configuration for Device

8.1.4 Power Sum Far End Crosstalk (PSFEXT)

FEXT is defined between TX (or RX) differential pair at the card edge side and adjacent TX (or RX) differential pair to the die of the end point package. The power summation of FEXT on one pair includes all the contribution of TX (or RX) pairs starting from the same side of the card edge. Figure 8-4 shows an example of the worst lanes contributing to PSFEXT however devices should consider the connector pinout, the ASIC pinout, and routing when choosing the lanes for PSFEXT measurements. PSFEXT is measured at where the signal route exits the gold finger.

PSFEXT at Gen 5.0:

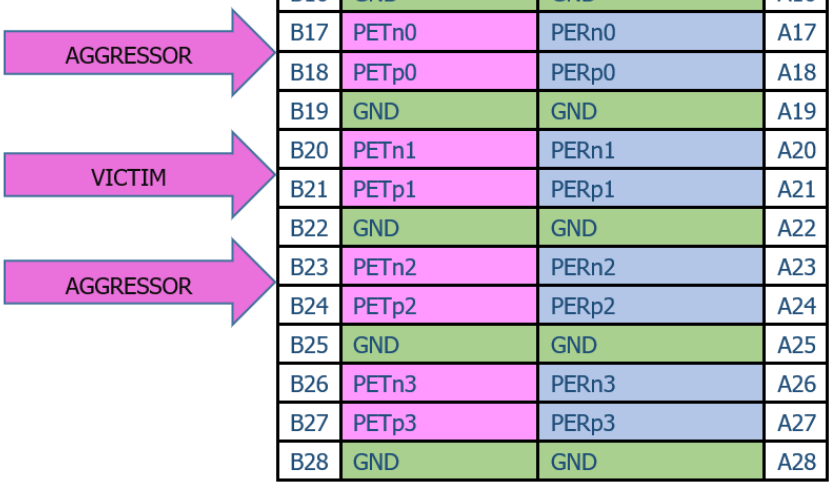
≤ -36 dB from 0 to 16 GHz

≤ -44 + 0.5 * f dB with f = 16 to 24 GHz (-32 dB at f = 24 GHz)

PSFEXT at Gen 6.0:

≤ -50 dB (0 to 16 GHz)

≤ -60 + 0.625 * f dB with f = 16 to 24 GHz (-45 dB at f = 24 GHz)



Pin	Signal	Signal	Pin
B16	GND	GND	A16
B17	PETn0	PERn0	A17
B18	PETp0	PERp0	A18
B19	GND	GND	A19
B20	PETn1	PERn1	A20
B21	PETp1	PERp1	A21
B22	GND	GND	A22
B23	PETn2	PERn2	A23
B24	PETp2	PERp2	A24
B25	GND	GND	A25
B26	PETn3	PERn3	A26
B27	PETp3	PERp3	A27
B28	GND	GND	A28

Figure 8-4. Example of PSFEXT Victim and Aggressors

8.2 Transmitter and Receiver Sensitivity Eye Limits

The following goes through the specific parameter deviations from the *PCI Express Card Electromechanical Specification* for the transmitter and receiver sensitivity (minimum Eye opening) for an PMM host and device to meet the PCIe electrical specifications. All methodologies and patterns shall follow what is documented in the *PCI Express Card Electromechanical Specification.* All measurements are based on simulations assuming test fixtures like what is used in the *PCI Express Card Electromechanical Specification.* The requirements in the tables below may change once test fixtures for PMM are produced.

8.2.1 PMM Device Transmitter Eye Mask

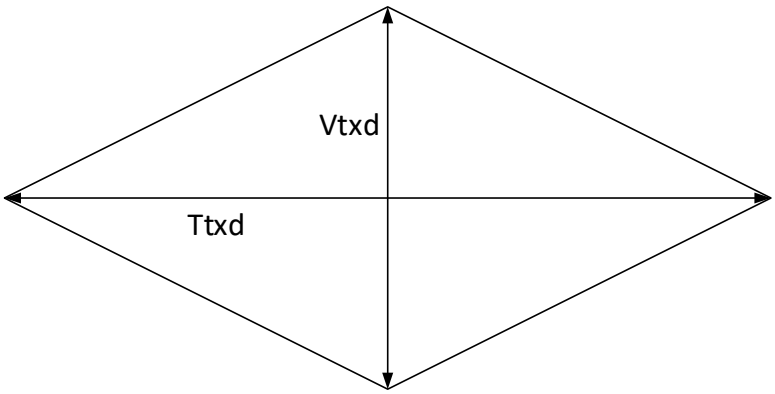


Figure 8-5. Eye Diagram for PMM Device Transmitter

Table 8-2. PMM Device Transmitter Eye Mask for PCIe at 32.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxd	24.70	1300	mV	
Ttxd	13.40		ps	

Table 8-3. PMM Device Transmitter Eye Mask for PCIe at 64.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxd	6.7		mV	
Ttxd	3.28		ps	

8.2.2 PMM Host Transmitter Eye Mask

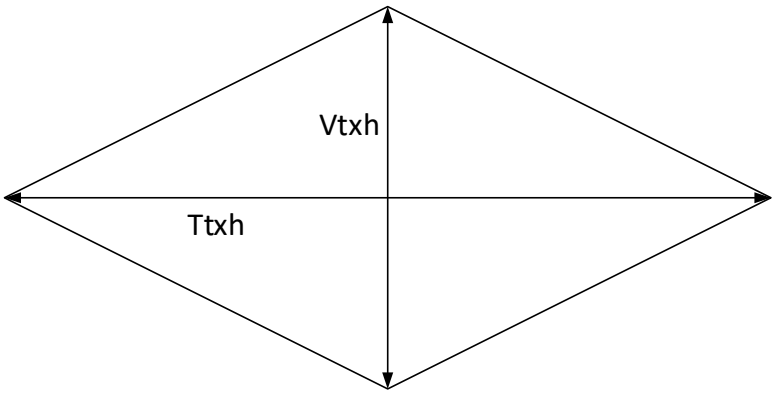


Figure 8-6. Eye Diagram for PMM Host Transmitter

Table 8-4. PMM Host Transmitter Eye Mask for PCIe at 32.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxh	16.60	1300	mV	
Ttxh	10.10		ps	

Table 8-5. PMM Host Transmitter Eye Mask for PCIe at 64.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxh	5.30		mV	
Ttxh	2.97		ps	

8.2.3 PMM Device Receiver Minimum Sensitivity

No deviations from the *PCI Express Card Electromechanical Specification* for 64.0 GT/s and below except for the following:

For 32.0 GT/s and 64.0 GT/s, receiver sensitivity testing shall be tested with all device TX lines terminated and programmed to the same swing as what was used for device transmitter eye testing. The TX lines shall be sending data during this testing.

8.2.4 PMM Host Receiver Minimum Sensitivity

No deviations from the *PCI Express Card Electromechanical Specification* for 64.0 GT/s and below.

9. Compatibility With Other Form Factors (Informative)

This section is provided to help system implementors with how to support the other devices listed below within the SFF-TA-1034 slot. This section is informative and is meant for guidance only.

9.1 OCP NIC 3.0

9.1.1 Overview

OCP NIC 3.0 devices using the SFF card size is intended to work within an SFF-TA-1034 system slot. Some considerations need to be made to support these devices. Note that the OCP NIC 3.0 cannot be plugged directly into a PMM slot so an interposer is required for full functionality. Section 9.1.4 explains in more details what is needed.

9.1.2 Mechanical Compatibility

The SFF-TA-1034 slot within a host system is much wider and longer than the OCP NIC 3.0 device. To account for this, a mechanical fixture (also called a carrier) would need to be supported such that the device can align and insert properly to the host connector, to retain the device once its inserted, and be able to extract the device. This carrier is the responsibility of the host.

9.1.3 PCIe Electrical Compatibility

If a host supports an OCP NIC 3.0 device then the host should follow the PCIe electrical budgets defined in the *OCP NIC 3.0 Design Specification*. If an interposer is used to connect the OCP NIC 3.0 device to the host then the host should account for the interposer in the overall electrical budget.

9.1.4 Functional Compatibility

If a host supports an OCP NIC 3.0 device then an interposer is needed to account for the sideband signaling differences. Figure 9-1 shows the differences and how the devices are connected to each other.

An ASIC is required to convert between NC-SI RBT signaling and SGMII KR signaling.

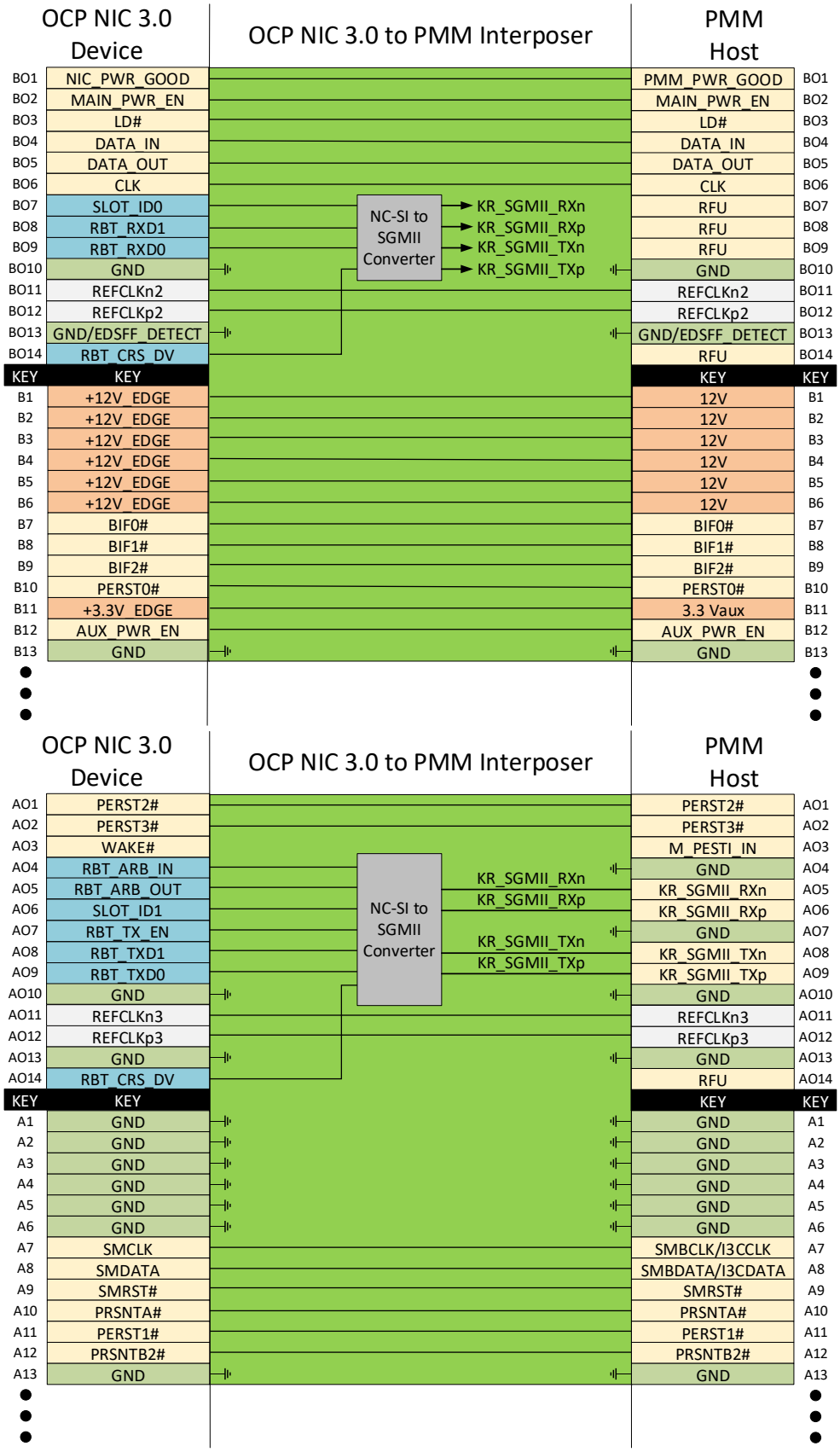


Figure 9-1. PMM Host Interposer for OCP NIC 3.0 Device

9.2 EDSFF E3 (SFF-TA-1008)

9.2.1 Overview

EDSFF devices using SFF-TA-1008 mechanicals (E3.S 1T, E3.S 2T, E3.L 1T, E3.L 2T) is intended to work within an SFF-TA-1034 system slot. Some considerations need to be made to support these devices.

An SFF-TA-1008 device supporting a 4C+ connector will be treated like an OCP NIC 3.0 device in a PMM slot. Please refer to Section 9.1 on how to support this device.

Other EDSFF devices using SFF-TA-1006 (E1.S) or SFF-TA-1007 (E1.L) mechanicals are not considered compatible with the SFF-TA-1034 host system slot. The primary side thickness of SFF-TA-1006 is larger than the secondary side thickness of SFF-TA-1034 which impacts the SFF-TA-1034 volume keep in. The length of SFF-TA-1007 is longer than the length of SFF-TA-1034 which impacts the SFF-TA-1034 volume keep in.

9.2.2 Mechanical Considerations

The SFF-TA-1034 slot within a host system is much wider and longer than the SFF-TA-1008 device. To account for this, a mechanical fixture (also called a carrier) would need to be supported such that the device can align and insert properly to the host connector, to retain the device once its inserted, and be able to extract the device. This carrier is the responsibility of the host.

9.2.3 PCIe Electrical considerations

If a host supports an EDSFF device then it should follow the PCIe electrical budgets defined in *SFF-TA-1009 Enterprise and Datacenter Standard Form Factor Pin and Signal Specification*

9.2.4 Functional Compatibility

If a host supports an EDSFF device then the host will need to configure the pins correctly since there are some pin differences between EDSFF and PMM. One method to do this is by using the GND/EDSFF_DETECT pin. The signals should be configured as EDSFF or PMM prior to or simultaneous with 12 V power being applied to the device. For specific pin configuration details, see Figure 9-2 as reference.

EDSFF Device		PMM Host	
	BO13	GND/EDSFF_DETECT	Host has pull-up on this pin to determine if EDSFF or PMM
	BO14	RFU	
KEY	KEY	KEY	
12V	B1	12V	Same usage for both EDSFF and PMM
12V	B2	12V	Same usage for both EDSFF and PMM
12V	B3	12V	Same usage for both EDSFF and PMM
12V	B4	12V	Same usage for both EDSFF and PMM
12V	B5	12V	Same usage for both EDSFF and PMM
12V	B6	12V	Same usage for both EDSFF and PMM
MFG	B7	BIF0#	If EDSFF_DETECT is “High”, host sets Hi-Z per SFF-TA-1009
RFU	B8	BIF1#	If EDSFF_DETECT is “High”, host sets Hi-Z per SFF-TA-1009
DUALPORTEN#	B9	BIF2#	If EDSFF_DETECT is “High”, host drives signal per SFF-TA-1009
PERST0#	B10	PERST0#	Same usage for both EDSFF and PMM
3.3 Vaux	B11	3.3 Vaux	Same usage for both EDSFF and PMM
PWRDIS	B12	AUX_PWR_EN	If EDSFF_DETECT is “High”, host drives signal per SFF-TA-1009
GND	B13	GND	Same usage for both EDSFF and PMM

EDSFF Device		PMM Host	
	AO13	GND	
	AO14	RFU	
KEY	KEY	KEY	
GND	A1	GND	Same usage for both EDSFF and PMM
GND	A2	GND	Same usage for both EDSFF and PMM
GND	A3	GND	Same usage for both EDSFF and PMM
GND	A4	GND	Same usage for both EDSFF and PMM
GND	A5	GND	Same usage for both EDSFF and PMM
GND	A6	GND	Same usage for both EDSFF and PMM
SMBCLK/I3CCLK	A7	SMBCLK/I3CCLK	Same usage for both EDSFF and PMM
SMBDATA/I3CDATA	A8	SMBDATA/I3CDATA	Same usage for both EDSFF and PMM
SMRST#	A9	SMRST#	Same usage for both EDSFF and PMM
LED	A10	PRSNTA#	If EDSFF_DETECT is “High”, host drives signal per SFF-TA-1009
PERST1#/CLKREQ#	A11	PERST1#	Same usage for both EDSFF and PMM (CLKREQ# not supported)
PRSNT0#	A12	PRSNTB2#	Same usage for both EDSFF and PMM
GND	A13	GND	Same usage for both EDSFF and PMM

Figure 9-2. PMM Host Signal Changes for EDSFF Device