

New Project Proposal: SFF-TA-1033

Presentation Date: March 22, 2024

Editor: Paul Coddington [Amphenol]

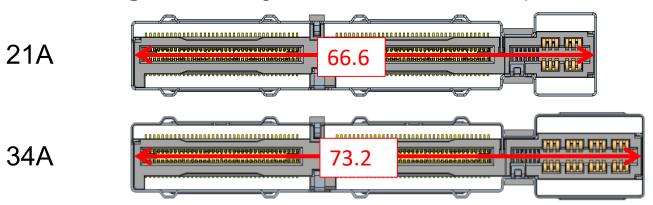
Supporters: Paul Coddington [Amphenol],

Glen Hanna [Lenovo], & Scott Shuey [Lotes]



- SFF-TA-1033 Editor: Paul Coddington [Amphenol]
- Supporters:
 - 1. Amphenol
 - 2. Lenovo
 - 3. Lotes

Some Background: High Power version comparisons

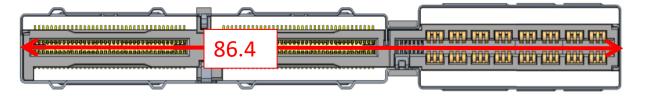


10.5A per power pin/ 21A total

8.5A per power pin/ 34A total

- When designing the 55A version ...
 - Connector length, 86.4mm, was considered too long would require stricter SMT reflow process.
 - T-Rise will exceed 30°C. To control within 30°C, we might need more CU layers to support.

Early 55A design



6.875A per power pin (Assumed)/ 55A total with ΔT ~32°C

Alternative design chosen

Rev 1.0 55A design



27.5A per power pin/55A total



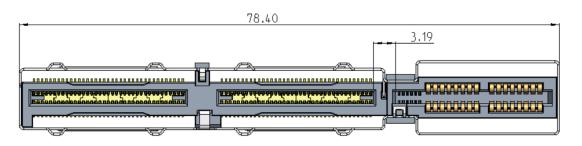
Issue with current 55A design

- In addition to mating plugs, these connectors can also accept an AIC.
- What if someone plugs in an AIC expecting 21A or plugs in an AIC expecting 34A into the 55A connector?
 - Bad things can happen.

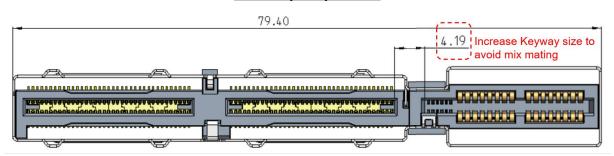
Solution:

 Increasing the keyway between the high speed signal portion of the connector and the sideband & power portion of the connector by 1mm will prevent unwanted AICs from accidentally plugging into the 55A connector.

Existing design (SFF-TA-1033 Rev 1.0)

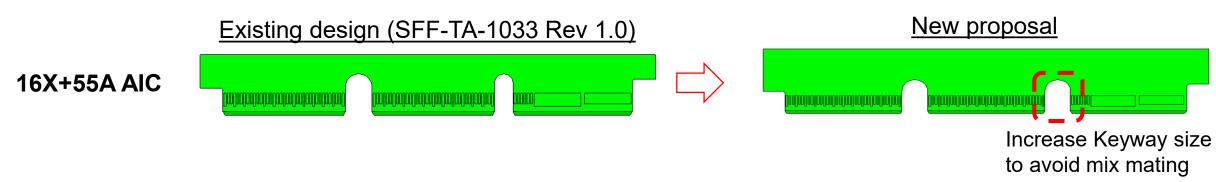


New proposal





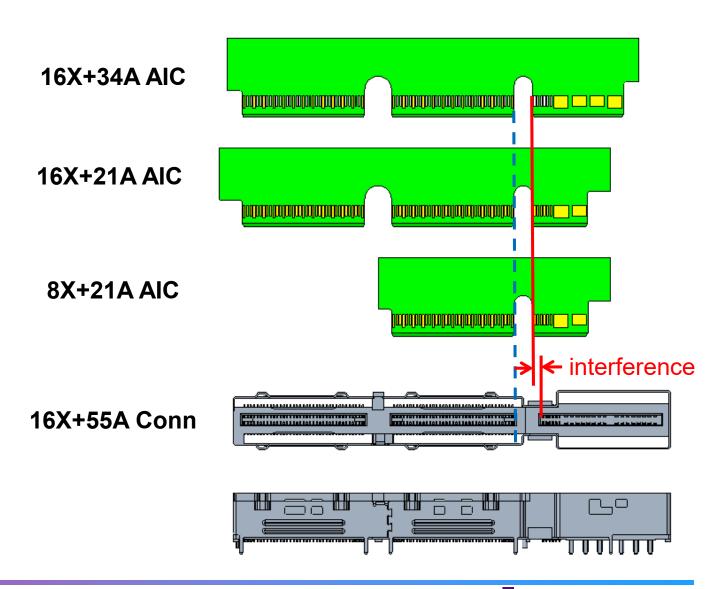
 To go along with the proposed 55A connector key width change, a change to the 55A AIC keyway width is required.



- The same keyway width modification will be needed for the 55A plugs to maintain compatibility.
- Will add some text in Rev 2.0 to highlight incompatibility with the Rev 1.0 55A plugs, AICs, & connectors. Will also add warning notes for the mating matrix conditions indicated in yellow on slides 10 & 11 of this presentation.

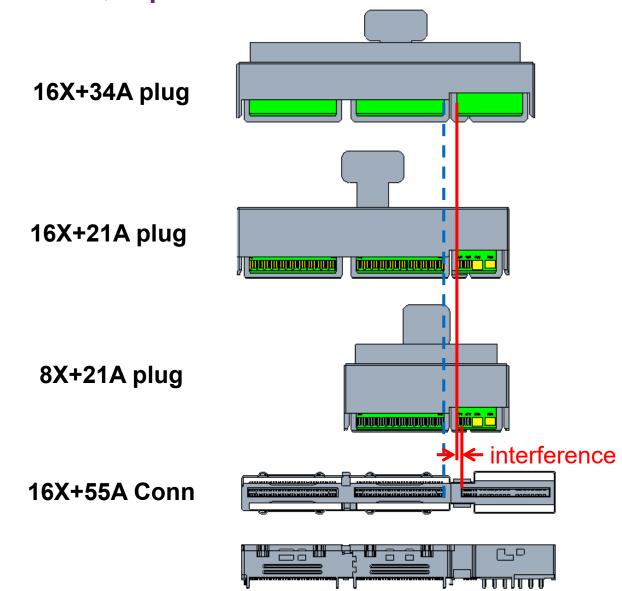
• Mix Mating Avoided ...

 AIC (16X+34A, 16X+21A, & 8X+21A) cannot be plugged in after the 16X+55A connector key width design change.



• Mix Mating Avoided ...

 Cable plug (16X+34A, 16X+21A, & 8X+21A) cannot be plugged in after the 16X+55A connector key width design change.

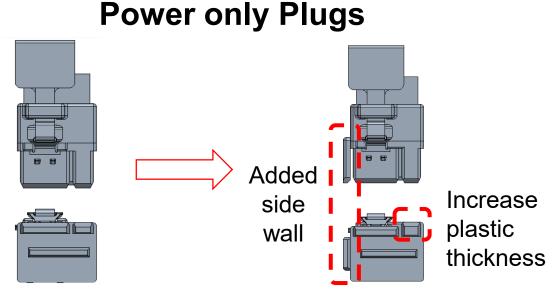


- Another potential mix mating of a plug connector with the wrong receptacle connector ...
 - The Rev 1.0 lower amperage power-only Power Plugs could potentially plug into the 55A receptacle connectors, which could have bad results.

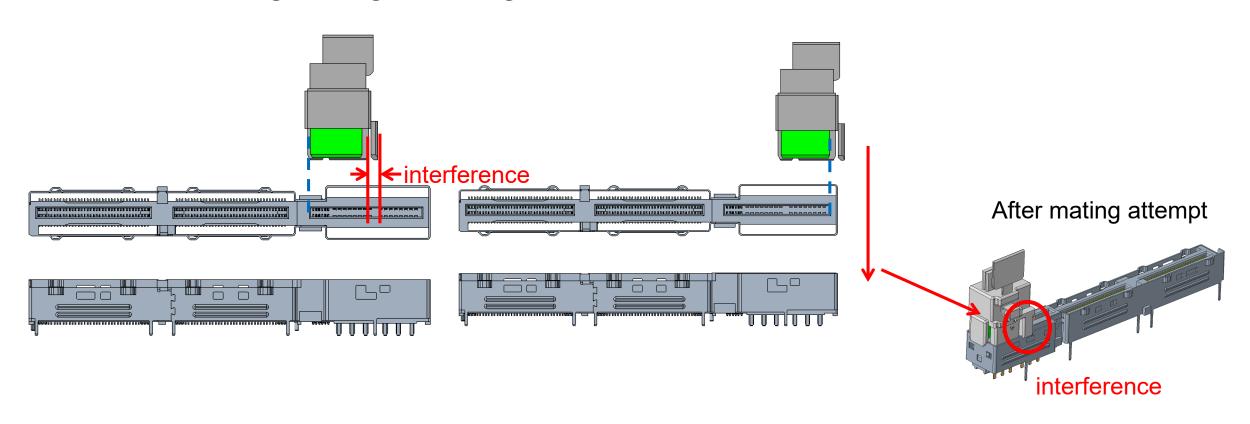
Solution:

 Add a side wall to the power-only Power Plugs to prevent plugging into the wrong receptacle connector.

 Increase the plastic thickness of an existing wall to cause mating interference when trying to plug into the wrong receptacle connector.



- Mix Mating Avoided ...
- Power Plug cables cannot be plugged into the 16X+55A connector after the Power Plug design change.



AIC AIC 16X+34A 16X+21A 16X+55A 8X+21A **Power only Mating Matrix Power only** 8X+21A 16X+21A 16X+34A 16X+55A

Plugs Plug 16X+55A **Power only** 8X+21A 16X+21A 16X+34A **Mating Matrix Power only** 8X+21A 16X+21A 16X+34A 16X+55A

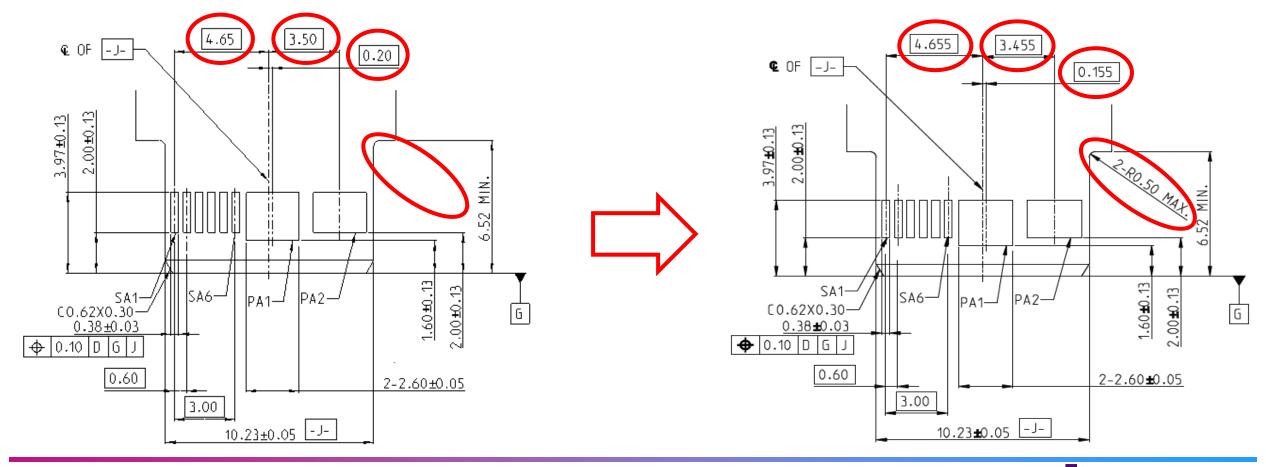
Updates to Table 5-1 Datum Descriptions

- Modify the description of Datum C for further clarification
- Add Datum R (used in Figures 6-20, 6-22, & 6-24), was missing from the table

Table 5-1 Datum Descriptions

Datum	Description
Α	-Mating Surfaces to the PCB or PCB Pads
В	Plug and Receptacle Mechanical Stop
С	Centerline of the Receptacle Paddle Card Slot Height / Mating Interface Centerline
D	Centerline of Paddle Card Thickness
E	Bottom Surface of Plug Body
F	Centerline of Key
G	Leading Edge of Paddle Card
J	Centerline of the Receptacle Width
K	Centerline of Plug Body
L	Receptacle Shell Surface
Р	Receptacle Shell Surface
<u>R</u>	Power Paddle Card Interface Width Centerline
V	Centerline of the Receptacle's Locating Peg
W	Centerline of the Receptacle's Locating Peg

- Corrections to 21A Power AIC (Figure 6-27)
 - Modify pad location dimensions from Datum J, as show below
 - Add missing radius dimension, as shown below



• IP Declaration:

- NOTE: The document will undergo a new IP disclosure period once published as a new Rev 2.0 per the SNIA SFF Process Guide
- General timeline for project completion (subject to change)
 - Initial Project Start Approval: March 22, 2024
 - DRAFT Revision 1.0.1 estimated by April 15, 2024?
 - Review Ballot estimated to end by May 15, 2024?
 - Comment Resolution & updated revision estimated by June 7, 2024?
 - Approval Ballot end estimated by July 10, 2024?
 - Comment Resolution & final Published revision estimated by July 22, 2024?
 - IP Declaration completion estimated by September 20, 2024?

