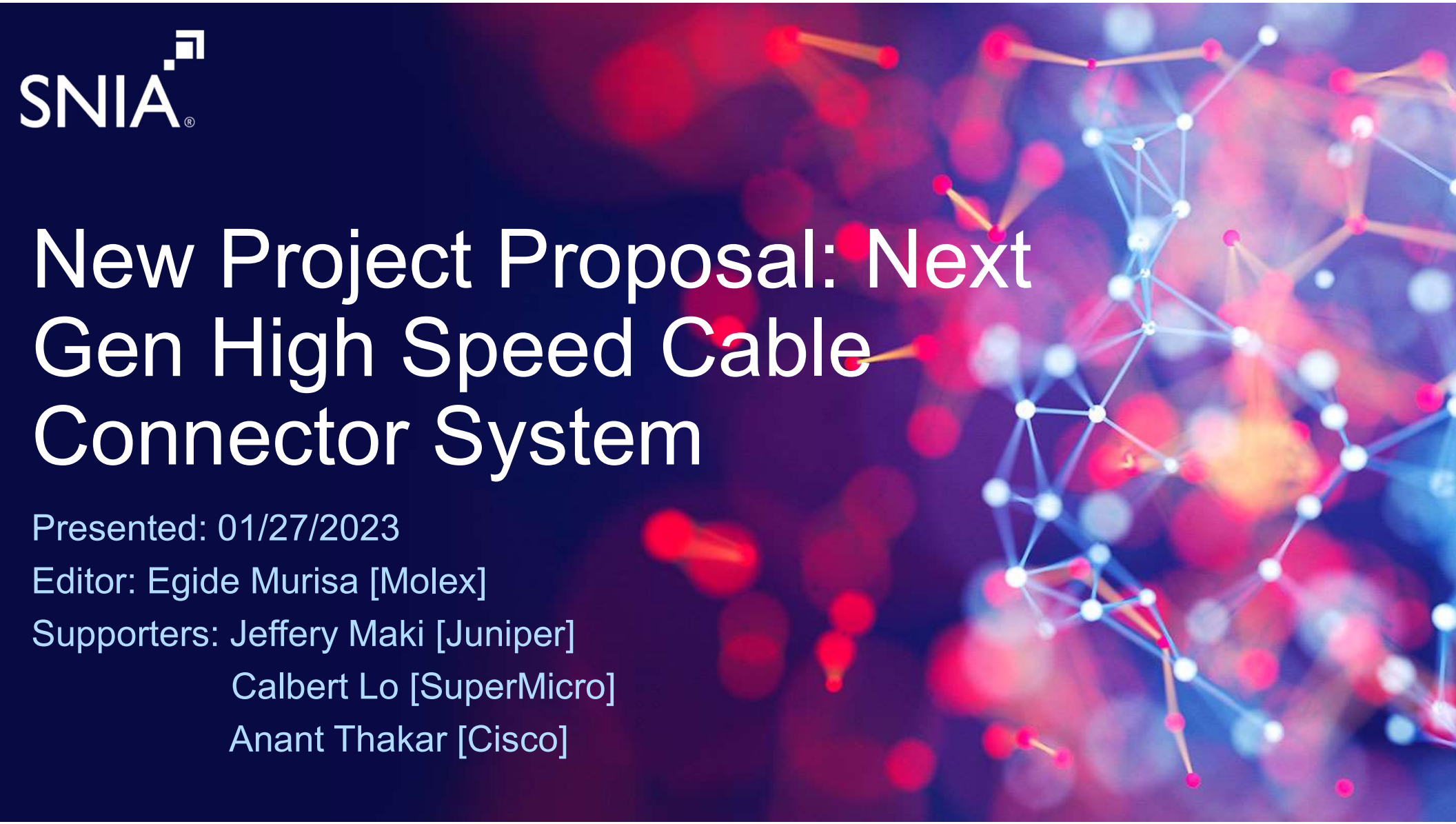

New Project Proposal: Next Gen High Speed Cable Connector System

Presented: 01/27/2023

Editor: Egide Murisa [Molex]

Supporters: Jeffery Maki [Juniper]

Calbert Lo [SuperMicro]

Anant Thakar [Cisco]

New Project Proposal: Document Number Needed

- To provide an internal cable and connector form factor to enable next generation higher speed capabilities
- Features include superior SI performance with advanced mechanical structure, scalable on supporting various configs to fulfill system design needs
- Editor: Egide Murisa [Molex]
- Supporters:
  1. Molex
  2. Juniper
  3. SuperMicro
  4. Cisco

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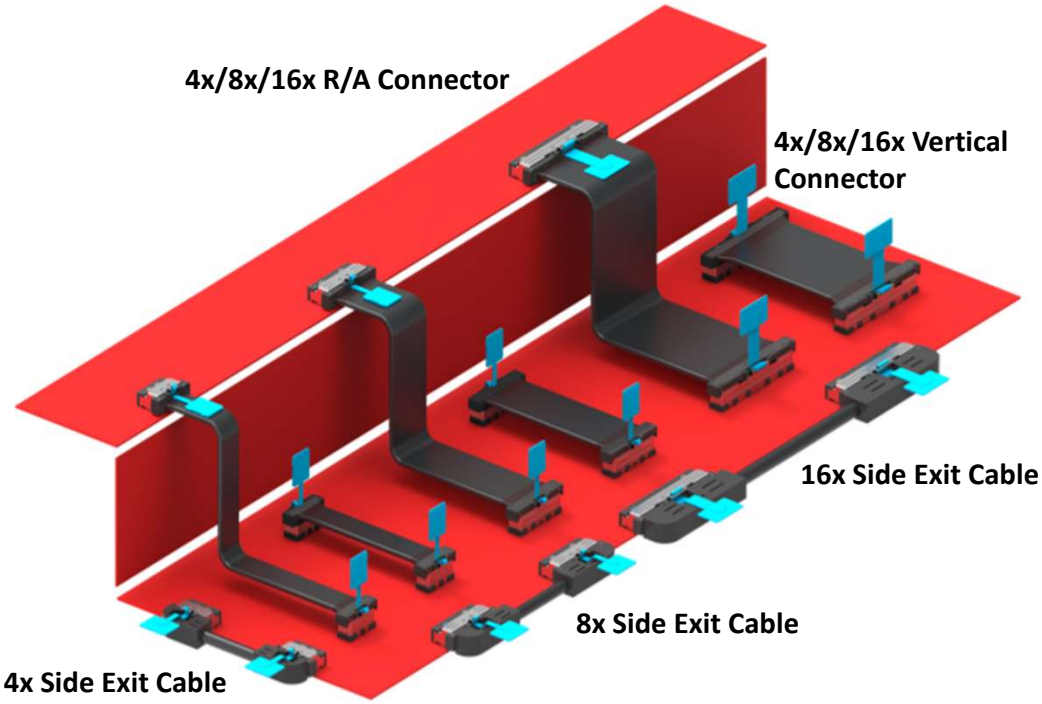
Next Generation High Speed Product Family



Support : Silicon to Silicon, Silicon to IO, Silicon to backplane, Silicon to Raiser, Main Board to OCP-NIC, Main Board to Storage/NVMe.

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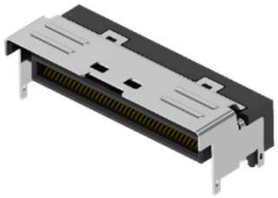
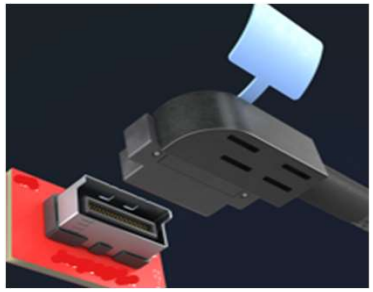
General Spec scope

Vertical

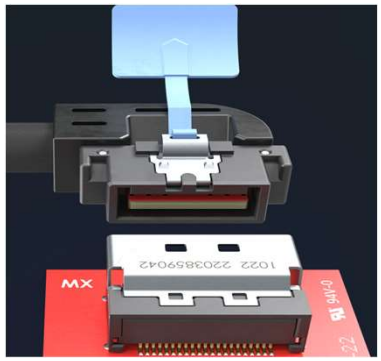


Right Angle

Target Standard	PCIe 6.0 and Beyond
Data Rates	64 GT/s and Beyond
Mating Cycles	250
Fix/ Lock	Latch Fixed
Wire Gauge	28~32 AWG
Wire Type	Discrete and Ribbon Twinax Cable
Pitch Width	0.6mm
Impedance	85ohm
PCIe Channel	X4(42P) , X8(80P), X16(130P), X20(160P)
Cable Plug Type	Straight; Right Angle Down; Side Exit
Connector Type	Vertical and Right Angle
Connector Mounting	SMT Soldering



Vertical Exit



Side Exit

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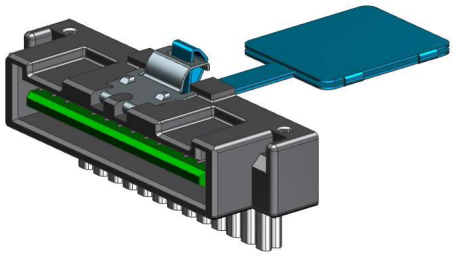
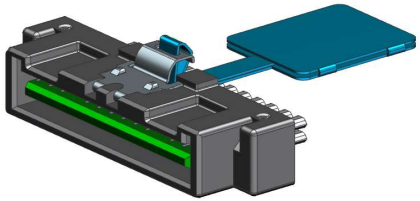
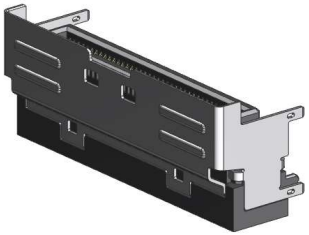
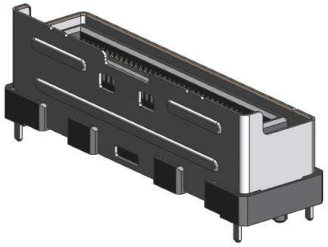
Mechanical Features

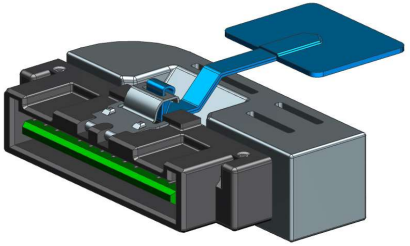
- Paddle Card/Gold Fingers Protection by Full Shrouded Cable Plug Housing
- Anti-Slant
- Anti-Reverse
- Easy Installing with Guiding/Stopping Features











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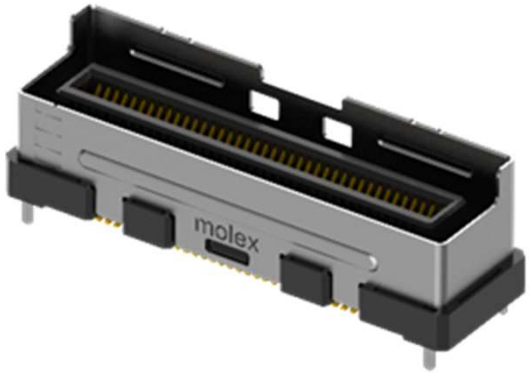
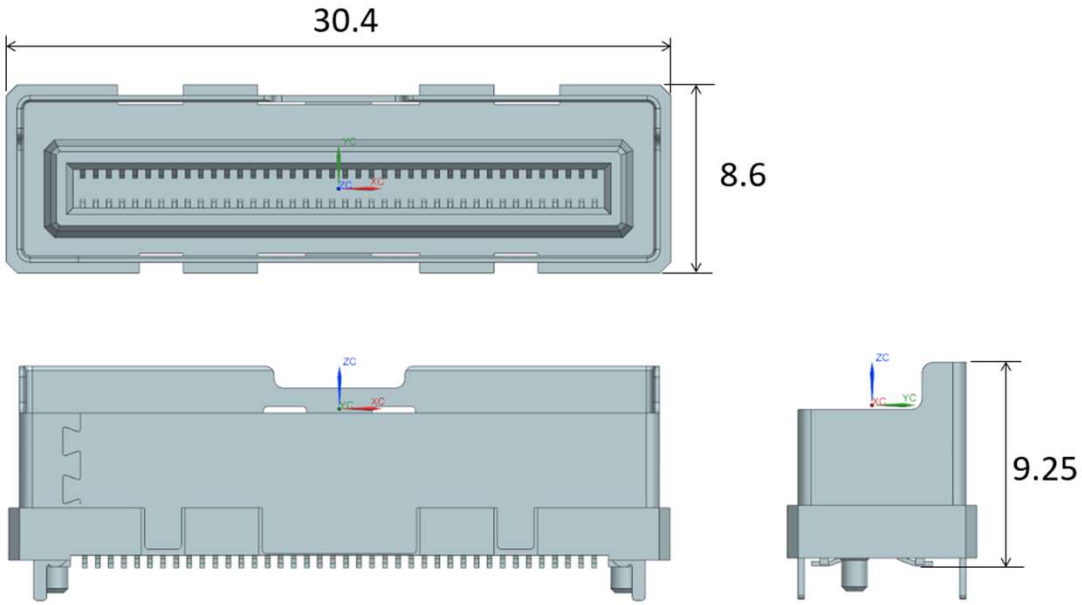
Board Connector :



Vertical Type 80pins



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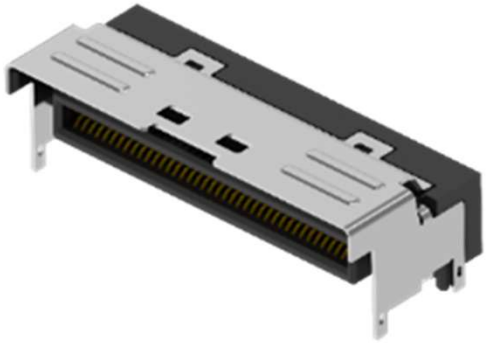
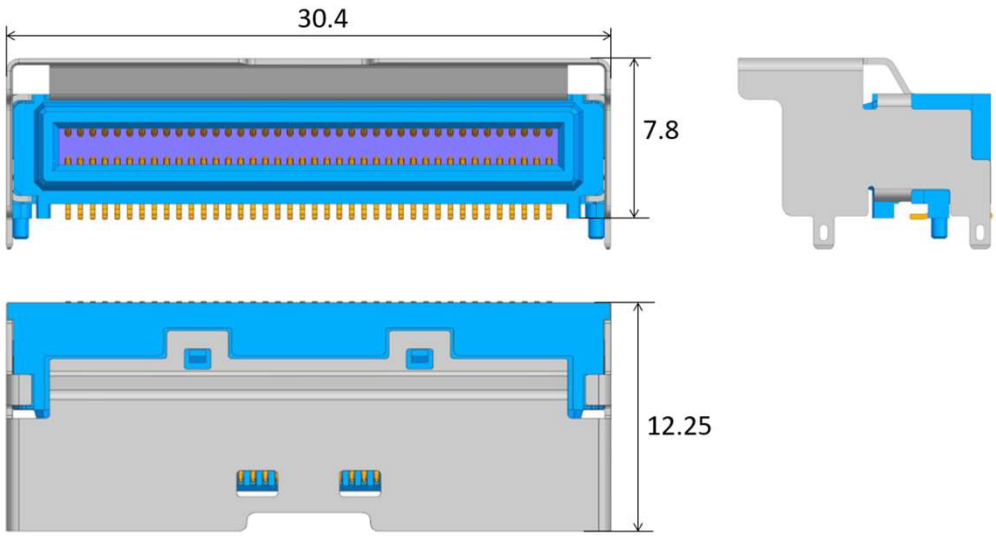
Board Connector :



Right Angel Type 80pins



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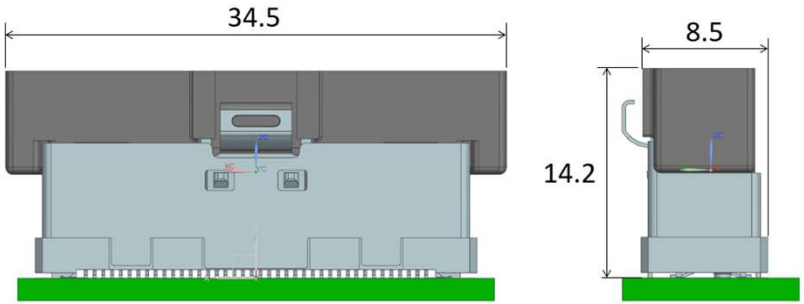
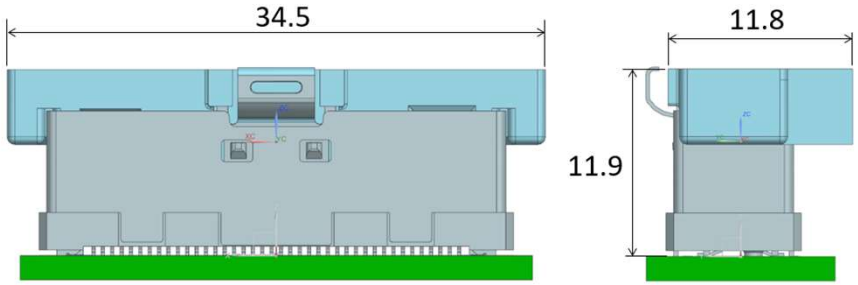
Mating Dimensions:



Vertical Exit 80pins



Right Angle Exit 80pins

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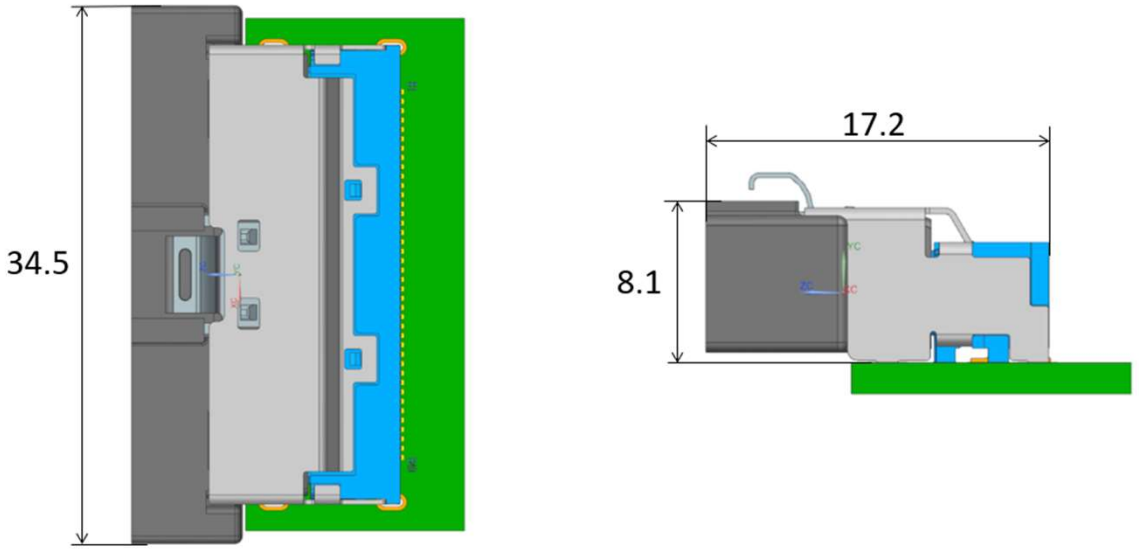
Mating Dimensions:



Straight Exit with RA Conn. 80pins

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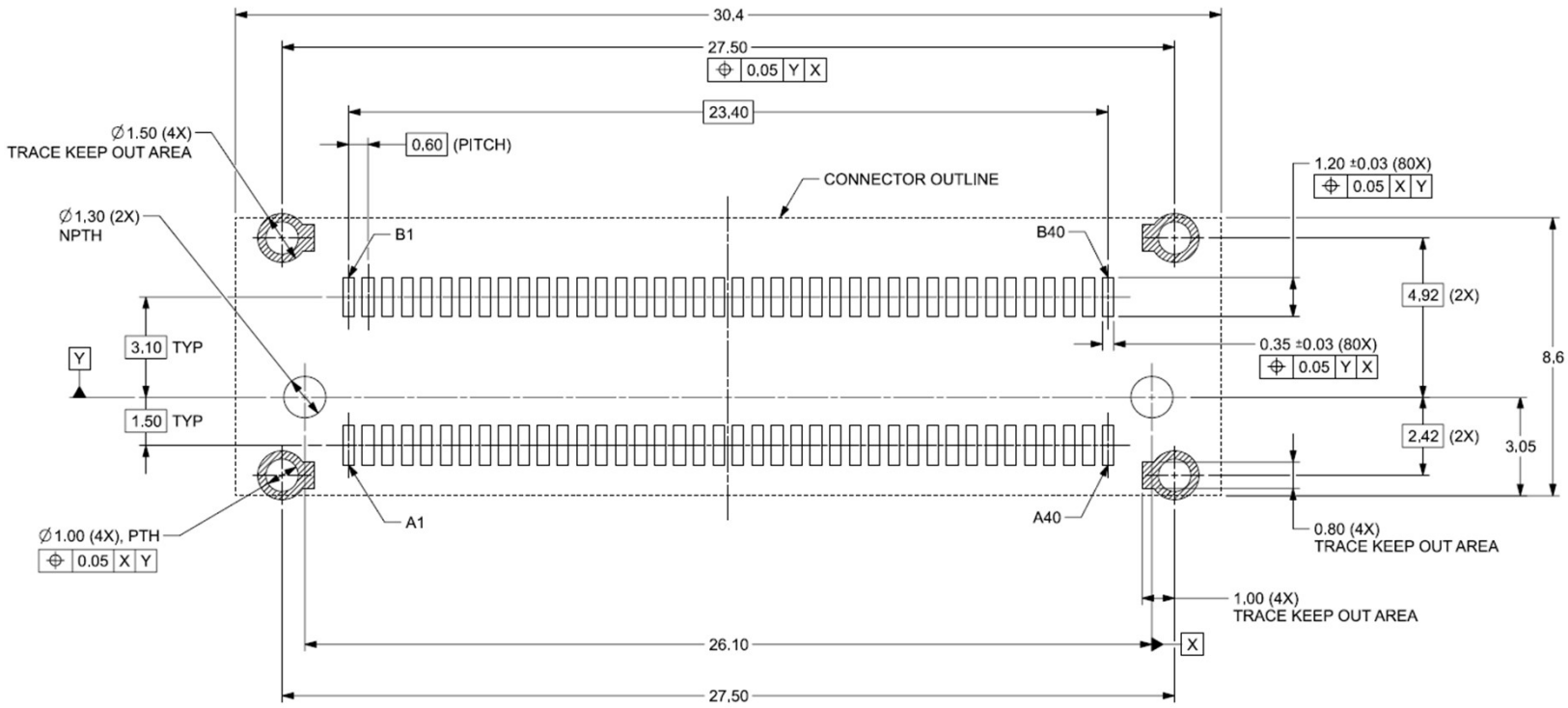
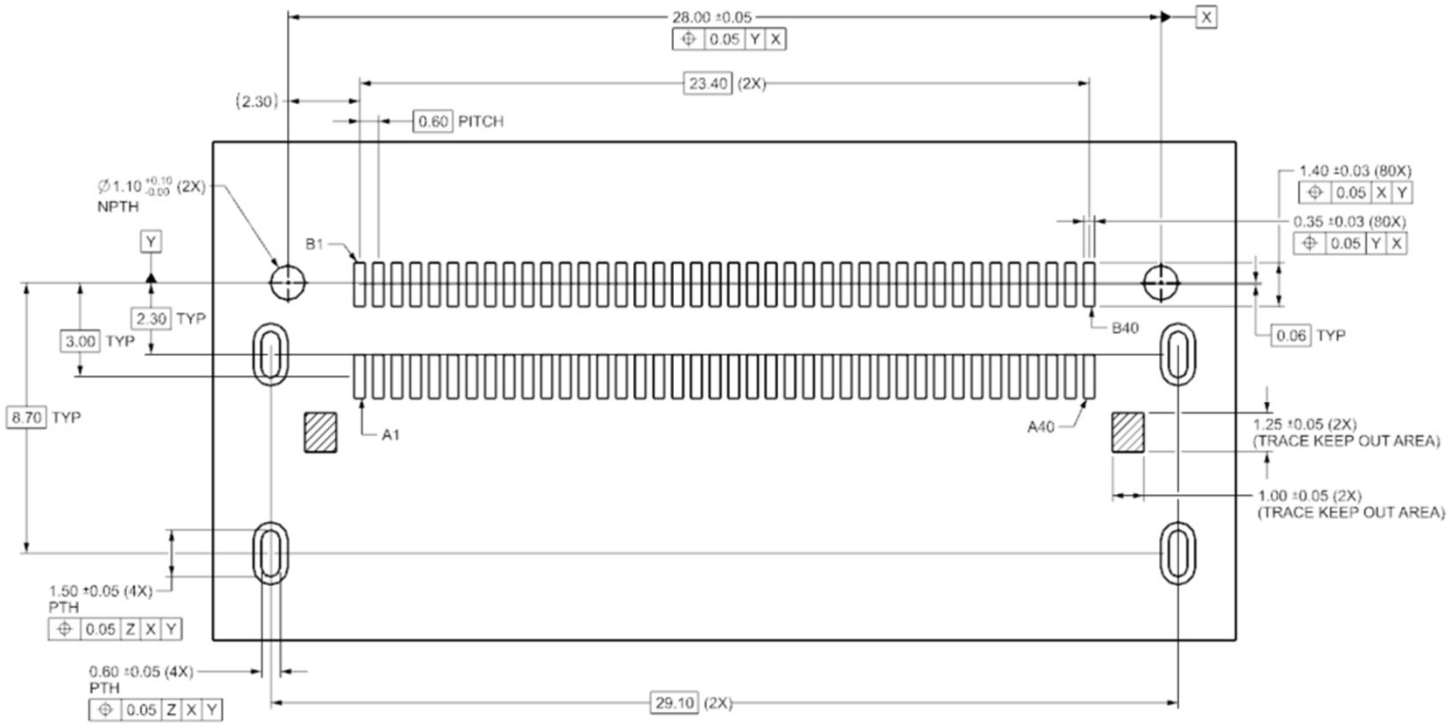
- Footprint (Vertical board connector 80pins)



RECOMMENDED PCB LAYOUT
(GENERAL TOLERANCES: ±0.05)

- Footprint (RA board connector 80pins)



RECOMMENDED PCB LAYOUT
(GENERAL TOLERANCES: ±0.05)

New Project Proposal: Document Number Needed

- IP Declaration:
  - NOTE: The document will undergo an IP disclosure period prior to publication per the SNIA SFF Process Guide

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