SFF-TA-1021

Specification for

PCIe® Enclosure Compatible Form Factor Specification (PECFF)

Rev 1.0 February, 19 2020

SECRETARIAT: SFF TA TWG
This specification is made available for public review at http://www.snia.org/sff/specifications. Comments may be submitted at http://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

The description of the connector in this specification does not assure that the specific component is available from connector suppliers. If such a connector is supplied, it should comply with this specification to achieve interoperability between suppliers. This specification originates from the Gen Z Consortium and supersedes their prior documents.

ABSTRACT: This specification defines the PCIe® Enclosure Compatible Form Factor Specification (PECFF). This form factor maintains mechanical compatibility with existing PCIe add-in-card enclosures while integrating the SFF-TA-1002 connector interface, addressing mechanical integration challenges in 1U systems and providing additional power, bandwidth, and top edge connectivity.

POINTS OF CONTACT:

John Norton
Distinguished Technologist
Hewlett Packard Enterprise
11445 Compaq Center Drive W
Houston, TX 77070
Email: john.norton@hpe.com

Anthony Constantine
Intel Corporation
2111 NE 25th Ave
MS JF5-270
Hillsboro, OR 97124
Email: anthony.m.constantine@intel.com

Chairman SFF TA TWG
Email: SFF-Chair@snia.org

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Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at http://www.snia.org/sff/join.

Revision History

Rev 1.0 *February 19, 2020*

- Initial Release

Contents

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1. Scope

This specification defines a PCIe Enclosure Compatible Form Factor (PECFF) that is mechanically compatible with enclosures that support a PCI Express® Card Electromechanical (CEM) add-in card (AIC). The specification defines PECFF with connector interfaces based on SFF-TA-1002 and SFF-TA-1020 connectors.

2. References and Conventions

2.1. Industry Documents

The following documents are relevant to this specification:

- ASME Y14.5 Dimensioning and Tolerancing
- EIA-364-1000 Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Controlled Environment Applications
- OCP NIC 3.0 Design Specification
- PCI Express Card Electromechanical Specification
- REF-TA-1011 Cross Reference to Select SFF Connectors
- SFF-TA-1002 Protocol Agnostic Multi-Lane High Speed Connector
- SFF-TA-1020 SFF-TA-1002 Cables and Connector Variants Based on SFF-TA-1002
- SFF-TA-1022 PECFF (PCIe Enclosure Compatible Form Factor) Thermal Reporting Specification

2.2. Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at http://www.snia.org/sff/specifications. Suggestions for improvement of this specification will be welcome, they should be submitted to http://www.snia.org/feedback.

Copies of PCIe standards may be obtained from PCI-SIG (http://pcisig.com).

Copies of ASME standards may be obtained from the American Society of Mechanical Engineers (https://www.asme.org).

Copies of Electronic Industries Alliance (EIA) standards may be obtained from the Electronic Components Industry Association (ECIA) (https://www.ecianow.org).

Copies of Open Compute Project specifications may be obtained from https://www.opencompute.org/

2.3. Conventions

The following conventions are used throughout this document:

DEFINITIONS
Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE
If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS
Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a. red (i.e., one of the following colors):
    A. crimson; or
    B. pink;
b. blue; or
c. green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1. top;
2. middle; and
3. bottom.

Lists are associated with an introductory paragraph or phrase, and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

DIMENSIONING CONVENTIONS
The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

NUMBERING CONVENTIONS
The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1. Keywords

May/ may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Defines the signal on a connector contact [when] its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies the restricted designation, then the restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word, or field (e.g., a restricted byte uses the same value as defined for a reserved byte).

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2. Acronyms and Abbreviations

AIC: Add in Card
CEM: Card Electro-Mechanical
NIC: Network Interface Controller
PCB: Printed Circuit Board
PECFF: PCIe Enclosure Compatible Form Factor
RAND: Reasonable And Non-Discriminatory
REFCLK: Reference Clock
Res: Reserved
Rx: Receive
Tx: Transmit
VEN_DEF: Vendor Defined

3.3. Definitions

Connector: Each half of an interface that, when joined together, establish electrical contact and mechanical retention between two components. In this specification, the term connector does not apply to any specific gender; it is used to describe the receptacle, the plug or the card edge, or the union of receptacle to plug or card edge. Other common terms include: connector interface, mating interface, and separable interface.

4. General Description

4.1. Overview

This specification defines a PCIe Enclosure Compatible Form Factor (PECFF) that is mechanically compatible with enclosures that support a PCI Express® Card Electromechanical (CEM) add-in card (AIC). PECFF complies with the SFF-TA-1002 mating interface, supports high power solutions (up to 660W at 12V and up to 1024W at 48V), supports up to 64 differential pairs (optional), and specifies AIC-to-AIC high-speed data connectivity. PECFF specifies features and areas in which the PECFF differs from a PCIe® CEM AIC. Developers should refer to the *PCI Express Card Electromechanical Specification* for all details not defined in this specification. Refer to *SFF-TA-1022 PECFF (PCIe Enclosure Compatible Form Factor) Thermal Reporting Specification* for requirements for thermal characterization of PECFF AICs.

4.1.1. General Description

PECFF supports the PCIe AIC mechanical form factor variations including but not limited to the following:

- Length: Half-length, Three-quarter-length, and Full-length

  Developer Note: *As illustrated in* Figure 5-4*, the half-length high-mass AIC is slightly longer than a PCIe CEM AIC. The additional length enables designs to minimize system board trace length and signal loss irrespective of PECFF AIC size.*

  A non-high-mass PECFF half-length AIC can be the same length as a PCIe CEM AIC as the high-mass retention feature is not required.
- Height: Standard-height, Low-profile
- Slot width: Single, Double, and Triple
  Developer Note: *Wider slots can be used by actively or passively cooled high-power AICs*
- High-Mass (as defined by the *PCI Express Electromechanical Specification*)

4.1.2. Interoperability

A PECFF AIC shall interoperate with any slot connected with high-speed signals as permitted by mechanical keying specified in *SFF-TA-1002* and the *PCI Express Card Electromechanical Specification*

4.2. Use Cases

The following figures illustrate example PECFF use cases, enabled features, and enclosure compatibility points.

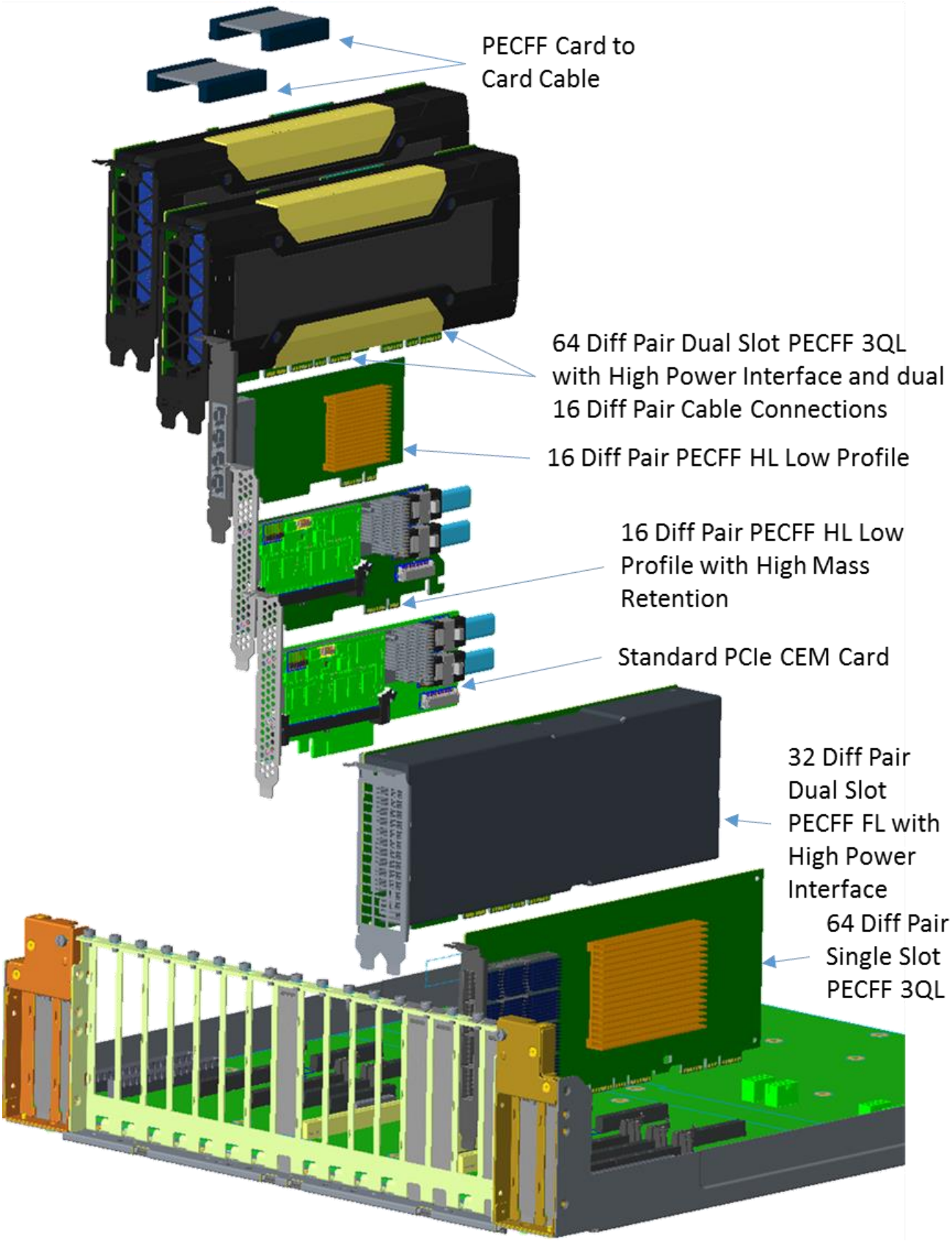


Figure 4-1. Example Enclosure that Supports PCIe CEM and PECFF AICs

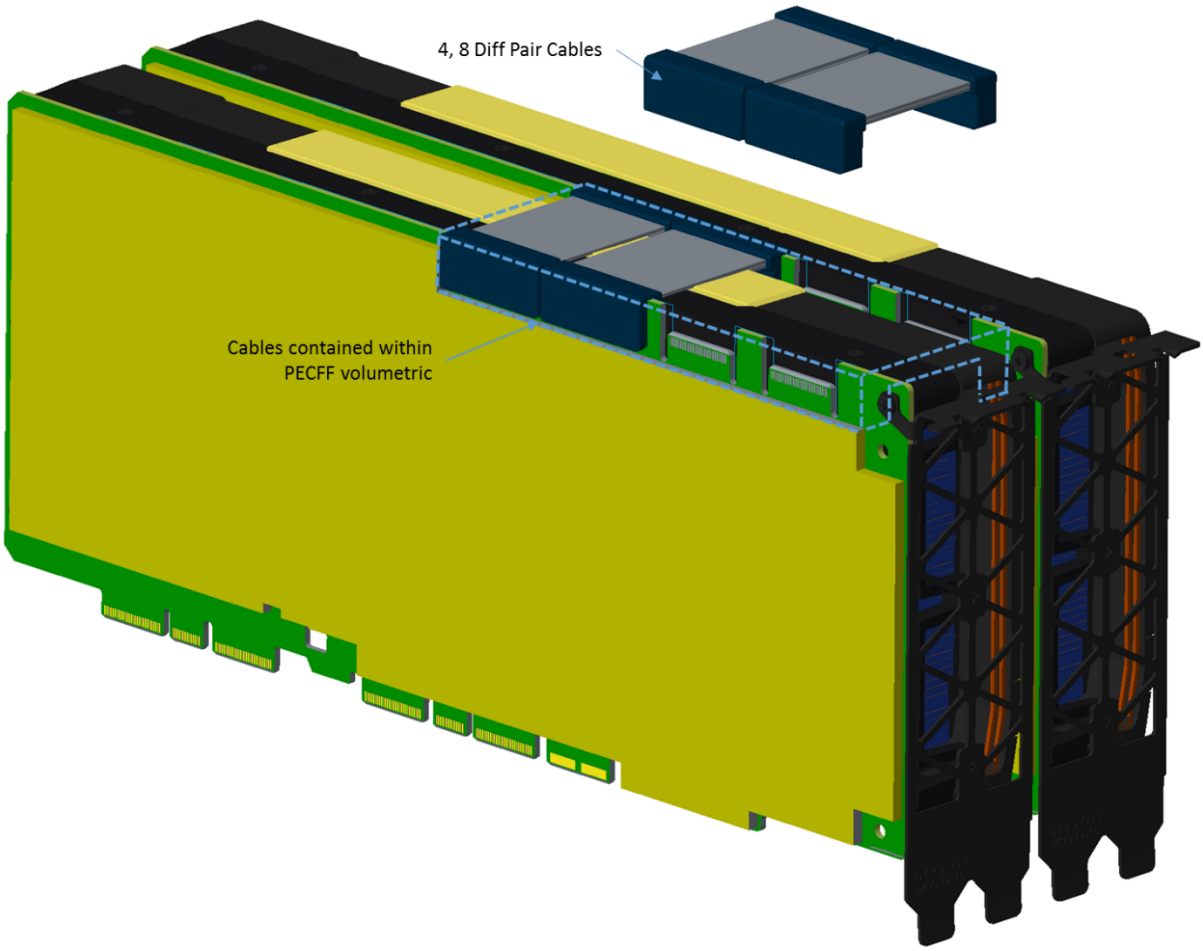


Figure 4-2. AIC-to-AIC Cable Connectivity

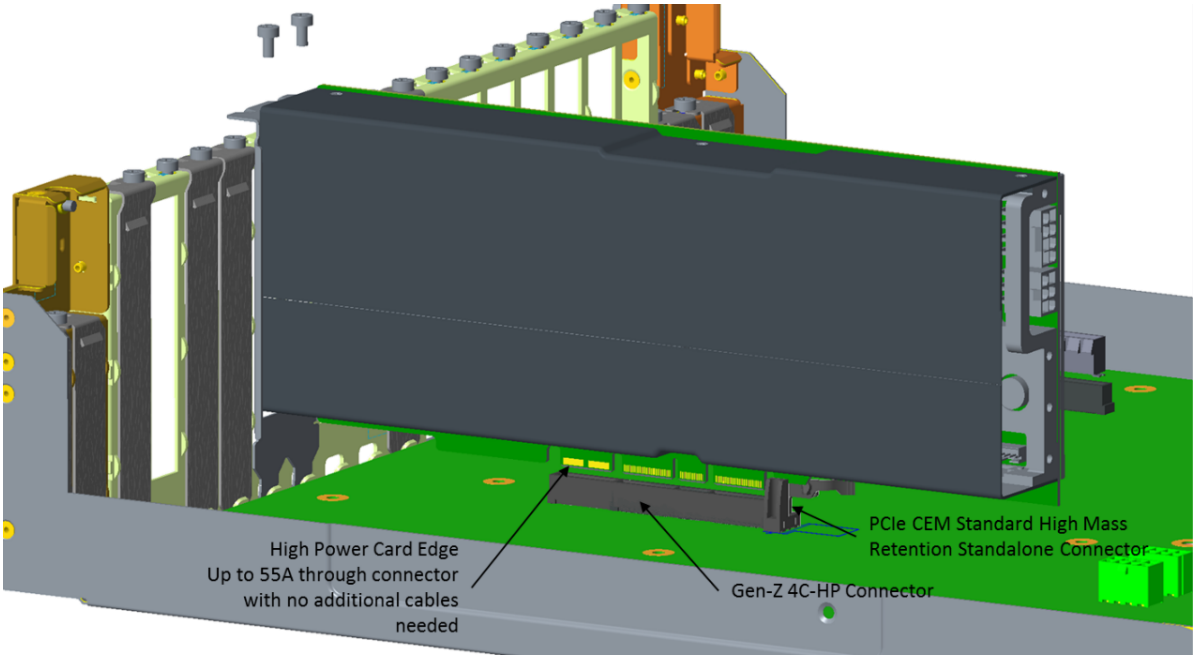


Figure 4-3. High-power Delivery through SFF-TA-1020 4C-HP Connector

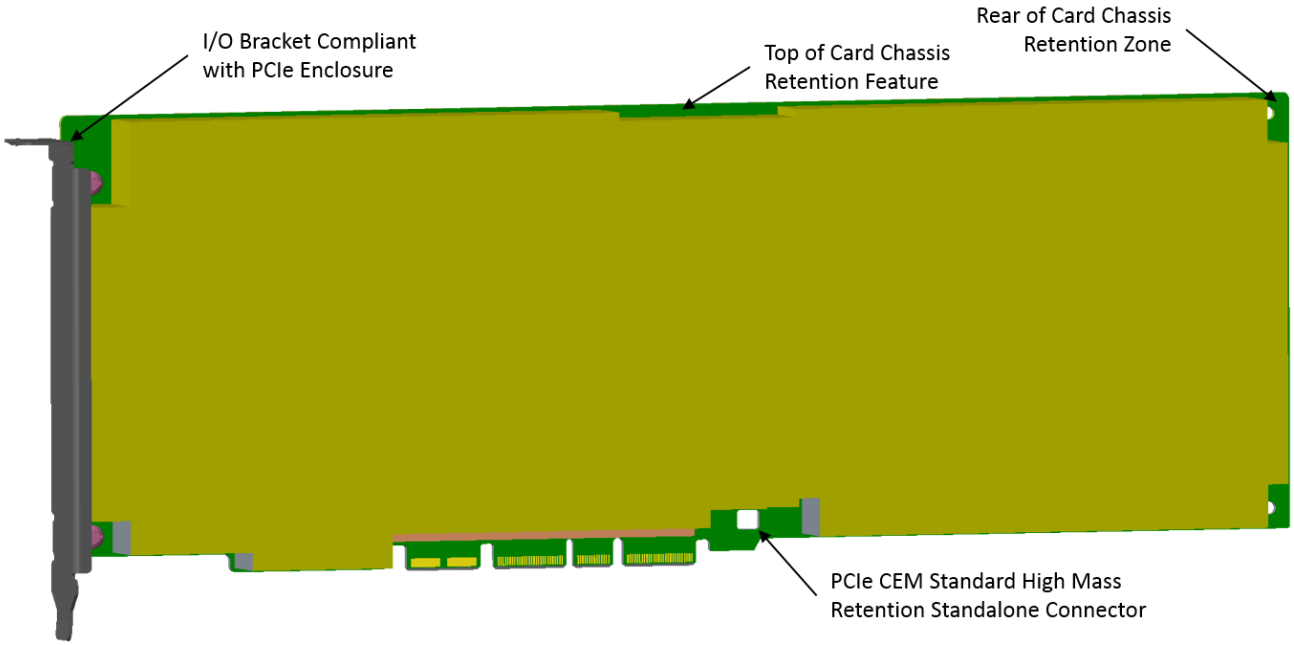


Figure 4-4. PECFF Reuse of PCIe CEM Enclosure Interface Points

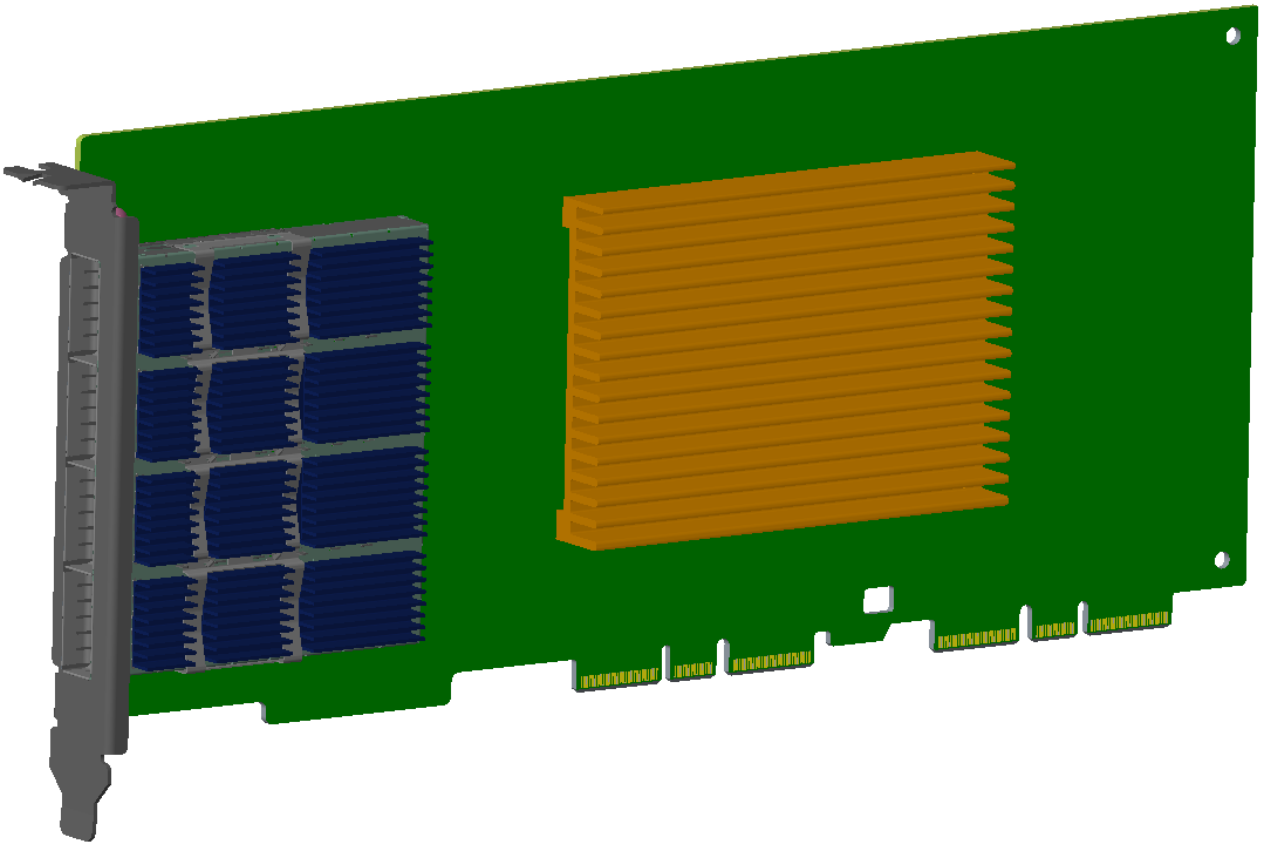


Figure 4-5. Example PECFF Quad-port 400GbE QSFP-DD NIC Using 64 Differential Signals

5. PECFF Mechanical Specification

5.1. Overview

The following mechanical requirements apply to PECFF:

- PECFF utilizes the same high-mass retention attachment point defined in *PCI Express Card Electromechanical Specification.* To ensure interoperability, PECFF three-quarter-length and full-length AICs shall support the cutouts in all implementations.
- PECFF supports an optional inline high-power interface as specified in the *SFF-TA-1020*. For connector mechanical and electrical requirements and 48V power implementation details refer to *SFF-TA-1020*.
- A PECFF AIC may support up to 64 differential pairs using an additional 4C interface.

  Developer Note: To optimize routing and signal integrity between the AIC interface and component, the *additional* 4C interface is rotated 180 degrees with respect to the first connector to group high-speed signals on the AIC interface.
- If plating tie bars are used for plating purposes, all tie bars shall be removed on all PECFF variations.

All dimensions and tolerances in the following figures are in millimeters, and conform to ASME Y14.5-2009.

5.2. PECFF Standard Height AIC

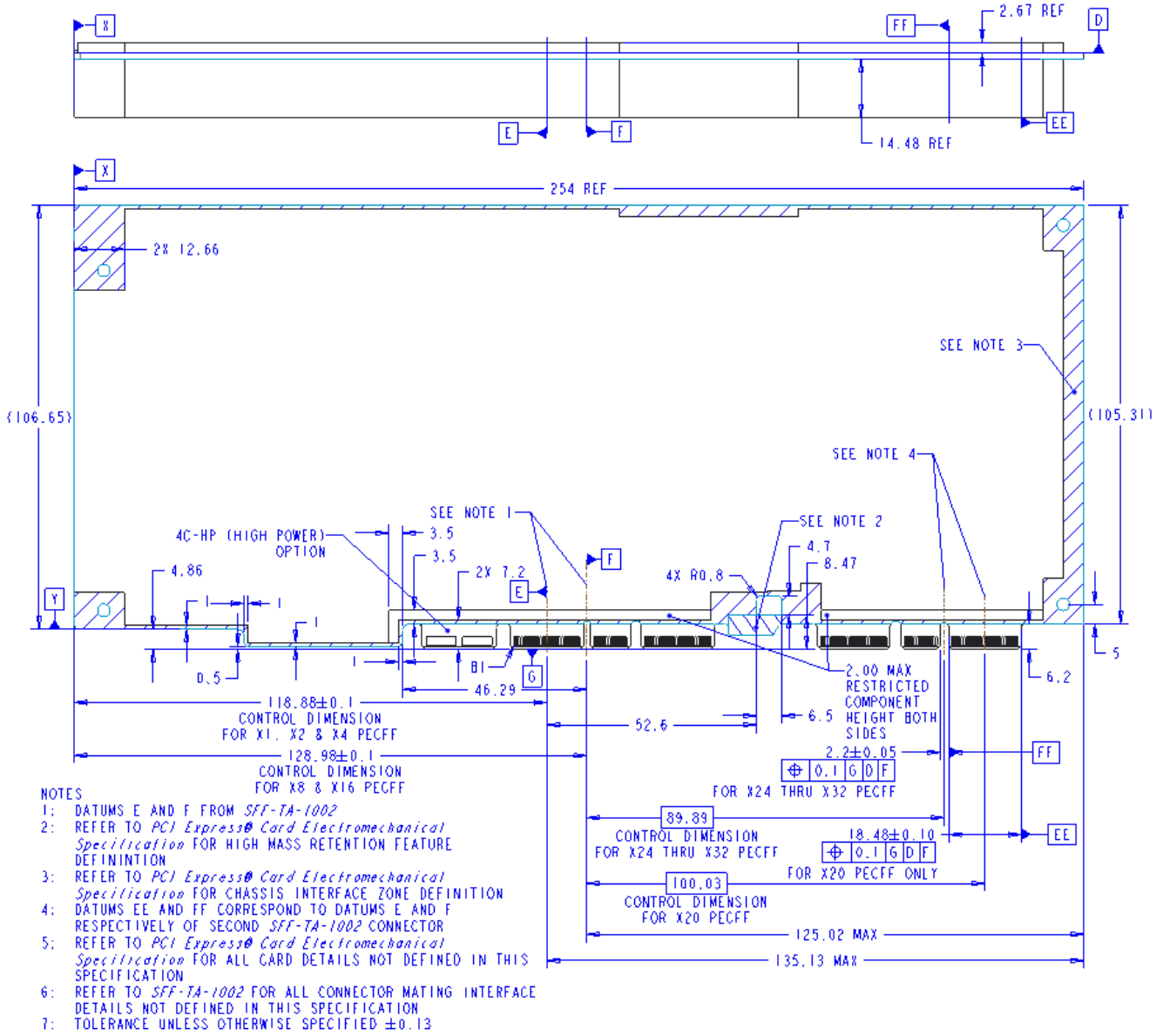


Figure 5-1. PECFF Three-quarter-length AIC without I/O Bracket

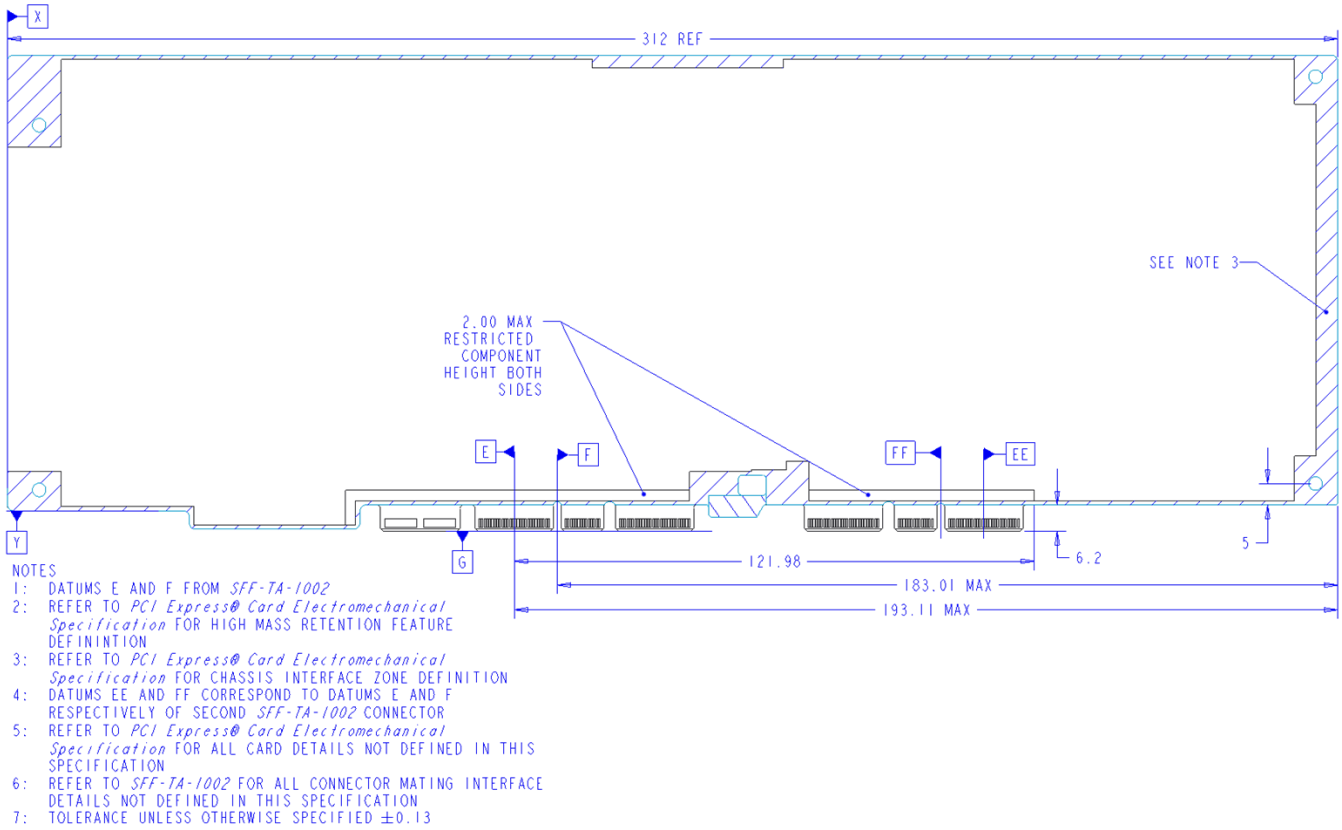
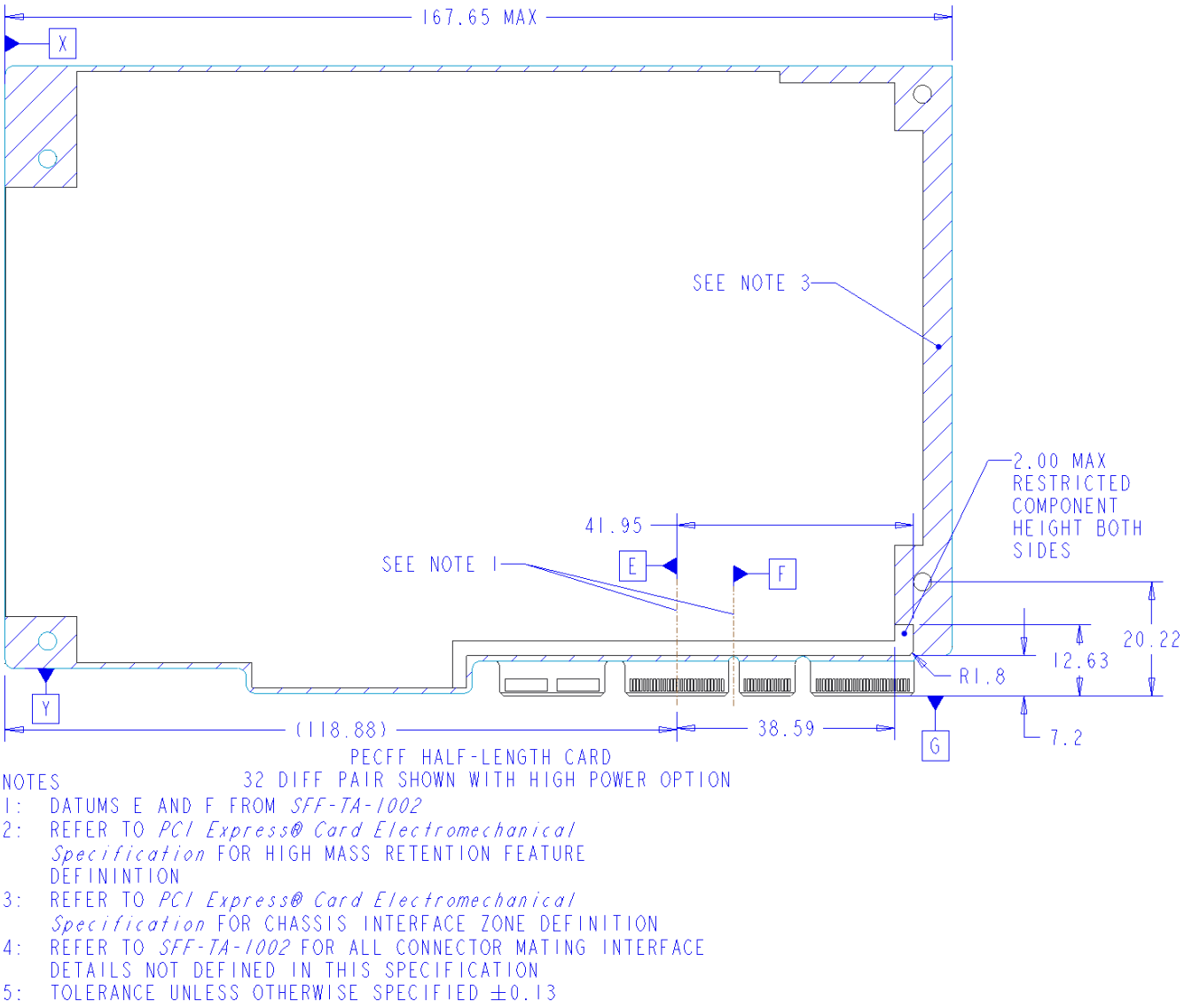


Figure 5-2. PECFF Full-length AIC without I/O Bracket



NOTES

1: DATUMS E AND F FROM *SFF-TA-1002*
2: REFER TO *PCI Express® Card Electromechanical Specification* FOR HIGH MASS RETENTION FEATURE DEFININTION
3: REFER TO *PCI Express® Card Electromechanical Specification* FOR CHASSIS INTERFACE ZONE DEFINITION
4: REFER TO *SFF-TA-1002* FOR ALL CONNECTOR MATING INTERFACE DETAILS NOT DEFINED IN THIS SPECIFICATION
5: TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.13

Figure 5-3. PECFF Half-length AIC without I/O Bracket

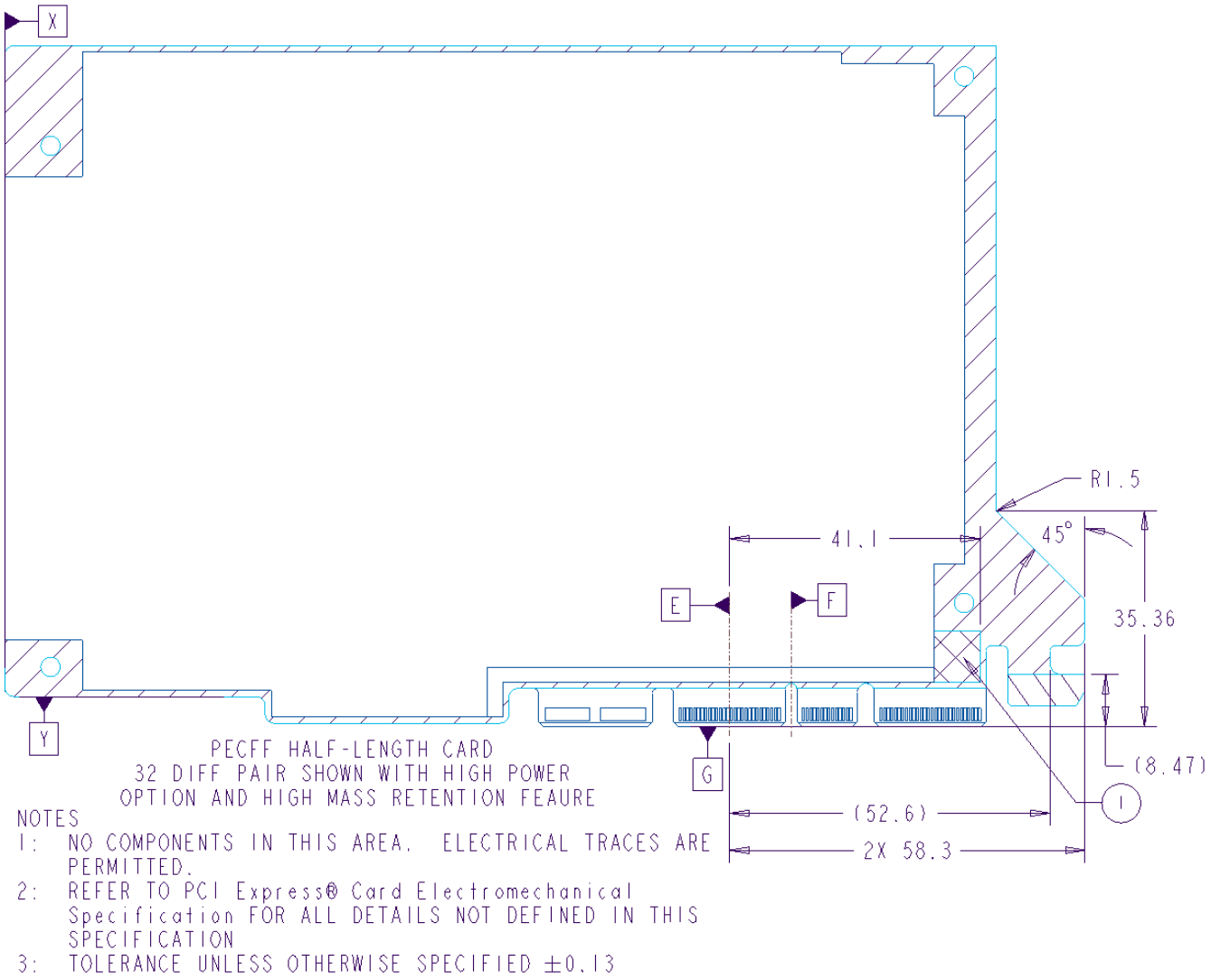


Figure 5-4. PECFF High-mass Half-length AIC without I/O Bracket

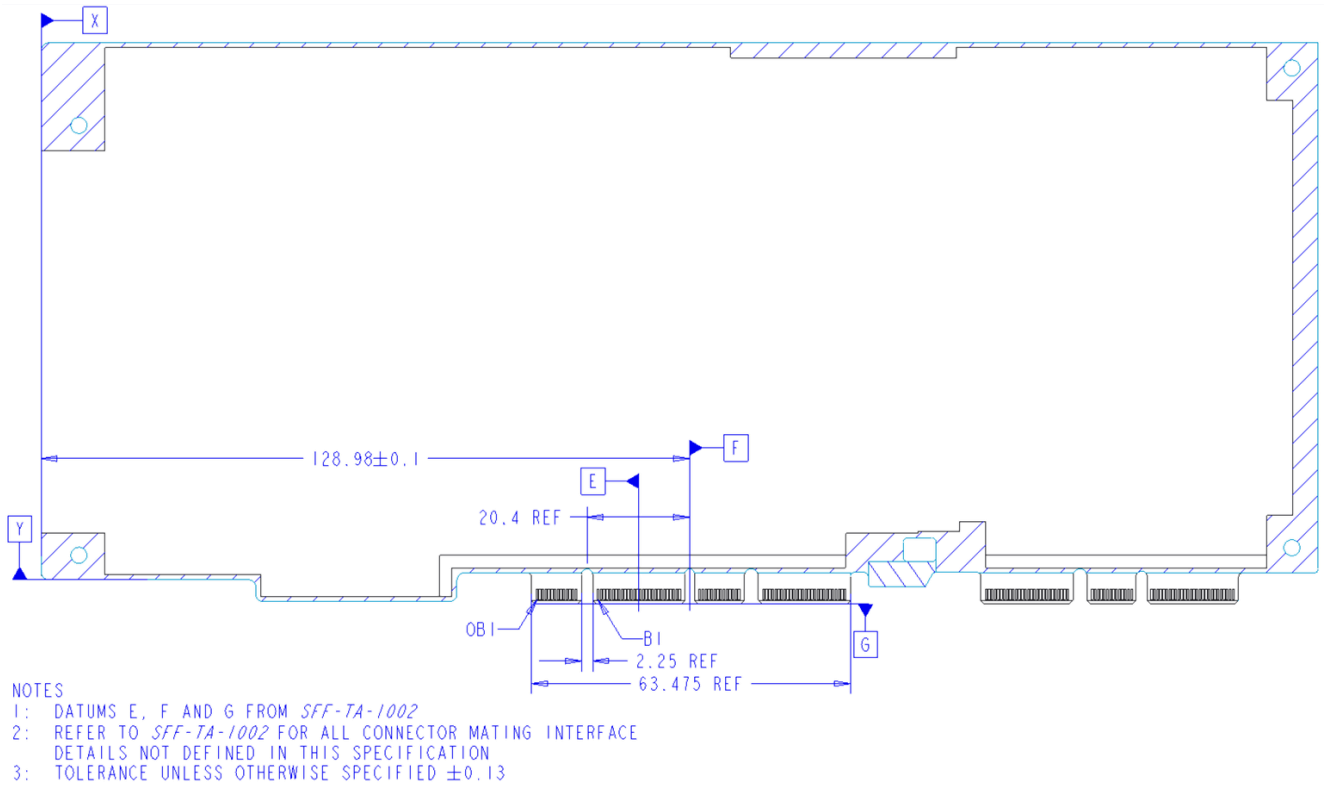
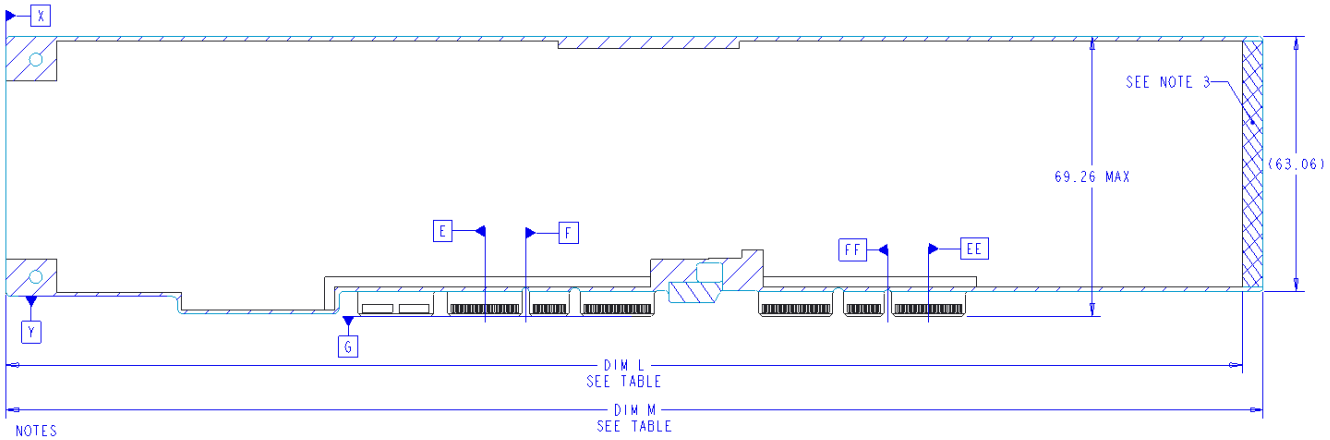


Figure 5-5. PECFF 4C+ AIC Variation without I/O Bracket

5.3. PECFF Low-Profile AIC



NOTES
1: DATUMS E AND F FROM *SFF-TA-1002*
2: REFER TO *PCI Express® Card Electromechanical Specification* FOR HIGH MASS RETENTION FEATURE DEFININTION
3: REFER TO *PCI Express® Card Electromechanical Specification* FOR CHASSIS INTERFACE ZONE DEFINITION
4: DATUMS EE AND FF CORRESPOND TO DATUMS E AND F RESPECTIVELY OF SECOND *SFF-TA-1002* CONNECTOR
5: REFER TO *PCI Express® Card Electromechanical Specification* FOR ALL CARD DETAILS NOT DEFINED IN THIS SPECIFICATION
6: REFER TO *SFF-TA-1002* FOR ALL CONNECTOR MATING INTERFACE DETAILS NOT DEFINED IN THIS SPECIFICATION
7: TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.13

LENGTH INTERVAL	DIM L	DIM M
HALF LENGTH	166.65	167.65 MAX
THREE-QUARTER LENGTH	248.92	254.00 MAX
FULL LENGTH	306.92	312.00 MAX

Figure 5-6. PECFF Low-profile AIC without I/O Bracket for 4C+ and 4C-HP Variations

5.4. PECFF I/O Bracket

PECFF uses a modified PCIe CEM I/O bracket to enable improved AIC stacking. Figure 5-8 illustrates the modified dimensions for the full height bracket and also applies to low profile brackets.

- The I/O bracket may be perforated for thermal enablement.

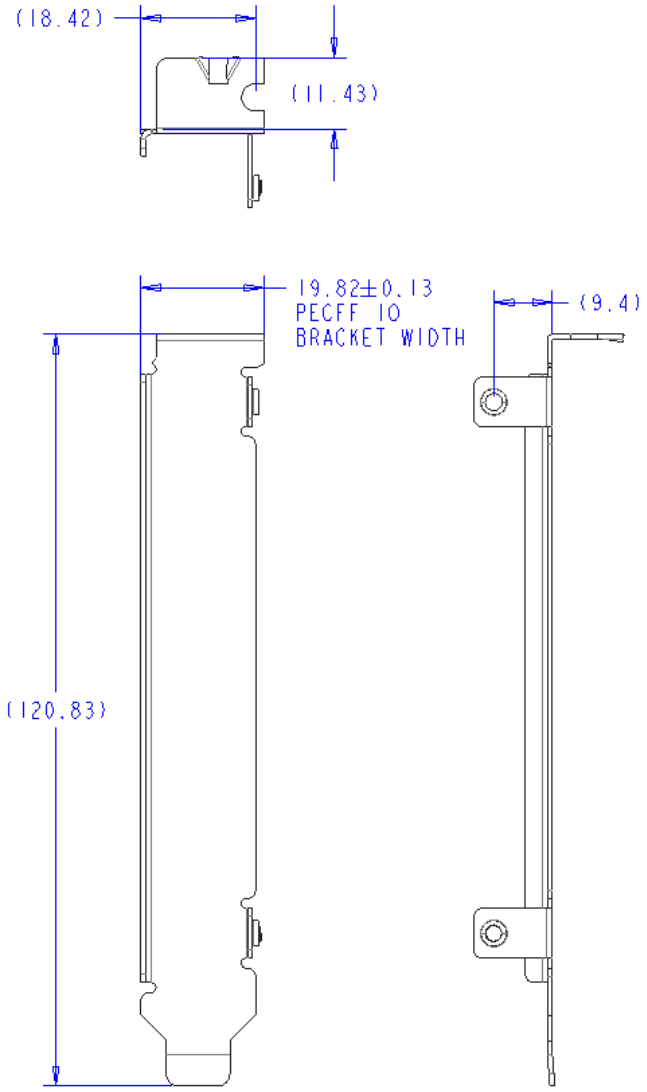


Figure 5-7. PECFF I/O Bracket – Full high and Low profile

6. PECFF Electrical Pinouts

The following specifies the connector pinouts for PECFF AICs.

- All side-band signals shall be as defined in the *PCI Express Card Electromechanical Specification*.
- 12V and 48V high-power pins shall be as specified in the *SFF-TA-1020.*
- GND pins shall be mating sequence one.
- PRSNT[1,2,3…]# mating sequence shall be as specified in *SFF-TA-1002*.
- Tx, Rx and REFCLK signals shall be mating sequence two.
- Non-TX or RX signals should follow the mating sequence illustrated in the following pinouts.
- Irrespective of the number of provisioned high-speed signals, to ensure proper mechanical alignment between the connector contacts and the AIC pads and to avoid AIC and system damage, a PECFF AIC shall support at least the full 1C AIC interface including board dimensions and plated pads as specified in *SFF-TA-1002*.
    - All unused high-speed signals shall be electrically disconnected.
- For pinouts of the PECFF 4C+ variation primary and secondary connectors refer to the *OCP NIC 3.0 Design Specification*
- MFG shall be used for manufacturing only. In manufacturing mode, the manufacturer may use MFG to convert a subset of pins to manufacturing functionality such as a JTAG interface. MFG functionality shall not be recoverable post manufacturing. This signal shall be Wake# post manufacturing.

Developers Notes:

- *A PECFF 4C+ AIC can interoperate with a PECFF 4C host slot and vice versa. It is up to the implementer to enable complete functionality through proper routing and multi-purposing of pins.*
- *A PECFF 4C+ AIC is keyed by the connector to prevent insertion into a 4C-HP connector. A PECFF 4C-HP AIC is keyed by the connector to prevent insertion into a 4C+ connector.*

Table 6-1. PECFF 12V PCIe Pinout for 2-64 Differential Pairs Configurations

PECFF 12V Pinouts

Connector (lower row)			Connector (upper row)		PECFF Variations								
Row	**Seq**	**Side B Signals**	**Side A Signals**	**Seq**									
H1	2	**12V High Power**	**12V High Power**	2	12V High Power Option								
H0	1	**GND**	**GND**	1									
		Key	**Key**										
1	2	**12V**	**GND**	1	2 Diff Pair PECFF	4 Diff Pair PECFF	8 Diff Pair PECFF	12 Diff Pair PECFF (16 Diff Pair w/ 4 Diff Pair Reserved)	16 Diff Pair PECFF	32 Diff Pair PECFF	40 Diff Pair PECFF	48 Diff Pair PECFF	64 Diff Pair PECFF
2	2	**12V**	**GND**	1									
3	2	**12V**	**GND**	1									
4	2	**12V**	**GND**	1									
5	2	**12V**	**GND**	1									
6	2	**12V**	**GND**	1									
7	2	**Wake#/MFG**	**SMCLK**	2									
8	2	**PWR_BREAK**	**SMDAT**	2									
9	2	**DualPortEn#**	**SMRST#/RFU**	2									
10	2	**PERST0#**	**Res**	2									
11	2	**3.3VAux**	**CLKREQ**	2									
12	2	**PWRDIS**	**PRSNT1#**	2									
13	1	**GND**	**GND**	1									
14	2	**REFCLKn0**	**REFCLKn1**	2									
15	2	**REFCLKp0**	**REFCLKp1**	2									
16	1	**GND**	**GND**	1									
17	2	**PETn0**	**PERn0**	2									
18	2	**PETp0**	**PERp0**	2									
19	1	**GND**	**GND**	1									
20	2	**PETn1**	**PERn1**	2									
21	2	**PETp1**	**PERp1**	2									
22	1	**GND**	**GND**	1									

23	2	PETn2	PERn2	2		
24	2	PETp2	PERp2	2		
25	1	GND	GND	1		
26	2	PETn3	PERn3	2		
27	2	PETp3	PERp3	2		
28	1	GND	GND	1		
		Key	Key			
29	1	GND	GND	1		
30	2	PETn4	PERn4	2		
31	2	PETp4	PERp4	2		
32	1	GND	GND	1		
33	2	PETn5	PERn5	2		
34	2	PETp5	PERp5	2		
35	1	GND	GND	1		
36	2	PETn6	PERn6	2		
37	2	PETp6	PERp6	2		
38	1	GND	GND	1		
39	2	PETn7	PERn7	2	RES	
40	2	PETp7	PERp7	2		
41	1	GND	GND	1		
42	2	PRSNT2#	Res	2		
		Key	Key			
43	1	GND	GND	1		
44	2	PETn8	PERn8	2		
45	2	PETp8	PERp8	2		
46	1	GND	GND	1		
47	2	PETn9	PERn9	2		
48	2	PETp9	PERp9	2		
49	1	GND	GND	1		
50	2	PETn10	PERn10	2		
51	2	PETp10	PERp10	2		
52	1	GND	GND	1		
53	2	PETn11	PERn11	2		
54	2	PETp11	PERp11	2		

55	1	GND	GND	1				
56	2	PETn12	PERn12	2				
57	2	PETp12	PERp12	2				
58	1	GND	GND	1				
59	2	PETn13	PERn13	2				
60	2	PETp13	PERp13	2				
61	1	GND	GND	1				
62	2	PETn14	PERn14	2				
63	2	PETp14	PERp14	2				
64	1	GND	GND	1				
65	2	PETn15	PERn15	2				
66	2	PETp15	PERp15	2				
67	1	GND	GND	1				
68	2	Res	Res	2				
69	2	Res	Res	2				
70	2	PRSNT_3C#	Res	2				

1	2	Res	Res	2
2	2	Res	Res	2
3	2	Res	Res	2
4	2	Res	Res	2
5	2	Res	Res	2
6	2	Res	Res	2
7	2	Res	Res	2
8	2	Res	Res	2
9	2	Res	Res	2
10	2	Res	Res	2
11	2	Res	Res	2
12	2	Res	PRSNT6#	2
13	2	Res	Res	2
14	2	Res	Res	2
15	2	Res	Res	2
16	1	GND	GND	1
17	2	PERn31	PETn31	2

18	2	**PERp31**	**PETp31**	2		
19	1	**GND**	**GND**	1		
20	2	**PERn30**	**PETn30**	2		
21	2	**PERp30**	**PETp30**	2		
22	1	**GND**	**GND**	1		
23	2	**PERn29**	**PETn29**	2		
24	2	**PERp29**	**PETp29**	2		
25	1	**GND**	**GND**	1		
26	2	**PERn28**	**PETn28**	2		
27	2	**PERp28**	**PETp28**	2		
28	1	**GND**	**GND**	1		
		Key	**Key**			
29	1	**GND**	**GND**	1		48 Diff Pair PECFF cont.
30	2	**PERn27**	**PETn27**	2		
31	2	**PERp27**	**PETp27**	2		
32	1	**GND**	**GND**	1		
33	2	**PERn26**	**PETn26**	2		
34	2	**PERp26**	**PETp26**	2		
35	1	**GND**	**GND**	1		
36	2	**PERn25**	**PETn25**	2		
37	2	**PERp25**	**PETp25**	2		
38	1	**GND**	**GND**	1		
39	2	**PERn24**	**PETn24**	2		
40	2	**PERp24**	**PETp24**	2		
41	1	**GND**	**GND**	1		
42	2	**PRSNT5#**	**Res**	2		
		Key	**Key**			

43	1	**GND**	**GND**	1			
44	2	**PERn23**	**PETn23**	2			
45	2	**PERp23**	**PETp23**	2			
46	1	**GND**	**GND**	1			
47	2	**PERn22**	**PETn22**	2			
48	2	**PERp22**	**PETp22**	2			
49	1	**GND**	**GND**	1			
50	2	**PERn21**	**PETn21**	2			
51	2	**PERp21**	**PETp21**	2			
52	1	**GND**	**GND**	1			
53	2	**PERn20**	**PETn20**	2			
54	2	**PERp20**	**PETp20**	2			
55	1	**GND**	**GND**	1			
56	2	**PERn19**	**PETn19**	2			
57	2	**PERp19**	**PETp19**	2			
58	1	**GND**	**GND**	1			
59	2	**PERn18**	**PETn18**	2			
60	2	**PERp18**	**PETp18**	2			
61	1	**GND**	**GND**	1			
62	2	**PERn17**	**PETn17**	2			
63	2	**PERp17**	**PETp17**	2			
64	1	**GND**	**GND**	1			
65	2	**PERn16**	**PETn16**	2			
66	2	**PERp16**	**PETp16**	2			
67	1	**GND**	**GND**	1			
68	2	**Res**	**Res**	2			
69	2	**Res**	**Res**	2			
70	2	**PRSNT4#**	**Res**	2			

40 Diff Pair PECFF cont.

48 Diff Pair PECFF cont.

Table 6-2. PECFF 48V Pinout for 2-64 Differential Pairs Configurations

PECFF 48V Pinouts

Connector (lower row)			Connector (upper row)		PECFF Variations							
Row	**Seq**	**Side B Signals**	**Side A Signals**	**Seq**	2 Diff Pair 48V PECFF	4 Diff Pair 48V PECFF	8 Diff Pair 48V PECFF	12 Diff Pair PECFF (16 Diff Pair w/ 4 Diff Pair Reserved)	16 Diff Pair 48V PECFF	32 Diff Pair 48V PECFF	40 Diff Pair 48V PECFF	48 Diff Pair 48V PECFF	64 Diff Pair 48V PECFF
H1	2	**48V High Power**	**48V High Power**	2									
H0	1	**GND**	**GND**	1									
		Key	**Key**										
1	2	**Res**	**Res**	1									
2	2	**Res**	**Res**	1									
3	2	**Res**	**Res**	1									
4	2	**Res**	**Res**	1									
5	2	**Res**	**Res**	1									
6	2	**Res**	**Res**	1									
7	2	**Wake#/MFG**	**SMCLK**	2									
8	2	**PWR_BREAK**	**SMDAT**	2									
9	2	**DualPortEn#**	**SMRST#/RFU**	2									
10	2	**PERST0#**	**Res**	2									
11	2	**3.3VAux**	**CLKREQ**	2									
12	2	**PWRDIS**	**PRSNT1#**	2									
13	1	**GND**	**GND**	1									
14	2	**REFCLKn0**	**REFCLKn1**	2									
15	2	**REFCLKp0**	**REFCLKp1**	2									
16	1	**GND**	**GND**	1									
17	2	**PETn0**	**PERn0**	2									
18	2	**PETp0**	**PERp0**	2									
19	1	**GND**	**GND**	1									
20	2	**PETn1**	**PERn1**	2									
21	2	**PETp1**	**PERp1**	2									
22	1	**GND**	**GND**	1									

23	2	PETn2	PERn2	2								
24	2	PETp2	PERp2	2								
25	1	GND	GND	1								
26	2	PETn3	PERn3	2								
27	2	PETp3	PERp3	2								
28	1	GND	GND	1								
		Key	Key									
29	1	GND	GND	1								
30	2	PETn4	PERn4	2								
31	2	PETp4	PERp4	2								
32	1	GND	GND	1								
33	2	PETn5	PERn5	2								
34	2	PETp5	PERp5	2								
35	1	GND	GND	1								
36	2	PETn6	PERn6	2								
37	2	PETp6	PERp6	2								
38	1	GND	GND	1								
39	2	PETn7	PERn7	2								
40	2	PETp7	PERp7	2								
41	1	GND	GND	1								
42	2	PRSNT2#	Res	2								
		Key	Key									
43	1	GND	GND	1								
44	2	PETn8	PERn8	2								
45	2	PETp8	PERp8	2								
46	1	GND	GND	1								
47	2	PETn9	PERn9	2								
48	2	PETp9	PERp9	2								
49	1	GND	GND	1								
50	2	PETn10	PERn10	2								
51	2	PETp10	PERp10	2								
52	1	GND	GND	1								
53	2	PETn11	PERn11	2								
54	2	PETp11	PERp11	2								

RES

55	1	GND	GND	1					
56	2	PETn12	PERn12	2					
57	2	PETp12	PERp12	2					
58	1	GND	GND	1					
59	2	PETn13	PERn13	2					
60	2	PETp13	PERp13	2					
61	1	GND	GND	1					
62	2	PETn14	PERn14	2					
63	2	PETp14	PERp14	2					
64	1	GND	GND	1					
65	2	PETn15	PERn15	2					
66	2	PETp15	PERp15	2					
67	1	GND	GND	1					
68	2	Res	Res	2					
69	2	Res	Res	2					
70	2	PRSNT_3C#	Res	2					
1	2	Res	Res	2					
2	2	Res	Res	2					
3	2	Res	Res	2					
4	2	Res	Res	2					
5	2	Res	Res	2					
6	2	Res	Res	2					
7	2	Res	Res	2					
8	2	Res	Res	2					
9	2	Res	Res	2					
10	2	Res	Res	2					
11	2	Res	Res	2					
12	2	Res	PRSNT6#	2					
13	2	Res	Res	2					
14	2	Res	Res	2					
15	2	Res	Res	2					
16	1	GND	GND	1					
17	2	PERn31	PETn31	2					

18	2	**PERp31**	**PETp31**	2		
19	1	**GND**	**GND**	1		
20	2	**PERn30**	**PETn30**	2		
21	2	**PERp30**	**PETp30**	2		
22	1	**GND**	**GND**	1		
23	2	**PERn29**	**PETn29**	2		
24	2	**PERp29**	**PETp29**	2		
25	1	**GND**	**GND**	1		
26	2	**PERn28**	**PETn28**	2		
27	2	**PERp28**	**PETp28**	2		
28	1	**GND**	**GND**	1		
		Key	**Key**			
29	1	**GND**	**GND**	1		48 Diff Pair 48V PECFF cont.
30	2	**PERn27**	**PETn27**	2		
31	2	**PERp27**	**PETp27**	2		
32	1	**GND**	**GND**	1		
33	2	**PERn26**	**PETn26**	2		
34	2	**PERp26**	**PETp26**	2		
35	1	**GND**	**GND**	1		
36	2	**PERn25**	**PETn25**	2		
37	2	**PERp25**	**PETp25**	2		
38	1	**GND**	**GND**	1		
39	2	**PERn24**	**PETn24**	2		
40	2	**PERp24**	**PETp24**	2		
41	1	**GND**	**GND**	1		
42	2	**PRSNT5#**	**Res**	2		
		Key	**Key**			

43	1	**GND**	**GND**	1		40 Diff Pair 40 PECFF cont.	48 Diff Pair 48V PECFF cont.
44	2	**PERn23**	**PETn23**	2			
45	2	**PERp23**	**PETp23**	2			
46	1	**GND**	**GND**	1			
47	2	**PERn22**	**PETn22**	2			
48	2	**PERp22**	**PETp22**	2			
49	1	**GND**	**GND**	1			
50	2	**PERn21**	**PETn21**	2			
51	2	**PERp21**	**PETp21**	2			
52	1	**GND**	**GND**	1			
53	2	**PERn20**	**PETn20**	2			
54	2	**PERp20**	**PETp20**	2			
55	1	**GND**	**GND**	1			
56	2	**PERn19**	**PETn19**	2			
57	2	**PERp19**	**PETp19**	2			
58	1	**GND**	**GND**	1			
59	2	**PERn18**	**PETn18**	2			
60	2	**PERp18**	**PETp18**	2			
61	1	**GND**	**GND**	1			
62	2	**PERn17**	**PETn17**	2			
63	2	**PERp17**	**PETp17**	2			
64	1	**GND**	**GND**	1			
65	2	**PERn16**	**PETn16**	2			
66	2	**PERp16**	**PETp16**	2			
67	1	**GND**	**GND**	1			
68	2	**Res**	**Res**	2			
69	2	**Res**	**Res**	2			
70	2	**PRSNT4#**	**Res**	2			

7. AIC-to-AIC Cabling

Multiple PECFF AICs may be interconnected using cables that are attached across the AIC top edge.

- Each Cable supports up to 16 differential pairs.
- Each Cable may be partitioned into multiple electrical links
- Each Cable may support a vendor-defined physical layer and / or protocol.
- A half-length AIC may support Cables 1, 2 and 5, 6.
- A three-quarter-length AIC may support Cables 1 through 6.
- A full-length AIC may support Cables 1 through 8.
- Cables shall be populated in numerical order.
- Cables shall be positioned to optimize routing and signaling integrity between the device component and the gold finger interface.
- System boards should be designed to enable cabled AICs to be adjacent to one another.

The following figures specify the high-speed signal gold finger connections for each AIC length and the form factor areas that may be used for implementing cable mechanical attachment. If an AIC does not support AIC-to-AIC cabling, then these form factor areas may be used for non-cable purposes.

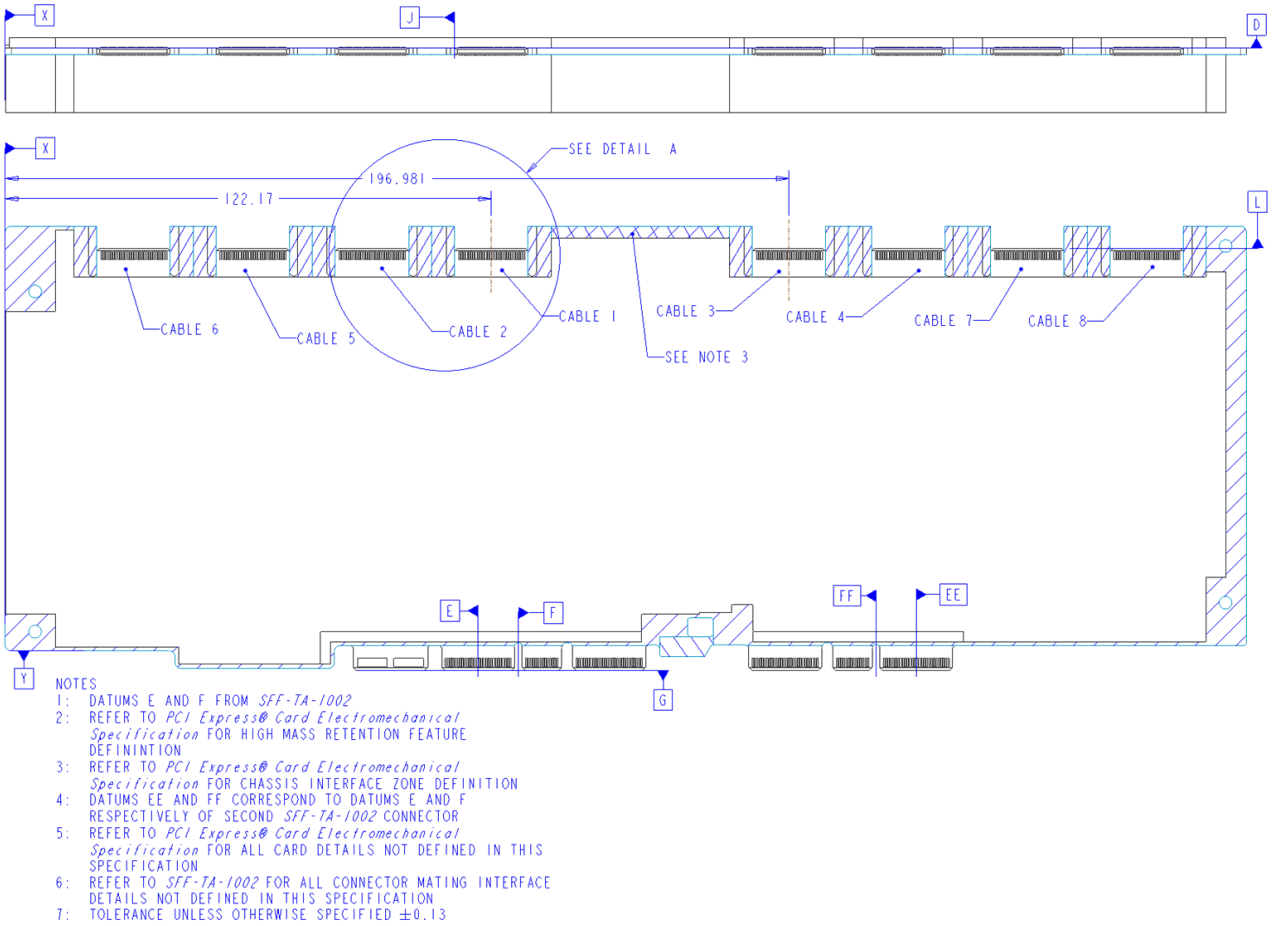


Figure 7-1. PECFF AIC-to-AIC Cabling Definition (Full-length PECFF Illustrated)

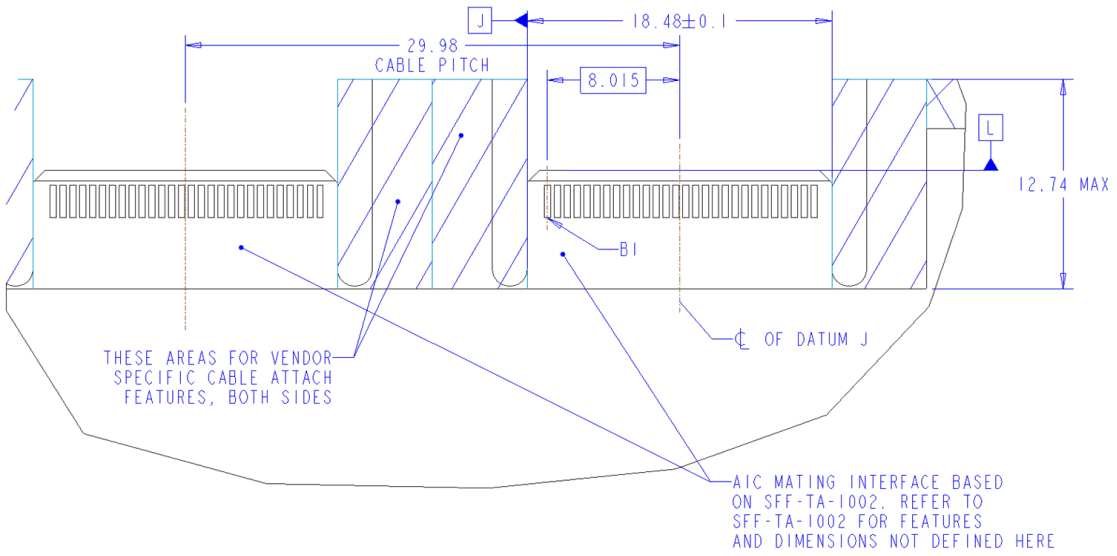


Figure 7-2. Detail A – PECFF AIC-to-AIC Cabling Interface Based on SFF-TA-1002

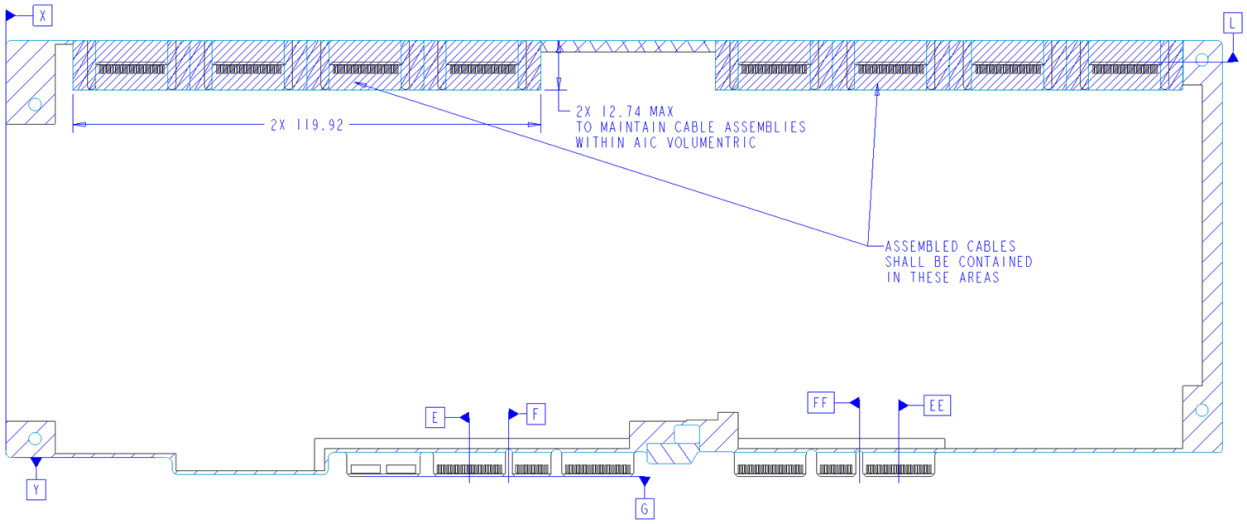


Figure 7-3. PECFF Cable Assembly Keep-in

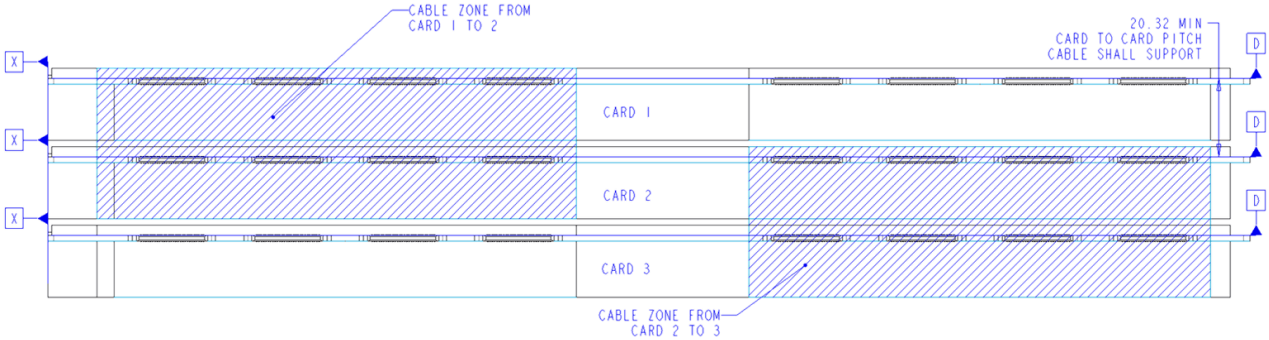


Figure 7-4. Minimum Pitch for PECFF AIC-to-AIC Cabling

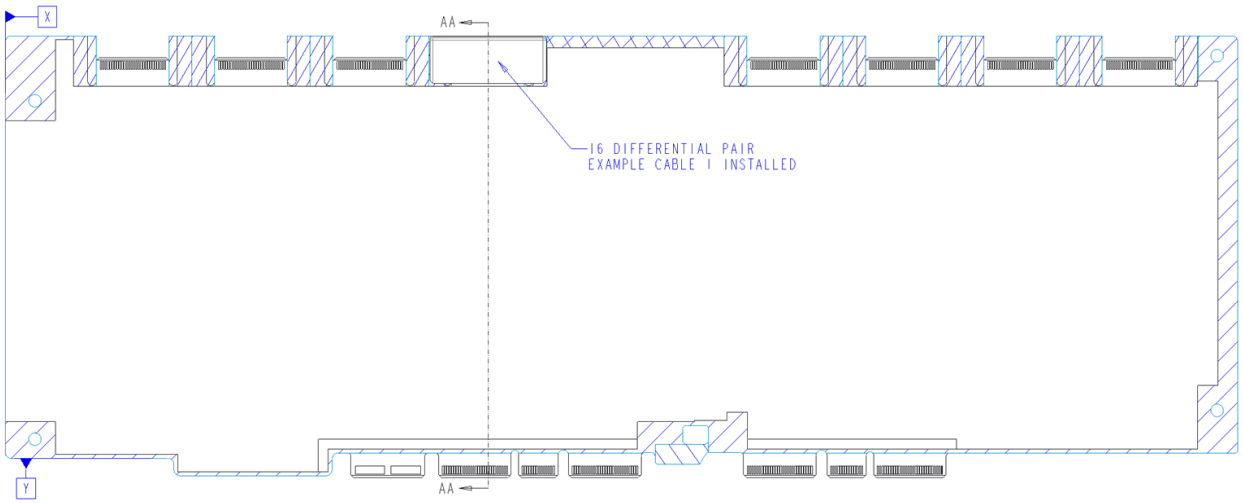


Figure 7-5. Example 16 Differential Pair Cable Attached

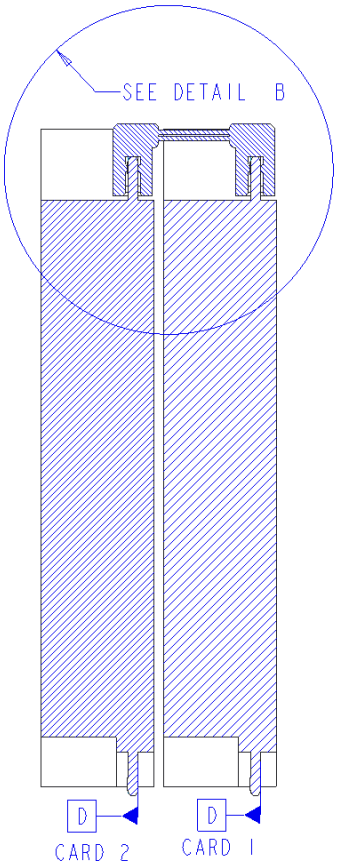


Figure 7-6. Cross Section A Through Two Mated Cards

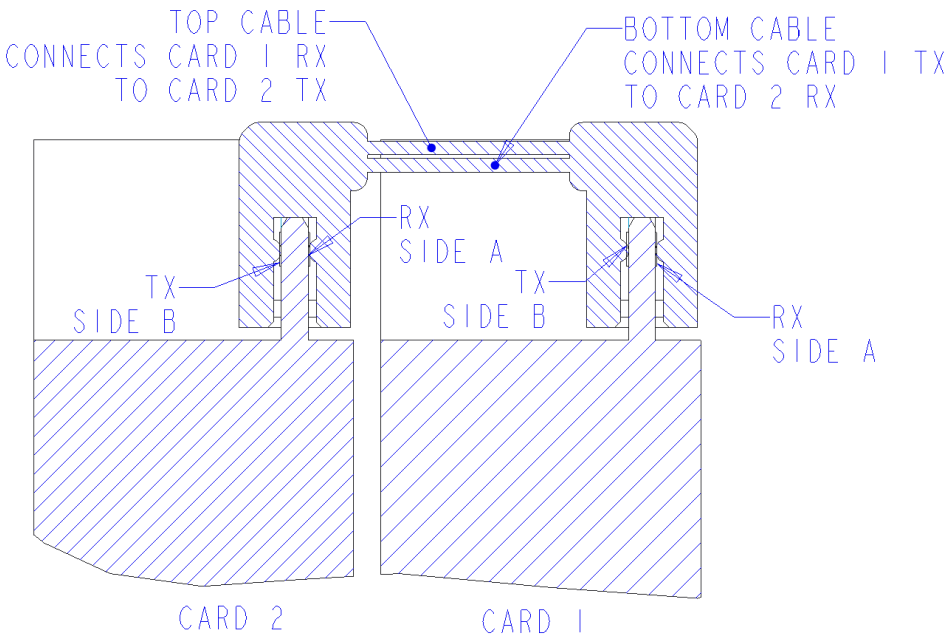


Figure 7-7. Detail B–Tx and Rx Connections Through Cable

Figure 7-1 specifies the pinout for the cable and gold finger interface.

- This pinout applies to Cables 1 through 8 with PRSNTC[0,…7] 0# assigned respectively.
- VEN_DEF pins are for vendor-defined functions. If unused, these signals shall be electrically disconnected.
- The pinouts illustrate the Tx and Rx assignments for symmetric transmission.
- Signals are defined from the AIC perspective, using the views illustrated in *Minimum Pitch for PECFF AIC-to-AIC Cabling* and *Detail B–Tx and Rx Connections Through Cable* for reference, in which Tx pins on the AIC in slot 1 connect to corresponding Rx pins on the AIC in slot 2, and Rx pins on AIC in slot 1 connect to corresponding Tx pins on AIC in slot 2. Tx and Rx signal and functional requirements are vendor-defined.

Table 7-1. PECFF AIC-to-AIC Cable Pinout

Row	Seq	Side B Signals	Side A Signals	Seq
B1	2	VEN_DEF	VEN_DEF	2
B2	2	VEN_DEF	VEN_DEF	2
B3	2	VEN_DEF	PRSNTC[0, 1, 2, 3, 4, 5, 6, 7]_0#	2
B4	1	GND	GND	1
B5	2	TXn0	RXn0	2
B6	2	TXp0	RXp0	2
B7	1	GND	GND	1
B8	2	TXn1	RXn1	2
B9	2	TXp1	RXp1	2
B10	1	GND	GND	1

B11	2	**TXn2**	**RXn2**	2
B12	2	**TXp2**	**RXp2**	2
B13	1	**GND**	**GND**	1
B14	2	**TXn3**	**RXn3**	2
B15	2	**TXp3**	**RXp3**	2
B16	1	**GND**	**GND**	1
B17	2	**TXn4**	**RXn4**	2
B18	2	**TXp4**	**RXp4**	2
B19	1	**GND**	**GND**	1
B20	2	**TXn5**	**RXn5**	2
B21	2	**TXp5**	**RXp5**	2
B22	1	**GND**	**GND**	1
B23	2	**TXn6**	**RXn6**	2
B24	2	**TXp6**	**RXp6**	2
B25	1	**GND**	**GND**	1
B26	2	**TXn7**	**RXn7**	2
B27	2	**TXp7**	**RXp7**	2
B28	1	**GND**	**GND**	1

Appendix A. PCB Footprints

All material within this section, whether defined as normative or informative, is subject to IP disclosure and RAND terms by SNIA SFF TA TWG member companies. The following footprint is provided for reference and illustrates the position of the high mass retention connector relative to the *SFF-TA-1002* connectors and recommended placement of the second 4C connector. For dimensions not illustrated in this drawing refer to *SFF-TA-1002* and *SFF-TA-1020*.

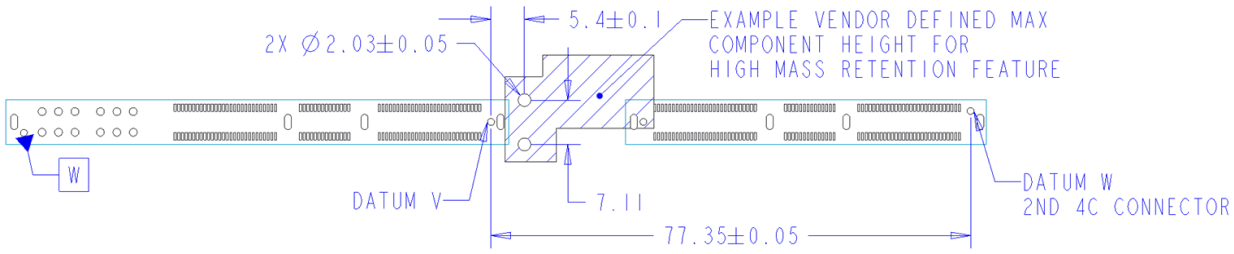


Figure A-1. Recommended PECFF Footprint with Optional High-mass Retention and 4C-HP Connector

Refer to *SFF-TA-1002* for 4C+ recommended footprint dimensions.