

DRILL CHART						
TOOL #	QUANTITY	DRILLING DIA TOL	FINISHED DIA TOL	PLATING	TYPE	NOTES
2	178	0.2032±0.025	A/R	YES	HOLE	△8
3	716	0.254±0.025	A/R	YES	HOLE	△8
4	280	0.3±0.03	A/R	YES	HOLE	△8
5	80	1.75±0.05	1.65±0.05	YES	HOLE	△8
6	2	2.4±0.05	A/R	YES	HOLE	△8

IMPEDANCE CHART						
SIGNAL LAYERS	TRACE GEOMETRY	REF LAYER	TRACE WIDTH TOLERANCE	IMP	IMP TYPE	IMP TOL
LAYER 2	0.1905	1/3	±10%	42.5	SE	±5%
LAYER 7	0.1905	6/8	±10%	42.5	SE	±5%
TOP LAYER	0.2794-0.1524-0.165-0.1524-0.2794	2	±10%	90	DIFF	±5%
BOTTOM LAYER	0.2794-0.1524-0.165-0.1524-0.2794	7	±10%	90	DIFF	±5%

NOTES

- FABRICATE PER ANSI/IPC-6012B CLASS 2 (GENERAL INDUSTRY).
- UPON RECEIPT OF PURCHASE ORDER CONFIRM DELIVERY ADDRESS.
- SUPPLIED ARTWORK IS NON-COMPENSATED. ARTWORK COMPENSATION FOR MANUFACTURING PROCESSES IS PERMITTED, PROVIDED FINISHED PRODUCT MATCHES INITIAL ARTWORK. ANY DEVIATION OUTSIDE OF TOLERANCE FOR FINISHED PRODUCT, ARTWORK, DIELECTRIC THICKNESS, OR OTHER BOARD CHARACTERISTICS SPECIFIED IN THIS FABRICATION PACKAGE MUST BE APPROVED BY TE ENGINEERING PRIOR TO IMPLEMENTATION.
- MANUFACTURER SHALL NOT REMOVE NON-FUNCTIONAL PADS.
- ROBBER PATTERNS ARE NOT PERMITTED. IF FABRICATOR BELIEVES ROBBER PATTERS ARE REQUIRED, CONTACT ENGINEERING FOR MODIFICATIONS.
- THIS OUTLINE LAYER IS NON-COMPENSATED FOR BIT WIDTH AND SHOULD REPRESENT THE FINISHED EDGE OF THE BOARD.
- GERBER FILE 'SFF-TA-1002\_SM\_4C\_REV1' MUST BE USED TO MANUFACTURE THIS PART.
- PACKAGE CONTAINS ONE SET WITH 2 PIECES. MULTIPLE SETS MAY BE ARRAYED ON 1 PANEL. SETS CAN BE SPLIT ACROSS PANELS

- SIGNAL IMPEDANCES SHALL BE AS SPECIFIED. ENGINEERING APPROVAL IS REQUIRED IF MANUFACTURER MUST CHANGE BOARD GEOMETRY BEYOND MANUFACTURING TOLERANCES.
- INDIVIDUAL PCB'S MUST BE ROTATED 12.7 DEGREES PRIOR TO PANELIZATION

FINAL BOARD FINISH: ENIG  
GOLD AND ELECTROLESS NICKEL TO MEET IPC-4552 MINIMUMS OR GOLD FLASH 0.00008-0.00018  
OVER 0.00381-0.00635 ELECTROLYTIC NICKEL PER ASTM-B-689 TYPE 2. MUST MEET SOLDERABILITY PER  
DEFAULT REQUIREMENTS OF JEDEC JESD22-B102D, METHOD1, FOR LEAD-FREE SOLDER.

SILKSCREEN USING PERMANENT, NONCONDUCTIVE, WHITE EPOXY INK.  
SILKSCREEN SHOULD NOT EXTEND ONTO FUNCTIONAL LANDS OR PADS.

SOLDERMASK PER IPC-SM-840, CLASS H <LPI> COLOR GREEN

LAMINATES SHALL BE NELCO N4000-13SI MATERIAL, AND NOT INCLUDE #106 OR #1080 GLASS IN BETWEEN LAYER 1-2, 2-3, 6-7, AND 7-8.

MANUFACTURER SHALL MARK EACH PIECE WITH 2 DISTINCT WHITE EPOXY MARKINGS:  
DATE OF MANUFACTURE (YYWW) PER MIL-STD-1285 AND VENDOR NAME OR LOGO.

COPPER PLATING SHALL HAVE A MINIMUM THICKNESS OF 0.0254 IN HOLES.

17 N/A

CARBON DIOXIDE LASER DRILL FROM SPECIFIED SIDE, LAYER CONTROLLED DRILLING. LASER DEPTH NOT TO EXTEND BEYOND TARGET LAYER PAD. SPECIFIED SIZES ARE DRILL AND NOT FINISHED HOLE SIZES

VIA FILL IS REQUIRED. VIAS MUST BE COMPLETELY FILLED WITH A 100% NON-CONDUCTIVE SOLID FILL MATERIAL. THE CORRESPONDING SIDE SHALL BE PLANARIZED AND PLATED OVER WITH COPPER AND SURFACE FINISH. THE OPPOSITE SIDE MAY BE PLANARIZED BUT SHALL NOT BE OVERPLATED. THE PLATED CAP MUST ADHERE TO THE FILL MATERIAL AFTER 550 DEGREE FARENHEIGHT SOLDER SHOCK.

MATING INTERFACE GOLD PADS TO BE PLATED WITH MINIMUM OF 0.000762 (30 MICROINCHES) OF GOLD OVER A MINIMUM OF 0.00381 (150 MICROINCHES) OF NICKEL.

NETLIST TEST 100% FOR CONTINUITY AND ISOLATION USING IPC-D-356A NETLIST SUPPLIED WITH FABRICATION PACKAGE. CERTIFICATION REQUIRED.

SUPPLY IMPEDANCE TESTING REPORT FOR EACH SIGNAL LAYER. CERTIFICATION REQUIRED.

23 N/A

24 NOTIFY ENGINEERING PRIOR TO SHIPMENT WITH TRACKING INFORMATION.

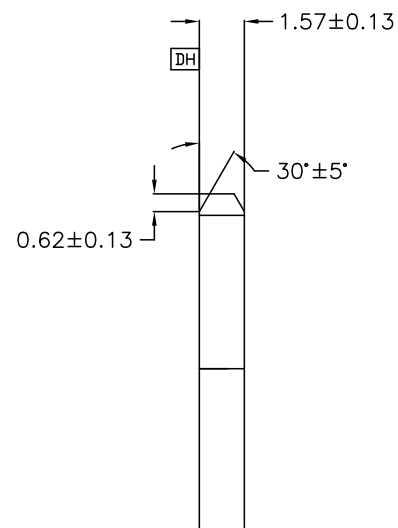
BOARD EDGE TO BE FREE OF SHARPNESS AND BURRS. SURFACE ROUGHNESS OF BEVELED LEAD-IN NOT TO EXCEED 125 MICRO-INCHES. CHAMFER IS NOT PERMITTED TO IMPACT OR DISTURB CONTACT PADS. ANY MACHINING OF CONTACTS PADS IS REJECTABLE CONDITION AND WILL BE CONSIDERED NON-COMPLIANT

PCB STACKUP				
△4 DIELECTRIC THICKNESS	CROSS SECTION	Cu OZ	DESCRIPTION	FILE NAME
OVERALL THICKNESS 1.57±0.13			PRIMARY SIDE FINISH: ENIG △1	
			PRIMARY SIDE SILKSCREEN △2	SFF-TA-1002_SM_4C.GTO
			PRIMARY SIDE SOLDERMASK △3	SFF-TA-1002_SM_4C.GTS
		0.5	PRIMARY SIDE	SFF-TA-1002_SM_4C.GTL
0.127±0.025		0.5	L2_SIGNAL △9	SFF-TA-1002_SM_4C.G1
0.1524±0.025		0.5	L3_GND	SFF-TA-1002_SM_4C.G2
REF		0.5	L4_GND	SFF-TA-1002_SM_4C.G3
0.0762±0.025		0.5	L5_GND	SFF-TA-1002_SM_4C.G4
REF		0.5	L6_GND	SFF-TA-1002_SM_4C.G5
0.1524±0.025		0.5	L7_SIGNAL △9	SFF-TA-1002_SM_4C.G6
0.127±0.025		0.5	SECONDARY SIDE	SFF-TA-1002_SM_4C.GBL
			SECONDARY SIDE SOLDERMASK △3	SFF-TA-1002_SM_4C.GBS
			SECONDARY SIDE SILKSCREEN △2	SFF-TA-1002_SM_4C.GBO
			SECONDARY SIDE FINISH: ENIG △1	
			OUTLINE △6	SFF-TA-1002_SM_4C.GM1
			VIA FILL PRIMARY SIDE △9	SFF-TA-1002_SM_4C.GM6
			VIA FILL SECONDARY SIDE △9	SFF-TA-1002_SM_4C.GM7
			EXCELLON DRILL- THRU HOLE △6	SFF-TA-1002_SM_4C.TXT
			PRIMARY SIDE MICRO-VIA TO L2 △8	SFF-TA-1002_SM_4C.TX1
			SECONDARY SIDE MICRO-VIA TO L7 △8	SFF-TA-1002_SM_4C.TX2
			NETLIST △1	SFF-TA-1002_SM_4C.IPC

						DIMENSIONS: mm		TOLERANCES UNLESS OTHERWISE SPECIFIED:		DWN	MATERIAL	HEAT TREAT
						0 PL C ± .05		1 PL C ± .05		CHK		
						2 PL C ± .05		3 PL C ± .05		APVD		
						4 PL C ± .05				NAME	PRINTED CIRCUIT BOARD, TEST FIXTURE	
										SCALE	SIZE	DRAWING NO
										2:1	A1	SFF-TA-1002 SM 4C
										SHEET	OF	REV
										1	4	1



						DIMENSIONS:		TOLERANCES, UNLESS OTHERWISE SPECIFIED:		CHK				
						mm				APVD				
								0 PLC ± .05 1 PLC ± .05 2 PLC ± .05 3 PLC ± .05 4 PLC ± .05						
- SEE SHEET 1						- - -				NAME		PRINTED CIRCUIT BOARD, TEST FIXTURE SFF-TA-1002 STRADDLE MOUNT 4C		
P	LTR	REVISION RECORD		DATE	DWN	APVD	ANGLES± - SURFACE TEXTURE		SCALE 2:1	SIZE A1	DRAWING NO SFF-TA-1002 SM 4C	SHEET 3	OF 4	REV 1



3308-8 (1/15)