# SFF-TA-1015

Specification for

# Fabric Device Pinout Specification

Rev 1.0 March 05, 2019

SECRETARIAT: SFF TA TWG

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The description of the connector in this specification does not assure that the specific component is available from connector suppliers. If such a connector is supplied, it must comply with this specification to achieve interoperability between suppliers.

ABSTRACT: This specification defines the Fabric Device signal list, connector pinout and VPD EEPROM definition.

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**Foreword**

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at http://www.snia.org/sff/join.

**Revision History**

**Rev 1.0** *March 05, 2019*:
- Initial approved release of document
- Fabric Device Pinout Specification

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# 1. Scope

This specification defines the Fabric Device Pinout Specification. This document comvers the signal list, signal definitions and connector pinout.

# 2. References and Conventions

## 2.1 Industry Documents

- ENG-46158 Serial-GMII Specification
- IEEE Std 1149.1 IEEE Standard Test Access Port and Boundary-Scan Architecture
- REF-TA-1011 Cross Reference to Select SFF Connectors
- SFF-8679 QSFP+ 4X Hardware and Electrical Specification
- SFF-TA-1014 Fabric Attached Devices Connector Specification
- SPRUGP1 Universal Asynchronous Receiver/Transmitter (UART)
- UM10204 I2C-bus Specification and user manual

## 2.2 Sources

The complete list of SFF documents which have been completed, are currently being worked on, or that have been expired by the SFF Committee can be found at http://www.snia.org/sff/specifications. Suggestions for improvement of this specification will be welcome, they should be submitted to http://www.snia.org/feedback.

Copies of ANSI standards may be obtained from the InterNational Committee for Information Technology Standards (http://www.techstreet.com/incitsgate.tmpl).

Copies of PCIe standards may be obtained from PCI-SIG (http://pcisig.com).

Copies of InfiniBand standards may be obtained from the InfiniBand Trade Association (IBTA) (http://www.infinibandta.org).

Copies of IEEE standards may be obtained from the Institute of Electrical and Electronics Engineers (IEEE) (https://www.ieee.org).

Copies of SAS standards may be obtained from the International Committee for Information Technology Standards (INCITS) (http://www.incits.org).

Copies of JEDEC standards may be obtained from the Joint Electron Device Engineering Council (https://www.jedec.org).

Copies of OIF Implementation Agreements may be obtained from the Optical Internetworking Forum (http://www.oiforum.com).

Copies of ASME standards may be obtained from the American Society of Mechanical Engineers (https://www.asme.org).

Copies of Electronic Industries Alliance (EIA) standards may be obtained from the Electronic Components Industry Association (ECIA) (https://www.ecianow.org).

## 2.3 Conventions

The following conventions are used throughout this document:

**DEFINITIONS**
Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

**ORDER OF PRECEDENCE**
If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

**LISTS**
Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a. red (i.e., one of the following colors):
    A. crimson; or
    B. pink;
b. blue; or
c. green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1. top;
2. middle; and
3. bottom.

Lists are associated with an introductory paragraph or phrase, and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

**DIMENSIONING CONVENTIONS**
The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

**NUMBERING CONVENTIONS**
The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

| American | French | ISO |
|---|---|---|
| 0.6 | 0,6 | 0.6 |
| 1,000 | 1 000 | 1 000 |
| 1,323,462.9 | 1 323 462,9 | 1 323 462.9 |

# 3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

## 3.1 Keywords

**May/ may not:** A keyword that indicates flexibility of choice with no implied preference.

**Obsolete:** A keyword indicating that an item was defined in prior specifications but has been removed from this specification.

**Optional:** A keyword that describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

**Prohibited:** A keyword used to describe a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

**Reserved:** A keyword used for defining the signal on a connector contact [when] its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

**Restricted:** A keyword referring to features, bits, bytes, words, and fields that are set aside for other identified standardization purposes. A restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word or field in the context where the restricted designation appears.

**Shall:** A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

**Should:** A keyword indicating flexibility of choice with a strongly preferred alternative.

**Vendor specific:** A keyword indicating something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

## 3.2 Acronyms and Abbreviations

**RO:** Read Only
**RX:** Receiver
**TX:** Transmitter
**VPD:** Vital Product Data

### 3.3 Definitions

**Module:** In this specification, module refers to an assembly that is terminated at the end of a direct attach copper (DAC) or an active optical cable (AOC), intended to mate to a device.

**Termination:** A term used to describe a connector's non-separable attachment point such as [a connector contact to a bulk cable/ a cage to a PCB or flex circuit/ bulk cable to a PCB or flex circuit/ solder tail to PCB]. Common PCB terminations include: surface mount (SMT), plated through hole termination (PTH), and press fit (PF). Common cable terminations include insulation displacement contact (IDC), insulation displacement termination (IDT), wire slots, solder, welds, crimps, and brazes.

# 4. Signal List

The signal summary, definitions and signal placement for the Fabric Device connector are detailed in this section. All signals listed are presented relative to the Fabric Device, IN is an input to the Fabric Device, OUT is an output from the Fabric Device, RX is an input to the Fabric Device and TX is an output from the Fabric Device.

**Table 4-1 Signal List**

| Interface | Signal Name | Fabric Device I/O | Function |
|---|---|---|---|
| Power and Ground | 12V | I | 12V Source |
| | GND | I | Return Current Path |
| High Speed Data | PORT_A_1P_IN | I | Port A High Speed Data differential inputs |
| | PORT_A_1N_IN | I | |
| | PORT_A_2P_IN | I | |
| | PORT_A_2N_IN | I | |
| | PORT_A_3P_IN | I | |
| | PORT_A_3N_IN | I | |
| | PORT_A_4P_IN | I | |
| | PORT_A_4N_IN | I | |
| | PORT_B_1P_IN | I | Port B High Speed Data differential inputs |
| | PORT_B_1N_IN | I | |
| | PORT_B_2P_IN | I | |
| | PORT_B_2N_IN | I | |
| | PORT_B_3P_IN | I | |
| | PORT_B_3N_IN | I | |
| | PORT_B_4P_IN | I | |
| | PORT_B_4N_IN | I | |
| | PORT_A_1P_OUT | O | Port A High Speed Data differential outputs |
| | PORT_A_1N_OUT | O | |
| | PORT_A_2P_OUT | O | |
| | PORT_A_2N_OUT | O | |
| | PORT_A_3P_OUT | O | |
| | PORT_A_3N_OUT | O | |

**Table 4-1 Signal List**

| | | | |
|---|---|---|---|
| | PORT_A_4P_OUT | O | |
| | PORT_A_4N_OUT | O | |
| | PORT_B_1P_OUT | O | Port B High Speed Data differential outputs |
| | PORT_B_1N_OUT | O | |
| | PORT_B_2P_OUT | O | |
| | PORT_B_2N_OUT | O | |
| | PORT_B_3P_OUT | O | |
| | PORT_B_3N_OUT | O | |
| | PORT_B_4P_OUT | O | |
| | PORT_B_4N_OUT | O | |
| Low Speed Interface | PORT_A_MODSEL | O | Port A QSFP Mode Select output |
| | PORT_A_RESETL | O | Port A QSFP Reset output |
| | PORT_A_I2C_SCL | O | Port A QSFP Serial Clock |
| | PORT_A_I2C_SDA | I/O | Port A QSFP Serial Data |
| | PORT_A_LPMODE | O | Port A QSFP Low Power Mode output |
| | PORT_A_3V3 | Pwr | Port A VccRx, VccTx, andr Vcc1 to be filtered individually if needed |
| | PORT_A_INTL | I | Port A QSFP Interrupt |
| | PORT_A_MODPRSL | I | Port A QSFP Module Present input |
| | PORT_B_MODSEL | O | Port B QSFP Mode Select output |
| | PORT_B_RESETL | O | Port B QSFP Reset output |
| | PORT_B_I2C_SCL | O | Port B QSFP Serial Clock |
| | PORT_B_I2C_SDA | I/O | Port B QSFP Serial Data |
| | PORT_B_LPMODE | O | Port B QSFP Low Power Mode output |
| | PORT_B_3V3 | Pwr | Port B VccRx, VccTx, and Vcc1 to be filtered individually if needed |
| | PORT_B_INTL | I | Port B QSFP Interrupt |
| | PORT_B_MODPRSL | I | Port B QSFP Module Present input |
| Fabric Status LED | PORT_A_LNK_LED | O | Port A Link LED |
| | PORT_A_ACT_LED | O | Port A Activity LED |
| | PORT_B_LNK_LED | O | Port B Link LED |
| | PORT_B_ACT_LED | O | Port B Activity LED |
| I2C Interface | I2C_SCL | I | I2C clock input |
| | I2C_SDA | I/O | I2C data |
| UART | UART_TX | O | UART transmit data |
| | UART_RX | I | UART receive data |
| Device LEDs | OK_LED_IN | I | OK LED input |
| | ID_LED_IN | I | ID LED input |
| | FLT_LED_IN | I | FAULT LED input |
| Management | INT_L_OUT | O | Interrupt active low output |
| | PWR_EN_IN | I | Power Enable input |

**Table 4-1 Signal List**

| | | | |
|---|---|---|---|
| | PWR_OK_L_IN | I | Power OK input |
| | AC_OK_L | I | Source power is OK |
| | SYS_ALIVE_H_IN | I | Indicator from management controller that system is alive |
| | RESET_L_IN | I | Reset active low input |
| | SGMII_P_OUT | O | Ethernet Management port differiential outputs |
| | SGMII_N_OUT | O | |
| | SGMII_P_IN | I | Ethernet Management port differiential inputs |
| | SGMII_N_IN | I | |
| GPIO | GPIO_0 | I/O | General purpose I/O |
| | GPIO_1 | I/O | General purpose I/O |
| JTAG | JTAG_TDI | I | Test Data In |
| | JTAG_TDO | O | Test Data Out |
| | JTAG_TMS | I | Test Mode Select |
| | JTAG_TCK | I | Test Clock |
| | JTAG_TRSTN | I | Test Reset active low |
| Slot Address | SLOT_0_IN | I | System assigns a slot number (0x0 thru 0xF) to each Device |
| | SLOT_1_IN | I | |
| | SLOT_2_IN | I | |
| | SLOT_3_IN | I | |
| Present | PRSNT_L | O | Idndicates the Fabric Device is present. Pulled low through a 100Ohm resistor on Fabric Device. |
| | BLANK_PRESENT_L | O | Indicates the Fabric Device is a blank nonoperational Device. Pulled low through a 100Ohm resistor on Fabric Device |
| Reserved | RESERVED2 | I/O | |
| | RESERVED3 | I/O | |

### 4.1 Power and Grounds

The Fabric Device supports a 12V power source to power all circuitry on the Device. The 12V rails is expected to be powered at all times while the Fabric Device is inserted in the system.

### 4.2 High Speed Ports

The high speed fabric interface provides two (2), four (4) lane ports for external connectivity. The external connectivity is defined by the specific Device and will have connectivity according to the enclosure the Device is inserted into. These ports consist of two (2) differential ports each, one for Tx and one for Rx.
PORT_A/B*P/N_IN pair is defined as an input to the Fabric Device
PORT_A/B*P/N_OUT pair is defined as an output from the Fabric Device

### 4.3 Low Speed Interface

The low speed interface signals combine with Fabric interfaces for cabled systems, these signals will have connectivity according to the enclosure the Device is inserted into. All signals listed in this section shall follow electrical specifications defined in SFF-8679.

### 4.3.1 PORT_A/B_MODSEL

Port A and B ModSelL is an active low signal and is used by the Fabric Device to enable communication on the 2-wire serial bus of the module.

### 4.3.2 PORT_A/B_RESETL

Port A and B RESETL is an active low signal and is used by the Fabric Device to reset the module.

### 4.3.3 PORT_A/B_3V3

Port A and B 3.3V is a power source to the module connected to the enclosure, these 3.3V source pins are all connected to the same power source within the Fabric Device.

### 4.3.4 PORT_A/B_SCL

Port A and B 2-wire serial interface clock. The port 2-wire interface is defined in SFF-8679. The Fabric Device does not provide a pullup on this signal.

### 4.3.5 Port_A/B_SDA

Port A and B 2-wire serial interface data signal. The port 2-wire interface is defined in SFF-8679. The Fabric Device does not provide a pullup on this signal.

### 4.3.6 PORT_A/B_LPMODE

Port A and B low power mode hardware control pin to be used in combination with fabric connections. LPMODE is an active high signal and is defined by SFF-8679.

### 4.3.7 PORT_A/B_INTL

Port A and B INTL is an active low interrupt output from the fabric cable possibly indicating a module operation fault. The Fabric Device identifies the fault using the 2-wire interface.

### 4.3.8 PORT_A/B_MODPRSL

Port A and B module present is an active low output from the fabric cable indicating a module present.

## 4.4 Fabric Status LED

Fabric Status LEDs for both the A and B:
PORT_A_LNK_LED drives the port A link LED on the fabric connector.
PORT_A_ACT_LED drives the port A activity LED on the fabric connector.
PORT_B_LNK_LED drives the port B link LED on the fabric connector.
PORT_B_ACT_LED drives the port B activity LED on the fabric connector.
These LEDs are defined by the specific fabric operation of the Fabric Device.

## 4.5 I2C Interface

This I2C is a standard 2-wire serial interface following I2C-bus specification for low speed out of band management of the Fabric Device. This 2-wire serial interface must have a Fabric Device VPD EEPROM at I2C address 0xA0 and a general purpose device at address 0x60 defined by Fabric Device vendor.

## 4.6 UART Interface

The UART interface to the Fabric Device is a low-level debug interface that may be connected to any intelligent part of the Device that requires access to a UART from the enclosure.

## 4.7 Fabric Device Status LEDs

The Fabric Device status LEDs are optional LEDS on the Fabric Device that can be driven by the Device itself or from the enclosure. These are inputs to the Fabric Device and have internal 10k pulldown resistors.
OK_LED_IN is a green LED indicating the Fabric Device is OK
ID_LED_IN is a blue LED identifying the Fabric Device.
FLT_LED_IN is an amber LED indicating the Fabric Device has a fault.

### 4.8 Management

The management interface for the Fabric Device is primarily over the 1G SGMII interface.

### 4.9 INT_L_OUT

Interrupt out is an active low signal to the enclosure from the Fabric Device.

### 4.10 PWR_EN_IN

Power enable input is an active high signal to the Device used by the enclosure to allow full power operation on the Fabric Device. The Device shall not consume more than 5 Watts of power while PWR_EN_IN is logic low.

### 4.11 PWR_OK_L_IN

Power OK is an active low signal from the enclosure power supplies indicating the power from the PSUs is OK

#### 4.11.1 AC_OK_L

AC OK is an active low signal from the enclosure power supplies indicating the AC to the power supplies is OK

#### 4.11.2 SYS_ALIVE_H_IN

System alive is an active high input to the Fabric Device indicating the system is OK.

#### 4.11.3 RESET_L_IN

Reset in is an active low signal used by the enclosure to reset the Fabric Device. Reset has an internal 10kOhm pullup to 3.3V

#### 4.11.4 SGMII Interface

The SGMII port is the primary management interface into the Fabric Device. This interface follows the specification defined in ENG-46158.

### 4.12 GPIO

There are two GPIO signals on the connector for the Fabric Device, these two signals are marked as reserved.

### 4.13 JTAG

The JTAG interface follows standard IEEE1149 with the chain inside the Fabric Device. This interface should be used for any components that get reprogrammed via JTAG.

### 4.14 Slot Address

The 4 bits of slot address indicate to the Fabric Device what slot in an enclosure it is installed in.

### 4.15 Present

PRSNT_L is an active low signal that indicates the Fabric Device is present in the system. This signal shall be pulled to ground through a 100Ohm resistor on the Fabric Device.
BLANK_PRSNT_L is an active low signal to indicate that the Fabric Device is a blank Device and does not have any functionality. This signal shall be pulled to ground through a 100Ohm resistor on the Fabric Device.

### 4.16 Reserved

There are two (2) reserved pins for future use of Fabric Devices.

# 5. Connector Pinout Definition

**Table 5-1 Fabric Device Connector Pinout**

| | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|
| T | AC_OK_L | GND | PWR_OK_L_IN | GND | UART_RX | GND | UART_TX | GND | T |
| S | GND | PORT_A_2N_OUT | GND | PORT_A_1N_OUT | GND | PORT_B_2N_OUT | GND | PORT_B_1N_OUT | S |
| R | PORT_A_4N_OUT | PORT_A_2P_OUT | PORT_A_3N_OUT | PORT_A_1P_OUT | PORT_B_4N_OUT | PORT_B_2P_OUT | PORT_B_3N_OUT | PORT_B_1P_OUT | R |
| Q | PORT_A_4P_OUT | GND | PORT_A_3P_OUT | GND | PORT_B_4P_OUT | GND | PORT_B_3P_OUT | GND | Q |
| P | GND | PORT_A_2N_IN | GND | PORT_A_1N_IN | GND | PORT_B_2N_IN | GND | PORT_B_1N_IN | P |
| O | PORT_A_4N_IN | PORT_A_2P_IN | PORT_A_3N_IN | PORT_A_1P_IN | PORT_B_4N_IN | PORT_B_2P_IN | PORT_B_3N_IN | PORT_B_1P_IN | O |
| N | PORT_A_4P_IN | GND | PORT_A_3P_IN | GND | PORT_B_4P_IN | GND | PORT_B_3P_IN | GND | N |
| M | GND | JTAG_TRSTN | GND | PORT_B_RESETL | GND | PORT_A_RESETL | GND | 12V | M |
| L | SLOT_3_IN | JTAG_TCK | PORT_B_MODPRSL | PORT_B_MODSEL | PORT_A_MODPRSL | PORT_A_MODSEL | I2C_SDA | 12V | L |
| K | SLOT_2_IN | GND | PORT_B_INTL | GND | PORT_A_INTL | GND | I2C_SCL | GND | K |
| J | GND | JTAG_TMS | GND | RESERVED2 | GND | FLT_LED_IN | GND | 12V | J |
| I | SLOT_1_IN | JTAG_TDO | PORT_B_3V3 | RESERVED1 | PORT_A_3V3 | ID_LED_IN | 12V | 12V | I |
| H | SLOT_0_IN | GND | PORT_B_3V3 | GND | PORT_A_3V3 | GND | 12V | GND | H |
| G | GND | JTAG_TDI | GND | PRSNT_L | GND | OK_LED_IN | GND | 12V | G |
| F | SGMII_N_IN | SYS_ALIVE_H_IN | PORT_B_LPMODE | RESET_L_IN | PORT_A_LPMODE | PORT_B_ACT_LED | 12V | 12V | F |
| E | SGMII_P_IN | GND | PORT_B_I2C_SDA | GND | PORT_A_I2C_SDA | GND | 12V | GND | E |
| D | GND | GPIO_1 | GND | PWR_EN_IN | GND | PORT_B_LNK_LED | GND | 12V | D |
| C | SGMII_N_OUT | GPIO_0 | PORT_B_I2C_SCL | INT_L_OUT | PORT_A_I2C_SCL | PORT_A_ACT_LED | 12V | 12V | C |
| B | SGMII_P_OUT | GND | PORT_B_3V3 | GND | PORT_A_3V3 | GND | 12V | GND | B |
| A | GND | GND | GND | BLANK_PRSNT_L | GND | PORT_A_LNK_LED | GND | GND | A |
| | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |

# 6. VPD Contents

The Fabric Device has a slave I2C bus that operates at 100kHz. The Fabric Device has a VPD EEPROM located at 2 wire serial interface address 0xA0. The VPD data is set at manufacturing and is not changed during runtime. The VPD data is defined in Table 6-1 Vital Product Data. All strings are all 8-bit ASCII, left justified, null terminated, with trailing nulls.

**Table 6-1 Vital Product Data**

| Addr | Size (B) | R/W | Value type | Function | Default Value | Description |
|---|---|---|---|---|---|---|
| 0 | 1 | RO | Unsigned Int | Version | Vendor | Format version |
| 1 | 3 | RO | | | 0 | Reserved |
| 4 | 1 | RO | Unsigned Int | Device Class | Vendor | Identifies Device class type |
| 5 | 1 | RO | Unsigned Int | | Vendor | Identifies Device subclass type |
| 6 | 40 | RO | 8-bit ASCII | ID | Vendor | Vendor name string |
| 46 | 40 | RO | 8-bit ASCII | | Vendor | Serial number string |
| 86 | 40 | RO | 8-bit ASCII | | Vendor | Model number string |
| 126 | 40 | RO | 8-bit ASCII | | Vendor | Part number string |
| 166 | 36 | RO | 8-bit ASCII | | Vendor | UUID string (with hyphens) |
| 202 | 8 | RO | 8-bit ASCII | | Vendor | MFG Date String "DDMMYYYY" |
| 210 | 12 | RO | | | 0 | Reserved |
| 222 | 1 | RO | Unsigned Int | Fabric | Vendor | Protocol |
| 223 | 1 | RO | Unsigned Int | | Vendor | Active Ports |
| 224 | 2 | RO | | | 0 | Reserved |
| 226 | 1 | RO | Unsigned Int | Port 0 | Vendor | Maximum Link speed |
| 227 | 1 | RO | Unsigned Int | | Vendor | Maximum Link width (#) |
| 228 | 1 | RO | Unsigned Int | Port 1 | Vendor | Maximum Link speed |
| 229 | 1 | RO | Unsigned Int | | Vendor | Maximum Link width (#) |
| 230 | 2 | RO | Unsigned Int | Initial Power[17] | Vendor | Initial power requirement (W) |
| 232 | 2 | RO | Unsigend Int | | Vendor | Initial power duration (ms) |
| 234 | 2 | RO | | | 0 | Reserved |
| 236 | 2 | RO | Unsigned Int | Operational Power[17] | Vendor | Maximum 12V Rail power (W) |
| 238 | 2 | RO | Unsigned Int | | Vendor | Minimum 12V Rail power (W) |
| 240 | 4 | RO | Unsigned Int | Power Hold-up[17] | Vendor | Maximum discharge time (ms) |
| 244 | 4 | RO | Unsigned Int | | Vendor | Maximum discharge current (mA) |
| 248 | 4 | RO | Unsigned Int | | 0 | Reserved |
| 252 | 2 | RO | Unsigned int | UART | Vendor | Maximum speed (kHz) |
| 254 | 2 | RO | Unsigned int | Extensibility | Vendor | Capability List pointer |

**Table 6-2: Device Classes**

| ID | Device Class |
|---|---|
| 0 | Blank |
| 1 | Other |
| 2 | Storage |
| 3 | Memory |
| 4 | Compute |
| 5 | Uninterruptible Power Supply |
| 6-Fh | Reserved |

**Table 6-3: Storage Subclasses**

| ID | Device Subclass |
|---|---|
| 0 | None |
| 1 | Other |
| 2 | Solid State Storage |
| 3 | Hard Disk Drive |
| 4-Fh | Reserved |

**Table 6-4: Compute Subclasses**

| ID | Device Subclass |
|---|---|
| 0 | None |
| 1 | Other |
| 2 | CPU |
| 3 | GPU |
| 4 | FPGA |
| 5 | ASIC |
| 6-Fh | Reserved |

**Table 6-5: Memory Subclasses**

| ID | Device Subclass |
|---|---|
| 0 | None |
| 1 | Other |
| 2 | Volatile Memory |
| 3 | Non-Volatile Memory |
| 4-Fh | Reserved |

**Table 6-6: Power Storage Subclasses**

| ID | Device Subclass |
|---|---|
| 0 | None |
| 1 | Other |
| 2 | Battery |
| 3 | Capacitor |
| 4-Fh | Reserved |

**Table 6-7: Protocols**

| ID | Device |
|---|---|
| 0 | None |
| 1 | Other |
| 2 | Ethernet |
| 3 | Infiniband |
| 4 | PCIe |
| 5 | Fibre Channel |
| 6 | Gen-Z |
| 7 | SAS |
| 8-Fh | Reserved |

**Table 6-8: Active Ports**

| ID | Device |
|---|---|
| 0 | No ports active |
| 1 | Port 0 active |
| 2 | Port 1 active |
| 3 | Both ports active |
| 4-Fh | Reserved |

**Table 6-9: Link Speeds**

| ID | Device |
|---|---|
| 0 | None |
| 1 | Other |
| 2 | 1 Gb |
| 3 | 6 Gb |
| 4 | 10 Gb |
| 5 | 12 Gb |
| 6 | 16 Gb |
| 7 | 24 Gb |
| 8 | 25 Gb |
| 9 | 32 Gb |
| A | 56 Gb |
| B-Fh | Reserved |

## 6.1 Initial Power

The initial power fields are intended to describe power draw behavior that is transient shortly after power on. For example, a Device may need to charge power loss protection capacitors and will draw a higher than maximum operational power until charged.

## 6.2 Operational Power

These fields indicate the power consumption limits under normal operation. The maximum power field indicates what the maximum power that this Device will consume is. The minimum power field indicates the minimum power required for this Device to function. Powering the Device at minimum power does not guarantee any level of performance. The minimum power level is meant to indicate what the minimum power for this Device to respond to requests over the fabric interfaces.

## 6.3 Power Hold Up

The power hold-up fields are meant to describe behavior of the Device after a power loss event. For a Power storage Device, these fields can be used to determine how long it can sustain other Devices in the enclosure. For a non-power storage Device, these fields indicate how long the Device will remain operational under its own internal holdup power.

## 6.4 Capability List

The capability list allows for the discovery of optional extended features. These structures are optional. The data structure is constructed as a linked list. The pointer (if any) located at offset 254, points to the first capability structure whose format is shown in Table 6-10 I2C Standard Capability Data Structure. The Capability data structure has a 4-byte header. The first 2 bytes identify the Capability ID of the feature. A Capability ID of 0xFE indicates a vendor specific capability as shown in Table 6-11 I2C Vendor Specific Capability Data Structure. The second two bytes of the capability header are Next Address field and contain a pointer to the next capability in the list. Subsequent bytes are defined by each specific capability or are vendor specific. A value of zero in the Next Address field indicates the end of the linked list.

### 6.5 Standard Capability Data Structure

**Table 6-10 I2C Standard Capability Data Structure**

| Byte 3 | Byte 2 | Byte 1 | Byte 0 |
|---|---|---|---|
| Next Address Pointer | | Capability ID | |
| Optional parameters specific to each capability | | | |

### 6.6 Vendor Specific Capability Data Structure

Table 6-11 I2C Vendor Specific Capability Data Structure

| Byte 3 | Byte 2 | Byte 1 | Byte 0 |
|---|---|---|---|
| Next Address Pointer | | 0xFE | |
| Optional parameters specific to each capability | | | |

# 7. Dynamic Data

Optional Dynamic Data are hosted by a Device on the I2C bus at address 0x30 (i.e., slave address bits 7-0 correspond to 0011_000). The dynamic data is a single 128-byte vendor defined register. As the primary method of interfacing with the Fabric Device from the chassis management processor is the internal 1Gb Ethernet link, the use of the Dynamic Data over I2C interface is to provide diagnostic information as to why that internal 1Gb Ethernet link is not viable. As the usage of the Dynamic Data is to help with debugging efforts, the data layout and fields are not defined in this standard and are to be set by each Device vendor. The purpose of defining the Dynamic Data address 0x30 and length of 128 Bytes is to allow management software utilities and applications to acquire a standardized quantity of data from any Device that may then be passed on to Customer Support Representatives for interpretation