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REF-TA-1012

Specification for

Pin Assignment Reference for SFF-TA-1002 Connectors

Rev 0.0.2 November 08, 2018

Secretariat: SFF TA TWG

This specification provides a common reference for systems manufacturers, system integrators, and suppliers.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

The description of a connector in this specification does not assure that the specific component is actually available from connector suppliers. If such a connector is supplied it must comply with this specification to achieve interoperability between suppliers.

ABSTRACT: This specification is a reference document that describes pin assignments from application specifications across the industry for the connector defined by SFF-TA-1002. Some of the signal definitions are specified by organizations outside of SNIA and include Gen-Z, and Open Compute Platform (OCP).

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Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at:
http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee is contained in the document SFF-8000 which can be found at:
http://www.snia.org/sff/specifications

Suggestions for improvement of this specification will be welcome, they should be submitted to:
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Revision History

Rev 0.0.1 *November 7, 2018*:
-Initial draft

Rev 0.0.2 *November 8, 2018*:
-Added PECFF and 4C+/OCP segment pinouts
-Added clarification details to Overview section

CONTENTS

TABLES

1. Scope

This reference document lists a series of pin assignments for the connector defined by SFF-TA-1002. This document is for reference only and represents a snapshot in time. Signal assignments shown in this document include the following:

- EDSFF form factor signal assignments as defined by SFF-TA-1009
- Open Compute Platform NIC signal assignments as defined by OCP NIC 3.0 pinout table
- Gen-Z signal assignments defined by Gen-Z Scalable Connector Specification 1.1
- PCIe® Add-in Card signal assignments defined by PCIe Enclosure Compatible Form Factor (PECFF) Specification 1.0

2. References

2.1 Industry Documents

- SFF-TA-1002 Protocol Agnostic Multi-Lane High Speed Connector
- SFF-TA-1009 Enterprise and Datacenter SSD Pin and Signal Specification
- OCP NIC 3.0 0v82
- Gen-Z Scalable Connector Specification v1.1
- Gen-Z PECFF Specification v1.0

2.2 Conventions

Signals in Table 3-1 are color coded according to their general function. The signal groupings include power, ground, control, and data path. Pin assignments for power, ground, and data path are required to be the same for all variations of the SFF-TA-1002 connector. Control signals are not required to be the same for the different variations. The definition for the color coding is shown in Table 2-1

TABLE 2-1 COLOR CODE REFERENCE

Power Signals	
Ground Signals	
Control Signals	
Data Path Signals	
Connector Key	
Unsupported Signals	

3. SFF-TA-1002 Connector Variations

3.1 Overview

The SFF-TA-1002 connector system supports five configurations referred to as 1C, 2C, 4C+ and 4C-HP. These configurations are summarized for reference in this documents below. Refer to SFF-TA-1002 for complete definitions of these connectors.

a. 1C Connector: A connector with 56 contacts with up to 18 differential pairs of data signals in a GSSGSSG configuration.
b. 2C Connector: A connector with 84 contacts with up to 26 differential pairs of data signals in a GSSGSSG configuration.
c. 4C Connector: A connector with 140 contacts with up to 44 differential pairs of data signals in a GSSGSSG configuration.
d. 4C+ Connector: A connector with 168 contacts with up to 52 differential pairs of data signals in a GSSGSSG configuration.
e. 4C-HP Connector: A connector with 140 contacts with up to 44 differential pairs of data signals in a GSSGSSG

configuration and a high power segment with two key sizes for different power voltages as defined in the Gen-Z Scalable Connector Specification v1.1.

Each interface variation (EDSFF, OCP, and Gen-Z) supports x4, x8, and x16 device connections. OCP and PECFF also have the option to support a x32 interface by connecting to two 4C (x16) connectors. For the purposes of describing these configurations in this document, the first 4C connector with the first 32 differential pairs is termed "Primary" and the second 4C connector with the second group of 32 differential pairs is termed "Secondary". PECFF may support either a 4C+ or a 4C-HP interface but not both simultaneously.

3.2 Signal Assignments

The following table shows pin assignments for SFF-TA-1002

TABLE 3-1 SFF-TA-1002 PIN ASSIGNMENTS

Pin	TA-1009	OCP NIC (Primary)	OCP NIC (Secondary)	GEN-Z	PECFF (Primary OCP or High Pwr)	PECFF (Secondary)
AO1		PERST2#			PERST2#	
AO2		PERST3#			PERST3#	
AO3		WAKE#			WAKE#	
AO4		RBT_ARB_IN			RBT_ARB_IN	
AO5		RBT_ARB_OUT			RBT_ARB_OUT	
AO6		SLOT_ID1			SLOT_ID1	
AO7		RBT_TX_EN			RBT_TX_EN	
AO8		RBT_TXD1			RBT_TXD1	
AO9		RBT_TXD0			RBT_TXD0	
AO10		GND			GND	
AO11		REFCLKn3			REFCLKn3	
AO12		REFCLKp3			REFCLKp3	
AO13		GND			GND	
AO14		RBT_CLK_IN			RBT_CLK_IN	
		KEY			KEY	
AH1				12V / 48V (note 1)	12V / 48V (note 1)	
AH2				GND	GND	
				KEY	KEY	
A1	GND	GND	GND	GND/Res	GND/Res	Res
A2	GND	GND	GND	GND/Res	GND/Res	Res
A3	GND	GND	GND	GND/Res	GND/Res	Res
A4	GND	GND	GND	GND/Res	GND/Res	Res
A5	GND	GND	GND	GND/Res	GND/Res	Res
A6	GND	GND	GND	GND/Res	GND/Res	Res
A7	SMBCLK	SMCLK	SMCLK	MGMT_CLK	SMCLK	Res
A8	SMBDAT	SMDAT	SMDAT	MGMT_DAT	SMDAT	Res
A9	SMBRST#	SMRST#	SMRST#	MGMT_RST#	SMRST#	Res
A10	LED#/ACTIVITY	PRSNTA#	PRSNTA#	LED#/ACTIVITY	Res	Res
A11	PERST1#/CLKREQ#	PERST1#	PERST1#	PERST1#/CLKREQ#	CLKREQ#	Res
A12	PRSNT0#	PRSNTB2#	PRSNTB2#	PRSNT_1C#	PRSNT1#	PRSNT6#
A13	GND	GND	GND	GND	GND	Res
A14	REFCLKn1	REFCLKn1	REFCLKn1	REFCLKn1	REFCLKn1	Res
A15	REFCLKp1	REFCLKp1	REFCLKp1	REFCLKp1	REFCLKp1	Res
A16	GND	GND	GND	GND	GND	GND
A17	PERn0	PERn0	PERn0	RX0n	PERn0	PETn31
A18	PERp0	PERp0	PERp0	RX0p	PERp0	PETp31
A19	GND	GND	GND	GND	GND	GND
A20	PERn1	PERn1	PERn1	RX1n	PERn1	PETn30

A21	PERp1	PERp1	PERp1	RX1p	PERp1	PETp30
A22	GND	GND	GND	GND	GND	GND
A23	PERn2	PERn2	PERn2	RX2n	PERn2	PETn29
A24	PERp2	PERp2	PERp2	RX2p	PERp2	PETp29
A25	GND	GND	GND	GND	GND	GND
A26	PERn3	PERn3	PERn3	RX3n	PERn3	PETn28
A27	PERp3	PERp3	PERp3	RX3p	PERp3	PETp28
A28	GND	GND	GND	GND	GND	GND
	KEY	KEY	KEY	KEY	Key	Key
A29	GND	GND	GND	GND	GND	GND
A30	PERn4	PERn4	PERn4	RX4n	PERn4	PETn27
A31	PERp4	PERp4	PERp4	RX4p	PERp4	PETp27
A32	GND	GND	GND	GND	GND	GND
A33	PERn5	PERn5	PERn5	RX5n	PERn5	PETn26
A34	PERp5	PERp5	PERp5	RX5p	PERp5	PETp26
A35	GND	GND	GND	GND	GND	GND
A36	PERn6	PERn6	PERn6	RX6n	PERn6	PETn25
A37	PERp6	PERp6	PERp6	RX6p	PERp6	PETp25
A38	GND	GND	GND	GND	GND	GND
A39	PERn7	PERn7	PERn7	RX7n	PERn7	PETn24
A40	PERp7	PERp7	PERp7	RX7p	PERp7	PETp24
A41	GND	GND	GND	GND	GND	GND
A42	RFU	PRSNTB1#	PRSNTB1#	Res	Res	Res
	KEY	KEY	KEY	KEY	Key	Key
A43	GND	GND	GND	GND	GND	GND
A44	PERn8	PERn8	PERn8	RX8n	PERn8	PETn23
A45	PERp8	PERp8	PERp8	RX8p	PERp8	PETp23
A46	GND	GND	GND	GND	GND	GND
A47	PERn9	PERn9	PERn9	RX9n	PERn9	PETn22
A48	PERp9	PERp9	PERp9	RX9p	PERp9	PETp22
A49	GND	GND	GND	GND	GND	GND
A50	PERn10	PERn10	PERn10	RX10n	PERn10	PETn21
A51	PERp10	PERp10	PERp10	RX10p	PERp10	PETp21
A52	GND	GND	GND	GND	GND	GND
A53	PERn11	PERn11	PERn11	RX11n	PERn11	PETn20
A54	PERp11	PERp11	PERp11	RX11p	PERp11	PETp20
A55	GND	GND	GND	GND	GND	GND
A56	PERn12	PERn12	PERn12	RX12n	PERn12	PETn19
A57	PERp12	PERp12	PERp12	RX12p	PERp12	PETp19
A58	GND	GND	GND	GND	GND	GND
A59	PERn13	PERn13	PERn13	RX13n	PERn13	PETn18
A60	PERp13	PERp13	PERp13	RX13p	PERp13	PETp18
A61	GND	GND	GND	GND	GND	GND

A62	PERn14	PERn14	PERn14	RX14n	PERn14	PETn17
A63	PERp14	PERp14	PERp14	RX14p	PERp14	PETp17
A64	GND	GND	GND	GND	GND	GND
A65	PERn15	PERn15	PERn15	RX15n	PERn15	PETn16
A66	PERp15	PERp15	PERp15	RX15p	PERp15	PETp16
A67	GND	GND	GND	GND	GND	GND
A68	RFU	USB_DATn	UART_RX	Res	Res	Res
A69	RFU	USB_DATp	UART_TX	Res	Res	Res
A70	RFU	PWRBRK#	PWRBRK#	Res	Res	Res

Note 1: Gen-Z and PECFF supports optional power pins to allow for high power implementations. The high power options support either 12V or 48V implementations. Pins A1-6 and B1-6 are Res in 48V pinouts.

Table 3-1 SFF-TA-1002 Alternate Signal Assignments (continued)

Pin	TA-1009	OCP NIC (Primary)	OCP NIC (Secondary)	GEN Z	PECFF (Primary OCP or High Pwr)	PECFF (Secondary)
BO1		NIC_PWR_GOOD			NIC_PWR_GOOD	
BO2		MAIN_PWR_EN			MAIN_PWR_EN	
BO3		LD#			LD#	
BO4		DATA_IN			DATA_IN	
BO5		DATA_OUT			DATA_OUT	
BO6		CLK			CLK	
BO7		SLOT_ID0			SLOT_ID0	
BO8		RBT_RXD1			RBT_RXD1	
BO9		RBT_RXD0			RBT_RXD0	
BO10		GND			GND	
BO11		REFCLKn2			REFCLKn2	
BO12		REFCLKp2			REFCLKp2	
BO13		GND			GND	
BO14		RBT_CRS_DV			RBT_CRS_DV	
		KEY			KEY	
BH1				12V / 48V (note 1)	12V / 48V (note 1)	
BH0				GND	GND	
				KEY	KEY	
B1	12 V	+12V_EDGE	+12V_EDGE	12 V / Res (note 2)	12V/Res	Res
B2	12 V	+12V_EDGE	+12V_EDGE	12 V / Res (note 2)	12V/Res	Res
B3	12 V	+12V_EDGE	+12V_EDGE	12 V / Res (note 2)	12V/Res	Res
B4	12 V	+12V_EDGE	+12V_EDGE	12 V / Res (note 2)	12V/Res	Res
B5	12 V	+12V_EDGE	+12V_EDGE	12 V / Res (note 2)	12V/Res	Res
B6	12 V	+12V_EDGE	+12V_EDGE	12 V / Res (note 2)	12V/Res	Res
B7	MFG	BIF0#	BIF0#	Wake#/MFG	Wake#/MFG	Res
B8	RFU	BIF1#	BIF1#	PWR_BREAK	PWR_BREAK	Res
B9	DUALPORTEN#	BIF2#	BIF2#	DualPortEn#	DualPortEn#	Res
B10	PERST0#	PERST0#	PERST0#	PERST0#	PERST0#	Res
B11	3.3 VAux	+3.3V_EDGE	+3.3V_EDGE	3.3 VAux	3.3VAux	Res
B12	PWRDIS	AUX_PWR_EN	AUX_PWR_EN	PWRDIS	PWRDIS	Res
B13	GND	GND	GND	GND	GND	Res
B14	REFCLKn0	REFCLKn0	REFCLKn0	REFCLKn0	REFCLKn0	Res
B15	REFCLKp0	REFCLKp0	REFCLKp0	REFCLKp0	REFCLKp0	Res
B16	GND	GND	GND	GND	GND	GND
B17	PETn0	PETn0	PETn0	TX0n	PETn0	PERn31
B18	PETp0	PETp0	PETp0	TX0p	PETp0	PERp31

B19	GND	GND	GND	GND	GND	GND
B20	PETn1	PETn1	PETn1	TX1n	PETn1	PERn30
B21	PETp1	PETp1	PETp1	TX1p	PETp1	PERp30
B22	GND	GND	GND	GND	GND	GND
B23	PETn2	PETn2	PETn2	TX2n	PETn2	PERn29
B24	PETp2	PETp2	PETp2	TX2p	PETp2	PERp29
B25	GND	GND	GND	GND	GND	GND
B26	PETn3	PETn3	PETn3	TX3n	PETn3	PERn28
B27	PETp3	PETp3	PETp3	TX3p	PETp3	PERp28
B28	GND	GND	GND	GND	GND	GND
	KEY	KEY	KEY	KEY	Key	Key
B29	GND	GND	GND	GND	GND	GND
B30	PETn4	PETn4	PETn4	TX4n	PETn4	PERn27
B31	PETp4	PETp4	PETp4	TX4p	PETp4	PERp27
B32	GND	GND	GND	GND	GND	GND
B33	PETn5	PETn5	PETn5	TX5n	PETn5	PERn26
B34	PETp5	PETp5	PETp5	TX5p	PETp5	PERp26
B35	GND	GND	GND	GND	GND	GND
B36	PETn6	PETn6	PETn6	TX6n	PETn6	PERn25
B37	PETp6	PETp6	PETp6	TX6p	PETp6	PERp25
B38	GND	GND	GND	GND	GND	GND
B39	PETn7	PETn7	PETn7	TX7n	PETn7	PERn24
B40	PETp7	PETp7	PETp7	TX7p	PETp7	PERp24
B41	GND	GND	GND	GND	GND	GND
B42	PRSNT1#	PRSNTB0#	PRSNTB0#	Res	PRSNT2#	PRSNT5#
	KEY	KEY	KEY	KEY	Key	Key
B43	GND	GND	GND	GND	GND	GND
B44	PETn8	PETn8	PETn8	TX8n	PETn8	PERn23
B45	PETp8	PETp8	PETp8	TX8p	PETp8	PERp23
B46	GND	GND	GND	GND	GND	GND
B47	PETn9	PETn9	PETn9	TX9n	PETn9	PERn22
B48	PETp9	PETp9	PETp9	TX9p	PETp9	PERp22
B49	GND	GND	GND	GND	GND	GND
B50	PETn10	PETn10	PETn10	TX10n	PETn10	PERn21
B51	PETp10	PETp10	PETp10	TX10p	PETp10	PERp21
B52	GND	GND	GND	GND	GND	GND
B53	PETn11	PETn11	PETn11	TX11n	PETn11	PERn20
B54	PETp11	PETp11	PETp11	TX11p	PETp11	PERp20
B55	GND	GND	GND	GND	GND	GND
B56	PETn12	PETn12	PETn12	TX12n	PETn12	PERn19
B57	PETp12	PETp12	PETp12	TX12p	PETp12	PERp19
B58	GND	GND	GND	GND	GND	GND
B59	PETn13	PETn13	PETn13	TX13n	PETn13	PERn18

B60	PETp13	PETp13	PETp13	TX13p	PETp13	PERp18
B61	GND	GND	GND	GND	GND	GND
B62	PETn14	PETn14	PETn14	TX14n	PETn14	PERn17
B63	PETp14	PETp14	PETp14	TX14p	PETp14	PERp17
B64	GND	GND	GND	GND	GND	GND
B65	PETn15	PETn15	PETn15	TX15n	PETn15	PERn16
B66	PETp15	PETp15	PETp15	TX15p	PETp15	PERp16
B67	GND	GND	GND	GND	GND	GND
B68	RFU	RFU1, NC	RFU1, NC	Res	Res	Res
B69	RFU	RFU2, NC	RFU2, NC	Res	Res	Res
B70	PRSNT2#	PRSNTB3#	PRSNTB3#	Res	PRSNT_3C#	PRSNT4#

Note 2: Gen-Z and PECFF supports a 12V and a 48V power option. In the 12V option these pins are assigned to 12V. In the 48V option these pins are reserved.