1 2 3 4 5	SFF TWG Technology Affiliate
6 7	SFF-TA-1015
8	Specification for
9	Fabric Device Pinout Specification
10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 4 35	Rev 0.0.5 January 14, 2019 SECRETARIAT: SFF TA TWG This specification is made available for public review at http://www.snia.org/sff/specifications . Comments may be submitted at http://www.snia.org/sff/specifications . Comments may be submitted at http://www.snia.org/feedback . Comments received will be considered for inclusion in future revisions of this specification. The description of the connector in this specification does not assure that the specific component is available from ponector suppliers. ABSTRACT: This specification defines the Fabric Device signal list, connector pinout and VPD EEPROM definition. POINTS OF CONTACT: TC McNally Chairman SFF TA TWG Western Digital Corporation Spio Federal Drive Suite 100 Colorado Spings, C0 80921. Chairman SFF TA TWG Email: SFF-Chair@snia.org .

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Foreword The develop

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

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Revision History

12		
13	Rev 0.0.1	October 12, 2018:
14		-Initial release of document
15		-Description
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17		-Internal review
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24		
25		
26		

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1. Scope 1

2 This specification defines the Fabric Device Pinout Specification. This document convers the signal list, signal 3 definitions and connector pinout.

2. References and Conventions 4

- 5 2.1 Industry Documents
- 6

Serial-GMII Specification - ENG-46158

- 7 8 - IEEE Std 1149.1 IEEE Standard Test Access Port and Boundary-Scan Architecture
- Cross Reference to Select SFF Connectors 9 - REF-TA-1011
- 10 - SFF-8679 OSFP+ 4X Hardware and Electrical Specification
- SFF-TA-1014 Fabric Attached Devices Connector Specification 11
- 12 - SPRUGP1 Universal Asynchronous Receiver/Transmitter (UART)
- I2C-bus Specification and user manual 13 - UM10204 14

15 2.2 Sources

16 The complete list of SFF documents which have been completed, are currently being worked on, or that have been expired by the SFF Committee can be found at <u>http://www.snia.org/sff/specifications</u>. Suggestions for improve-17 ment of this specification will be welcome, they should be submitted to http://www.snia.org/feedback. 18 19

Copies of ANSI standards may be obtained from the InterNational Committee for Information Technology Standards 20 21 (http://www.techstreet.com/incitsgate.tmpl). 22

23 Copies of PCIe standards may be obtained from PCI-SIG (http://pcisig.com). 24

25 Copies of InfiniBand standards may be obtained from the InfiniBand Trade Association (IBTA) 26 (http://www.infinibandta.org). 27

28 Copies of IEEE standards may be obtained from the Institute of Electrical and Electronics Engineers (IEEE) 29 (https://www.ieee.org). 30

31 Copies of SAS standards may be obtained from the International Committee for Information Technology Standards (INCITS) (http://www.incits.org). 32 33

Copies of JEDEC standards may be obtained from the Joint Electron Device Engineering Council 34 (https://www.jedec.org). 35

37 Copies of OIF Implementation Agreements may be obtained from the Optical Internetworking Forum 38 (http://www.oiforum.com). 39

40 Copies of ASME standards may be obtained from the American Society of Mechanical Engineers 41 (https://www.asme.org).

43 Copies of Electronic Industries Alliance (EIA) standards may be obtained from the Electronic Components Industry 44 Association (ECIA) (https://www.ecianow.org).

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1 2.3 Conventions

The following conventions are used throughout this document:

34 **DEFINITIONS**

Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

8 ORDER OF PRECEDENCE

9 If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then 10 tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and 11 values.

LISTS

14 Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items. 15

16 EXAMPLE 1 - The following list shows no relationship between the named items:

- a. red (i.e., one of the following colors):
 - A. crimson; or
 - B. pink;
- b. blue; or
 - c. green.

23 Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 - The following list shows an ordered relationship between the named items:

- 1. top;
 - 2. middle; and
 - 3. bottom.

Lists are associated with an introductory paragraph or phrase, and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

33 DIMENSIONING CONVENTIONS

The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

3738 NUMBERING CONVENTIONS

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

42

3. Keywords, Acronyms, and Definitions

2 For the purposes of this document, the following keywords, acronyms, and definitions apply.

3 3.1 Keywords

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4 **May/ may not:** A keyword that indicates flexibility of choice with no implied preference.

Obsolete: A keyword indicating that an item was defined in prior specifications but has been removed from this
 specification.

Optional: A keyword that describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: A keyword used to describe a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: A keyword used for defining the signal on a connector contact [when] its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: A keyword referring to features, bits, bytes, words, and fields that are set aside for other identified standardization purposes. A restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word or field in the context where the restricted designation appears.

Shall: A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

30 **Should:** A keyword indicating flexibility of choice with a strongly preferred alternative.

32 Vendor specific: A keyword indicating something (e.g., a bit, field, code value) that is not defined by this 33 specification. Specification of the referenced item is determined by the manufacturer and may be used differently 34 in various implementations. 35

- 36 **3.2** Acronyms and Abbreviations
- 37 RO: Read Only
- 38 **RX:** Receiver
- 39 **TX:** Transmitter
- 40 **VPD:** Vital Product Data

1 3.3 Definitions

7 **Termination:** A term used to describe a connector's non-separable attachment point such as [a connector contact 8 to a bulk cable/ a cage to a PCB or flex circuit/ bulk cable to a PCB or flex circuit/ solder tail to PCB]. Common PCB 9 terminations include: surface mount (SMT), plated through hole termination (PTH), and press fit (PF). Common 10 cable terminations include insulation displacement contact (IDC), insulation displacement termination (IDT), wire

Module: In this specification, module refers to an assembly that is terminated at the end of a direct attach copper

11 slots, solder, welds, crimps, and brazes.

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4. Signal List 13

14 The signal summary, definitions and signal placement for the Fabric Device connector are detailed in this section. 15 All signals listed are presented relative to the Fabric Device, IN is an input to the Fabric Device, OUT is an output 16

	5					
6	from the Fabric	Device, RX is ar	input to the Fabric	Device and TX is a	n output from the F	abric Device.

(DAC) or an active optical cable (AOC), intended to mate to a device.

Interface	Signal Name	Fabric Device I/O	Function
Power and	12V	I	12V Source
Ground	GND	Ι	Return Current Path
	PORT_A_1P_IN	I	
	PORT_A_1N_IN	Ι	
	PORT_A_2P_IN	Ι	
	PORT_A_2N_IN	Ι	Port A High Speed Data differential inputs
	PORT_A_3P_IN	Ι	
	PORT_A_3N_IN	Ι	
	PORT_A_4P_IN	Ι	
	PORT_A_4N_IN	Ι	
	PORT_B_1P_IN	Ι	
	PORT_B_1N_IN	Ι	
High Speed	PORT_B_2P_IN	Ι	
Data	PORT_B_2N_IN	Ι	Port B High Speed Data differential inputs
	PORT_B_3P_IN	Ι	Tore b right speed bata anterendar inputs
	PORT_B_3N_IN	Ι	
	PORT_B_4P_IN	Ι	
	PORT_B_4N_IN	Ι	
	PORT_A_1P_OUT	0	
	PORT_A_1N_OUT	0	
	PORT_A_2P_OUT	0	Port A High Speed Data differential outputs
	PORT_A_2N_OUT	0	
	PORT_A_3P_OUT	0	
	PORT_A_3N_OUT	0	

Table 4-1 Signal List

Table 4-1 Signal List

PORT_A_4P_OUT O PORT_B_1P_OUT O PORT_B_1N_OUT O PORT_B_1N_OUT O PORT_B_2P_OUT O PORT_B_3N_OUT O PORT_B_3N_OUT O PORT_B_3N_OUT O PORT_B_4P_OUT O PORT_B_4P_OUT O PORT_B_4N_OUT O PORT_B_4N_OUT O PORT_A_RESETL O PORT_A_2CS_L O PORT_A_2N3 Pwr PORT_B_1N_1 I PORT_B_1Z_2CS_L O PORT_B_1Z_2CS_L O PORT_B_1Z_2CS_L O PORT_B_1Z_2CS_L O PORT_B_1Z_2CS_L O PORT_B_1Z_2CS_L O PORT_B_1Z_2CS_L	···· ····		[
PORT_B_IP_OUT O PORT_B_IN_OUT O PORT_B_2P_OUT O PORT_B_3N_OUT O PORT_B_3N_OUT O PORT_B_3N_OUT O PORT_B_AP_OUT O PORT_B_AP_OUT O PORT_A_RESETL O PORT_A_RESETL O PORT_A_RESETL O PORT_A_IZC_SCL O PORT_A_IZC_SCL O PORT_A_RESETL O PORT_A_RESETL O PORT_A_IZC_SCL O PORT_A_OPPODE O PORT_A_OPPODE Port A QSFP Low Power Mode output PORT_A_INTIL I PORT_A_MODPRSL I PORT_B_MODSEL O PORT_B_ARDOPRSL I PORT_B_NODEEL O PORT_B_RESETL O PORT_B_RESETL O PORT_B_RESETL O PORT_B_RODESL Port B_QSFP Mode Select output PORT_B_RESETL O PORT_B_RESETL		PORT_A_4P_OUT	0	
PORT_B_IN_OUTOPORT_B_2P_OUTOPORT_B_3N_OUTOPORT_B_3N_OUTOPORT_B_3N_OUTOPORT_B_AN_OUTOPORT_B_AN_OUTOPORT_B_AN_OUTOPORT_A_DODSELOPORT_A_RESETLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_12C_SCLOPORT_A_100DPRSLIPORT_A_100DPRSLIPORT_B_12C_SCLOPORT_B_12C_SCLOPORT_B_12C_SCLOPORT_B_12C_SCLOPORT_B_12C_SCLOPORT_B_100DEOPORT_B_100DEPort B_05PP Serial DataPORT_B_100DEOPORT_B_100DEPort B_05PP Serial ClockPORT_B_100DEOPORT_B_100DEPort B_05PP Seri		PORT_A_4N_OUT	0	
PORT_B_2P_OUT O PORT_B_2N_OUT O PORT_B_3P_OUT O PORT_B_3N_OUT O PORT_B_4N_OUT O PORT_B_4N_OUT O PORT_B_4N_OUT O PORT_B_4N_OUT O PORT_A_12C_SCL O PORT_A_12C_SCL O PORT_A_12C_SCL O PORT_A_12C_SCL O PORT_A_12C_SCL O PORT_A_12C_SCL O PORT_A_2CSCL O PORT_A_12C_SCL O PORT_A_12C_SCL O PORT_A_20C_SCL O PORT_A_20C_SCL O PORT_A_20C_SCL O PORT_A_3V3 Pwr PORT_A_3V3 Pwr PORT_B_MODSEL O PORT_B_BOSEL O PORT_B_BOSEL O PORT_B_ROSEL O PORT_B_ROSEL O PORT_B_ROSEL O PORT_B_ROSEL O PORT_B_ROSEL		PORT_B_1P_OUT	0	
PORT_B_2N_OUT O Port B High Speed Data differential outputs PORT_B_3P_OUT O Port B High Speed Data differential outputs PORT_B_4P_OUT O Port A QSFP Mode Select output PORT_A_MODSEL O Port A QSFP Mode Select output PORT_A_RESETL O Port A QSFP Serial Clock PORT_A_1ZC_SCL O Port A QSFP Serial Data PORT_A_1ZC_SCL O Port A QSFP Mode Select output PORT_A_MODE O Port A QSFP Mode Select output PORT_A_MODESL I Port A QSFP Mode Select output PORT_A_MODPRSL I Port A QSFP Mode Select output PORT_B_B_NODE O Port B QSFP Mode Select output PORT_B_B_1Z_C_SCL O Port B QSFP Mode Select output PORT_B_B_1Z_C_SCL O Port B QSFP Mode Select output PORT_B_NODESL O Port B QSFP Mode Select output PORT_B_1Z		PORT_B_1N_OUT	0	
PORT_B_3P_OUT O Port B night Speed Data dimensional outputs PORT_B_3N_OUT O PORT_B_3N_OUT O PORT_B_4P_OUT O PORT_B_4N_OUT O PORT_A_RESETL O Port A QSFP Mode Select output PORT_A CSC PORT_A_RESETL O Port A QSFP Serial Clock PORT_A LIZC_SCL O PORT_A_1ZC_SDA I/O Port A QSFP Serial Data PORT_A LIZC_SDA Port A QSFP Serial Data PORT_A_ADMODE O Port A QSFP Mode Select output Port A QSFP Mode Select output PORT_A ARST PORT_A_INTL I Port A QSFP Mode Select output PORT_A INTL PORT A QSFP Mode Select output PORT_B_MODPRSL I Port A QSFP Mode Select output PORT_B INDL PORT B QSFP Serial Data PORT_B_NODPRSL I Port B QSFP Mode Select output PORT_B INDL PORT B QSFP Mode Select output PORT_B_NODPRSL I Port B QSFP Mode Select output PORT_B INDL PORT B QSFP Mode Present input PORT_B_NODPRSL I Port B QSFP Mode Present input PORT B INDL Port B QSFP Mode Present input P		PORT_B_2P_OUT	0	
PORT_B_3P_OUT O PORT_B_3N_OUT O PORT_B_4P_OUT O PORT_B_4N_OUT O PORT_B_AN_OUT O PORT_B_AN_OUT O PORT_B_AN_ODSEL O Port A QSFP Mode Select output PORT_A_RESETL O Port A QSFP Serial Clock PORT_A_12C_SDA I/O Port A QSFP Serial Data PORT_A_IPMODE O Port A QSFP Mode Select output PORT_A_IDMODE O Port A QSFP Serial Data PORT_A_INTL I Port A QSFP Interrupt PORT_B_NODESL I Port A QSFP Mode Select output PORT_B_NODESL I Port A QSFP Module Present input PORT_B_NODESL I Port A QSFP Module Present input PORT_B_NODESL I Port A QSFP Serial Clock PORT_B_NODESL O Port B QSFP Serial Clock PORT_B_NODESL O Port B QSFP Serial Clock PORT_B_NODESL I Port B QSFP Serial Clock PORT_B_NODESL I Port B QSFP Module Present input PORT_B_NODPRSL<		PORT_B_2N_OUT	0	Port P High Speed Data differential outputs
PORT B 4P OUT O PORT B 4N OUT O PORT B 4N OUT O PORT A MODSEL O Port A QSFP Mode Select output PORT A RESETL O Port A QSFP Reset output PORT A I2C SCL O Port A QSFP Serial Clock PORT A I2C SDA I/O Port A QSFP Serial Data PORT A I2C SDA I/O Port A VCRX, VcCTx, andr VcC1 to be filtered PORT A INTL I Port A QSFP Mode Select output PORT A INTL I Port A QSFP Mode Select output PORT A MODPRSL I Port A QSFP Mode Select output PORT B MODSEL O Port B QSFP Mode Select output PORT B NDDSEL O Port B QSFP Serial Clock PORT B I2C SCL O Port B QSFP Serial Clock PORT B I2C SCL O Port B QSFP Serial Clock PORT B I2C SCL O Port B QSFP Serial Clock PORT B I2C SCL O Port B QSFP Mode output PORT B I2C SCL O Port B QSFP Mode output PORT B I2C SCL O Port B QSFP Module Present input </td <td></td> <td>PORT_B_3P_OUT</td> <td>0</td> <td>Port B high speed Data differential outputs</td>		PORT_B_3P_OUT	0	Port B high speed Data differential outputs
PORT_B_4N_OUT O PORT_A_MODSEL O Port A QSFP Mode Select output PORT_A_RESETL O Port A QSFP Reset output PORT_A_IZC_SCL O Port A QSFP Serial Clock PORT_A_IZC_SCL O Port A QSFP Serial Data PORT_A_IZC_SCL O Port A QSFP Serial Data PORT_A_IZC_SCL O Port A QSFP Serial Data PORT_A_INTL I Port A QSFP Iow Power Mode output PORT_A_MODPRSL I Port A QSFP Iow Power Mode output PORT_B_MODPRSL I Port A QSFP Mode Select output PORT_B_MODPRSL I Port B QSFP Mode Select output PORT_B_MODPRSL O Port B QSFP Mode Select output PORT_B_MODPRSL O Port B QSFP Mode Select output PORT_B_IZC_SDA I/O Port B QSFP Mode output PORT_B_IZC_SDA I/O Port B QSFP Serial Data PORT_B_IZC_SDA I/O Port B QSFP Mode output PORT_B_BAV3 Pwr individually if needed PORT_B_INTL I Port B QSFP Module Present input PORT_		PORT_B_3N_OUT	0	
PORT_A_MODSELOPort A QSFP Mode Select outputPORT_A_RESETLOPort A QSFP Serial ClockPORT_A_I2C_SCLOPort A QSFP Serial ClockPORT_A_I2C_SDAI/OPort A QSFP Serial ClockPORT_A_I2C_SDAI/OPort A QSFP Serial ClockPORT_A_IPMODEOPort A QSFP Serial DataPORT_A_INTLIPort A QSFP Low Power Mode outputPORT_A_INTLIPort A QSFP InterruptPORT_A_MODPRSLIPort A QSFP Mode Select outputPORT_B_MODSELOPort B QSFP Mode Select outputPORT_B_RESETLOPort B QSFP Mode Select outputPORT_B_RESETLOPort B QSFP Serial ClockPORT_B_12C_SCLOPort B QSFP Low Power Mode outputPORT_B_12C_SDAI/OPort B QSFP Low Power Mode outputPORT_B_12C_SDAI/OPort B QSFP Low Power Mode outputPORT_B_NODERSLIPort B QSFP InterruptPORT_B_NODERSLIPort B QSFP InterruptPORT_B_NODERSLIPort B QSFP Module Present inputPORT_B_LNK_LEDOPort A Link LEDPORT_B_LNK_LEDOPort A Link LEDPORT_B_LNK_LEDOPort A Link LEDPORT_B_LNK_LEDOPort B Activity LEDIL2C_SCLI <td></td> <td>PORT_B_4P_OUT</td> <td>0</td> <td></td>		PORT_B_4P_OUT	0	
PORT_A_RESETLOPort A QSFP Reset outputPORT_A_I2C_SCLOPort A QSFP Serial ClockPORT_A_I2C_SDAI/OPort A QSFP Serial DataPORT_A_LPMODEOPort A QSFP Low Power Mode outputPORT_A_IPMODEOPort A VccRx, VccTx, andr Vcc1 to be filteredindividually if neededPORT_A_INTLIPORT_A_INTLIPort A QSFP Module Present inputPORT_B_MODSELOPort B QSFP Mode Select outputPORT_B_MODSELOPort B QSFP Reset outputPORT_B_I2C_SCLOPort B QSFP Serial ClockPORT_B_I2C_SCLOPort B QSFP Serial ClockPORT_B_I2C_SCLOPort B QSFP Serial ClockPORT_B_I2C_SCLOPort B QSFP Serial ClockPORT_B_I2C_SCLOPort B QSFP Nodule Present inputPORT_B_I2C_SCLOPort B QSFP Nodule OutputPORT_B_I2C_SCLOPort B QSFP Nodule Present inputPORT_B_I2C_SCLOPort B QSFP InterruptPORT_B_INTLIPort B QSFP InterruptPORT_B_ACT_LEDOPort A Link LEDPORT_B_ACT_LEDOPort A Activity LEDI2CILCII2C clock inputI2C_SCLIII2C clock inputI2C_SCLIII2C clock inputI2C_SDAI/OI2C clock inputI2C_SDAI/OI2C clock inputI2C_SDAI/OI2C clock inputI2C_SDAI/OI2C clock inputI2C_SDAI/OI2C clock input <t< td=""><td></td><td>PORT_B_4N_OUT</td><td>0</td><td></td></t<>		PORT_B_4N_OUT	0	
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PORT_A_I2C_SCL O Port A QSFP Serial Clock PORT_A_I2C_SDA I/O Port A QSFP Serial Data PORT_A_LPMODE O Port A QSFP Low Power Mode output PORT_A_J3V3 Pwr individually if needed PORT_A_INTL I Port A QSFP Interrupt PORT_A_INTL I Port A QSFP Module Present input PORT_B_MODPRSL I Port A QSFP Mode Select output PORT_B_RESETL O Port B QSFP Mode Select output PORT_B_I2C_SCL O Port B QSFP Serial Clock PORT_B_I2C_SCL O Port B QSFP Low Power Mode output PORT_B_I2C_SCL O Port B QSFP Low Power Mode output PORT_B_I2C_SCL O Port B QSFP Low Power Mode output PORT_B_I2C_SCL O Port B QSFP Low Power Mode output PORT_B_I2C_SCL O Port B QSFP Low Power Mode output PORT_B_I2C_SCL O Port B QSFP Low Power Mode output PORT_B_I2C_SCL O Port B QSFP Low Power Mode output PORT_B_INTL I Port B QSFP Interrupt PORT_B_INTL I <t< td=""><td></td><td>PORT A RESETL</td><td>0</td><td></td></t<>		PORT A RESETL	0	
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Management INT_L_OUT O Interrupt active low output		OK_LED_IN	Ι	OK LED input
Management INT_L_OUT O Interrupt active low output	Device LEDs	ID_LED_IN	Ι	ID LED input
Management INT_L_OUT O Interrupt active low output		FLT_LED_IN	Ι	FAULT LED input
PWR_EN_IN I Power Enable input	Managamant	INT_L_OUT	0	
	manayement	PWR_EN_IN	Ι	Power Enable input

	PWR_OK_L_IN	Ι	Power OK input
	AC_OK_L	Ι	Source power is OK
	SYS_ALIVE_H_IN	I	Indicator from management controller that system is alive
	RESET_L_IN	I	Reset active low input
	SGMII_P_OUT	0	Ethernet Management port differiential outputs
	SGMII_N_OUT	0	Ethemet Management port dimenential outputs
	SGMII_P_IN	Ι	Ethernet Management port differiential inputs
	SGMII_N_IN	Ι	Ethemet Management port differential inputs
GPIO	GPIO_0	I/O	General purpose I/O
GFIO	GPIO_1	I/O	General purpose I/O
	JTAG_TDI	Ι	Test Data In
	JTAG_TDO	0	Test Data Out
JTAG	JTAG_TMS	I	Test Mode Select
	JTAG_TCK	I	Test Clock
	JTAG_TRSTN	I	Test Reset active low
	SLOT_0_IN	Ι	
Slot Address	SLOT_1_IN	I	System assigns a slot number (0x0 thru 0xF) to
SIOL AUULESS	SLOT_2_IN	I	each Device
	SLOT_3_IN	Ι	
	PRSNT_L	0	Idndicates the Fabric Device is present. Pulled low through a 1000hm resistor on Fabric Device.
Present			Indicates the Fabric Device is a blank
	BLANK PRESENT I	0	
Reserved			
	PRSNT_L BLANK_PRESENT_L RESERVED2 RESERVED3	0 0 I/0 I/0	low through a 1000hm resistor on Fabric Device.

1

2 4.1 Power and Grounds

The Fabric Device supports a 12V power source to power all circuitry on the Device. The 12V rails is expected to be powered at all times while the Fabric Device is inserted in the system.

5 4.2 High Speed Ports

6 The high speed fabric interface provides two (2), four (4) lane ports for external connectivity. The external 7 connectivity is defined by the specific Device and will have connectivity according to the enclosure the Device is 8 inserted into. These ports consist of two (2) differential ports each, one for Tx and one for Rx.

- 9 PORT_A/B*P/N_IN pair is defined as an input to the Fabric Device
- 10 PORT_A/B*P/N_OUT pair is defined as an output from the Fabric Device

11 4.3 Low Speed Interface

12 The low speed interface signals combine with Fabric interfaces for cabled systems, these signals will have 13 connectivity according to the enclosure the Device is inserted into. All signals listed in this section shall follow 14 electrical specifications defined in SFF-8679.

Fabric Device Pinout Specification

1 4.3.1 PORT_A/B_MODSEL

Port A and B ModSelL is an active low signal and is used by the Fabric Device to enable communication on the 2 wire serial bus of the module.

4 4.3.2 PORT_A/B_RESETL

5 Port A and B RESETL is an active low signal and is used by the Fabric Device to reset the module.

6 **4.3.3 PORT_A/B_3V3**

Port A and B 3.3V is a power source to the module connected to the enclosure, these 3.3V source pins are all
connected to the same power source within the Fabric Device.

9 **4.3.4 PORT_A/B_SCL**

Port A and B 2-wire serial interface clock. The port 2-wire interface is defined in SFF-8679. The Fabric Device does
 not provide a pullup on this signal.

12 4.3.5 Port_A/B_SDA

Port A and B 2-wire serial interface data signal. The port 2-wire interface is defined in SFF-8679. The Fabric Device
 does not provide a pullup on this signal.

15 4.3.6 PORT_A/B_LPMODE

Port A and B low power mode hardware control pin to be used in combination with fabric connections. LPMODE isan active high signal and is defined by SFF-8679.

18 **4.3.7 PORT_A/B_INTL**

Port A and B INTL is an active low interrupt output from the fabric cable possibly indicating a module operation
 fault. The Fabric Device identifies the fault using the 2-wire interface.

21 4.3.8 PORT_A/B_MODPRSL

22 Port A and B module present is an active low output from the fabric cable indicating a module present.

23 4.4 Fabric Status LED

- 24 Fabric Status LEDs for both the A and B:
- 25 PORT_A_LNK_LED drives the port A link LED on the fabric connector.
- 26 PORT_A_ACT_LED drives the port A activity LED on the fabric connector.
- 27 PORT_B_LNK_LED drives the port B link LED on the fabric connector.
- 28 PORT_B_ACT_LED drives the port B activity LED on the fabric connector.
- 29 These LEDs are defined by the specific fabric operation of the Fabric Device.

30 4.5 I2C Interface

- 31 This I2C is a standard 2-wire serial interface following I2C-bus specification for low speed out of band management
- of the Fabric Device. This 2-wire serial interface must have a Fabric Device VPD EEPROM at I2C address 0xA0 and a general purpose device at address 0x60 defined by Fabric Device vendor.

34 4.6 UART Interface

The UART interface to the Fabric Device is a low-level debug interface that may be connected to any intelligent part of the Device that requires access to a UART from the enclosure.

37 4.7 Fabric Device Status LEDs

- 38 The Fabric Device status LEDs are optional LEDS on the Fabric Device that can be driven by the Device itself or
- 39 from the enclosure. These are inputs to the Fabric Device and have internal 10k pulldown resistors.
- 40 OK_LED_IN is a green LED indicating the Fabric Device is OK
- 41 ID_LED_IN is a blue LED identifying the Fabric Device.
- 42 FLT_LED_IN is an amber LED indicating the Fabric Device has a fault.

Fabric Device Pinout Specification

1 4.8 Management

2 The management interface for the Fabric Device is primarily over the 1G SGMII interface.

3 4.9 INT_L_OUT

4 Interrupt out is an active low signal to the enclosure from the Fabric Device.

5 **4.10 PWR_EN_IN**

Power enable input is an active high signal to the Device used by the enclosure to allow full power operation on
 the Fabric Device. The Device shall not consume more than 5 Watts of power while PWR_EN_IN is logic low.

8 **4.11 PWR_OK_L_IN**

9 Power OK is an active low signal from the enclosure power supplies indicating the power from the PSUs is OK

10 4.11.1 AC_OK_L

11 AC OK is an active low signal from the enclosure power supplies indicating the AC to the power supplies is OK

12 **4.11.2 SYS_ALIVE_H_IN**

13 System alive is an active high input to the Fabric Device indicating the system is OK.

14 **4.11.3 RESET_L_IN**

Reset in is an active low signal used by the enclosure to reset the Fabric Device. Reset has an internal 10kOhm pullup to 3.3V

17 4.11.4 SGMII Interface

18 The SGMII port is the primary management interface into the Fabric Device. This interface follows the specification 19 defined in ENG-46158.

20 **4.12 GPIO**

21 There are two GPIO signals on the connector for the Fabric Device, these two signals are marked as reserved.

22 **4.13 JTAG**

The JTAG interface follows standard IEEE1149 with the chain inside the Fabric Device. This interface should be used for any components that get reprogrammed via JTAG.

25 4.14 Slot Address

26 The 4 bits of slot address indicate to the Fabric Device what slot in an enclosure it is installed in.

27 **4.15 Present**

- 28 PRSNT_L is an active low signal that indicates the Fabric Device is present in the system. This signal shall be pulled 29 to ground through a 1000hm resistor on the Fabric Device.
- 30 BLANK_PRSNT_L is an active low signal to indicate that the Fabric Device is a blank Device and does not have any
- 31 functionality. This signal shall be pulled to ground through a 1000hm resistor on the Fabric Device.

32 **4.16 Reserved**

- 33 There are two (2) reserved pins for future use of Fabric Devices.
- 34

35 **5. Connector Pinout Definition**

DRAFT

1 Table 5-1 Fabric Device Connector Pinout

2

	8	7	6	5	4	3	2	1	
т	AC_OK_L	GND	PWR_OK_L_IN	GND	UART_RX	GND	UART_TX	GND	т
S	GND	PORT_A_2N_O UT	GND	PORT_A_1N_O UT	GND	PORT_B_2N_O UT	GND	PORT_B_1N_O UT	s
R	PORT_A_4N_O UT	PORT_A_2P_O UT	PORT_A_3N_OU T	PORT_A_1P_O UT	PORT_B_4N_OU T	PORT_B_2P_O UT	PORT_B_3N_O UT	PORT_B_1P_0 UT	R
Q	PORT_A_4P_O UT	GND	PORT_A_3P_OU T	GND	PORT_B_4P_OU T	GND	PORT_B_3P_O UT	GND	Q
Р	GND	PORT_A_2N_I N	GND	PORT_A_1N_I N	GND	PORT_B_2N_IN	GND	PORT_B_1N_I N	Р
ο	PORT_A_4N_I N	PORT_A_2P_I N	PORT_A_3N_IN	PORT_A_1P_IN	PORT_B_4N_IN	PORT_B_2P_IN	PORT_B_3N_I N	PORT_B_1P_I N	0
N	PORT_A_4P_I N	GND	PORT_A_3P_IN	GND	PORT_B_4P_IN	GND	PORT_B_3P_I N	GND	N
М	GND	JTAG_TRSTN	GND	PORT_B_RESE TL	GND	PORT_A_RESET L	GND	12V	М
L	SLOT_3_IN	JTAG_TCK	PORT_B_MODP RSL	PORT_B_MODS EL	PORT_A_MODP RSL	PORT_A_MODS EL	I2C_SDA	12V	L
К	SLOT_2_IN	GND	PORT_B_INTL	GND	PORT_A_INTL	GND	I2C_SCL	GND	К
J	GND	JTAG_TMS	GND	RESERVED2	GND	FLT_LED_IN	GND	12V	J
Ι	SLOT_1_IN	JTAG_TDO	PORT_B_3V3	RESERVED1	PORT_A_3V3	ID_LED_IN	12V	12V	I
н	SLOT_0_IN	GND	PORT_B_3V3	GND	PORT_A_3V3	GND	12V	GND	н
G	GND	JTAG_TDI	GND	PRSNT_L	GND	OK_LED_IN	GND	12V	G
F	SGMII_N_IN	SYS_ALIVE_H_ IN	PORT_B_LPMOD E	RESET_L_IN	PORT_A_LPMOD E	PORT_B_ACT_L ED	12V	12V	F
E	SGMII_P_IN	GND	PORT_B_I2C_S DA	GND	PORT_A_I2C_S DA	GND	12V	GND	E
D	GND	GPIO_1	GND	PWR_EN_IN	GND	PORT_B_LNK_L ED	GND	12V	D
С	SGMII_N_OUT	GPIO_0	PORT_B_I2C_SC L	INT_L_OUT	PORT_A_I2C_SC L	PORT_A_ACT_L ED	12V	12V	С
В	SGMII_P_OUT	GND	PORT_B_3V3	GND	PORT_A_3V3	GND	12V	GND	В
А	GND	GND	GND	BLANK_PRSNT _L	GND	PORT_A_LNK_L ED	GND	GND	Α
	8	7	6	5	4	3	2	1	

1 6. VPD Contents

2 The Fabric Device has a slave I2C bus that operates at 100kHz. The Fabric Device has a VPD EEPROM located at

2 wire serial interface address 0xA0. The VPD data is set at manufacturing and is not changed during runtime.
 The VPD data is defined in Table 6-1 Vital Product Data. All strings are all 8-bit ASCII, left justified, null terminated,

5 with trailing nulls.

6

7 Table 6-1 Vital Product Data

Addr	Size (B)	R/W	Value type	Function	Default Value	Description
0	1	RO	Unsigned Int	Version	Vendor	Format version
1	3	RO		Version	0	Reserved
4	1	RO	Unsigned Int	Device Class	Vendor	Identifies Device class type
5	1	RO	Unsigned Int	Device Class	Vendor	Identifies Device subclass type
6	40	RO	8-bit ASCII		Vendor	Vendor name string
46	40	RO	8-bit ASCII		Vendor	Serial number string
86	40	RO	8-bit ASCII		Vendor	Model number string
126	40	RO	8-bit ASCII	ID	Vendor	Part number string
166	36	RO	8-bit ASCII		Vendor	UUID string (with hyphens)
202	8	RO	8-bit ASCII		Vendor	MFG Date String "DDMMYYYY"
210	12	RO			0	Reserved
222	1	RO	Unsigned Int		Vendor	Protocol
223	1	RO	Unsigned Int	Fabric	Vendor	Active Ports
224	2	RO			0	Reserved
226	1	RO	Unsigned Int	Port 0	Vendor	Maximum Link speed
227	1	RO	Unsigned Int	FULU	Vendor	Maximum Link width (#)
228	1	RO	Unsigned Int	Port 1	Vendor	Maximum Link speed
229	1	RO	Unsigned Int	FULL	Vendor	Maximum Link width (#)
230	2	RO	Unsigned Int		Vendor	Initial power requirement (W)
232	2	RO	Unsigend Int	Initial Power ¹⁷	Vendor	Initial power duration (ms)
234	2	RO 🗸			0	Reserved
236	2	RO	Unsigned Int	Operational Power ¹⁷	Vendor	Maximum 12V Rail power (W)
238	2	RO	Unsigned Int	Operational Power	Vendor	Minimum 12V Rail power (W)
240	4	RO	Unsigned Int		Vendor	Maximum discharge time (ms)
244	4	RO	Unsigned Int	Power Hold-up ¹⁷	Vendor	Maximum discharge current (mA)
248	4	RO	Unsigned Int		0	Reserved
252	2	RO	Unsigned int	UART	Vendor	Maximum speed (kHz)
254	2	RO	Unsigned int	Extensibility	Vendor	Capability List pointer

8 9

Table 6-2: Device Classes

ID	Device Class
0	Blank
1	Other
2	Storage
3	Memory
4	Compute
5	Uninterruptible Power Supply
6-Fh	Reserved

10

Table 6-3: Storage Subclasses

ID	Device Subclass
0	None
1	Other
2	Solid State Storage
3	Hard Disk Drive
4-Fh	Reserved

1

2 Table 6-4: Compute Subclasses

· · · · · · · · · · · · · · · · · · ·		
ID	Device Subclass	
0	None	
1	Other	
2	CPU	
3	GPU	
4	FPGA	
5	ASIC	
6-Fh	Reserved	

3

4 Table 6-5: Memory Subclasses

ID	Device Subclass
0	None
1	Other
2	Volatile Memory
3	Non-Volatile Memory
4-Fh	Reserved

5

6 **Table 6-6: Power Storage Subclasses**

ID	Device Subclass
0	None
1	Other
2	Battery
3	Capacitor
4-Fh	Reserved

7

8 Table 6-7: Protocols

ID	Device
0	None
1	Other
2	Ethernet
3	Infiniband
4	PCIe
5	Fibre Channel
6	Gen-Z
7	SAS
8-Fh	Reserved

9 10

Table 6-8: Active Ports

ID	Device
0	No ports active
1	Port 0 active
2	Port 1 active
3	Both ports active
4-Fh	Reserved

1

2 Table 6-9: Link Speeds

ID	Device
0	None
1	Other
2	1 Gb
3	6 Gb
4	10 Gb
5	12 Gb
6	16 Gb
7	24 Gb
8	25 Gb
9	32 Gb
А	56 Gb
B-Fh	Reserved

3

4 6.1 Initial Power

5 The initial power fields are intended to describe power draw behavior that is transient shortly after power on. For 6 example, a Device may need to charge power loss protection capacitors and will draw a higher than maximum 7 operational power until charged.

8 6.2 Operational Power

9 These fields indicate the power consumption limits under normal operation. The maximum power field indicates 10 what the maximum power that this Device will consume is. The minimum power field indicates the minimum power 11 required for this Device to function. Powering the Device at minimum power does not guarantee any level of 12 performance. The minimum power level is meant to indicate what the minimum power for this Device to respond 13 to requests over the fabric interfaces.

14 **6.3 Power Hold Up**

The power hold-up fields are meant to describe behavior of the Device after a power loss event. For a Power storage Device, these fields can be used to determine how long it can sustain other Devices in the enclosure. For a non-power storage Device, these fields indicate how long the Device will remain operational under its own internal holdup power.

19 6.4 Capability List

20 The capability list allows for the discovery of optional extended features. These structures are optional. The data structure is constructed as a linked list. The pointer (if any) located at offset 254, points to the first capability 21 22 structure whose format is shown in Table 6-10 I2C Standard Capability Data Structure. The Capability data structure 23 has a 4-byte header. The first 2 bytes identify the Capability ID of the feature. A Capability ID of 0xFE indicates a 24 vendor specific capability as shown in Table 6-11 I2C Vendor Specific Capability Data Structure. The second two 25 bytes of the capability header are Next Address field and contain a pointer to the next capability in the list. 26 Subsequent bytes are defined by each specific capability or are vendor specific. A value of zero in the Next Address 27 field indicates the end of the linked list.

1 6.5 Standard Capability Data Structure

2 Table 6-10 I2C Standard Capability Data Structure

Byte 3	Byte 2	Byte 1	Byte 0
Next Address Pointer		Capability ID	
Optional parameters specific to each capability			

4 6.6 Vendor Specific Capability Data Structure

Table 6-11 I2C Vendor Specific Capability Data Structure

Byte 3	Byte 2	Byte 1	Byte 0		
Next Address Pointer		0xFE			
Optional parameters specific to each capability					

5

3

6 7. Dynamic Data

7 Optional Dynamic Data are hosted by a Device on the I2C bus at address 0x30 (i.e., slave address bits 7-0 8 correspond to 0011 000). The dynamic data is a single 128-byte vendor defined register. As the primary method 9 of interfacing with the Fabric Device from the chassis management processor is the internal 1Gb Ethernet link, the 10 use of the Dynamic Data over I2C interface is to provide diagnostic information as to why that internal 1Gb Ethernet 11 link is not viable. As the usage of the Dynamic Data is to help with debugging efforts, the data layout and fields are not defined in this standard and are to be set by each Device vendor. The purpose of defining the Dynamic 12 Data address 0x30 and length of 128 Bytes is to allow management software utilities and applications to acquire a 13 14 standardized quantity of data from any Device that may then be passed on to Customer Support Representatives for interpretation 15