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SFF-9402

Reference Guide for

Multi-Protocol Internal Cables for SAS and/or PCIe

Rev 1.0 July 18, 2018

Secretariat: SFF TA TWG

Abstract: This reference guide provides a common naming convention and signal direction for SAS and PCI Express® cables. The purpose is to eliminate the confusion between CPU (PCIe) and Drive (SAS) centric solutions so that TX is always the input and RX is the output from the cable. The PCIe and SAS specifications employ different unique naming conventions making it difficult to create a multiprotocol cable pinout. It also recommends the pinouts for employing legacy connectors for these applications.

This document provides an implementation guide for systems manufacturers, system integrators, and suppliers. This is an internal working document of the SFF Committee, an industry ad hoc group.

This reference guide is made available for public review, and written comments are solicited from readers. Comments received will be considered for inclusion in future revisions of this document.

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Intellectual Property

The user's attention is called to the possibility that implementation of this Specification may require the use of an invention covered by patent rights. By distribution of this specification, no position is taken with respect to the validity of a claim or claims or of any patent rights in connection therewith.

This specification is considered SNIA Architecture and is covered by the SNIA IP Policy and as a result goes through a request for disclosure when it is published. Additional information can be found at the following locations:

- Results of IP Disclosures: <http://www.snia.org/sffdisclosures>
- SNIA IP Policy: <http://www.snia.org/ippolicy>

Change History

Rev 0.2 March 1, 2016

- Introduced as a Reference Guide

Rev 0.5 April 25, 2016

- Informal work group approved new Sideband assignments for MiniLink and Ultraport SlimSAS™
- Sideband naming revised - removed references to Sidebands 8 and 9, added in the alternate (A Sidebands for 0 and 1
- Added SClock to Sideband 0 and SLoad to Sideband 1
- Sideband 2 replaced Sideband 8//VSP8 was renamed VSP2
- Sideband 3 replaced Sideband 9//VSP9 was renamed VSP3

Rev 0.6 August 8, 2016

- Content completely restructured to clarify the presentation of the solutions.
- Pinouts did not change from previous revision.
- Additional tables provided to separate applications
- Added alternate pinout for legacy PCI Express® REFCLK implementation.

Rev 0.7 "(prior to comments)" September 12, 2016

- There are "NO" changes to any signal/ pin assignments with this revision.
- Section 4 item 6 include SFF-8485 next to SGPIO
- Section 4 item 11 spelled out Vendor Specific Pins to identify the VSP abbreviation.
- Section 4 item 12 changed 2-Wire types names from 2-Wire S-Type to Standard 2-Wire Type, 2-Wire A-Type to Other 2-Wire Type and added definition about signal logic level for the sidebands.
- In section 4 item 13 changed Backplane Type to Backplane_Type (BP_Type) to match SFF-8448
- Updated tables (All) signal naming conventions associated with PCIe and SAS
- Updated PCIe only tables to show their naming convention only.
- Updated SAS only tables to show their naming convention only
- Changed references from SFF-8612 to SFF-8611
- Renamed Nano-Pitch I/O™ to OCuLink or MiniLink where applicable throughout the document
- Renamed iPass+™ HD to Mini SAS HD or SFF-8643 where applicable throughout the document.
- Updated section 6 alternate sideband assignment to include improved board layout
- Added additional description about the use of color coding plus italics to show the difference between the two protocols
- Added definition of NC as "no connect"
- Added SFF-9639 Multifunction 6X Unshielded Connector Pinouts to the reference section

Rev 0.7J “(Includes Rev 0.7H plus comment resolutions to create Rev 0.7J (green text))” December 12, 2016

- Updated document header information
- Change document to show SNIA format.
- Updated Title description
- Changed the word “specification” to “Reference Guide or “document” where applicable throughout to indicate this is a reference document and not a specification.
- Updated Points of Contact
- Added dates to the different Change history rev levels.
- Updated Forward to reflect SNIA format
- Changes incorporated are editorial clarifications plus the removal of proposed mini-SAS HD Alternate for PCIe cable solutions per user comment.
- Reworded the abstract to clarify the purpose of this Reference Guide.
- Removed the Note:Content completely restructured to clarify the presentation of the solutions.
- Updated the Rev 0.7 revision section to correct typos.
- Section 1 Replaced Purpose with Scope and updated the statement.
- Added Section 1.1 Copyright for SNIA format
- Added Section 1.2 Disclaimer for SNIA format
- Section 2.1 Industry Documents, Added SFF-8485, SAS-3, SAS-4, SES-2 and SES-3
- Section 2.2 replaced with sources per SNIA format
- Added Section 2.3 Conventions per SNIA format
- Added Section 2.4 Definitions per SNIA format
- Throughout document changed SFF-8611 to SFF-8621 to include both the fixed (SFF-8612) and free (SFF-8611) interfaces.
- Throughout document changed Slimline SAS to SFF-8654
- All the tables and document headings in this document were updated to just show the SFF associated with the connector and removed the connector names to eliminate any issues with abbreviated trademark names.
- Section 4 updated opening sentence
- Section 4 Item 1 defined what is considered Other Protocol (O/P)
- Section 4 Item 2 replaced PCI Express® with Other Protocol implementations
- Section 4 Item 3 defined what connectors are considered Legacy.
- Section 4 Item 4 added the word signals after (HCSL).
- Section 4 Item 7 removed must be “SFF-9402 AWARE” and reworded sentence to “implementations must be aware”
- Section 4 Item 10 “New Item/ Definition” now defines signals and convention follow OCuLink specification (Prev. item 10 now 12)
- Section 4 Item 11 “New Item/ Definition” for device connections in tables (Prev. item 11 now 13)
- Section 4 Item 13 (Prev. Item 11) removed PCI Express® and indicated sidebands based on OCuLink and SFF-8448
- Section 4 Item 14 (Prev. Item 12) changed PCIe x8 to Other Protocol (x8) implementations.
- Section 4 Item 15 (Prev. Item 13) removed PCI Express® and replaced with OCuLink and Other Protocol.
- Section 4 Item 15b (Prev. Item 13b) removed PCI Express® replaced with SFF-8448 to indicate common 2-Wire signals
- Section 4 Item 16 (Prev. Item 14) improved the wording for full crossover cables and replaced specification with reference guide.
- Section 4 Item 17 “New item/ Definition” Added definition/ description about 3.3 Vact TX and RX usage.
- Section 4 Item 18 “New item/ Definition” Added definition/ description about Power 5V#1/ #2.
- Section 4 Item 19 was Item 15 in the previous level.
- Section 4 Previous Item 16 about REFCLK optimization was removed.
- Section 4 Item 19 (Prev. Item 15) reworded the first part of the sentence.

- Section 4 Item 20 (Prev. Item 17) changed legacy to SFF-8087/ SFF-8643 and Slimline SAS to SFF-8654.
- Section 4 Item 21 combined old Item 18 and 19 define the use of OCuLink signal naming convention.
- Section 4 Added Item 22 about CWAKE# / OBFF implementation.
- Section 4 Added Item 23 about CPERST# implementation.
- Section 5 Updated opening sentence such that references to x8 SFF-8621 or SFF-8654 are considered Other Protocol
- Section 5 Second paragraph grammar correction added associated prior to (PERST[A,B]#/ CPRSNT[A,B]#)
- Section 5 Third paragraph removed PCI Express® and replaced with OCuLink/ Other Protocol
- Section 5 Third paragraph changed state about reserve pins as no connects to “NO WIRE” Power pins being “NO WIRE”
- Section 5 Item 1 replaced PCI Express® with OCuLink and Other Protocol where applicable
- Section 5 Item 2 replaced PCI Express® (x8) with Other Protocol (x8)
- Section 5 Item 2a replaced “It is still recommended that pins associated with” with “must be” for the diff pairs
- Section 5 Item 3 replaced PCI Express® (x8) with Other Protocol.
- Table 5-1 Removed references to x8 PCIe, PCI Express® with the exception of the U.2 device
- Table 5-1 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module and MultiLink
- Table 5-1 Changed the endpoint high speed naming convention to match the OCuLink specification.
- Table 5-1 Changed NC to NO WIRE and changed the reserve pins for OCuLink to the Power pins called out in OCuLink specification external only.
- Table 5-1 Arrows cover SAS, OCuLink and Other Protocol. Dots were changed to dashes.
- Table 5-1 VSP+/- must be updated in OCuLink Specification
- Table 5-1 CWAKE#/OBFF (VSP) must be reflected in OCuLink.
- Table 5-2 Removed references to x8 PCIe, PCI Express® with the exception of the U.2 device
- Table 5-2 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module and MultiLink
- Table 5-2 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
- Table 5-2 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only
- Table 5-2 Removed double ground assignments A19 and B19 in tables
- Table 5-2 Arrows cover SAS, and Other Protocol. Dots were changed to dashes.
- Table 5-2 VSP+/- must be reflected in Other Protocol
- Table 5-2 CWAKE#/OBFF (VSP) must be reflected in OCuLink Specification
- Table 5-3 Removed references to x8 PCIe, PCI Express® with the exception of the U.2 device
- Table 5-3 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module and MultiLink
- Table 5-3 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
- Table 5-3 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only
- Table 5-3 Double ground assignments A19 and B19 still required for Y-cables
- Table 5-3 Arrows cover SAS, and Other Protocol. Dots were changed to dashes.
- Table 5-3 VSP+/- must be reflected in Other Protocol
- Section 6 Heading - removed PCI Express® replaced with OCuLink and added Other Protocol (O/P)
- Section 6 Opening sentence removed PCI Express® added (O/P)
- Section 6 First paragraph (Prev. version), about the alternate sideband pin assignments was removed.
- Section 6 First paragraph (Second in Prev. version) removed PCI Express® and reworded the description about the highlighted diff pairs in the table including the x8
- Section 6 Second paragraph (Third in Prev. version) removed PCI Express® and replaced with OCuLink, Other Protocol.
- Added new statement about pins designated as “POWER”
- Section 6 Item 1 Removed PCI Express® defined connectors that were not OCuLink x4 as Other Protocol x4/ x8 SFF-8621, SFF-8654 and SFF-8643.
- Section 6 Item 2 Replaced PCI Express® with Other Protocol (x8) updated to SFF-8654
- Section 6 Item 2 Updated description about pins associated with REFCLK must be wired as differential pairs.

- Section 6 Item 3 Replaced PCI Express® with Other Protocol
- Section 6 Item 3 Replaced “It is still recommended that pins associated with” with “must be”
- Table 6-1 Heading changed PCI Express® to OCuLink and added Other Protocol
- Table 6-1 Changed SFF-8643/ SFF-8654 from PCI Express® to Other Protocol (O/P)
- Table 6-1 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only.
- Table 6-1 Removed columns for mini-SAS HD (SFF-8643) Alternate.
- Table 6-1 VSP+/- must be updated in OCuLink specification.
- Table 6-1 CWAKE#/OBFF (VSP) must be reflected in OCuLink specification.
- Table 6-1 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
- Table 6-1 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module
- Table 6-1 Changed Dots to dashes for the grounds.
- Table 6-2 Heading changed PCI Express® to OCuLink and added Other
- Table 6-2 Changed SFF-8643, SFF-8654 (x8) and MiniLink (x8) from PCI Express® to Other Protocol (O/P)
- Table 6-2 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only.
- Table 6-2 Removed columns for mini-SAS HD (SFF-8643) Alternate.
- Table 6-2 Changed Dots to dashes for the grounds.
- Table 6-2 VSP+/- [A,B] must be updated in Other Protocol to line up with OCuLink
- Table 6-2 CWAKE#/OBFF (VSP) [A, B] and must be reflected in Other Protocol to line up with OCuLink
- Table 6-2 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
- Table 6-2 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module
- Table 6-2 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only.
- Table 6-3 Heading changed PCI Express® to OCuLink and added Other Protocol
- Table 6-3 Changed SFF-8643, SFF-8654 (x8) and MiniLink (x8) from PCI Express® to Other Protocol (O/P)
- Table 6-3 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only.
- Table 6-3 Removed columns for mini-SAS HD (SFF-8643) Alternate.
- Table 6-3 Changed Dots to dashes for the grounds.
- Table 6-3 Table 6-3 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
- Table 6-3 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module
- Table 6-3 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only.
- Table 6-4 Heading - Removed PCI Express® added Other Protocol
- Table 6-4 All x8 connectors, SFF-8654 and SFF-8643 defined as Other Protocol.
- Table 6-4 Removed columns for mini-SAS HD (SFF-8643) Alternate.
- Table 6-4 Changed Dots to dashes for the grounds.
- Table 6-4 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
- Table 6-4 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module
- Table 6-4 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external
- Table 6-4 CWAKE#/OBFF (VSP) [A, B] and must be reflected in Other Protocol to line up with OCuLink.
- Table 6-4 VSP+/- [A, B] must be updated in Other Protocol to line up with OCuLink specification.
- Table 6-5 Heading - Removed PCI Express® added Other Protocol
- Table 6-5 All x8 connectors, SFF-8654 and SFF-8643 defined as Other Protocol.
- Table 6-5 Removed columns for mini-SAS HD (SFF-8643) Alternate.

- Table 6-5 Changed Dots to dashes for the grounds.
 - Table 6-5 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external
 - Table 6-5 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
 - Table 6-5 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module
 - Section 7 Updated heading
 - Section 7 Updated opening sentence
 - Section 7 Changed SFF-8611 to SFF-8621
 - Section 7 Items 1-4 changed SFF-8611 to SFF-8621.
 - Section 7 Item 5 Added (SFF-8621/SFF-8654) after SAS-4 and (SFF-8643/ SFF-8087) after Legacy.
 - Section 7 Item 5 added second sentence inserted Sideband in front of signals are “highlighted”.
 - Tables 7-1 through 7-6 headings changed SFF-8611 to SFF-8621
 - Tables 7-1 through 7-6 Changed dots to dashes for the grounds
 - Tables 7-1 through 7-6 Changed Device column to SFF-8639/ U.2 connector versus Multilink
 - Tables 7-7 Added connector name above their associated SFF designations and changed dots to dashes for the grounds.
- Rev 0.7.1 (July 6, 2018):
- Replaced “Reference Guide” with “Published” in header
 - Added “Reference” watermark

REFERENCE

Foreword

The development work on this reference guide was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors. The SFF Committee provided a forum for system integrators and vendors to define the form factor of disk drives.

During their definition, other activities were suggested because participants in SFF faced more challenges than the form factors. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

In July 2016, the SFF Committee transitioned to SNIA (Storage Networking Industry Association), as a TA (Technology Affiliate) TWG (Technical Work Group).

Industry consensus is not a requirement to publish a reference guide because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF meets during the T10 (see www.t10.org) and T11 (see www.t11.org) weeks, and SSWG (Specific Subject Working Groups) are held at the convenience of the participants. Material presented to SFF becomes public domain, and there are no restrictions on the open mailing of the presented material by Members.

Many of the specifications/ reference guides developed by SFF have either been incorporated into standards or adopted as standards by ANSI, EIA, JEDEC and SAE.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at:
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The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:
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Suggestions for improvement of this specification will be welcome, they should be submitted to:
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1 Scope

Industry storage solutions are implementing both SAS and PCIe within the same or similar enclosures. This reference guide recommends the pinning out of cables to accommodate multiple protocols.

1.1 Copyright

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1.2 Disclaimer

The information contained in this publication is subject to change without notice. The SNIA makes no warranty of any kind with regard to this reference guide, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The SNIA shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this document.

Suggestions for revisions should be directed to <http://www.snia.org/feedback/>

2 References

2.1 Industry documents

- PCI Express OCuLink Specification Revision 1.0
- SFF-8087 Mini Multilane 4X Unshielded Connector Shell and Plug
- SFF-8448 SAS Sideband Signal Assignments
- SFF-8485 Specification for Serial GPIO (SGPIO) Bus
- SFF-8621 MiniLink 4/8X I/O Connector and Cable Assemblies
- SFF-8613 Mini Multilane 4/8X Unshielded Connector (HDun)
- SFF-8643 Mini Multilane 4/8X 12 Gb/s Unshielded Connector (HD12un)
- SFF-8673 Mini Multilane 4/8X 24 Gb/s Unshielded Connector (HD24un)
- SFF-8654 0.6mm 4/8X Unshielded I/O Connector
- SFF-9400 Universal 4/8X Pinout
- SFF-9639 Multifunction 6X Unshielded Connector Pinouts
- SCSI Enclosure Services - 2 (SES-2) T10/1559
- SCSI Enclosure Services - 3 (SES-3) T10/2149
- Serial Attached SCSI - 4 (SAS-4) T10/BSR INCITS 534
- Serial Attached SCSI - 3 (SAS-3) T10/2212
- PCI Express® Card Electromechanical (CEM) Specification Revision 3.0

2.2 Sources

There are several projects active within the SFF TWG. The complete list of specifications which have been completed or are still being worked on are listed in <http://www.snia.org/sff/specifications/SFF-8000.TXT>

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (<http://www.techstreet.com/incitsgate.tpm1>).

2.3 Conventions

The dimensioning conventions are described in ANSI-Y14.5M, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

2.4 Definitions

For the purpose of SFF Specifications and Reference Guides, the following definitions apply:

Reserved: Where this term is used for defining the signal on a connector pin its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields and code values; the bits, bytes, fields and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a reserved field or bit as zero, but the receiver should not check reserved fields or bits for zero.

3 General Description

The connector figures below are shown for reference only to show how the pinouts shown in the tables relate to the physical locations of the pins for each of the connector styles. These pinouts comply with the SAS pinouts defined in SFF-8448 and in the PCIe pinouts defined by OCUlink Rev 1.0. All are based on the fixed end definitions of the pin assignments.

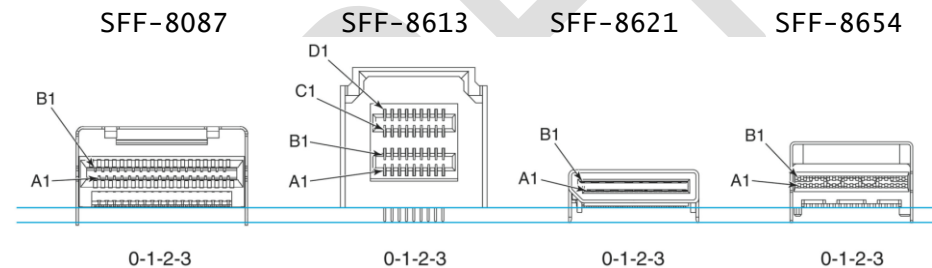


Figure 3-1 Connector Views

4 Pinout Tables with Implementation Notes

The following notes provide background information required to implement universal multiprotocol cables for SAS-4 (Controller/ Backplane/ Device) and OCuLink (Root/ Endpoint/ Device).

System Compatibility Issues

1. Caution - Present PCI Express® internal implementations using SFF-8643/8673/8654 connectors are vendor specific (Not standardized) and are defined in this document as Other Protocol (O/P). They do not align with SAS/SATA legacy SFF-8643/8673 implementations (Some range from 85 to 100 ohms; some have a white ring on fixed ends). As a result, PCIe cables utilizing SFF-8643/8673 connectors used for SFF-9402 can currently be plugged into legacy SAS/SATA implementations resulting in signal incompatibilities.
2. Multiple implementations exist for Other Protocol implementations based on SFF-8643/8673 connectors. SFF-9402 was created based on industry survey to enable a common pin assignment and a cable across multiple interfaces; therefore the previous protocol specific pinouts may not apply.
3. SAS/SATA SFF-8643/ SFF-8087 are defined as Legacy in this document and their internal connector pin assignments are based on SAS 2.1/ SAS-3 T-10 standards and SFF-8448.
4. SFF-9402 was based on, and now supersedes SFF-9401 to provide a common industry two cable solution. SAS-4 reassigned the four SAS sidebands 2, 3, 4, 5 and eliminated designations 8 and 9 for only the MiniLink and Ultraport SlimSAS™ SAS connectors. Moving forward, this provided better optimization of a common cable for SAS/ PCI Express® operation by eliminating the multiple grounds (two pins were freed up) so that SAS single-ended where not shared with PCIe High Speed Current Steering Logic (HCSL) signals. Refer to tables included in SAS-4 and SFF-9402 for their new locations.
5. Changing the pin assignments for SAS-4 impacted cable solutions when migrating from the legacy mini SAS (SFF-8087) / Mini SAS HD (SFF-8643) to MiniLink (SFF-8621) / Ultraport SlimSAS™ (SFF-8654) hybrid cables as follows.
 - a. SAS and OCuLink legacy hybrid solutions currently require independent cables for each specific protocol.
 - b. In addition SAS hybrid cables only are no longer reversible such that they cannot be flipped between controller and backplane. Example: A SAS cable designed such that the controller end is Mini SAS HD and the backplane end is MiniLink cannot be used where the controller has MiniLink and the backplane with Mini SAS HD.
6. SAS standards can incorporate SGPIO (SFF-8485) or Storage Enclosure Services (SES) depending on the physical sideband protocol utilized. SES provides a method to bridge the multiprotocol environment via 2-Wire interface to discover what backplane/end point is present prior to any in-band communication/operation.
7. Controller and Backplane implementations must aware of incompatibility issues with signal levels when migrating from legacy connectors such as SFF-8087/ SFF-8643 to SFF-8621/ SFF-8654 with OCuLink and SAS.
8. SFF-9402 signal assignments are controlled by the “Fixed” side initiator and “Fixed” side backplane only.

9. OCuLink defines the signals based on the "Fixed" ends of the interface. SFF-8448 defines them for SAS and also for the common signals shared with OCuLink.
10. The signal name assignments follow the OCuLink signal convention such that the TX pairs are inputs to and RX pairs are outputs from the cable.
11. Devices connections are defined as SFF-8639/ U.2 connector with pin numbers for PCI Express® and MultiLink SAS™ to eliminate confusion with signal directions between the cable and backplane receptacle connectors.
12. SFF-9400 defines the basic locations of undefined High Speed and Vendor Specific signals for the SFF-8621 and SFF-8654 connectors.
13. SFF-8643 Vendor Specific Pins (VSP)/ sideband assignments are based on the OCuLink and SFF-8448 definitions for consistency.
14. SFF-9402 (like the previous SFF-9401) aligns both OCuLink and SAS sideband assignments via SFF-8448 (SB0-7, SB+/-) where applicable. The addition of "Other 2-Wire Type" to SFF-8448 Rev 1.2 facilitates a common 2-Wire interface and Backplane_Type (BP_Type) for SAS, OCuLink (x4) and Other Protocol (x8) implementations for determining bus type operation. Note - because the use of sideband signals differs between protocols, each sideband signal should be isolated i.e. not commoned in the cable.
 - a. Sidebands 0-7 and VSP pins are defined as single ended, 3.3V logic and use open-drain when sourcing the signals.
 - b. Sidebands SB+/- and VSP+/- utilizes High Speed Current Steering Logic (HCSL) signal levels only.
15. The sidebands signal names shown provide recommended uses for SAS, OCuLink and Other Protocol applications.
 - a. The SAS implementation also includes an associated sideband number as defined in SFF-8448.
 - b. SFF-8448 indicates the common signals between the Standard 2-Wire Type and Other 2-Wire Type. The remaining sidebands are labeled VSP and must refer to the OCuLink 1.0 or later specification.

Implementation Notes:

16. The pinouts in this reference guide define full crossover cables (The A row on one end crosses over to the B row on the other end) unless otherwise noted. This enables the use of ribbon cable construction solutions.
 - a. Based on a full crossover the TX (inputs to the cable at one end) crossover to RX (outputs from the cable at the other end).
 - b. The sideband signals also implement a full crossover such that the Root/ Controller and Endpoint/ Backplane have different fixed end pin assignments.
17. The signals defined as POWER 3.3 Vact TX and POWER 3.3 Vact RX are associated with Active cable applications only.
 - a. These power connections are used for active components within the free ends only and do not propagate down the cable.
 - b. The Root and Endpoint must supply independent voltage sources for their associated fixed end.
 - c. They use the same pin assignments at both ends of the cable.
 - d. They may be commoned at each fixed end.

18. The signals defined as POWER 5 V #1 and POWER 5 V #2 sourced by the Root are specified for "External" applications only.
 - a. These power connections "Do Not" follow the full crossover (A side to B side) used by the signals.
 - b. They use the same pin assignments at both ends of the cable.
 - c. They may be commoned at each fixed end.
19. SAS cables built to this SFF-9402 pinout will still work on old initiators and backplanes based on legacy (SFF-8087 and SFF-8643) SAS pinouts.
20. SAS cables based on SFF-8087/ SFF-8643 and the new SAS-4 SFF-8621/ SFF-8654 which are considered "Hybrid" assemblies but they are no longer reversible. Example: A SAS cable designed such that the controller end is Mini SAS HD and the backplane end is MiniLink cannot be used where the controller has MiniLink and the backplane with Mini SAS HD.
21. These SFF-9402 tables define the lane and polarity of the high speed pairs.
 - a. Utilizes the OCUlink/ Other Protocol signal naming convention
 - b. Lane reversal is not mandatory for end point devices (See the PCI Express® CEM Spec).
22. Sideband signal CWAKE#/ OBFF which is optional, may be used as a VSP or go through some interim control logic between the root and SFF-8639 device itself such that it is not directly connected to the cable interface.
23. Sideband signal PERST# may go through some interim control logic between the root and SFF-8639 device itself such that it is not directly connected to the cable interface.

5 SAS-4 / OCuLink/ Other Protocol Multiprotocol Cables

The following five (5) tables provide signal assignments based on OCuLink, SAS-4 and SFF-8448 for multiprotocol SAS-4 and Other Protocol SFF-8621 (x8), SFF-8654 (x4, x8) applications. In addition cable signal direction and target/ endpoint device connections are also shown.

The high speed differential pairs including the sidebands for REFCLK (VSP+/-) and their reversible path (PERST#/ CPRSNT#) respectively are highlighted/ shaded in the x4 along with (VSP[A,B]+/-) and their associated (PERST[A,B]#/ CPRSNT[A,B]#) x8 connections. They must be wired as differential pairs to enable the cable being flipped between Root and Endpoint.

The high speed differential and sideband signals are color coded (SAS=Blue and OCuLink / Other Protocol=Green/ Italic) to indicate their associated naming convention and protocol. The arrows provide the signal flow direction between the Root/ Controller and Endpoint/ Backplane. In addition brown was used to identify double ground assignments where applicable between different connector types and Y-cables. The Reserved and Power pin connections between the Root/ Controller and Endpoint/ Backplane are defined as "NO WIRE".

1. SAS-4/ OCuLink (x4) Multiprotocol Cables

Table 5-1 defines multiprotocol cable interface for SAS-4 (SFF-8621, SFF-8654)/ OCuLink (SFF-8621)/ Other Protocol (SFF-8654) x4 connections only. These cables are fully reversible such that they can be flipped end to end between Controller/ Root and Backplane/ Endpoint

2. SAS-4/ Other Protocol (x8) Multiprotocol Cables

Table 5-2 and 5-3 defines multiprotocol cable interface for SAS/ Other Protocol for SFF-8621/ SFF-8654 x8 connections only. These cables are fully reversible such that they can be flipped end to end between Controller/ Root and Backplane/ Endpoint

a. Note: In the x8 configuration the sidebands designated with an "A" suffix are considered the primary path when only a single set of sidebands are required to manage the bus. The sideband bus with a "B" suffix is also shown with VSP indicating possible vendor specification. The pins associated with REFCLKB+/- (VSPB+/-) and PERSTB#/ CPRSNTB#) must be wired as differential pairs. Note: VSP[A,B]+/- are defined as High Speed Current Steering Logic (HSCL).

3. SAS-4/ Other Protocol (SFF-8621, SFF8654) (x8) to OCuLink/ MiniLink (SFF-8621) and Other Protocol (SFF-8654) Y-Cables

Table 5-4 and 5-5 define multiprotocol the cable interface for SAS/ Other Protocol for SFF-8621 / SFF-8654 x8 to a pair of x4 OCuLink or Other Protocol connections only. These cables are fully reversible such that they can be flipped end to end between Controller/ Root and Backplane/ Endpoint.

a. Note: Both sets of sidebands (A and B) are required to support a Y-cable configuration where two independent x4 interfaces are connected to a single x8 interface as described in the previous table.

Table 5-1 SAS-4/ OCuLink/ Other Protocol (x4) Cables (1 of 1)

SAS-4/ OCuLink / Other Protocol x4 Cables (Sheet 1 of 1)											
9400 Rev 0.2	Root / Controller				CABLE	Endpoint / Backplane				DEVICE(s)	
	SFF-8654 (38 Circuit)	SFF-8621 (42 Circuit)	9402 Multi-Protocol (OCuLink, Other Protocol (O/P), SAS-4) x4 Cable Interface			9402 Multi-Protocol (OCuLink, Other Protocol (O/P), SAS-4) x4 Cable Interface		SFF-8621 (42 Circuit)	SFF-8654 (38 Circuit)	SFF-8639 / U.2 Connector	
Type 1 4X	O/P SAS-4	OCuLink / SAS-4	OCuLink and SAS-4/ SFF-8448 Signal Names			OCuLink and SAS-4/ SFF-8448 Signal Names		OCuLink / SAS-4	O/P SAS-4	PCI Express® (x4) PIN	MultiLink SAS™ PIN
	PIN	PIN	ROOT	Controller	DIR	Endpoint	Backplane	PIN	PIN		
RSV		A1	POWER 3.3 Vact RX	RESERVED	NO WIRE	POWER 5 V #1	RESERVED	B1			
GND	A1	A2	GROUND	GROUND	—	GROUND	GROUND	B2	B1		
HS	A2	A3	PERp0	RX0+	←	PETp0	TX0+	B3	B2	E14 (PERp0)	S6 (TX0+)
HS	A3	A4	PERn0	RX0-	←	PETn0	TX0-	B4	B3	E13 (PERn0)	S5 (TX0-)
GND	A4	A5	GROUND	GROUND	—	GROUND	GROUND	B5	B4		
HS	A5	A6	PERp1	RX1+	←	PETp1	TX1+	B6	B5	S21 (PERp1)	S13 (TX1+)
HS	A6	A7	PERn1	RX1-	←	PETn1	TX1-	B7	B6	S20 (PERn1)	S12 (TX1-)
GND	A7	A8	GROUND	GROUND	—	GROUND	GROUND	B8	B7		
SB	A8	A9	BP_TYPE (VSP)	BP_TYPE(SB7)	↔	BP_TYPE(VSP)	BP_TYPE (SB7)	B9	B8		
SB	A9	A10	CWAKE#,OBFF (VSP)	RESET, SDataOut(SB4)	↔	CWAKE#,OBFF(VSP)	RESET, SDataOut (SB4)	B10	B9	P1 (WAKE#)	
SB	A10	A11	GND	GND(SB3)	—	GND	GND(SB3)	B11	B10		
SB	A11	A12	REFCLK+(VSP+)	(SB+)	→	REFCLK+(VSP+)	(SB+)	B12	B11	E7 (REFCLK+)	
SB	A12	A13	REFCLK-(VSP-)	(SB-)	→	REFCLK-(VSP-)	(SB-)	B13	B12	E8 (REFCLK-)	
GND	A13	A14	GROUND	GROUND	—	GROUND	GROUND	B14	B13		
HS	A14	A15	PERp2	RX2+	←	PETp2	TX2+	B15	B14	S27 (PERp2)	S21 (TX2+)
HS	A15	A16	PERn2	RX2-	←	PETn2	TX2-	B16	B15	S26 (PERn2)	S20 (TX2-)
GND	A16	A17	GROUND	GROUND	—	GROUND	GROUND	B17	B16		
HS	A17	A18	PERp3	RX3+	←	PETp3	TX3+	B18	B17	E21 (PERp3)	S27 (TX3+)
HS	A18	A19	PERn3	RX3-	←	PETn3	TX3-	B19	B18	E20 (PERn3)	S26 (TX3-)
GND	A19	A20	GROUND	GROUND	—	GROUND	GROUND	B20	B19		
RSV		A21	POWER 5 V #2	RESERVED	NO WIRE	POWER 3.3 Vact TX	RESERVED	B21			
RSV		B1	POWER 5 V #1	RESERVED	NO WIRE	POWER 3.3 Vact RX	RESERVED	A1			
GND	B1	B2	GROUND	GROUND	—	GROUND	GROUND	A2	A1		
HS	B2	B3	PETp0	TX0+	→	PERp0	RX0+	A3	A2	E10 (PETp0)	S2 (RX0+)
HS	B3	B4	PETn0	TX0-	→	PERn0	RX0-	A4	A3	E11 (PETn0)	S3 (RX0-)
GND	B4	B5	GROUND	GROUND	—	GROUND	GROUND	A5	A4		
HS	B5	B6	PETp1	TX1+	→	PERp1	RX1+	A6	A5	S17 (PETp1)	S9 (RX1+)
HS	B6	B7	PETn1	TX1-	→	PERn1	RX1-	A7	A6	S18 (PETn1)	S10 (RX1-)
GND	B7	B8	GROUND	GROUND	—	GROUND	GROUND	A8	A7		
SB	B8	B9	2W-CLK	2W-CLK, SClock(SB0)	↔	2W-CLK	2W-CLK, Sclock (SB0)	A9	A8		
SB	B9	B10	2W-DATA	2W-DATA, SLoad(SB1)	↔	2W-DATA	2W-DATA, Sload(SB1)	A10	A9		
SB	B10	B11	GND	GND (SB2)	—	GND	GND(SB2)	A11	A10		
SB	B11	B12	PERST#	ADD, SDataIn(SB5)	↔	PERST#	ADD, SDataIn(SB5)	A12	A11	E5 (PERST#)	
SB	B12	B13	CPRSNT#	CNTRLR_TYPE(SB6)	↔	CPRSNT#	CNTRLR_TYPE(SB6)	A13	A12		
GND	B13	B14	GROUND	GROUND	—	GROUND	GROUND	A14	A13		
HS	B14	B15	PETp2	TX2+	→	PERp2	RX2+	A15	A14	S23 (PETp2)	S17 (RX2+)
HS	B15	B16	PETn2	TX2-	→	PERn2	RX2-	A16	A15	S24 (PETn2)	S18 (RX2-)
GND	B16	B17	GROUND	GROUND	—	GROUND	GROUND	A17	A16		
HS	B17	B18	PETp3	TX3+	→	PERp3	RX3+	A18	A17	E17 (PETp3)	S23 (RX3+)
HS	B18	B19	PETn3 /	TX3-	→	PERn3	RX3-	A19	A18	E18 (PETn3)	S24 (RX3-)
GND	B19	B20	GROUND	GROUND	—	GROUND	GROUND	A20	A19		
RSV		B21	POWER 3.3 Vact TX	RESERVED	NO WIRE	POWER 5 V #2	RESERVED	A21			

Table 5-2 SAS-4/ SFF-8621/ SFF-8654 Other Protocol(x8) Cables (1 of 2)

SAS-4/ Other Protocol x8 Cables (Sheet 1 of 2)											
	Root / Controller					Endpoint / Backplane				DEVICE(s)	
9400 Rev 0.2	SFF-8654 (74 Circuit)	SFF-8621 (80 Circuit)	9402 Multi-Protocol (Other Protocol (O/P), SAS-4))		CABLE	9402 Multi-Protocol (Other Protocol (O/P), SAS-4))		SFF-8621 (80 Circuit)	SFF-8654 (74Circuit)	SFF-8639 / U.2 Connector (Pair of x4 devices)	
Type 1 8X	O/P SAS-4	O/P SAS-4	Other Protocol and SAS-4/ SFF-8448 Signal Names			Other Protocol and SAS-4/ SFF-8448 Signal Names		O/P SAS-4	O/P SAS-4	PCI Express® (x4)	MultiLink SAS™
	PIN	PIN	ROOT	Controller	DIR	Endpoint	Backplane	PIN	PIN	PIN	PIN
GND	A1	A1	GROUND	GROUND	—	GROUND	GROUND	B1	B1		
HS	A2	A2	PERp0	RX0+	←	PETp0	TX0+	B2	B2	E14 (PERp0)	S6 (TX0+)
HS	A3	A3	PERn0	RX0-	←	PETn0	TX0-	B3	B3	E13 (PERn0)	S5 (TX0-)
GND	A4	A4	GROUND	GROUND	—	GROUND	GROUND	B4	B4		
HS	A5	A5	PERp1	RX1+	←	PETp1	TX1+	B5	B5	S21 (PERp1)	S13 (TX1+)
HS	A6	A6	PERn1	RX1-	←	PETn1	TX1-	B6	B6	S20 (PERn1)	S12 (TX1-)
GND	A7	A7	GROUND	GROUND	—	GROUND	GROUND	B7	B7		
SB	A8	A8	BP_TYPEA(VSPA)	BP_TYPEA (SB7A)	↔	BP_TYPEA(VSPA)	BP_TYPEA(SB7A)	B8	B8		
SB	A9	A9	CWAKEA#,OBFFA (VSPA)	RESETA, SDataOutA (SB4A)	↔	CWAKEA#,OBFFA(VSPA)	RESETA, SDataOutA(SB4A)	B9	B9	P1 (WAKE#)	
SB	A10	A10	GROUND	GROUND (SB3A)	—	GROUND	GROUND (SB3A)	B10	B10		
SB	A11	A11	REFCLKA+(VSPA+)	(SBA+)	→	REFCLKA+(VSPA+)	(SBA+)	B11	B11	E7 (REFCLK+)	
SB	A12	A12	REFCLKA-(VSPA-)	(SBA-)	→	REFCLKA-(VSPA-)	(SBA-)	B12	B12	E8 (REFCLK-)	
GND	A13	A13	GROUND	GROUND	—	GROUND	GROUND	B13	B13		
HS	A14	A14	PERp2	RX2+	←	PETp2	TX2+	B14	B14	S27 (PERp2)	S21 (TX2+)
HS	A15	A15	PERn2	RX2-	←	PETn2	TX2-	B15	B15	S26 (PERn2)	S20 (TX2-)
GND	A16	A16	GROUND	GROUND	—	GROUND	GROUND	B16	B16		
HS	A17	A17	PERp3	RX3+	←	PETp3	TX3+	B17	B17	E21 (PERp3)	S27 (TX3+)
HS	A18	A18	PERn3	RX3-	←	PETn3	TX3-	B18	B18	E20 (PERn3)	S26 (TX3-)
GND	A19	A19	GROUND	GROUND	—	GROUND	GROUND	B19	B19		
RSV		A20	POWER 3.3 Vact RX	RESERVED	NO WIRE	POWER 5V #1	RESERVED	B20			
RSV		A21	POWER 3.3 Vact TX	RESERVED	NO WIRE	POWER 5V #2	RESERVED	B21			
GND		A22	GROUND	GROUND	—	GROUND	GROUND	B22			
HS	A20	A23	PERp4	RX4+	←	PETp4	TX4+	B23	B20	E14 (PERp0)	S6 (TX0+)
HS	A21	A24	PERn4	RX4-	←	PETn4	TX4-	B24	B21	E13 (PERn0)	S5 (TX0-)
GND	A22	A25	GROUND	GROUND	—	GROUND	GROUND	B25	B22		
HS	A23	A26	PERp5	RX5+	←	PETp5	TX5+	B26	B23	S21 (PERp1)	S13 (TX1+)
HS	A24	A27	PERn5	RX5-	←	PETn5	TX5-	B27	B24	S20 (PERn1)	S12 (TX1-)
GND	A25	A28	GROUND	GROUND	—	GROUND	GROUND	B28	B25		
SB	A26	A29	BP_TYPEB (VSPB)	BP_TYPEB (SB7B)	↔	BP_TYPEB(VSPB)	BP_TYPEB(SB7B)	B29	B26		
SB	A27	A30	CWAKEB#,OBFFB (VSPB)	RESETB, SDataOutB (SB4B)	↔	CWAKEB#,OBFFB(VSPB)	RESETB, SDataOutB (SB4B)	B30	B27	P1 (WAKE#)	
SB	A28	A31	GROUND	GROUND (SB3B)	—	GROUND	GROUND (SB3B)	B31	B28		
SB	A29	A32	REFCLKB+ (VSPB+)	(SBB+)	→	REFCLKB+(VSPB+)	(SBB+)	B32	B29	E7 (REFCLK+)	
SB	A30	A33	REFCLKB- (VSPB-)	(SBB-)	→	REFCLKB- (VSPB-)	(SBB-)	B33	B30	E8 (REFCLK-)	
GND	A31	A34	GROUND	GROUND	—	GROUND	GROUND	B34	B31		
HS	A32	A35	PERp6	RX6+	←	PETp6	TX6+	B35	B32	S27 (PERp2)	S21 (TX2+)
HS	A33	A36	PERn6	RX6-	←	PETn6	TX6-	B36	B33	S26 (PERn2)	S20 (TX2-)
GND	A34	A37	GROUND	GROUND	—	GROUND	GROUND	B37	B34		
HS	A35	A38	PERp7	RX7+	←	PETp7	TX7+	B38	B35	E21 (PERp3)	S27 (TX3+)
HS	A36	A39	PERn7	RX7-	←	PETn7	TX7-	B39	B36	E20 (PERn3)	S26 (TX3-)
GND	A37	A40	GROUND	GROUND	—	GROUND	GROUND	B40	B37		

Table 5-3 SAS-4/ SFF-8621/ SFF-8654 Other Protocol(x8) Cables (2 of 2)

SAS-4/ Other Protocol x8 Cables (Sheet 2 of 2)											
	Root / Controller					Endpoint / Backplane				DEVICE(s)	
9400 Rev 0.2	SFF-8654 (74 Circuit)	SFF-8621 (80 Circuit)	9402 Multi-Protocol (Other Protocol (O/P), SAS-4)		CABLE	9402 Multi-Protocol (Other Protocol (O/P), SAS-4)		SFF-8621 (80 Circuit)	SFF-8654 (74Circuit)	SFF-8639 / U.2 Connector (Pair of x4 devices)	
Type 1 8X	O/P SAS-4	O/P SAS-4	Other Protocol and SAS-4/ SFF-8448 Signal Names			Other Protocol and SAS-4/ SFF-8448 Signal Names		O/P SAS-4	O/P SAS-4	PCI Express® (x4)	Multilink SAS™
	PIN	PIN	ROOT	Controller	DIR	Endpoint	Backplane	PIN	PIN	PIN	PIN
GND	B1	B1	GROUND	GROUND	—	GROUND	GROUND	A1	A1		
HS	B2	B2	PETp0	TX0+	→	PERp0	RX0+	A2	A2	E10 (PETp0)	S2 (RX0+)
HS	B3	B3	PETn0	TX0-	→	PERn0	RX0-	A3	A3	E11 (PETn0)	S3 (RX0-)
GND	B4	B4	GROUND	GROUND	—	GROUND	GROUND	A4	A4		
HS	B5	B5	PETp1	TX1+	→	PERp1	RX1+	A5	A5	S17 (PETp1)	S9 (RX1+)
HS	B6	B6	PETn1	TX1-	→	PERn1	RX1-	A6	A6	S18 (PETn1)	S10 (RX1-)
GND	B7	B7	GROUND	GROUND	—	GROUND	GROUND	A7	A7		
SB	B8	B8	2W-CLKA	2W-CLKA, SCLockA (SB0A)	↔	2W-CLKA	2W-CLKA, SCLockA(SB0A)	A8	A8		
SB	B9	B9	2W-DATAA	2W-DATAA, SloadA (SB1A)	↔	2W-DATAA	2W-DATAA, SloadA(SB1A)	A9	A9		
SB	B10	B10	GND	GND (SB2A)	—	GND	GND(SB2A)	A10	A10		
SB	B11	B11	PERSTA#	ADDA, SDataInA (SB5A)	↔	PERSTA#	ADDA, SDataInA(SB5A)	A11	A11	E5 (PERST#)	
SB	B12	B12	CPRSNTA#	CNTRLR_TYPEA (SB6A)	↔	CPRSNTA#	CNTRLR_TYPEA(SB6A)	A12	A12		
GND	B13	B13	GROUND	GROUND	—	GROUND	GROUND	A13	A13		
HS	B14	B14	PETp2	TX2+	→	PERp2	RX2+	A14	A14	S23 (PETp2)	S17 (RX2+)
HS	B15	B15	PETn2	TX2-	→	PERn2	RX2-	A15	A15	S24 (PETn2)	S18 (RX2-)
GND	B16	B16	GROUND	GROUND	—	GROUND	GROUND	A16	A16		
HS	B17	B17	PETp3	TX3+	→	PERp3	RX3+	A17	A17	E17 (PETp3)	S23 (RX3+)
HS	B18	B18	PETn3	TX3-	→	PERn3	RX3-	A18	A18	E18 (PETn3)	S24 (RX3-)
GND	B19	B19	GROUND	GROUND	—	GROUND	GROUND	A19	A19		
RSV		B20	POWER 5V #1	RESERVED	NO WIRE	POWER 3.3 Vact RX	RESERVED	A20			
RSV		B21	POWER 5V #2	RESERVED	NO WIRE	POWER 3.3 Vact TX	RESERVED	A21			
GND		B22	GROUND	GROUND	—	GROUND	GROUND	A22			
HS	B20	B23	PETp4	TX4+	→	PERp4	RX4+	A23	A20	E10 (PETp0)	S2 (RX0+)
HS	B21	B24	PETn4	TX4-	→	PERn4	RX4-	A24	A21	E11 (PETn0)	S3 (RX0-)
GND	B22	B25	GROUND	GROUND	—	GROUND	GROUND	A25	A22		
HS	B23	B26	PETp5	TX5+	→	PERp5	RX5+	A26	A23	S17 (PETp1)	S9 (RX1+)
HS	B24	B27	PETn5	TX5-	→	PERn5	RX5-	A27	A24	S18 (PETn1)	S10 (RX1-)
GND	B25	B28	GROUND	GROUND	—	GROUND	GROUND	A28	A25		
SB	B26	B29	2W-CLKB (VSPB)	2W-CLKB, SCLockB (SB0B)	↔	2W-CLKB(VSPB)	2W-CLKB, SCLockB(SB0B)	A29	A26		
SB	B27	B30	2W-DATAB (VSPB)	2W-DATAB, SloadB (SB1B)	↔	2W-DATAB(VSPB)	2W-DATAB, SloadB(SB1B)	A30	A27		
SB	B28	B31	GND	GND (SB2B)	—	GND	GND(SB2B)	A31	A28		
SB	B29	B32	PERSTB# (VSPB)	ADDB, SDataInB (SB5B)	↔	PERSTB#(VSPB)	ADDB, SDataInB(SB5B)	A32	A29	E5 (PERST#)	
SB	B30	B33	CPRSNTB# (VSPB)	CNTRLR_TYPEB (SB6B)	↔	CPRSNTB#(VSPB)	CNTRLR_TYPEB(SB6B)	A33	A30		
GND	B31	B34	GROUND	GROUND	—	GROUND	GROUND	A34	A31		
HS	B32	B35	PETp6	TX6+	→	PERp6	RX6+	A35	A32	S23 (PETp2)	S17 (RX2+)
HS	B33	B36	PETn6	TX6-	→	PERn6	RX6-	A36	A33	S24 (PETn2)	S18 (RX2-)
GND	B34	B37	GROUND	GROUND	—	GROUND	GROUND	A37	A34		
HS	B35	B38	PETp7	TX7+	→	PERp7	RX7+	A38	A35	E17 (PETp3)	S23 (RX3+)
HS	B36	B39	PETn7	TX7-	→	PERn7	RX7-	A39	A36	E18 (PETn3)	S24 (RX3-)
GND	B37	B40	GROUND	GROUND	—	GROUND	GROUND	A40	A37		

Table 5-4 SAS-4/ SFF-8621/ SFF-8654 (x8) to SAS-4/ SFF-8621/ SFF-8654 Other Protocol(x4) Y-Cables (1 of 2)

SAS-4/ Other Protocol x8 to OCuLink/ Other Protocol/ SAS-4 (x4) Y-Cables (Sheet 1 of 2)											
9400 Rev 0.2	Root / Controller			CABLE	Endpoint / Backplane				DEVICE(s)		
	SFF-8654 (74 Circuit)	SFF-8621 (80 Circuit)	9402 Multi-Protocol (Other Protocol (O/P), SAS-4) x8 Cable Interface		9402 Multi-Protocol (OCuLink, Other Protocol (O/P), SAS-4) Pair of x4 Cable Interfaces		SFF-8621 (42 Circuit)	SFF-8654 (38 Circuit)	SFF-8639 / U.2 Connector (Pair of x4)		
Type 1 8X	O/P SAS-4	O/P SAS-4	Other Protocol and SAS-4/ SFF-8448 Signal Names			OCuLink, Other Protocol and SAS-4/ SFF-8448 Signal Names		OCuLink/ SAS-4	O/P SAS-4	PCI Express® (x4)	MultiLink SAS™
	PIN	PIN	ROOT	Controller	DIR	Endpoint	Backplane	PIN	PIN	PIN	PIN
					NO WIRE	POWER_5V		B1			
GND	A1	A1	GROUND	GROUND	—	GROUND	GROUND	B2	B1		
HS	A2	A2	PERp0	RX0+	←	PETp0	TX0+	B3	B2	E14 (PERp0)	S6 (TX0+)
HS	A3	A3	PERn0	RX0-	←	PETn0	TX0-	B4	B3	E13 (PERn0)	S5 (TX0-)
GND	A4	A4	GROUND	GROUND	—	GROUND	GROUND	B5	B4		
HS	A5	A5	PERp1	RX1+	←	PETp1	TX1+	B6	B5	S21 (PERp1)	S13 (TX1+)
HS	A6	A6	PERn1	RX1-	←	PETn1	TX1-	B7	B6	S20 (PERn1)	S12 (TX1-)
GND	A7	A7	GROUND	GROUND	—	GROUND	GROUND	B8	B7		
SB	A8	A8	BP_TYPEA(VSPA)	BP_TYPEA(SB7A)	↔	BP_TYPEA(VSPA)	BP_TYPEA(SB7A)	B9	B8		
SB	A9	A9	CWAKEA#,OBFFA (VSPA)	RESETA, SDataOutA(SB4A)	↔	CWAKEA#,OBFFA(VSPA)	RESETA, SDataOutA(SB4A)	B10	B9	P1 (WAKE#)	
SB	A10	A10	GND	GND(SB3A)	—	GND	GND(SB3A)	B11	B10		
SB	A11	A11	REFCLKA+(VSPA+)	(SBA+)	→	REFCLKA+(VSPA+)	(SBA+)	B12	B11	E7 (REFCLK+)	
SB	A12	A12	REFCLKA-(VSPA-)	(SBA-)	→	REFCLKA-(VSPA-)	(SBA-)	B13	B12	E8 (REFCLK-)	
GND	A13	A13	GROUND	GROUND	—	GROUND	GROUND	B14	B13		
HS	A14	A14	PERp2	RX2+	←	PETp2	TX2+	B15	B14	S27 (PERp2)	S21 (TX2+)
HS	A15	A15	PERn2	RX2-	←	PETn2	TX2-	B16	B15	S26 (PERn2)	S20 (TX2-)
GND	A16	A16	GROUND	GROUND	—	GROUND	GROUND	B17	B16		
HS	A17	A17	PERp3	RX3+	←	PETp3	TX3+	B18	B17	E21 (PERp3)	S27 (TX3+)
HS	A18	A18	PERn3	RX3-	←	PETn3	TX3-	B19	B18	E20 (PERn3)	S26 (TX3-)
GND	A19	A19	GROUND	GROUND	—	GROUND	GROUND	B20	B19		
RSV		A20	POWER 3.3 Vact RX	RESERVED	NC	POWER 3.3 Vact TX	RESERVED	B21			
RSV		A21	POWER 3.3 Vact TX	RESERVED	NC	POWER_5V #1	RESERVED	B1			
GND	A19	A22	GROUND	GROUND	—	GROUND	GROUND	B2	B1		
HS	A20	A23	PERp4	RX4+	←	PETp4	TX4+	B3	B2	E14 (PERp0)	S6 (TX0+)
HS	A21	A24	PERn4	RX4-	←	PETn4	TX4-	B4	B3	E13 (PERn0)	S5 (TX0-)
GND	A22	A25	GROUND	GROUND	—	GROUND	GROUND	B5	B4		
HS	A23	A26	PERp5	RX5+	←	PETp5	TX5+	B6	B5	S21 (PERp1)	S13 (TX1+)
HS	A24	A27	PERn5	RX5-	←	PETn5	TX5-	B7	B6	S20 (PERn1)	S12 (TX1-)
GND	A25	A28	GROUND	GROUND	—	GROUND	GROUND	B8	B7		
SB	A26	A29	BP_TYPEB(VSPB)	BP_TYPEB(SB7B)	↔	BP_TYPEB(VSPB)	BP_TYPEB(SB7B)	B9	B8		
SB	A27	A30	CWAKEB#,OBFFB (VSPB)	RESETB, SDataOutB(SB4B)	↔	CWAKEB#,OBFFB(VSPB)	RESETB, SDataOutB(SB4B)	B10	B9	P1 (WAKE#)	
SB	A28	A31	GND	GND(SB3B)	—	GND	GND(SB3B)	B11	B10		
SB	A29	A32	REFCLKB+(VSPB+)	(SBB+)	→	REFCLKB+(VSPB+)	(SBB+)	B12	B11	E7 (REFCLK+)	
SB	A30	A33	REFCLKB-(VSPB-)	(SBB-)	→	REFCLKB-(VSPB-)	(SBB-)	B13	B12	E8 (REFCLK-)	
GND	A31	A34	GROUND	GROUND	—	GROUND	GROUND	B14	B13		
HS	A32	A35	PERp6	RX6+	←	PETp6	TX6+	B15	B14	S27 (PERp2)	S21 (TX2+)
HS	A33	A36	PERn6	RX6-	←	PETn6	TX6-	B16	B15	S26 (PERn2)	S20 (TX2-)
GND	A34	A37	GROUND	GROUND	—	GROUND	GROUND	B17	B16		
HS	A35	A38	PERp7	RX7+	←	PETp7	TX7+	B18	B17	E21 (PERp3)	S27 (TX3+)
HS	A36	A39	PERn7	RX7-	←	PETn7	TX7-	B19	B18	E20 (PERn3)	S26 (TX3-)
GND	A37	A40	GROUND	GROUND	—	GROUND	GROUND	B20	B19		
					NO WIRE	POWER 3.3 Vact TX		B21			

Table 5-5 SAS-4/ SFF-8621/ SFF-8654 (x8) to SAS-4/ SFF-8621/ SFF-8654 Other Protocol(x4) Y-Cables (2 of 2)

SAS-4/ Other Protocol x8 to OCuLink/ Other Protocol/ SAS-4 (x4) Y-Cables (Sheet 2 of 2)											
9400 Rev 0.2	Root / Controller				CABLE	Endpoint / Backplane				DEVICE(s)	
	SFF-8654 (74 Circuit)	SFF-8621 (80 Circuit)	9402 Multi-Protocol (Other Protocol (O/P), SAS-4) x8 Cable Interface			9402 Multi-Protocol (OCuLink, Other Protocol (O/P), SAS-4) Pair of x4 Cable Interfaces		SFF-8621 (42 Circuit)	SFF-8654 (38 Circuit)	SFF-8639 / U.2 Connector (Pair of x4)	
Type 1 8X	O/P SAS-4	O/P SAS-4	Other Protocol and SAS-4/ SFF-8448 Signal Names			OCuLink and SAS-4/ SFF-8448 Signal Names		OCuLink/ SAS-4	O/P SAS-4	PCI Express® (x4)	MultiLink SAS™
	PIN	PIN	ROOT	Controller	DIR	Endpoint	Backplane	PIN	PIN	PIN	PIN
				RESERVED	NO WIRE	POWER 3.3 Vact RX	RESERVED	A1			
GND	B1	B1	GROUND	GROUND	—	GROUND	GROUND	A2	A1		
HS	B2	B2	PETp0	TX0+	→	PERp0	RX0+	A3	A2	E10 (PETp0)	S2 (RX0+)
HS	B3	B3	PETn0	TX0-	→	PERn0	RX0-	A4	A3	E11 (PETn0)	S3 (RX0-)
GND	B4	B4	GROUND	GROUND	—	GROUND	GROUND	A5	A4		
HS	B5	B5	PETp1	TX1+	→	PERp1	RX1+	A6	A5	S17 (PETp1)	S9 (RX1+)
HS	B6	B6	PETn1	TX1-	→	PERn1	RX1-	A7	A6	S18 (PETn1)	S10 (RX1-)
GND	B7	B7	GROUND	GROUND	—	GROUND	GROUND	A8	A7		
SB	B8	B8	2W-CLKA	2W-CLKA, SClOCKA (SB0A)	↔	2W-CLKA	2W-CLKA, SClOCKA(SB0A)	A9	A8		
SB	B9	B9	2W-DATAA	2W-DATAA, SloadA (SB1A)	↔	2W-DATAA	2W-DATAA, SloadA(SB1A)	A10	A9		
SB	B10	B10	GND	GND(SB2A)	—	GND	GND(SB2A)	A11	A10		
SB	B11	B11	PERSTA#	ADDA, SDataInA (SB5A)	↔	PERSTA#	ADDA, SDataInA(SB5A)	A12	A11	E5 (PERST#)	
SB	B12	B12	CPRSNTA#	CNTRLR_TYPEA (SB6A)	↔	CPRSNTA#	CNTRLR_TYPEA(SB6A)	A13	A12		
GND	B13	B13	GROUND	GROUND	—	GROUND	GROUND	A14	A13		
HS	B14	B14	PETp2	TX2+	→	PERp2	RX2+	A15	A14	S23 (PETp2)	S17 (RX2+)
HS	B15	B15	PETn2	TX2-	→	PERn2	RX2-	A16	A15	S24 (PETn2)	S18 (RX2-)
GND	B16	B16	GROUND	GROUND	—	GROUND	GROUND	A17	A16		
HS	B17	B17	PETp3	TX3+	→	PERp3	RX3+	A18	A17	E17 (PETp3)	S23 (RX3+)
HS	B18	B18	PETn3	TX3-	→	PERn3	RX3-	A19	A18	E18 (PETn3)	S24 (RX3-)
GND	B19	B19	GROUND	GROUND	—	GROUND	GROUND	A20	A19		
RSV		B20	POWER 5V #1	RESERVED	NO WIRE	POWER 5 V #2	RESERVED	A21			
RSV		B21	POWER 5V #2	RESERVED	NO WIRE	POWER 3.3 Vact RX	RESERVED	A1			
GND	B19	B22	GROUND	GROUND	—	GROUND	GROUND	A2	A1		
HS	B20	B23	PETp4	TX4+	→	PERp4	RX4+	A3	A2	E10 (PETp0)	S2 (RX0+)
HS	B21	B24	PETn4	TX4-	→	PERn4	RX4-	A4	A3	E11 (PETn0)	S3 (RX0-)
GND	B22	B25	GROUND	GROUND	—	GROUND	GROUND	A5	A4		
HS	B23	B26	PETp5	TX5+	→	PERp5	RX5+	A6	A5	S17 (PETp1)	S9 (RX1+)
HS	B24	B27	PETn5	TX5-	→	PERn5	RX5-	A7	A6	S18 (PETn1)	S10 (RX1-)
GND	B25	B28	GROUND	GROUND	—	GROUND	GROUND	A8	A7		
SB	B26	B29	2W-CLKB	2W-CLKB, SClOCKB(SB0B)	↔	2W-CLKB	2W-CLKB, SClOCKB(SB0B)	A9	A8		
SB	B27	B30	2W-DATAB	2W-DATAB, SloadB(SB1B)	↔	2W-DATAB	2W-DATAB, SloadB(SB1B)	A10	A9		
SB	B28	B31	GND	GND(SB2B)	—	GND	(SB2B)GND	A11	A10		
SB	B29	B32	PERSTB#(VSP5B)	ADDB, SDataInB(SB5B)	↔	PERSTB#	ADDB, SDataInB(SB5B)	A12	A11	E5 (PERST#)	
SB	B30	B33	CPRSNTB#(VSP6B)	CNTRLR_TYPEB(SB6B)	↔	CPRSNTB#	CNTRLR_TYPEB(SB6B)	A13	A12		
GND	B31	B34	GROUND	GROUND	—	GROUND	GROUND	A14	A13		
HS	B32	B35	PETp6	TX6+	→	PERp6	RX6+	A15	A14	S23 (PETp2)	S17 (RX2+)
HS	B33	B36	PETn6	TX6-	→	PERn6	RX6-	A16	A15	S24 (PETn2)	S18 (RX2-)
GND	B34	B37	GROUND	GROUND	—	GROUND	GROUND	A17	A16		
HS	B35	B38	PETp7	TX7+	→	PERp7	RX7+	A18	A17	E17 (PETp3)	S23 (RX3+)
HS	B36	B39	PETn7	TX7-	→	PERn7	RX7-	A19	A18	E18 (PETn3)	S24 (RX3-)
GND	B37	B40	GROUND	GROUND	—	GROUND	GROUND	A20	A19		
					NO WIRE	POWER 5 V #2	RESERVED	A21			

6 SFF-8621, SFF-8654, SFF-8643 OCuLink (x4)/ Other Protocol (x4/ x8) Cables

The following five (5) tables provide signal assignments for OCuLink x4 and Other Protocol x4/ x8 applications based on SFF-8621, SFF-8654 and SFF-8643.

The high speed differential pairs including the sidebands for REFCLK (VSP+/-) and their reversible path (PERST#/ CPRST#) respectively are highlighted/ shaded in the x4 along with (VSP[A,B]+/-) as well as their (PERST[A,B]#/ CPRST[A,B]#) x8 connections. They must be wired as differential pairs to cover the cable being flipped between Root and Endpoint.

The high speed differential and sideband signals are color coded (OCuLink, Other Protocol=Green/ Italic) to indicate their associated naming convention/ protocol. The arrows provide the signal flow direction between Root and Endpoint. In addition brown was used to identify double ground pin assignments where applicable between different connector types and Y-cables.

The pins designated "POWER" that are shown in these tables as "NO WIRE". Refer to section 4 Pinout Tables with Implementation Notes item 16 for more details

1. OCuLink SFF-8621 / Other Protocol SFF-8654/ SFF-8643 Other Protocol x4 Cables
Table 6-1 defines the cable interface between SFF-8621/ SFF-8654/ SFF-8643 connections only. These cables are fully reversible such that they can be flipped end to end between Root and Endpoint
2. Other Protocol SFF-8621 / SFF-8654 / SFF-8643 x8 Cables
Tables 6-2 and 6-3 define the cable interface for SFF-8621/ SFF-8654 to SFF-8643 connections only. These cables are fully reversible such that they can be flipped end to end between Root and Endpoint
 - a. Note: In the x8 configuration the sidebands designated with an "A" suffix are considered the primary path when only a single set of sidebands are required to manage the bus. The sideband bus with a "B" suffix is also shown with VSP indicating possible vendor specific specification. The pins associated with associated with REFCLKB+/- (VSPB+/-) and PERSTB#/ CPRSTB#) must be implemented in the cable as differential pairs.
3. Other Protocol SFF-8621, SFF-8654, SFF-8643 x8 to SFF-8621, SFF-8654, SFF-8643 Y-Cables
Tables 6-4 and 6-5 defines the cable interface for Other Protocol x8 SFF-8621/ SFF-8654/ SFF-8643 to OCuLink (SFF-8621)/ Other Protocol SFF-8654/ SFF-8643 x4 "Y-Cable" connections only. These cables are fully reversible such that they can be flipped end to end between Root and Endpoint
 - a. Note: Both sets of sidebands are required to support a Y-cable configuration where two independent x4 interfaces are connected to a single x8 interface as described in the previous table.

Table 6-1 SFF-8621/ SFF-8654/ SFF-8643 OCuLink and Other Protocol(x4) Cables (1 of 1)

OCuLink, Other Protocol x4 Cables (Sheet 1 of 1)										
	Root					End Point				DEVICE
9400 Rev 0.2	SFF-8643	SFF-8654 (38 Circuit)	SFF-8621 (42 Circuit)	9402 Multi-Protocol OCuLink, Other Protocol (O/P) x4 Cable Interface	Cable	9402 Multi-Protocol OCuLink, Other Protocol (O/P) x4 Cable Interface	SFF-8621 (42 Circuit)	SFF-8654 (38 Circuit)	SFF-8643	SFF-8639 / U.2 Connector
Type 1 4X	O/P	O/P	OCuLink	OCuLink Signal Names		OCuLink Signal Names	OCuLink	O/P	O/P	PCI Express® (x4)
	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN
RSV			A1	POWER 3.3 Vact RX	NO WIRE	POWER 5 V #1	B1			
GND	B3	A1	A2	GROUND	—	GROUND	B2	B1	D3	
HS	B4	A2	A3	PERp0	←	PETp0	B3	B2	D4	E14 (PERp0)
HS	B5	A3	A4	PERn0	←	PETn0	B4	B3	D5	E13 (PERn0)
GND	A3	A4	A5	GROUND	—	GROUND	B5	B4	C3	
HS	A4	A5	A6	PERp1	←	PETp1	B6	B5	C4	S21 (PERp1)
HS	A5	A6	A7	PERn1	←	PETn1	B7	B6	C5	S20 (PERn1)
GND	A6	A7	A8	GROUND	—	GROUND	B8	B7	C6	
SB	A1	A8	A9	BP_TYPE (VSP)	↔	BP_TYPE(VSP)	B9	B8	A2	
SB	B1	A9	A10	CWAKE#,OBFF (VSP)	↔	CWAKE#,OBFF(VSP)	B10	B9	B2	P1 (WAKE#)
SB		A10	A11	GND	—	GND	B11	B10		
SB	C1	A11	A12	REFCLK+ (VSP+)	→	REFCLK+ (VSP+)	B12	B11	C2	E7 (REFCLK+)
SB	D1	A12	A13	REFCLK- (VSP-)	→	REFCLK- (VSP-)	B13	B12	D2	E8 (REFCLK-)
GND	B6	A13	A14	GROUND	—	GROUND	B14	B13	D6	
HS	B7	A14	A15	PERp2	←	PETp2	B15	B14	D7	S27 (PERp2)
HS	B8	A15	A16	PERn2	←	PETn2	B16	B15	D8	S26 (PERn2)
GND	B9	A16	A17	GROUND	—	GROUND	B17	B16	D9	
HS	A7	A17	A18	PERp3	←	PETp3	B18	B17	C7	E21 (PERp3)
HS	A8	A18	A19	PERn3	←	PETn3	B19	B18	C8	E20 (PERn3)
GND	A9	A19	A20	GROUND	—	GROUND	B20	B19	C9	
RSV			A21	POWER 5 V #2	NO WIRE	POWER 3.3 Vact TX	B21			
RSV			B1	POWER 5 V #1	NO WIRE	POWER 3.3 Vact RX	A1			
GND	D3	B1	B2	GROUND	—	GROUND	A2	A1	B3	
HS	D4	B2	B3	PETp0	→	PERp0	A3	A2	B4	E10 (PETp0)
HS	D5	B3	B4	PETn0	→	PERn0	A4	A3	B5	E11 (PETn0)
GND	C3	B4	B5	GROUND	—	GROUND	A5	A4	A3	
HS	C4	B5	B6	PETp1	→	PERp1	A6	A5	A4	S17 (PETp1)
HS	C5	B6	B7	PETn1	→	PERn1	A7	A6	A5	S18 (PETn1)
GND	C6	B7	B8	GROUND	—	GROUND	A8	A7	A6	
SB	A2	B8	B9	2W-CLK	↔	2W-CLK	A9	A8	A1	
SB	B2	B9	B10	2W-DATA	↔	2W-DATA	A10	A9	B1	
SB		B10	B11	GND	—	GND	A11	A10		
SB	C2	B11	B12	PERST#	→	PERST#	A12	A11	C1	E5 (PERST#)
SB	D2	B12	B13	CPRSNT#	←	CPRSNT#	A13	A12	D1	
GND	D6	B13	B14	GROUND	—	GROUND	A14	A13	B6	
HS	D7	B14	B15	PETp2	→	PERp2	A15	A14	B7	S23 (PETp2)
HS	D8	B15	B16	PETn2	→	PERn2	A16	A15	B8	S24 (PETn2)
GND	D9	B16	B17	GROUND	—	GROUND	A17	A16	B9	
HS	C7	B17	B18	PETp3	→	PERp3	A18	A17	A7	E17 (PETp3)
HS	C8	B18	B19	PETn3	→	PERn3	A19	A18	A8	E18 (PETn3)
GND	C9	B19	B20	GROUND	—	GROUND	A20	A19	A9	
RSV			B21	POWER 3.3 Vact TX	NO WIRE	POWER 5 V #2	A21			

Table 6-2 SFF-8621/ SFF-8654/ SFF-8643 (x8) Other Protocol (O/P) Cables (1 of 2)

Other Protocol SFF-8643/SFF-8654/ SFF-8621 (x8) to SFF-8643/ SFF-8654/ SFF-8621 (x8) Cables (Sheet 1 of 2)										
9400 Rev 0.2	SFF-8643	Root			CABLE	Endpoint			DEVICE	
		SFF-8654 (74 Circuit)	SFF-8621 (80 Circuit)	9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface		9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface	SFF-8621 (80 Circuit)	SFF-8654 (74-Circuit)		SFF-8643
Type 1 8X	O/P x4	O/P x8	O/P x8	Other Protocol Signal Names		Other Protocol Signal Names	O/P x8	O/P x8	O/P x4	PCI Express®
	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN
GND	B3	A1	A1	GROUND	—	GROUND	B1	B1	D3	
HS	B4	A2	A2	PERp0	←	PETp0	B2	B2	D4	E14 (PERp0)
HS	B5	A3	A3	PERn0	←	PETn0	B3	B3	D5	E13 (PERn0)
GND	A3	A4	A4	GROUND	—	GROUND	B4	B4	C3	
HS	A4	A5	A5	PERp1	←	PETp1	B5	B5	C4	S21 (PERp1)
HS	A5	A6	A6	PERn1	←	PETn1	B6	B6	C5	S20 (PERn1)
GND	A6	A7	A7	GROUND	—	GROUND	B7	B7	C6	
SB	A1	A8	A8	BP_TYPEA(VSPA)	↔	BP_TYPEA(VSPA)	B8	B8	A2	
SB	B1	A9	A9	CWAKEA#,OBFFA,(VSPA)	↔	CWAKEA#,OBFFA(VSPA)	B9	B9	B2	P1 (WAKE#)
SB		A10	A10	GND	—	GND	B10	B10		
SB	C1	A11	A11	REFCLKA+ (VSPA+)	→	REFCLKA+ (VSPA+)	B11	B11	C2	E7 (REFCLK+)
SB	D1	A12	A12	REFCLKA- (VSPA-)	→	REFCLKA- (VSPA-)	B12	B12	D2	E8 (REFCLK-)
GND	B6	A13	A13	GROUND	—	GROUND	B13	B13	D6	
HS	B7	A14	A14	PERp2	←	PETp2	B14	B14	D7	S27 (PERp2)
HS	B8	A15	A15	PERn2	←	PETn2	B15	B15	D8	S26 (PERn2)
GND	B9	A16	A16	GROUND	—	GROUND	B16	B16	D9	
HS	A7	A17	A17	PERp3	←	PETp3	B17	B17	C7	E21 (PERp3)
HS	A8	A18	A18	PERn3	←	PETn3	B18	B18	C8	E20 (PERn3)
GND	A9	A19	A19	GROUND	—	GROUND	B19	B19	C9	
RSV			A20	POWER 3.3 Vact RX	NO WIRE	POWER 5V #1	B20			
RSV			A21	POWER 3.3 Vact TX	NO WIRE	POWER 5V #2	B21			
GND	B3		A22	GROUND	—	GROUND	B22		D3	
HS	B4	A20	A23	PERp4	←	PETp4	B23	B20	D4	E14 (PERp0)
HS	B5	A21	A24	PERn4	←	PETn4	B24	B21	D5	E13 (PERn0)
GND	A3	A22	A25	GROUND	—	GROUND	B25	B22	C3	
HS	A4	A23	A26	PERp5	←	PETp5	B26	B23	C4	S21 (PERp1)
HS	A5	A24	A27	PERn5 /	←	PETn5	B27	B24	C5	S20 (PERn1)
GND	A6	A25	A28	GROUND	—	GROUND	B28	B25	C6	
SB	A1	A26	A29	BP_TYPEB(VSPB)	↔	BP_TYPEB(VSPB)	B29	B26	A2	
SB	B1	A27	A30	CWAKEB#,OBFFB,(VSPB)	↔	CWAKEB#,OBFFB(VSPB)	B30	B27	B2	P1 (WAKE#)
SB		A28	A31	GND	—	GND	B31	B28		
SB	C1	A29	A32	REFCLKB+(VSPB+)	→	REFCLKB+(VSPB+)	B32	B29	C2	E7 (REFCLK+)
SB	D1	A30	A33	REFCLKB-(VSPB-)	→	REFCLKB-(VSPB-)	B33	B30	D2	E8 (REFCLK-)
GND	B6	A31	A34	GROUND	—	GROUND	B34	B31	D6	
HS	B7	A32	A35	PERp6	←	PETp6	B35	B32	D7	S27 (PERp2)
HS	B8	A33	A36	PERn6	←	PETn6	B36	B33	D8	S26 (PERn2)
GND	B9	A34	A37	GROUND	—	GROUND	B37	B34	D9	
HS	A7	A35	A38	PERp7	←	PETp7	B38	B35	C7	E21 (PERp3)
HS	A8	A36	A39	PERn7	←	PETn7	B39	B36	C8	E20 (PERn3)
GND	A9	A37	A40	GROUND	—	GROUND	B40	B37	C9	

Table 6-3 SFF-8621/ SFF-8654/ SFF-8643 (x8) Other Protocol Cables (O/P) (2 of 2)

Other Protocol SFF-8643/ SFF-8654/ SFF-8621 (x8) to SFF-8643/ SFF-8654/ SFF-8621 (x8) Cables (Sheet 2 of 2)										
9400 Rev 0.2	SFF-8643	SFF-8654 (74 Circuit)	SFF-8621 (80 Circuit)	9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface	CABLE	Endpoint				DEVICE
						9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface	SFF-8621 (80 Circuit)	SFF-8654 (74-Circuit)	SFF-8643	
Type 1 8X	O/P x4	O/P x8	O/P x8	Other Protocol Signal Names		Other Protocol Signal Names	O/P x8	O/P x8	O/P x4	PCI Express®
	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN
GND	D3	B1	B1	GROUND	—	GROUND	A1	A1	B3	
HS	D4	B2	B2	PETp0	→	PERp0	A2	A2	B4	E10 (PETp0)
HS	D5	B3	B3	PETn0	→	PERn0	A3	A3	B5	E11 (PETn0)
GND	C3	B4	B4	GROUND	—	GROUND	A4	A4	A3	
HS	C4	B5	B5	PETp1	→	PERp1	A5	A5	A4	S17 (PETp1)
HS	C5	B6	B6	PETn1	→	PERn1	A6	A6	A5	S18 (PETn1)
GND	C6	B7	B7	GROUND	—	GROUND	A7	A7	A6	
SB	A2	B8	B8	2W-CLKA	↔	2W-CLKA	A8	A8	A1	
SB	B2	B9	B9	2W-DATAA	↔	2W-DATAA	A9	A9	B1	
SB		B10	B10	GND	—	GND	A10	A10		
SB	C2	B11	B11	PERSTA#	→	PERSTA#	A11	A11	C1	E5 (PERST#)
SB	D2	B12	B12	CPRSNTA#	←	CPRSNT#	A12	A12	D1	
GND	D6	B13	B13	GROUND	—	GROUND	A13	A13	B6	
HS	D7	B14	B14	PETp2	→	PERp2	A14	A14	B7	S23 (PETp2)
HS	D8	B15	B15	PETn2	→	PERn2	A15	A15	B8	S24 (PETn2)
GND	D9	B16	B16	GROUND	—	GROUND	A16	A16	B9	
HS	C7	B17	B17	PETp3	→	PERp3	A17	A17	A7	E17 (PETp3)
HS	C8	B18	B18	PETn3	→	PERn3	A18	A18	A8	E18 (PETn3)
GND	C9	B19	B19	GROUND	—	GROUND	A19	A19	A9	
RSV			B20	POWER 5V #1	NO WIRE	POWER 3.3 Vact RX	A20			
RSV			B21	POWER 5V #2	NO WIRE	POWER 3.3 Vact TX	A21			
GND	D3		B22	GROUND	—	GROUND	A22		B3	
HS	D4	B20	B23	PETp4	→	PERp4	A23	A20	B4	E10 (PETp0)
HS	D5	B21	B24	PETn4	→	PERn4	A24	A21	B5	E11 (PETn0)
GND	C3	B22	B25	GROUND	—	GROUND	A25	A22	A3	
HS	C4	B23	B26	PETp5	→	PERp5	A26	A23	A4	S17 (PETp1)
HS	C5	B24	B27	PETn5	→	PERn5	A27	A24	A5	S18 (PETn1)
GND	C6	B25	B28	GROUND	—	GROUND	A28	A25	A6	
SB	A2	B26	B29	2W-CLKB (VSPB)	↔	2W-CLKB (VSPB)	A29	A26	A1	
SB	B2	B27	B30	2W-DATAB (VSPB)	↔	2W-DATAB (VSPB)	A30	A27	B1	
SB		B28	B31	GND	—	GND	A31	A28		
SB	C2	B29	B32	PERSTB# (VSPB)	→	PERSTB# (VSPB)	A32	A29	C1	E5 (PERST#)
SB	D2	B30	B33	CPRSNTB# (VSPB)	←	CPRSNTB# (VSPB)	A33	A30	D1	
GND	D6	B31	B34	GROUND	—	GROUND	A34	A31	B6	
HS	D7	B32	B35	PETp6/	→	PERp6	A35	A32	B7	S23 (PETp2)
HS	D8	B33	B36	PETn6	→	PERn6	A36	A33	B8	S24 (PETn2)
GND	D9	B34	B37	GROUND	—	GROUND	A37	A34	B9	
HS	C7	B35	B38	PETp7	→	PERp7	A38	A35	A7	E17 (PETp3)
HS	C8	B36	B39	PETn7	→	PERn7	A39	A36	A8	E18 (PETn3)
GND	C9	B37	B40	GROUND	—	GROUND	A40	A37	A9	

Table 6-4 SFF-8621/ SFF-8654/ SFF-8643 (x8) to OCuLink / Other Protocol (x4) Y-Cables (1 of 2)

Other Protocol (O/P) SFF-8643/ SFF-8654/ SFF-8621 (x8) to OCuLink SFF-8621 , O/P SFF-8654/ SFF-8643 (x4) Y-Cables (Sheet 1 of 2)										
	Root					Endpoint				DEVICE
9400 Rev 0.2	SFF-8643	SFF-8654 (74-Circuit)	SFF-8621 (80-Circuit)	9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface	CABLE	9402 Multi-Protocol (OCuLink, Other Protocol (O/P)) Pair of x4 Cable Interfaces	SFF-8621 (42 Circuit)	SFF-8654 (38 Circuit)	SFF-8643	SFF-8639 / U.2 Connector (Pair of x4)
Type 1 8X	O/P	O/P	O/P	Other Protocol Signal Names		Other Protocol Signal Names	OCuLink x4	O/P x4	O/P x4	PCI Express®
	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN
					NO WIRE	POWER 5 V #1	B1			
GND	B3	A1	A1	GROUND	—	GROUND	B2	B1	D3	
HS	B4	A2	A2	PERp0	←	PETp0	B3	B2	D4	E14 (PERp0)
HS	B5	A3	A3	PERn0	←	PETn0	B4	B3	D5	E13 (PERn0)
GND	A3	A4	A4	GROUND	—	GROUND	B5	B4	C3	
HS	A4	A5	A5	PERp1	←	PETp1	B6	B5	C4	S21 (PERp1)
HS	A5	A6	A6	PERn1	←	PETn1	B7	B6	C5	S20 (PERn1)
GND	A6	A7	A7	GROUND	—	GROUND	B8	B7	C6	
SB	A1	A8	A8	BP_TYPEA(VSPA)	↔	BP_TYPEA(VSPA)	B9	B8	A2	
SB	B1	A9	A9	CWAKEA#,OBFFA,(VSPA)	↔	CWAKEA#,OBFFA(VSPA)	B10	B9	B2	P1 (WAKE#)
SB		A10	A10	GND	—	GND	B11	B10		
SB	C1	A11	A11	REFCLKA+ (VSPA+)	→	REFCLKA+ (VSPA+)	B12	B11	C2	E7 (REFCLK+)
SB	D1	A12	A12	REFCLKA- (VSPA-)	→	REFCLKA- (VSPA-)	B13	B12	D2	E8 (REFCLK-)
GND	B6	A13	A13	GROUND	—	GROUND	B14	B13	D6	
HS	B7	A14	A14	PERp2	←	PETp2	B15	B14	D7	S27 (PERp2)
HS	B8	A15	A15	PERn2	←	PETn2	B16	B15	D8	S26 (PERn2)
GND	B9	A16	A16	GROUND	—	GROUND	B17	B16	D9	
HS	A7	A17	A17	PERp3	←	PETp3	B18	B17	C7	E21 (PERp3)
HS	A8	A18	A18	PERn3	←	PETn3	B19	B18	C8	E20 (PERn3)
GND	A9	A19	A19	GROUND	—	GROUND	B20	B19	C9	
RSV			A20	POWER 3.3 Vact RX	NO WIRE	POWER 3.3 Vact TX	B21			
RSV			A21	POWER 3.3 Vact TX	NO WIRE	POWER_5V #1	B1			
GND	B3	A19	A22	GROUND	—	GROUND	B2	B1	D3	
HS	B4	A20	A23	PERp4	←	PETp4	B3	B2	D4	E14 (PERp0)
HS	B5	A21	A24	PERn4	←	PETn4	B4	B3	D5	E13 (PERn0)
GND	A3	A22	A25	GROUND	—	GROUND	B5	B4	C3	
HS	A4	A23	A26	PERp5	←	PETp5	B6	B5	C4	S21 (PERp1)
HS	A5	A24	A27	PERn5 /	←	PETn5	B7	B6	C5	S20 (PERn1)
GND	A6	A25	A28	GROUND	—	GROUND	B8	B7	C6	
SB	A1	A26	A29	BP_TYPEB (VSPB)	↔	BP_TYPEB (VSPB)	B9	B8	A2	
SB	B1	A27	A30	CWAKEB#,OBFFB,(VSPB)	↔	CWAKEB#,OBFFB (VSPB)	B10	B9	B2	P1 (WAKE#)
SB		A28	A31	GND	—	GND	B11	B10		
SB	C1	A29	A32	REFCLKB+(VSPB+)	→	REFCLKB+(VSPB+)	B12	B11	C2	E7 (REFCLK+)
SB	D1	A30	A33	REFCLKB-(VSPB-)	→	REFCLKB-(VSPB-)	B13	B12	D2	E8 (REFCLK-)
GND	B6	A31	A34	GROUND	—	GROUND	B14	B13	D6	
HS	B7	A32	A35	PERp6	←	PETp6	B15	B14	D7	S27 (PERp2)
HS	B8	A33	A36	PERn6	←	PETn6	B16	B15	D8	S26 (PERn2)
GND	B9	A34	A37	GROUND	—	GROUND	B17	B16	D9	
HS	A7	A35	A38	PERp7	←	PETp7	B18	B17	C7	E21 (PERp3)
HS	A8	A36	A39	PERn7	←	PETn7	B19	B18	C8	E20 (PERn3)
GND	A9	A37	A40	GROUND	—	GROUND	B20	B19	C9	
					NO WIRE	POWER 3.3 Vact TX	B21			

Table 6-5 SFF-8621/ SFF-8654/ SFF-8643 (x8) to OCuLink/ Other Protocol Y-Cables (2 of 2)

Other Protocol (O/P) SFF-8643/ SFF-8654/ SFF-8621 (x8) to OCuLink SFF-8621 , O/P SFF-8654/ SFF-8643 (x4) Y-Cables (Sheet 2 of 2)										
	Root					Endpoint				DEVICE
9400 Rev 0.2	SFF-8643	SFF-8654 (74-Circuit)	SFF-8621 (80-Circuit)	9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface	CABLE	9402 Multi-Protocol (OCuLink, Other Protocol (O/P)) Pair of x4 Cable Interfaces	SFF-8621 (42 Circuit)	SFF-8654 (38 Circuit)	SFF-8643	SFF-8639 / U.2 Connector (Pair of x4)
Type 1 8X	O/P	O/P	O/P	Other Protocol Signal Names		Other Protocol Signal Names	OCuLink 1.0 x4	O/P x4	O/P x4	PCI Express®
	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN
					NO WIRE	POWER	A1			
GND	D3	B1	B1	GROUND	—	GROUND	A2	A1	B3	
HS	D4	B2	B2	PETp0	→	PERp0	A3	A2	B4	E10 (PETp0)
HS	D5	B3	B3	PETn0	→	PERn0	A4	A3	B5	E11 (PETn0)
GND	C3	B4	B4	GROUND	—	GROUND	A5	A4	A3	
HS	C4	B5	B5	PETp1	→	PERp1	A6	A5	A4	S17 (PETp1)
HS	C5	B6	B6	PETn1	→	PERn1	A7	A6	A5	S18 (PETn1)
GND	C6	B7	B7	GROUND	—	GROUND	A8	A7	A6	
SB	A2	B8	B8	2W-CLKA	↔	2W-CLKA	A9	A8	A1	
SB	B2	B9	B9	2W-DATAA	↔	2W-DATAA	A10	A9	B1	
SB		B10	B10	GND	—	GND	A11	A10		
SB	C2	B11	B11	PERSTA#	→	PERSTA#	A12	A11	C1	E5 (PERST#)
SB	D2	B12	B12	CPRSNTA#	←	CPRSNT#	A13	A12	D1	
GND	D6	B13	B13	GROUND	—	GROUND	A14	A13	B6	
HS	D7	B14	B14	PETp2	→	PERp2	A15	A14	B7	S23 (PETp2)
HS	D8	B15	B15	PETn2	→	PERn2	A16	A15	B8	S24 (PETn2)
GND	D9	B16	B16	GROUND	—	GROUND	A17	A16	B9	
HS	C7	B17	B17	PETp3	→	PERp3	A18	A17	A7	E17 (PETp3)
HS	C8	B18	B18	PETn3	→	PERn3	A19	A18	A8	E18 (PETn3)
GND	C9	B19	B19	GROUND	—	GROUND	A20	A19	A9	
RSV			B20	POWER 5V #1	NO WIRE	POWER 5 V #2	A21			
RSV			B21	POWER 5V #2	NO WIRE	POWER 3.3 Vact RX	A1			
GND	D3	B19	B22	GROUND	—	GROUND	A2	A1	B3	
HS	D4	B20	B23	PETp4	→	PERp4	A3	A2	B4	E10 (PETp0)
HS	D5	B21	B24	PETn4	→	PERn4	A4	A3	B5	E11 (PETn0)
GND	C3	B22	B25	GROUND	—	GROUND	A5	A4	A3	
HS	C4	B23	B26	PETp5	→	PERp5	A6	A5	A4	S17 (PETp1)
HS	C5	B24	B27	PETn5	→	PERn5	A7	A6	A5	S18 (PETn1)
GND	C6	B25	B28	GROUND	—	GROUND	A8	A7	A6	
SB	A2	B26	B29	2W-CLKB	↔	2W-CLKB	A9	A8	A1	
SB	B2	B27	B30	2W-DATAB	↔	2W-DATAB	A10	A9	B1	
SB	B28	B31	B31	GND	—	GND	A11	A10		
SB	C2	B29	B32	PERSTB#	→	PERSTB#	A12	A11	C1	E5 (PERST#)
SB	D2	B30	B33	CPRSNTB#	←	CPRSNTB#	A13	A12	D1	
GND	D6	B31	B34	GROUND	—	GROUND	A14	A13	B6	
HS	D7	B32	B35	PETp6/	→	PERp6	A15	A14	B7	S23 (PETp2)
HS	D8	B33	B36	PETn6	→	PERn6	A16	A15	B8	S24 (PETn2)
GND	D9	B34	B37	GROUND	—	GROUND	A17	A16	B9	
HS	C7	B35	B38	PETp7	→	PERp7	A18	A17	A7	E17 (PETp3)
HS	C8	B36	B39	PETn7	→	PERn7	A19	A18	A8	E18 (PETn3)
GND	C9	B37	B40	GROUND	—	GROUND	A20	A19	A9	
					NO WIRE	POWER 5 V #2	A21			

7 SAS-4 (SFF-8621/ SFF-8654), Mini SAS HD (SFF-8643), Mini SAS (SFF-8087) (Legacy) Cables

The following seven (7) tables provide recommended signal assignments for SAS-4 (SFF-8621/ SFF-8654) and SAS-2.1/ 3 (SFF-8087/ SFF-8643) only applications.

These cables are “NOT” reversible such that they cannot be flipped end to end between controller and a backplane. The SAS-4 specification moved SB4 and SB5 to allow SB+/- to be placed on dedicated pins to better optimize the SFF-8621/ SFF-8654 interfaces for multiprotocol operation. This indirectly impacted physical pin assignments for SB1/ SB2 and SB3/ SB4 on the x4 and SB[A,B]1, SB[A,B]2, SB[A,B]3 and SB[A,B]4 on the x8 configurations.

1. SAS (x4) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane
Table 7-1 defines a cable solution between a controller with SFF-8087/ SFF-8643 to a backplane with SFF-8621/ SFF-8654
2. SAS (x4) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane
Table 7-2 defines a cable solution between a controller with SFF-8621/ SFF-8654 to a backplane with legacy SFF-8087/ SFF-8643.
3. SAS (x8) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane
Table 7-3 and 7-4 defines a cable solution between a controller with SFF-8087/ SFF-8654 to a backplane with SAS-4 SFF-8621/ SFF-8654.
 - a. Note: This configuration could be considered as a Y-Cable for a pair of legacy x4 on a controller to backplane with x8 SAS-4 connections.
4. SAS (x8) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane
Table 7-5 and 7-6 defines a cable solution between a controller with SAS-4 SFF-8621/ SFF-8654 and a backplane with legacy SFF-8087/ SFF-8654 x8.
 - a. Note: This configuration could be considered as a Y-Cable with a SAS-4 x8 on the controller and a pair of legacy x4s on a backplane connections.
5. SFF-9402 SAS Sidebands SAS-4 (SFF-8621/ SFF-8654) and SAS-2.1/ SAS 3 Legacy(SFF-8643/ SFF-8087)
Table 7-7 was provided to show non-reversible SAS sideband physical pin assignments for cables that utilize SFF-8087 / SFF-8643 (Legacy) and SFF-8621/ SFF-8654 (SAS-4). The sideband signals are “highlighted” to indicate why these assemblies cannot be flipped between controller and backplane. This condition was due to changes in the SAS-4 specification that moved SB4 and SB5 to allow SB+/- to be placed on dedicated pins to better optimize the SFF-8621/ SFF-8654 interfaces for multiprotocol operations. This indirectly impacted physical pin assignments for SB1/ SB2 and SB3/ SB4 on the x4 and SB[A,B]1, SB[A,B]2, SB[A,B]3 and SB[A,B]4 on the x8 configurations.

Table 7-1 SAS (x4) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane (SH 1 of 1)

SAS Legacy (SFF-8087/ SFF-8643) (x4) Controller to SAS-4 (SFF-8621/SFF-8654) (x4) Backplane (Sheet 1 of 1)								
9400 Rev 0.2	Controller			CABLE	Backplane			DEVICE
	SFF-8087	SFF-8643	9402 SAS Non-Symmetrical Legacy (SFF-8087, SFF-8643) to SAS-4 (x4) Cable Interface		SAS-4 to Legacy (SFF-8087, SFF-8643) (x4) Cable Interface	SFF-8621 (42 Circuit)	SFF-8654 (38 circuit)	
Type 1 4X	SAS-2.1	SAS-2.1, 3	SAS Only Cable SFF-8448		SAS Only Cable SFF-8448	SAS-4	SAS-4	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
RSV			RESERVED	NO WIRE	RESERVED	B1		
GND	A1	B3	GROUND	—	GROUND	B2	B1	
HS	A2	B4	RX0+	←	TX0+	B3	B2	S6 (TX0+)
HS	A3	B5	RX0-	←	TX0-	B4	B3	S5 (TX0-)
GND	A4	A3	GROUND	—	GROUND	B5	B4	
HS	A5	A4	RX1+	←	TX1+	B6	B5	S13 (TX1+)
HS	A6	A5	RX1-	←	TX1-	B7	B6	S12 (TX1-)
GND	A7	A6	GROUND	—	GROUND	B8	B7	
SB	A8	A1	BP_TYPE(SB7)	←	BP_TYPE (SB7)	B9	B8	
SB	A10	C1	RESET, SDataOut(SB4)	→	RESET, SDataOut (SB4)	B10	B9	
SB	A9	B1	GND(SB3)	—	GND (SB3)	B11	B10	
SB			(SB+)	→	(SB+)	B12	B11	
SB			(SB-)	→	(SB-)	B13	B12	
GND	A12	B6	GROUND	—	GROUND	B14	B13	
HS	A13	B7	RX2+	←	TX2+	B15	B14	S21 (TX2+)
HS	A14	B8	RX2-	←	TX2-	B16	B15	S20 (TX2-)
GND	A15	B9	GROUND	—	GROUND	B17	B16	
HS	A16	A7	RX3+	←	TX3+	B18	B17	S27 (TX3+)
HS	A17	A8	RX3-	←	TX3-	B19	B18	S26 (TX3-)
GND	A18	A9	GROUND	—	GROUND	B20	B19	
RSV			RESERVED	NO WIRE	RESERVED	B21		
RSV			RESERVED	NO WIRE	RESERVED			
GND	B1	D3	GROUND	—	GROUND	A2	A1	
HS	B2	D4	TX0+	→	RX0+	A3	A2	S2 (RX0+)
HS	B3	D5	TX0-	→	RX0-	A4	A3	S3 (RX0-)
GND	B4	C3	GROUND	—	GROUND	A5	A4	
HS	B5	C4	TX1+	→	RX1+	A6	A5	S9 (RX1+)
HS	B6	C5	TX1-	→	RX1-	A7	A6	S10 (RX1-)
GND	B7	C6	GROUND	—	GROUND	A8	A7	
SB	B8	A2	2W-CLK, SClOCK(SB0)	↔	2W-CLK, SClOCK (SB0)	A9	A8	
SB	B9	B2	2W-DATA, Sload(SB1)	↔	2W-DATA, Sload (SB1)	A10	A9	
SB	B10	C2	GND(SB2)	—	(SB2)GND(SB2)	A11	A10	
SB	A11	D1	ADD, SDataIn(SB5)	↔	ADD, SDataIn (SB5)	A12	A11	
SB	B11	D2	CNTRLR_TYPE(SB6)	→	CNTRLR_TYPE (SB6)	A13	A12	
GND	B12	D6	GROUND	—	GROUND	A14	A13	
HS	B13	D7	TX2+	→	RX2+	A15	A14	S17 (RX2+)
HS	B14	D8	TX2-	→	RX2-	A16	A15	S18 (RX2-)
GND	B15	D9	GROUND	—	GROUND	A17	A16	
HS	B16	C7	TX3+	→	RX3+	A18	A17	S23 (RX3+)
HS	B17	C8	TX3-	→	RX3-	A19	A18	S24 (RX3-)
GND	B18	C9	GROUND	—	GROUND	A20	A19	
RSV			RESERVED	NO WIRE	RESERVED	A21		

Table 7-2 SAS (x4) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane (1 of 1)

SAS-4 (SFF-8621/SFF-8654) (x4) Controller to SAS (SFF-8087/ SFF-8643) (x4) Backplane (Sheet 1 of 1)								
	Controller				Backplane			DEVICE
9400 Rev 0.2	SFF-8654 (38 Circuit)	SFF-8621 (42 Circuit)	9402 SAS Non-Symmetrical SAS-4 to Legacy (SFF-8087, SFF-8643) (x4) Cable Interface	CABLE	9402 SAS Non-Symmetrical Legacy (SFF-8087, SFF-8643) to SAS-4 (x4) Cable Interface	SFF-8643	SFF-8087	SFF-8639/ U.2 Connector
Type 1 4X	SAS-4	SAS-4	SAS Only Cable SFF-8448		SAS Only Cable SFF-8448	SAS-2.1, 3	SAS-2.1	Multilink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
RSV		A1	RESERVED	NO WIRE	RESERVED			
GND	A1	A2	GROUND	—	GROUND	D3	B1	
HS	A2	A3	RX0+	←	TX0+	D4	B2	S6 (TX0+)
HS	A3	A4	RX0-	←	TX0-	D5	B3	S5 (TX0-)
GND	A4	A5	GROUND	—	GROUND	C3	B4	
HS	A5	A6	RX1+	←	TX1+	C4	B5	S13 (TX1+)
HS	A6	A7	RX1-	←	TX1-	C5	B6	S12 (TX1-)
GND	A7	A8	GROUND	—	GROUND	C6	B7	
SB	A8	A9	BP_TYPE(SB7)	←	BP_TYPE (SB7)	A2	B8	
SB	A9	A10	RESET, SDataOut(SB4)	↔	RESET, SDataOut (SB4)	C2	B10	
SB	A10	A11	GND(SB3)	—	GND (SB3)	B2	B9	
SB	A11	A12	(SB+)	→	(SB+)			
SB	A12	A13	(SB-)	→	(SB-)			
GND	A13	A14	GROUND	—	GROUND	D6	B12	
HS	A14	A15	RX2+	←	TX2+	D7	B13	S21 (TX2+)
HS	A15	A16	RX2-	←	TX2-	D8	B14	S20 (TX2-)
GND	A16	A17	GROUND	—	GROUND	D9	B15	
HS	A17	A18	RX3+	←	TX3+	C7	B16	S27 (TX3+)
HS	A18	A19	RX3-	←	TX3-	C8	B17	S26 (TX3-)
GND	A19	A20	GROUND	—	GROUND	C9	B18	
RSV		A21	RESERVED	NC	RESERVED			
RSV		B1	RESERVED	NC	RESERVED			
GND	B1	B2	GROUND	—	GROUND	B3	A1	
HS	B2	B3	TX0+	→	RX0+	B4	A2	S2 (RX0+)
HS	B3	B4	TX0-	→	RX0-	B5	A3	S3 (RX0-)
GND	B4	B5	GROUND	—	GROUND	A3	A4	
HS	B5	B6	TX1+	→	RX1+	A4	A5	S9 (RX1+)
HS	B6	B7	TX1-	→	RX1-	A5	A6	S10 (RX1-)
GND	B7	B8	GROUND	—	GROUND	A6	A7	
SB	B8	B9	2W-CLK, SClOCK(SB0)	↔	2W-CLK, SClOCK (SB0)	A1	A8	
SB	B9	B10	2W-DATA, Sload(SB1)	↔	2W-DATA, Sload (SB1)	B1	A9	
SB	B10	B11	GND(SB2)	—	(SB2)GND(SB2)	C1	A10	
SB	B11	B12	ADD, SDataIn(SB5)	↔	ADD, SDataIn (SB5)	D2	B11	
SB	B12	B13	CNTRLR_TYPE(SB6)	→	CNTRLR_TYPE (SB6)	D1	A11	
GND	B13	B14	GROUND	—	GROUND	B6	A12	
HS	B14	B15	TX2+	→	RX2+	B7	A13	S17 (RX2+)
HS	B15	B16	TX2-	→	RX2-	B8	A14	S18 (RX2-)
GND	B16	B17	GROUND	—	GROUND	B9	A15	
HS	B17	B18	TX3+	→	RX3+	A7	A16	S23 (RX3+)
HS	B18	B19	TX3-	→	RX3-	A8	A17	S24 (RX3-)
GND	B19	B20	GROUND	—	GROUND	A9	A18	
RSV		B21	RESERVED	NO WIRE	RESERVED			

Table 7-3 SAS (x8) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane (1 of 2)

SAS (x4 Pair) (SFF-8087/ SFF-8643) Controller to SAS-4 (SFF-8621/ SFF-8654) x8 Backplane (Sheet 1 of 2)								
9400 Rev 0.2	Controller			CABLE	Backplane			DEVICE
	SFF-8087	SFF-8643	9402 SAS Non-Symmetrical Legacy (SFF-8087, SFF-8643) (x4) Pair to SAS-4 (x8) Cable Interface		SAS-4 (x8) to Legacy (SFF-8087, SFF-8643) (x4) Pair Cable Interface	SFF-8621 (80 Circuit)	SFF-8654 (74 Circuit)	
Type 1 8X	SAS-2.1 x4	SAS-2.1, 3 x4	Pair of (x4) SAS Legacy/ SFF-8448 Cables		8x SAS-4/ SFF-8448 Cable	SAS-4 x8	SAS-4 x8	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
GND	A1	B3	GROUND	—	GROUND	B1	B1	
HS	A2	B4	RX0+	←	TX0+	B2	B2	S6 (TX0+)
HS	A3	B5	RX0-	←	TX0-	B3	B3	S5 (TX0-)
GND	A4	A3	GROUND	—	GROUND	B4	B4	
HS	A5	A4	RX1+	←	TX1+	B5	B5	S13 (TX1+)
HS	A6	A5	RX1-	←	TX1-	B6	B6	S12 (TX1-)
GND	A7	A6	GROUND	—	GROUND	B7	B7	
SB	A8	A1	BP_TYPEA(SB7A)	←	BP_TYPEA (SB7A)	B8	B8	
SB	A10	C1	RESETA, SDataOutA(SB4A)	←	RESETA, SDataOutA (SB4A)	B8	B9	
SB	A9	B1	GND(SB3A)	—	GND (SB3A)	B10	B10	
SB			SBA+	→	(SBA+)	B11	B11	
SB			(SBA-)	→	(SBA-)	B12	B12	
GND	A12	B6	GROUND	—	GROUND	B13	B13	
HS	A13	B7	RX2+	←	TX2+	B14	B14	S21 (TX2+)
HS	A14	B8	RX2-	←	TX2-	B15	B15	S20 (TX2-)
GND	A15	B9	GROUND	—	GROUND	B16	B16	
HS	A16	A7	RX3+	←	TX3+	B17	B17	S27 (TX3+)
HS	A17	A8	RX3-	←	TX3-	B18	B18	S26 (TX3-)
GND	A18	A9	GROUND	—	GROUND	B19	B19	
RSV			RESERVED	NO WIRE	RESERVED	B20		
RSV			RESERVED	NO WIRE	RESERVED	B21		
GND	A1	B3	GROUND	—	GROUND	B22	B19	
HS	A2	B4	RX4+	←	TX4+	B23	B20	S6 (TX0+)
HS	A3	B5	RX4-	←	TX4-	B24	B21	S5 (TX0-)
GND	A4	A3	GROUND	—	GROUND	B25	B22	
HS	A5	A4	RX5+	←	TX5+	B26	B23	S13 (TX1+)
HS	A6	A5	RX5-	←	TX5-	B27	B24	S12 (TX1-)
GND	A7	A6	GROUND	—	GROUND	B28	B25	
SB	A8	A	BP_TYPEB(SB7B)	←	BP_TYPEB (SB7B)	B29	B26	
SB	A10	C1	RESETB, SDataOutB(SB4B)	→	RESETB, SDataOutB (SB4B)	B30	B27	
SB	A9	B1	GND(SB3B)	—	GND (SB3B)	B31	B28	
SB			(SBB+)	→	(SBB+)	B32	B29	
SB			(SBB-)	→	(SBB-)	B33	B30	
GND	A12	B6	GROUND	—	GROUND	B34	B31	
HS	A13	B7	RX6+	←	TX6+	B35	B32	S21 (TX2+)
HS	A14	B8	RX6-	←	TX6-	B36	B33	S20 (TX2-)
GND	A15	B9	GROUND	—	GROUND	B37	B34	
HS	A16	A7	RX7+	←	TX7+	B38	B35	S27 (TX3+)
HS	A17	A8	RX7-	←	TX7-	B39	B36	S26 (TX3-)
GND	A18	A9	GROUND	—	GROUND	B40	B37	

Table 7-4 SAS (x8) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane (2 of 2)

SAS (x4 Pair) (SFF-8087/ SFF-8643) Controller to SAS-4 (SFF-8621/ SFF-8654) x8 Backplane (Sheet 2 of 2)								
9400 Rev 0.2	Controller			CABLE	Backplane			DEVICE
	SFF-8087	SFF-8643	9402 SAS Non-Symmetrical Legacy (SFF-8087, SFF-8643) (x4) Pair to SAS-4 (x8) Cable Interface		SAS-4 (x8) to Legacy (SFF-8087, SFF-8643) (x4) Pair Cable Interface	SFF-8621 (80 Circuit)	SFF-8654 (74 Circuit)	
Type 1 8X	SAS-2.1 x4	SAS-2.1, 3 x4	Pair of (x4) SAS Legacy/ SFF-8448 Cables		8x SAS-4/ SFF-8448 Cable	SAS-4 x8	SAS-4 x8	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
GND	B1	D3	GROUND	—	GROUND	A1	A1	
HS	B2	D4	TX0+	→	RX0+	A2	A2	S2 (RX0+)
HS	B3	D5	TX0-	→	RX0-	A3	A3	S3 (RX0-)
GND	B4	C3	GROUND	—	GROUND	A4	A4	
HS	B5	C4	TX1+	→	RX1+	A5	A5	S9 (RX1+)
HS	B6	C5	TX1-	→	RX1-	A6	A6	S10 (RX1-)
GND	B7	C6	GROUND	—	GROUND	A7	A7	
SB	B8	A2	2W-CLKA, SCLockA(SB0A)	↔	2W-CLKA, SCLockA (SB0A)	A8	A8	
SB	B9	B2	2W-DATAA, SLoadA(SB1A)	↔	2W-DATAA, SLoadA (SB1A)	A9	A9	
SB	B10	C2	GND(SB2A)	—	GND (SB2A)	A10	A10	
SB	A11	D1	ADDA, SDataInA(SB5A)	↔	ADDA, SDataInA (SB5A)	A11	A11	
SB	B11	D2	CNTRLR_TYPEA(SB6A)	→	CNTRLR_TYPEA (SB6)	A12	A12	
GND	B12	D6	GROUND	—	GROUND	A13	A13	
HS	B13	D7	TX2+	→	RX2+	A14	A14	S17 (RX2+)
HS	B14	D8	TX2-	→	RX2-	A15	A15	S18 (RX2-)
GND	B15	D9	GROUND	—	GROUND	A16	A16	
HS	B16	C7	TX3+	→	RX3+	A17	A17	S23 (RX3+)
HS	B17	C8	TX3-	→	RX3-	A18	A18	S24 (RX3-)
GND	B18	C9	GROUND	—	GROUND	A19	A19	
RSV			RESERVED	NO WIRE	RESERVED	A20		
RSV			RESERVED	NO WIRE	RESERVED	A21		
GND	B1	D3	GROUND	—	GROUND	A22	A19	
HS	B2	D4	TX4+	→	RX4+	A23	A20	S2 (RX0+)
HS	B3	D5	TX4-	→	RX4-	A24	A21	S3 (RX0-)
GND	B4	C3	GROUND	—	GROUND	A25	A22	
HS	B5	C4	TX5+	→	RX5+	A26	A23	S9 (RX1+)
HS	B6	C5	TX5-	→	RX5-	A27	A24	S10 (RX1-)
GND	B7	C6	GROUND	—	GROUND	A28	A25	
SB	B8	A2	2W-CLKB, SCLockB(SB0B)	↔	2W-CLKB, SCLockB (SB0B)	A29	A26	
SB	B9	B2	2W-DATAB, SLoadB(SB1B)	↔	2W-DATAB, SLoadB (SB1B)	A30	A27	
SB	B10	C2	GND(SB2B)	—	GND (SB2B)	A31	A28	
SB	A11	D1	ADDB, SDataInB(SB5B)	↔	ADDB, SDataIn (SB5B)	A32	A29	
SB	B11	D2	CNTRLR_TYPEB(SB6B)	→	CNTRLR_TYPEB (SB6B)	A33	A30	
GND	B12	D6	GROUND	—	GROUND	A34	A31	
HS	B13	D7	TX6+	→	RX6+	A35	A32	S17 (RX2+)
HS	B14	D8	TX6-	→	RX6-	A36	A33	S18 (RX2-)
GND	B15	D9	GROUND	—	GROUND	A37	A34	
HS	B16	C7	TX7+	→	RX7+	A38	A35	S23 (RX3+)
HS	B17	C8	TX7-	→	RX7-	A39	A36	S24 (RX3-)
GND	B18	C9	GROUND	—	GROUND	A40	A37	

Table 7-5 SAS (x8) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane (1 of 2)

SAS-4 (SFF-8621/ SFF-8654) x8 Controller to SAS (x4 Pair) (SFF-8087/ SFF-8643) Backplane (Sheet 1 of 2)								
	Controller				Backplane			DEVICE
9400 Rev 0.2	SFF-8654 (74 Circuit)	SFF-8621 (80 Circuit)	9402 SAS Non-Symmetrical SAS-4 (x8) to Legacy (SFF-8087, SFF-8643) (x4) Pair Cable Interface	CABLE	9402 SAS Non-Symmetrical Legacy (SFF-8087, SFF-8643) (x4) Pair to SAS-4 (x8) Cable Interface	SFF-8643	SFF-8087	SFF-8639/ U.2 Connector (Pair of x4)
Type 1 8X	SAS-4 x8	SAS-4 x8	8X SAS Cables SFF-8448		8X SAS Cables SFF-8448	SAS-2.1, 3 x4	SAS-2.1 x4	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
GND	A1	A1	GROUND	—	GROUND	D3	B1	
HS	A2	A2	RX0+	←	TX0+	D4	B2	S6 (TX0+)
HS	A3	A3	RX0-	←	TX0-	D5	B3	S5 (TX0-)
GND	A4	A4	GROUND	—	GROUND	C3	B4	
HS	A5	A5	RX1+	←	TX1+	C4	B5	S13 (TX1+)
HS	A6	A6	RX1-	←	TX1-	C5	B6	S12 (TX1-)
GND	A7	A7	GROUND	—	GROUND	C6	B7	
SB	A8	A8	BP_TYPEA(SB7A)	←	BP_TYPEA (SB7A)	A2	B8	
SB	A9	A9	RESETA, SDataOutA(SB4A)	↔	RESETA, SDataOutA (SB4A)	C2	B10	
SB	A10	A10	GND(SB3A)	—	GND (SB3A)	B2	B9	
SB	A11	A11	(SBA+)	→	(SBA+)			
SB	A12	A12	(SBA-)	→	(SBA-)			
GND	A13	A13	GROUND	—	GROUND	D6	B12	
HS	A14	A14	RX2+	←	TX2+	D7	B13	S21 (TX2+)
HS	A15	A15	RX2-	←	TX2-	D8	B14	S20 (TX2-)
GND	A16	A16	GROUND	—	GROUND	D9	B15	
HS	A17	A17	RX3+	←	TX3+	C7	B16	S27 (TX3+)
HS	A18	A18	RX3-	←	TX3-	C8	B17	S26 (TX3-)
GND	A19	A19	GROUND	—	GROUND	C9	B18	
RSV		A20	RESERVED	NO WIRE	RESERVED			
RSV		A21	RESERVED	NO WIRE	RESERVED			
GND	A19	A22	GROUND	—	GROUND	D3	B1	
HS	A20	A23	RX4+	←	TX4+	D4	B2	S6 (TX0+)
HS	A21	A24	RX4-	←	TX4-	D5	B3	S5 (TX0-)
GND	A22	A25	GROUND	—	GROUND	C3	B4	
HS	A23	A26	RX5+	←	TX5+	C4	B5	S13 (TX1+)
HS	A24	A27	RX5-	←	TX5-	C5	B6	S12 (TX1-)
GND	A25	A28	GROUND	—	GROUND	C6	B7	
SB	A26	A29	BP_TYPEB(SB7B)	←	BP_TYPEB (SB7B)	A2	B8	
SB	A27	A30	RESETB, SDataOutB(SB4B)	↔	RESETB, SDataOutB (SB4B)	C2	B10	
SB	A28	A31	GND(SB3B)	—	GND (SB3B)	B2	B9	
SB	A29	A32	(SBB+)	→	(SBB+)			
SB	A30	A33	(SBB-)	→	(SBB-)			
GND	A31	A34	GROUND	—	GROUND	D6	B12	
HS	A32	A35	RX6+	←	TX6+	D7	B13	S21 (TX2+)
HS	A33	A36	RX6-	←	TX6-	D8	B14	S20 (TX2-)
GND	A34	A37	GROUND	—	GROUND	D9	B15	
HS	A35	A38	RX7+	←	TX7+	C7	B16	S27 (TX3+)
HS	A36	A39	RX7-	←	TX7-	C8	B17	S26 (TX3-)
GND	A37	A40	GROUND	—	GROUND	C9	B18	

Table 7-6 SAS (x8) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane (2 of 2)

SAS-4 (SFF-8621/ SFF-8654) x8 Controller to SAS (x4 Pair) (SFF-8087/ SFF-8643) Backplane (Sheet 2 of 2)								
9400 Rev 0.2	Controller			CABLE	Backplane			DEVICE
	SFF-8654 (74 Circuit)	SFF-8621 (80 Circuit)	9402 SAS Non-Symmetrical SAS-4 (x8) to Legacy (SFF-8087, SFF-8643) (x4) Pair Cable Interface		9402 SAS Non-Symmetrical Legacy (SFF-8087, SFF-8643) (x4) Pair to SAS-4 (x8) Cable Interface	SFF-8643	SFF-8087	
Type 1 8X	SAS-4 x8	SAS-4 x8	8X SAS Cables SFF-8448		8X SAS Cables SFF-8448	SAS-2.1, 3 x4	SAS-2.1 x4	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
GND	B1	B1	GROUND	—	GROUND	B3	A1	
HS	B2	B2	TX0+	→	RX0+	B4	A2	S2 (RX0+)
HS	B3	B3	TX0-	→	RX0-	B5	A3	S3 (RX0-)
GND	B4	B4	GROUND	—	GROUND	A3	A4	
HS	B5	B5	TX1+	→	RX1+	A4	A5	S9 (RX1+)
HS	B6	B6	TX1-	→	RX1-	A5	A6	S10 (RX1-)
GND	B7	B7	GROUND	—	GROUND	A6	A7	
SB	B8	B8	2W-CLKA, SClockA(SB0A)	↔	2W-CLKA, SClockA (SB0A)	A1	A8	
SB	B9	B9	2W-DATAA, SLoadA(SB1A)	↔	2W-DATAA, SloadA (SB1A)	B1	A9	
SB	B10	B10	GND(SB2A)	—	GND (SB2A)	C1	A10	
SB	B11	B11	ADDA, SDataInA(SB5A)	↔	ADDA, SDataInA (SB5A)	D2	B11	
SB	B12	B12	CNTRLR_TYPEA(SB6A)	→	CNTRLR_TYPEA (SB6)	D1	A11	
GND	B13	B13	GROUND	—	GROUND	B6	A12	
HS	B14	B14	TX2+	→	RX2+	B7	A13	S17 (RX2+)
HS	B15	B15	TX2-	→	RX2-	B8	A14	S18 (RX2-)
GND	B16	B16	GROUND	—	GROUND	B9	A15	
HS	B17	B17	TX3+	→	RX3+	A7	A16	S23 (RX3+)
HS	B18	B18	TX3-	→	RX3-	A8	A17	S24 (RX3-)
GND	B19	B19	GROUND	—	GROUND	A9	A18	
RSV		B20	RESERVED	NO WIRE	RESERVED			
RSV		B21	RESERVED	NO WIRE	RESERVED			
GND	B19	B22	GROUND	—	GROUND	B3	A1	
HS	B20	B23	TX4+	→	RX4+	B4	A2	S2 (RX0+)
HS	B21	B24	TX4-	→	RX4-	B5	A3	S3 (RX0-)
GND	B22	B25	GROUND	—	GROUND	A3	A4	
HS	B23	B26	TX5+	→	RX5+	A4	A5	S9 (RX1+)
HS	B24	B27	TX5-	→	RX5-	A5	A6	S10 (RX1-)
GND	B25	B28	GROUND	—	GROUND	A6	A7	
SB	B26	B29	2W-CLKB, SClockB(SB0B)	↔	2W-CLKB, SClockB (SB0B)	A1	A8	
SB	B27	B30	2W-DATAB, SLoadB(SB1B)	↔	2W-DATAB, SloadB (SB1B)	B1	A9	
SB	B28	B31	GND(SB2B)	—	GND (SB2B)	C1	A10	
SB	B29	B32	ADDB, SDataInB(SB5B)	↔	ADDB, SDataInB (SB5B)	D2	B11	
SB	B30	B33	CNTRLR_TYPEB(SB6B)	→	CNTRLR_TYPEB (SB6B)	D1	A11	
GND	B31	B34	GROUND	—	GROUND	B6	A12	
HS	B32	B35	TX6+	→	RX6+	B7	A13	S17 (RX2+)
HS	B33	B36	TX6-	→	RX6-	B8	A14	S18 (RX2-)
GND	B34	B37	GROUND	—	GROUND	B9	A15	
HS	B35	B38	TX7+	→	RX7+	A7	A16	S23 (RX3+)
HS	B36	B39	TX7-	→	RX7-	A8	A17	S24 (RX3-)
GND	B37	B40	GROUND	—	GROUND	A9	A18	

Table 7-7 SAS-4 and SAS-2.1/ SAS 3 Sidebands Only (1 of 1)

SFF-9402 SAS-4 (SFF-8621/ SFF-8654) and SAS-2.1/ SAS 3 (SFF-8087/ SFF-8643) Sidebands Only (Sheet 1 of 1)									
	Controller					Backplane			
SFF- 9402 Cable Interface for SAS	SFF-8087	SFF-8643	SFF-8654	SFF-8621	CABLE	SFF-8621	SFF-8654	SFF-8643	SFF-8087
SAS Only Cable SFF-8448	SAS-2.1	SAS-2.1, 3	SAS-4	SAS-4		SAS-4	SAS-4	SAS-2.1, 3	SAS-2.1
Signal Name	PIN	PIN	PIN	PIN	DIR	PIN	PIN	PIN	PIN
BP_TYPE(SB7)	A8(SB7)	A1(SB7)	A8(SB7)	A9(SB7)	←	B9(SB7)	B8(SB7)	A2(SB7)	B8(SB7)
RESET, SDataOut(SB4)	A10(SB4)	C1(SB4)	A9(SB4)	A10(SB4)	→	B10(SB4)	B9(SB4)	C2(SB4)	B10(SB4)
GND(SB3)	A9(SB3)	B1(SB3)	A10(SB3)	A11 (SB3)	—	B11(SB3)	B10(SB3)	B2(SB3)	B9(SB3)
(SB+)			A11(SB+)	A12(SB+)	→	B12(SB+)	B11(SB+)		
(SB-)			A12(SB-)	A13(SB-)	→	B13(SB-)	B12(SB-)		
2W-CLK, SClock(SB0)	B8(SB0)	A2(SB0)	B8(SB0)	B9(SB0)	↔	A9(SB0)	A8(SB0)	A1(SB0)	A8(SB0)
2W-DATA, Sload(SB1)	B9(SB1)	B2(SB1)	B9(SB1)	B10(SB1)	↔	A10(SB1)	A9(SB1)	B1(SB1)	A9(SB1)
GND(SB2)	B10(SB2)	C2(SB2)	B10(SB2)	B11(SB2)	—	A11(SB2)	A10(SB2)	C1(SB2)	A10(SB2)
ADD, SDataIn(SB5)	A11(SB5)	D1(SB5)	B11(SB5)	B12(SB5)	↔	A12(SB5)	A11(SB5)	D2(SB5)	B11(SB5)
CNTRLR_TYPE(SB6)	B11(SB6)	D2(SB6)	B12(SB6)	B13(SB6)	→	A13(SB6)	A12(SB6)	D1(SB6)	A11(SB6)