

This document was developed by the SFF Committee prior to it becoming the SFF TA (Technology Affiliate) TWG (Technical Working Group) of the SNIA (Storage Networking Industry Association) in 2016.

The information below should be used instead of the equivalent herein.

POINTS OF CONTACT: SFF TA TWG Chair Email: sff-chair@snia.org.

LOCATION OF SFF DOCUMENTS: <http://www.snia.org/sff/specifications>.

Suggestions for improvement of this specification are welcome and should be submitted to <http://www.snia.org/feedback>.

If you are interested in participating in the activities of the SFF TA TWG, additional information and the membership application can be found at:

<http://www.snia.org/sff>.

SFF specifications are available at <http://www.snia.org/sff/specifications>

SFF Committee

SFF-9401

Specification for

Universal Multi-Protocol Single Cable for SAS/PCIe

Rev 1.0 November 30, 2016

Secretariat: SFF Committee

Abstract: This specification recommends the pinouts to enable a universal internal SAS-4 (pre Rev 0.7) (MiniLink) / PCIe (OCuLink) cable assembly. It also recommends the pinouts enabling universal cables employing previous SAS connectors.

This specification provides a common reference for systems manufacturers, system integrators, and suppliers. This is an internal working specification of the SFF Committee, an industry ad hoc group.

This specification is made available for public review, and written comments are solicited from readers. Comments received will be considered for inclusion in future revisions of this specification.

Support: This specification is supported by the identified member companies of the SFF Committee.

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Change History

Rev 0.1

- Presentation incorporated as an i-specification

Rev 0.2

- Introduced as a Development project

Rev 0.3

- Formatted to the current style

Rev 0.4

- Recognized contributor of pinout tables
- Updated Figure 3-1
- Corrected typos and software translation errors within the tables
- Created Section 4
- Added Table 4-4 and Table 4-5

Rev 0.5

- Changed Table 4-1, 4-2 and 4-3 color tones

Rev 0.6

- Changed title

Rev 0.8

- Changed Abstract to be more descriptive of the content of the specification
- Renamed Section 4 to match purpose
- Reordered the Implementation notes and added space between them to improve readability
- Reordered the tables to put the examples first
- Corrected Table 4-1 column 2 to add color bars back that did not transfer in a previous Revision
- Corrected Ground symbols in Tables column 6 (CABLE) that did not transfer properly in a previous Revision
- Updated 9400 sideband naming convention per HP feedback
- Added note re 8X sideband pin assignments

Rev 0.9

- Renamed the Specification for clarity
- Reordered the tables and reformatted the presentation of the tables for clarity based on input from members; no sidebands were reassigned
- Reordered the notes and revised for clarity, added column for SFF-9400
- Added references to SFF-9402

Rev 1.0

- Superseded by SFF-9402

Foreword

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

If you are interested in participating or wish to follow the activities of the SFF Committee, the sign up for membership and/or documentation can be found at:

www.sffcommittee.com/ie/join.html

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

<ftp://ftp.seagate.com/sff/SFF-8000.TXT>

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:

<ftp://ftp.seagate.com/sff/SFF-8032.TXT>

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

SUPERSEDED by SFF-9402

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SUPERSEDED BY SFF-9402

1. Scope

Industry storage solutions are implementing both SAS and PCIe within the same or similar enclosures. This specification recommends the pinning out of standardized connectors to accommodate multiple protocols.

2. References

2.1 Industry Documents

- OCuLink Spec Rev 1.0
- SFF-8087 Mini Multilane 4X Unshielded Connector Shell and Plug
- SFF-8448 SAS Sideband Signal Assignments
- SFF-8611 MiniLink 4/8X I/O Cable Assemblies
- SFF-8612 MiniLink 4/8X Shielded Connector
- SFF-8613 Mini Multilane 4/8X Unshielded Connector (HDun)
- SFF-8654 0.6mm 4/8X Unshielded I/O Connector
- SFF-9400 Universal 4/8X Pinout
- SFF-9402 Universal Multi-Protocol Dual Cable for SAS/PCIe

2.2 SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at <ftp://ftp.seagate.com/sff/SFF-8000.TXT>

2.3 Sources

Those who join the SFF Committee as an Observer or Member receive electronic copies of the minutes and SFF specifications (<http://www.sffcommittee.com/ie/join.html>).

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (<http://www.techstreet.com/incitsgate.tmpl>).

3. General Description

The connector figures below are shown for reference only to show how the pinouts shown in the tables relate to the physical locations of the pins for each of the connector styles. These pinouts comply with the SAS pinouts defined in SFF-8448 and in the PCIe pinouts defined by OCuLink. All are based on the fixed end definitions of the pin assignments.

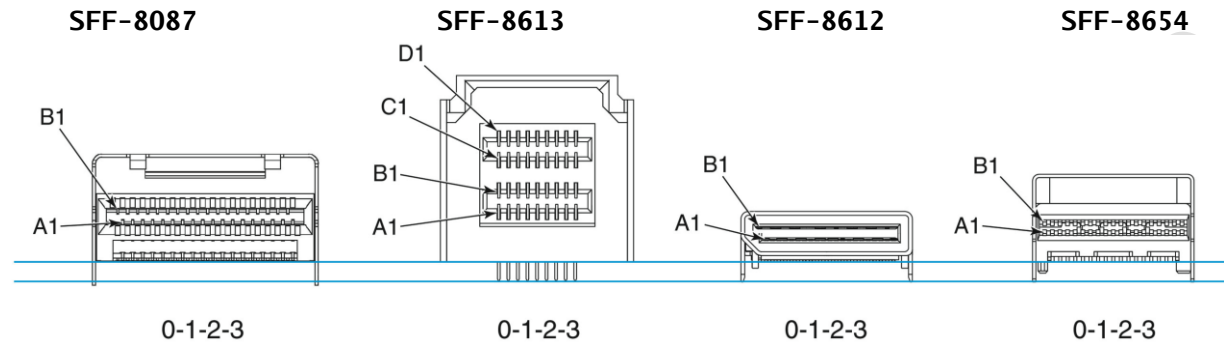


FIGURE 3-1 CONNECTOR VIEWS

4. Pinout Tables with System Compatibility Issues and Implementation Notes

The following notes provide the background information required to implement a universal multiprotocol single cable for SAS and PCIe (SAS/PCIE).

System Compatibility Issues

1. Present PCI Express legacy internal implementations using SFF-8643/73 connectors are vendor specific (Not standardized) and do not align with legacy SAS/SATA implementations. Some are 85Ω; some have a white ring on fixed ends. As a result, PCIe cables utilizing SFF-8643/73 connectors can currently be plugged into legacy SAS/SATA implementations resulting in signal incompatibilities.
2. Legacy SAS/SATA internal pin assignments for SFF-8673 connectors are based on SAS 2.1/ SAS-3 T-10 standards and SFF-8448.
3. SFF-9402 enables a two cable solution for SAS specific and PCIe specific implementations
4. SAS standards can incorporate SGPIO or SCSI Enclosure Services (SES) depending on the physical sideband protocol utilized. SES provides a method to bridge the multiprotocol environment via 2Wire interface to discover what backplane/end point is present prior to any in-band communication/operation.
5. Controllers and Backplanes that are designed to be aware of 9401 can avoid incompatibility issues with signal levels when migrating from legacy to MiniLink, Slimline SAS and OCuLink.
6. SFF-9401 signal assignments are controlled by the Fixed side initiator and Fixed side backplane only. PCIe OCuLink 1.0 defines the signals based on the Fixed ends of the interface; SFF-8448 defines them for SAS. SFF-9400 defines the basic locations of undefined High Speed and Vendor Specific signals for the SFF-8612 and 8654 connectors.
7. PCIe mini-SAS HD vendor specific/sideband assignments are based on OCuLink 1.0 definitions.

8. SFF-9401 aligns both PCIe and SAS sideband assignments via SFF-8448 (SB0-9). The addition of “Other Bus Types” to SFF-8448 Rev 1.0 facilitates a common 2W interface and BP Type for both SAS and PCIe for determining bus type operation. Note – because the use of sideband signals differs between protocols, each sideband signal must be isolated i.e. not commoned in the cable.

Implementation Notes:

9. The pinouts in this spec define full crossover cables (The A row on one end crosses over to the B row on the other end).
10. New SAS cables built to this pinout will still work on old initiators and backplanes that were pinned out to the appropriate SAS standard.
11. The sideband pin assignments for the SFF-8643/73 connector have been optimized to support PCIe sideband (REFCLK) signals if required, and would revert back to the SAS definitions for SAS applications.
12. The tables define the lane and polarity of the high speed pairs.
13. Lane reversal is not mandatory for end point devices (See the PCI Express CEM Spec).
14. Multiple implementations exist for PCI Express based on SFF-8087 and SFF-8643/73. This specification was created to enable a common cable across multiple interfaces; therefore the previous protocol specific pinouts may not apply.
15. Care should be taken to drive all signals as defined by the pinouts in SFF-9401 to enable the benefits of the design.
16. On the x8 sideband pin assignments the “A-Side” is associated with lanes 0-3 and the “B-side” with 4-7. Both are considered independent out of band interfaces.
17. In a x8 only implementation, the sidebands designated as “A” are considered to be primary.

TABLE 4-1 PINOUT FOR A 4X INTERFACE WITH SIDEBANDS

	Controller / Initiator / Root (Downstream)								CABLE	Backplane/ Endpoint (Upstream)								DEVICE	DEVICE	
9400 Rev 0.2	8087	8643	mini-SAS HD	8654	SlimLine SAS	8612	OCuLink 1.0	9401 Universal Multi-Protocol Single Cable for SAS/PCIE		9401 Universal Multi-Protocol Single Cable for SAS/PCIE	OCuLink 1.0	8612	SlimLine SAS	8654	mini-SAS HD	8643	8087	SFF-8639	MultiLink	
Type 1 4X	SAS-2.1	SAS-2.1.3	PCIE	SAS-4	PCIE	SAS-4	PCIE	4X Single Cable OCuLink 1.0 / SFF-8448		4X Single Cable SFF-8448/OCuLink 1.0	PCIE	SAS-4	PCIE	SAS-4	PCIE	SAS-2.1.3	SAS-2.1	PCIE	SAS	
	PIN	PIN	PIN	PIN	PIN	PIN	PIN	ROOT / Controller	DIR	Backplane/ END Point	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN
RSV						A1(RSVd)	A1(RESERVED)	RESERVED	NC	RESERVED	B1(RESERVED)	B1(RSVd)								
GND	A1	B3	B3	A1	A1	A2	A2	GROUND	GROUND	B2	B2	B1	B1	D3	D3	B1			
HS	A2	B4	B4	A2	A2	A3	A3	PER(RX)p0	←	PET(TX)p0	B3	B3	B2	B2	D4	D4	B2	E14 (PERp0)	S6 (TX0+)	
HS	A3	B5	B5	A3	A3	A4	A4	PER(RX)n0	←	PET(TX)n0	B4	B4	B3	B3	D5	D5	B3	E13 (PERn0)	S5 (TX0-)	
GND	A4	A3	A3	A4	A4	A5	A5	GROUND	GROUND	B5	B5	B4	B4	C3	C3	B4			
HS	A5	A4	A4	A5	A5	A6	A6	PER(TX)p1	←	PET(TX)p1	B6	B6	B5	B5	C4	C4	B5	S21 (PERp1)	S13 (TX1+)	
HS	A6	A5	A5	A6	A6	A7	A7	PER(RX)n1	←	PET(TX)n1	B7	B7	B6	B6	C5	C5	B6	S20 (PERn1)	S12 (TX1-)	
GND	A7	A6	A6	A7	A7	A8	A8	GROUND	GROUND	B8	B8	B7	B7	C6	C6	B7			
SB	A8(SB7)	A1(SB7)	A1(VSP7)	A8(SB7)	A8(VSP7)	A9(SB7)	A9(BP_TYPE)	BP_TYPE(VSP7) / BP_TYPE(SB7)	←	(SB7)BP_TYPE / (VSP7)BP_TYPE	B9(SB7)	B8(VSP7)	B8(SB7)	B8(VSP7)	A2(SB7)	A2(SB7)	B8(SB7)			
SB	A9(SB3)	B1(SB3)	B1(VSP3)	A9(SB3)	A9(VSP3)	A10(SB3)	A10(CWAKEH/OBFF)	CWAKEH_OBFF(VSP3) / GND(SB3)	↔	(SB3)GND / (VSP3)CWAKEH_OBFF	B10(SB3)	B9(VSP3)	B9(SB3)	B9(VSP3)	B2(VSP3)	B2(SB3)	B9(SB3)	P1 (WAKE#)		
SB				A10(SB9)	A10(VSP9)	A11(SB9)	A11(GND)	GND(VSP9) / GND(SB9)	(SB9)GND / (VSP9)GND	B11(SB9)	B10(VSP9)	B10(SB9)	B10(VSP9)						
SB	A10(SB4)	C1(SB4)	C1(VSP4)	A11(SB4)	A11(VSP4)	A12(SB4)	A12(VSP)(REFCLK+)	REFCLK+(VSP4) / RESET_SDataOut(SB4)	→	(SB4)SDataOut_RESET / (VSP4)REFCLK+	B12(VSP)(REFCLK+)	B12(SB4)	B11(VSP4)	B11(SB4)	C2(VSP4)	C2(SB4)	B10(SB4)	E7 (REFCLK+)		
SB	A11(SB5)	D1(SB5)	D1(VSP5)	A12(SB5)	A12(VSP5)	A13(SB5)	A13(VSP)(REFCLK-)	REFCLK-(VSP5) / ADD_SDataIn(SB5)	↔	(SB5)SDataIn_ADD / (VSP5)REFCLK-	B13(VSP)(REFCLK-)	B13(SB5)	B12(VSP5)	B12(SB5)	D2(VSP5)	D2(SB5)	B11(SB5)	E8 (REFCLK-)		
GND	A12	B6	B6	A13	A13	A14	A14	GROUND	GROUND	B14	B14	B13	B13	D6	D6	B12			
HS	A13	B7	B7	A14	A14	A15	A15	PER(RX)p2	←	PETp2	B15	B15	B14	B14	D7	D7	B13	S27 (PERp2)	S21 (TX2+)	
HS	A14	B8	B8	A15	A15	A16	A16	PER(RX)n2	←	PETn2	B16	B16	B15	B15	D8	D8	B14	S26 (PERn2)	S20 (TX2-)	
GND	A15	B9	B9	A16	A16	A17	A17	GROUND	GROUND	B17	B17	B16	B16	D9	D9	B15			
HS	A16	A7	A7	A17	A17	A18	A18	PER(RX)p3	←	PET(TX)p3	B18	B18	B17	B17	C7	C7	B16	E21 (PERp3)	S27 (TX3+)	
HS	A17	A8	A8	A18	A18	A19	A19	PER(RX)n3	←	PET(TX)n3	B19	B19	B18	B18	C8	C8	B17	E20 (PERn3)	S26 (TX3-)	
GND	A18	A9	A9	A19	A19	A20	A20	GROUND	GROUND	B20	B20	B19	B19	C9	C9	B18			
RSV						A21(RSVd)	A21(RESERVED)	RESERVED	NC	RESERVED	B21(RESERVED)	B21(RSVd)								
RSV						B1(RSVd)	B1(RESERVED)	RESERVED	NC	RESERVED	A1(RESERVED)	A1(RSVd)								
GND	B1	D3	D3	B1	B1	B2	B2	GROUND	GROUND	A2	A2	A1	A1	B3	B3	A1			
HS	B2	D4	D4	B2	B2	B3	B3	PET(TX)p0	→	PER(RX)p0	A3	A3	A2	A2	B4	B4	A2	E10 (PETp0)	S2 (RX0+)	
HS	B3	D5	D5	B3	B3	B4	B4	PER(RX)n0	→	PER(RX)n0	A4	A4	A3	A3	B5	B5	A3	E11 (PERn0)	S3 (RX0-)	
GND	B4	C3	C3	B4	B4	B5	B5	GROUND	GROUND	A5	A5	A4	A4	A3	A3	A4			
HS	B5	C4	C4	B5	B5	B6	B6	PET(TX)p1	→	PER(RX)p1	A6	A6	A5	A5	A4	A4	A5	S17 (PETp1)	S9 (RX1+)	
HS	B6	C5	C5	B6	B6	B7	B7	PET(TX)n1	→	PER(RX)n1	A7	A7	A6	A6	A5	A5	A6	S18 (PETn1)	S10 (RX1-)	
GND	B7	C6	C6	B7	B7	B8	B8	GROUND	GROUND	A8	A8	A7	A7	A6	A6	A7			
SB	B8(SB0)	A2(SB0)	A2(VSP0)	B8(SB0)	B8(VSP0)	B9(SB0)	B9(2W-CLK)	2W-CLK(VSP0) / 2W-CLK(SB0)	↔	(SB0)2W-CLK / (VSP0)2W-CLK	A9(2W-CLK)	A9(SB0)	A8(VSP0)	A8(SB0)	A1(VSP0)	A1(SB0)	A8(SB0)			
SB	B9(SB1)	B2(SB1)	B2(VSP1)	B9(SB1)	B9(VSP1)	B10(SB1)	B10(2W-DATA)	2W-DATA(VSP1) / 2W-DATA(SB1)	↔	(SB1)2W-DATA / (VSP1)2W-DATA	A10(2W-DATA)	A10(SB1)	A9(VSP1)	A9(SB1)	B1(VSP1)	B1(SB1)	A9(SB1)			
SB				B10(SB8)	B10(VSP8)	B11(SB8)	B11(GND)	GND(VSP8) / GND(SB8)	(SB8)GND / (VSP8)GND	A11(GND)	A11(SB8)	A10(VSP8)	A10(SB8)						
SB	B10(SB2)	C2(SB2)	C2(VSP2)	B11(SB2)	B11(VSP2)	B12(SB2)	B12(PERST#)	PERSTH(VSP2) / GND(SB2)	↔	(SB2)GND / (VSP2)PERSTH	A12(PERST#)	A12(SB2)	A11(VSP2)	A11(SB2)	C1(VSP2)	C1(SB2)	A10(SB2)	E5 (PERST#)		
SB	B11(SB6)	D2(SB6)	D2(VSP6)	B12(SB6)	B12(VSP6)	B13(SB6)	B13(CPRSNT#)	CPRSNTH(VSP6) / CNTRLR_TYPE(SB6)	↔	(SB6)CNTRLR_TYPE / (VSP6)CPRSNT#	A13(CPRSNT#)	A13(SB6)	A12(VSP6)	A12(SB6)	D1(VSP6)	D1(SB6)	A11(SB6)			
GND	B12	D6	D6	B13	B13	B14	B14	GROUND	GROUND	A14	A14	A13	A13	B6	B6	A12			
HS	B13	D7	D7	B14	B14	B15	B15	PET(TX)p2	→	PER(RX)p2	A15	A15	A14	A14	B7	B7	A13	S23 (PETp2)	S17 (RX2+)	
HS	B14	D8	D8	B15	B15	B16	B16	PER(RX)n2	→	PER(RX)n2	A16	A16	A15	A15	B8	B8	A14	S24 (PERn2)	S18 (RX2-)	
GND	B15	D9	D9	B16	B16	B17	B17	GROUND	GROUND	A17	A17	A16	A16	B9	B9	A15			
HS	B16	C7	C7	B17	B17	B18	B18	PET(TX)p3	→	PER(RX)p3	A18	A18	A17	A17	A7	A7	A16	E17 (PETp3)	S23 (RX3+)	
HS	B17	C8	C8	B18	B18	B19	B19	PER(RX)n3	→	PER(RX)n3	A19	A19	A18	A18	A8	A8	A17	E18 (PERn3)	S24 (RX3-)	
GND	B18	C9	C9	B19	B19	B20	B20	GROUND	GROUND	A20	A20	A19	A19	A9	A9	A18			
RSV						B21(RSVd)	B21(RESERVED)	RESERVED	NC	RESERVED	A21(RESERVED)	A21(RSVd)								

TABLE 4-2 EXAMPLE PINOUT FROM SAS SFF-8643 TO SAS SFF-8612

9400 Rev 0.2	Controller (Downstream)			CABLE	Backplane (Upstream)			DEVICE
	8643	9401 Universal Multi-Protocol Single Cable for SAS/PCIe			9401 Universal Multi-Protocol Single Cable for SAS/PCIe	8612	8654	
Type 1 4X	SAS-2.1, 3	4X Single Cable SFF-8448			4X Single Cable SFF-8448	SAS-4	SAS-4	SAS
	PIN	Controller	DIR		Backplane	PIN	PIN	PIN
RSV		RESERVED	NC		RESERVED	B1(RSVD)		
GND	B3	GROUND		GROUND	B2	B1	
HS	B4	PER(RX)p0	←		PET(TX)p0	B3	B2	S6 (TX0+)
HS	B5	PER(RX)n0	←		PET(TX)n0	B4	B3	S5 (TX0-)
GND	A3	GROUND		GROUND	B5	B4	
HS	A4	PER(RX)p1	←		PET(TX)p1	B6	B5	S13 (TX1+)
HS	A5	PER(RX)n1	←		PET(TX)n1	B7	B6	S12 (TX1-)
GND	A6	GROUND		GROUND	B8	B7	
SB	A1(SB7)	BP_TYPE(SB7)	←		(SB7)BP_TYPE	B9(SB7)	B8(SB7)	
SB	B1(SB3)	GND(SB3)	↔		(SB3)GND	B10(SB3)	B9(SB3)	
SB		GND(SB9)		(SB9)GND	B11(SB9)	B10(SB9)	
SB	C1(SB4)	RESET, SDataOut(SB4)	→		(SB4)SDataOut,RESET	B12(SB4)	B11(SB4)	
SB	D1(SB5)	ADD, SDataIn(SB5)	↔		(SB5)SDataIn,ADD	B13(SB5)	B12(SB5)	
GND	B6	GROUND		GROUND	B14	B13	
HS	B7	PER(RX)p2	←		PETp2	B15	B14	S21 (TX2+)
HS	B8	PER(RX)n2	←		PETn2	B16	B15	S20 (TX2-)
GND	B9	GROUND		GROUND	B17	B16	
HS	A7	PER(RX)p3	←		PET(TX)p3	B18	B17	S27 (TX3+)
HS	A8	PER(RX)n3	←		PET(TX)n3	B19	B18	S26 (TX3-)
GND	A9	GROUND		GROUND	B20	B19	
RSV		RESERVED	NC		RESERVED	B21(RSVD)		
RSV		RESERVED	NC		RESERVED	A1(RSVD)		
GND	D3	GROUND		GROUND	A2	A1	
HS	D4	PET(TX)p0	→		PER(RX)p0	A3	A2	S2 (RX0+)
HS	D5	PET(TX)n0	→		PER(RX)n0	A4	A3	S3 (RX0-)
GND	C3	GROUND		GROUND	A5	A4	
HS	C4	PET(TX)p1	→		PER(RX)p1	A6	A5	S9 (RX1+)
HS	C5	PET(TX)n1	→		PER(RX)n1	A7	A6	S10 (RX1-)
GND	C6	GROUND		GROUND	A8	A7	
SB	A2(SB0)	2W-CLK(SB0)	↔		(SB0)2W-CLK	A9(SB0)	A8(SB0)	
SB	B2(SB1)	2W-DATA(SB1)	↔		(SB1)2W-DATA	A10(SB1)	A9(SB1)	
SB		GND(SB8)		(SB8)GND	A11(SB8)	A10(SB8)	
SB	C2(SB2)	GND(SB2)	→		(SB2)GND	A12(SB2)	A11(SB2)	
SB	D2(SB6)	CNTRLR_TYPE(SB6)	↔		(SB6)CNTRLR_TYPE	A13(SB6)	A12(SB6)	
GND	D6	GROUND		GROUND	A14	A13	
HS	D7	PET(TX)p2	→		PER(RX)p2	A15	A14	S17 (RX2+)
HS	D8	PET(TX)n2	→		PER(RX)n2	A16	A15	S18 (RX2-)
GND	D9	GROUND		GROUND	A17	A16	
HS	C7	PET(TX)p3	→		PER(RX)p3	A18	A17	S23 (RX3+)
HS	C8	PET(TX)n3	→		PER(RX)n3	A19	A18	S24 (RX3-)
GND	C9	GROUND		GROUND	A20	A19	
RSV		RESERVED	NC		RESERVED	A21(RSVD)		

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TABLE 4-3 EXAMPLE PINOUT FROM MINI-SAS HD SFF-8613 TO OCULINK 1.0

	Root (Downstream)			Endpoint (Upstream)			DEVICE
9400 Rev 0.2	mini-SAS HD	9401 Universal Multi-Protocol Single Cable for SAS/PCIe	CABLE	9401 Universal Multi-Protocol Single Cable for SAS/PCIe	OCuLink 1.0	SlimLine SAS	SFF-8639
Type 1 4X	PCIE	4X Single Cable OCuLink 1.0		4X Single Cable OCuLink 1.0	PCIE	PCIE	PCIE
	PIN	ROOT	DIR	END Point	PIN	PIN	PIN
RSV		RESERVED	NC	RESERVED	B1(RESERVED)		
GND	B3	GROUND	GROUND	B2	B1	
HS	B4	PER(RX)p0	←	PET(TX)p0	B3	B2	E14 (PERp0)
HS	B5	PER(RX)n0	←	PET(TX)n0	B4	B3	E13 (PERn0)
GND	A3	GROUND	GROUND	B5	B4	
HS	A4	PER(RX)p1	←	PET(TX)p1	B6	B5	S21 (PERp1)
HS	A5	PER(RX)n1	←	PET(TX)n1	B7	B6	S20 (PERn1)
GND	A6	GROUND	GROUND	B8	B7	
SB	A1(VSP7)	BP_TYPE(VSP7)	←	(VSP7)BP_TYPE	B9 (BP_TYPE)	B8(VSP7)	
SB	B1(VSP3)	CWAKE#,OBFF(VSP3)	↔	(VSP3)CWAKE#,OBFF	B10 (CWAKE#/OBFF)	B9(VSP3)	P1 (WAKE#)
SB		GND(VSP9)	(VSP9)GND	B11(GND)	B10(VSP9)	
SB	C1(VSP4)	REFCLK+(VSP4)	→	(VSP4)REFCLK+	B12 (VSP)REFCLK+	B11(VSP4)	E7 (REFCLK+)
SB	D1(VSP5)	REFCLK-(VSP5)	↔	(VSP5)REFCLK-	B13(VSP)(REFCLK-)	B12(VSP5)	E8 (REFCLK-)
GND	B6	GROUND	GROUND	B14	B13	
HS	B7	PER(RX)p2	←	PETp2	B15	B14	S27 (PERp2)
HS	B8	PER(RX)n2	←	PETn2	B16	B15	S26 (PERn2)
GND	B9	GROUND	GROUND	B17	B16	
HS	A7	PER(RX)p3	←	PET(TX)p3	B18	B17	E21 (PERp3)
HS	A8	PER(RX)n3	←	PET(TX)n3	B19	B18	E20 (PERn3)
GND	A9	GROUND	GROUND	B20	B19	
RSV		RESERVED	NC	RESERVED	B21(RESERVED)		
RSV		RESERVED	NC	RESERVED	A1(RESERVED)		
GND	D3	GROUND	GROUND	A2	A1	
HS	D4	PET(TX)p0	→	PER(RX)p0	A3	A2	E10 (PETp0)
HS	D5	PET(TX)n0	→	PER(RX)n0	A4	A3	E11 (PETn0)
GND	C3	GROUND	GROUND	A5	A4	
HS	C4	PET(TX)p1	→	PER(RX)p1	A6	A5	S17 (PETp1)
HS	C5	PET(TX)n1	→	PER(RX)n1	A7	A6	S18 (PETn1)
GND	C6	GROUND	GROUND	A8	A7	
SB	A2(VSP0)	2W-CLK(VSP0)	↔	(VSP0)2W-CLK	A9 (2W-CLK)	A8(VSP0)	
SB	B2(VSP1)	2W-DATA(VSP1)	↔	(VSP1)2W-DATA	A10 (2W-DATA)	A9(VSP1)	
SB		GND(VSP8)	(VSP8)GND	A11 (GND)	A10(VSP8)	
SB	C2(VSP2)	PERST#(VSP2)	→	(VSP2)PERST#	A12 (PERST#)	A11(VSP2)	E5 (PERST#)
SB	D2(VSP6)	CPRSNT#(VSP6)	↔	(VSP6)CPRSNT#	A13 (CPRSNT#)	A12(VSP6)	
GND	D6	GROUND	GROUND	A14	A13	
HS	D7	PET(TX)p2	→	PER(RX)p2	A15	A14	S23 (PETp2)
HS	D8	PET(TX)n2	→	PER(RX)n2	A16	A15	S24 (PETn2)
GND	D9	GROUND	GROUND	A17	A16	
HS	C7	PET(TX)p3	→	PER(RX)p3	A18	A17	E17 (PETp3)
HS	C8	PET(TX)n3	→	PER(RX)n3	A19	A18	E18 (PETn3)
GND	C9	GROUND	GROUND	A20	A19	
RSV		RESERVED	NC	RESERVED	A21(RESERVED)		

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TABLE 4-4 PINOUT FOR AN 8X INTERFACE WITH SIDEBANDS (1 OF 2)

Controller / Initiator / Root (Downstream)										Backplane / Endpoint (Upstream)										DEVICE	DEVICE
9400 Rev 0.2	8087	8643	mini-SAS HD	8654	SlimLine SAS	8612	OCuLink	9401 Universal Multi-Protocol Single Cable for SAS/PCIE	CABLE	9401 Universal Multi-Protocol Single Cable for SAS/PCIE	OCuLink	8612	SlimLine SAS	8654	mini-SAS HD	8643	8087	SFF-8639	MultiLink		
Type 1 8X	SAS-2.1 x4	SAS-2.1, 3 x4	PCIe x4	SAS-4 x8	PCIe x8	SAS-4 x8	PCIe x8	8X Single Cable OCuLink 1.0 / SFF-8448	DIR	8X Single Cable SFF-8448/OCuLink 1.0	PCIe x8	SAS-4 x8	PCIe x8	SAS-4 x8	PCIe x8	SAS-2.1, 3 x4	SAS-2.1 x4	PCIe	SAS		
	PIN	PIN	PIN	PIN	PIN	PIN	PIN	ROOT / Controller		Backplane / END Point	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	
GND	A1	B3	B3	A1	A1	A1	A1	GROUND	GROUND	B1	B1	B1	B1	D3	D3	B1				
HS	A2	B4	B4	A2	A2	A2	A2	PER(RX)p0	←	PET(TX)p0	B2	B2	B2	B2	D4	D4	B2	E14 (PERp0)	S6 (TX0+)		
HS	A3	B5	B5	A3	A3	A3	A3	PER(RX)n0	←	PET(TX)n0	B3	B3	B3	B3	D5	D5	B3	E13 (PERn0)	S5 (TX0-)		
GND	A4	A3	A3	A4	A4	A4	A4	GROUND	GROUND	B4	B4	B4	B4	C3	C3	B4				
HS	A5	A4	A4	A5	A5	A5	A5	PER(RX)p1	←	PET(TX)p1	B5	B5	B5	B5	C4	C4	B5	S21 (PERp1)	S13 (TX1+)		
HS	A6	A5	A5	A6	A6	A6	A6	PER(RX)n1	←	PET(TX)n1	B6	B6	B6	B6	C5	C5	B6	S20 (PERn1)	S12 (TX1-)		
GND	A7	A6	A6	A7	A7	A7	A7	GROUND	GROUND	B7	B7	B7	B7	C6	C6	B7				
SB	A8(SB7)	A1(SB7)	A1(VSP7)	A8(SB7A)	A8(VSP7A)	A8(SB7A)	A8(BP_TYPEA)	BP_TYPEA(VSP7A) / BP_TYPEA(SB7A)	←	(SB7A)BP_TYPEA / (VSP7A)BP_TYPEA	B8(BP_TYPEA)	B8(SB7A)	B8(VSP7A)	B8(SB7A)	A2(VSP7)	A2(SB7)	B8(SB7)				
SB	A9(SB3)	B1(SB3)	B1(VSP3)	A9(SB3A)	A9(VSP3A)	A9(SB3A)	A9(CWAKEA#/OBFFA)	CWAKEA#,OBFFA(VSP3A) / GND(SB3A)	↔	(SB3A)GND / (VSP3A)CWAKEA#,OBFFA	B9(CWAKEA#/OBFFA)	B8(SB3A)	B9(VSP3A)	B9(SB3A)	B2(VSP3)	B2(SB3)	B9(SB3)	P1 (WAKE#)			
SB				A10(SB9A)	A10(VSP9A)	A10(SB9A)	A10(GND)	GND(VSP9A) / GND(SB9A)	(SB9A)GND / (VSP9A)GND	B10(GND)	B10(SB9A)	B10(VSP9A)	B10(SB9A)							
SB	A10(SB4)	C1(SB4)	C1(VSP4)	A11(SB4A)	A11(VSP4A)	A11(SB4A)	A11(REFCLKA+)	REFCLK+(VSP4A) / RESETB, SDataOutB(SB4A)	→	(SB4A)DataOutA,ADD8 / (VSP4A)REFCLKA+	B11(VSP4)REFCLKA+	B11(SB4A)	B11(VSP4A)	B11(SB4A)	C2(VSP4)	C2(SB4)	B10(SB4)	E7 (REFCLK+)			
SB	A11(SB5)	D1(SB5)	D1(VSP5)	A12(SB5A)	A12(VSP5A)	A12(SB5A)	A12(VSPA)REFCLKA-	REFCLK-(VSPA) / ADDA, SDataInA(SB5A)	↔	(SB5A)SDataInA,ADDA / (VSPA)REFCLKA-	B12(VSPA)REFCLKA-	B12(SB5A)	B12(VSP5A)	B12(SB5A)	D2(VSP5)	D2(SB5)	B11(SB5)	E8 (REFCLK-)			
GND	A12	B6	B6	A13	A13	A13	A13	GROUND	GROUND	B13	B13	B13	B13	D6	D6	B12				
HS	A13	B7	B7	A14	A14	A14	A14	PER(RX)p2	←	PETp2	B14	B14	B14	B14	D7	D7	B13	S27 (PERp2)	S21 (TX2+)		
HS	A14	B8	B8	A15	A15	A15	A15	PER(RX)n2	←	PETn2	B15	B15	B15	B15	D8	D8	B14	S26 (PERn2)	S20 (TX2-)		
GND	A15	B9	B9	A16	A16	A16	A16	GROUND	GROUND	B16	B16	B16	B16	D9	D9	B15				
HS	A16	A7	A7	A17	A17	A17	A17	PER(RX)p3	←	PET(TX)p3	B17	B17	B17	B17	C7	C7	B16	E21 (PERp3)	S27 (TX3+)		
HS	A17	A8	A8	A18	A18	A18	A18	PER(RX)n3	←	PET(TX)n3	B18	B18	B18	B18	C8	C8	B17	E20 (PERn3)	S26 (TX3-)		
GND	A18	A9	A9	A19	A19	A19	A19	GROUND	GROUND	B19	B19	B19	B19	C9	C9	B18				
RSV					A20(RSVD)	A20(RSVD)	A20(RESERVED)	RESERVED	NC	RESERVED	B20(RESERVED)	B20(RSVD)									
RSV					A21(RSVD)	A21(RSVD)	A21(RESERVED)	RESERVED	NC	RESERVED	B21(RESERVED)	B21(RSVD)									
GND	A1	B3	B3		A22	A22	A22	GROUND	GROUND	B22	B22			D3	D3	B1				
HS	A2	B4	B4	A20	A20	A23	A23	PER(RX)p4	←	PET(TX)p4	B23	B23	B20	B20	D4	D4	B2	E14 (PERp0)	S6 (TX0+)		
HS	A3	B5	B5	A21	A21	A24	A24	PER(RX)n4	←	PET(TX)n4	B24	B24	B21	B21	D5	D5	B3	E13 (PERn0)	S5 (TX0-)		
GND	A4	A3	A3	A22	A22	A25	A25	GROUND	GROUND	B25	B25	B22	B22	C3	C3	B4				
HS	A5	A4	A4	A23	A23	A26	A26	PER(RX)p5	←	PET(TX)p5	B26	B26	B23	B23	C4	C4	B5	S21 (PERp1)	S13 (TX1+)		
HS	A6	A5	A5	A24	A24	A27	A27	PER(RX)n5	←	PET(TX)n5	B27	B27	B24	B24	C5	C5	B6	S20 (PERn1)	S12 (TX1-)		
GND	A7	A6	A6	A25	A25	A28	A28	GROUND	GROUND	B28	B28	B25	B25	C6	C6	B7				
SB	A8(SB7)	A1(SB7)	A1(VSP7)	A26(SB7B)	A26(VSP7B)	A29(SB7B)	A29(BP_TYPEB)	BP_TYPEB(VSP7B) / BP_TYPEB(SB7B)	←	(SB7B)BP_TYPEB / (VSP7B)BP_TYPEB	B29(BP_TYPEB)	B29(SB7B)	B26(VSP7B)	B26(SB7B)	A2(VSP7)	A2(SB7)	B8(SB7)				
SB	A9(SB3)	B1(SB3)	B1(VSP3)	A27(SB3B)	A27(VSP3B)	A30(SB3B)	A30(CWAKEB#/OBFFB)	CWAKEB#,OBFFB(VSP3B) / GND(SB3B)	↔	(SB3B)GND / (VSP3B)WAKEB#,OBFFB	B30(CWAKEB#/OBFFB)	B30(SB3B)	B27(VSP3B)	B27(SB3B)	B2(VSP3)	B2(SB3)	B9(SB3)	P1 (WAKE#)			
SB				A28(SB9B)	A28(VSP9B)	A31(SB9B)	A31(GND)	GND(VSP9B) / GND(SB9B)	(SB9B)GND / (VSP9B)GND	B31(GND)	B31(SB9B)	B28(VSP9B)	B28(SB9B)							
SB	A10(SB4)	C1(SB4)	C1(VSP4)	A29(SB4B)	A29(VSP4B)	A32(SB4B)	A32(VSPB)REFCLKB+	REFCLK+(VSP4B) / RESETB, SDataOutB(SB4B)	→	(SB4B)DataOutB,RESETB / (VSP4B)REFCLKB+	B32(VSPB)REFCLKB+	B32(SB4B)	B29(VSP4B)	B29(SB4B)	C2(VSP4)	C2(SB4)	B10(SB4)	E7 (REFCLK+)			
SB	A11(SB5)	D1(SB5)	D1(VSP5)	A30(SB5B)	A30(VSP5B)	A33(SB5B)	A33(VSPB)REFCLKB-	REFCLK-(VSP5B) / ADD8, SDataInB(SB5B)	↔	(SB5B)DataInB,ADD8 / (VSP5B)REFCLKB-	B33(VSPB)REFCLKB-	B33(SB5B)	B30(VSP5B)	B30(SB5B)	D2(VSP5)	D2(SB5)	B11(SB5)	E8 (REFCLK-)			
GND	A12	B6	B6	A31	A31	A34	A34	GROUND	GROUND	B34	B34	B31	B31	D6	D6	B12				
HS	A13	B7	B7	A32	A32	A35	A35	PER(RX)p6	←	PETp6	B35	B35	B32	B32	D7	D7	B13	S27 (PERp2)	S21 (TX2+)		
HS	A14	B8	B8	A33	A33	A36	A36	PER(RX)n6	←	PETn6	B36	B36	B33	B33	D8	D8	B14	S26 (PERn2)	S20 (TX2-)		
GND	A15	B9	B9	A34	A34	A37	A37	GROUND	GROUND	B37	B37	B34	B34	D9	D9	B15				
HS	A16	A7	A7	A35	A35	A38	A38	PER(RX)p7	←	PET(TX)p7	B38	B38	B35	B35	C7	C7	B16	E21 (PERp3)	S27 (TX3+)		
HS	A17	A8	A8	A36	A36	A39	A39	PER(RX)n7	←	PET(TX)n7	B39	B39	B36	B36	C8	C8	B17	E20 (PERn3)	S26 (TX3-)		
GND	A18	A9	A9	A37	A37	A40	A40	GROUND	GROUND	B40	B40	B37	B37	C9	C9	B18				

TABLE 4-5 PINOUT FOR AN 8X INTERFACE WITH SIDEBANDS (2 OF 2)

Controller / Initiator / Root (Downstream)									Backplane/ Endpoint (Upstream)									DEVICE	DEVICE
9400 Rev 0.2	8087	8643	mini-SAS HD	8654	SlimLine SAS	8612	OCuLink	9401 Universal Multi-Protocol Single Cable for SAS/PCIe	CABLE	9401 Universal Multi-Protocol Single Cable for SAS/PCIe	OCuLink	8612	SlimLine SAS	8654	mini-SAS HD	8643	8087	SFF-8639	MultiLink
Type 1 8X	SAS-2.1 x4	SAS-2.1, 3 x4	PCIe x4	SAS-4 x8	PCIe x8	SAS-4 x8	PCIe x8	8X Single Cable OCuLink 1.0 / SFF-8448	ROOT / Controller	8X Single Cable SFF-8448/OCuLink 1.0	PCIe x8	SAS-4 x8	PCIe x8	SAS-4 x8	PCIe x4	SAS-2.1, 3 x4	SAS-2.1 x4	PCIe	SAS
	PIN	PIN	PIN	PIN	PIN	PIN	PIN		DIR	Backplane/ END Point	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN
GND	B1	D3	D3	B1	B1	B1	B1	GROUND	GROUND	A1	A1	A1	A1	B3	B3	A1		
HS	B2	D4	D4	B2	B2	B2	B2	PET(TX)p0	→	PER(RX)p0	A2	A2	A2	A2	B4	B4	A2	E10 (PETp0)	S2 (RX0+)
HS	B3	D5	D5	B3	B3	B3	B3	PET(TX)n0	→	PER(RX)n0	A3	A3	A3	A3	B5	B5	A3	E11 (PETn0)	S3 (RX0-)
GND	B4	C3	C3	B4	B4	B4	B4	GROUND	GROUND	A4	A4	A4	A4	A3	A3	A4		
HS	B5	C4	C4	B5	B5	B5	B5	PET(TX)p1	→	PER(RX)p1	A5	A5	A5	A5	A4	A4	A5	S17 (PETp1)	S9 (RX1+)
HS	B6	C5	C5	B6	B6	B6	B6	PET(TX)n1	→	PER(RX)n1	A6	A6	A6	A6	A5	A5	A6	S18 (PETn1)	S10 (RX1-)
GND	B7	C6	C6	B7	B7	B7	B7	GROUND	GROUND	A7	A7	A7	A7	A6	A6	A7		
SB	B8(SB0)	A2(SB0)	A2(VSP0)	B8(SB0A)	B8(VSPOA)	B8(SB0A)	B8(2W-CLKA)	2W-CLKA(VSPOA) / 2W-CLKA(SB0A)	↔	(SB0A)2W-CLKA(VSPOA)2W-CLKA	A8(2W-CLKA)	A8(SB0A)	A8(VSPOA)	A8(SB0A)	A1(VSP0)	A1(SB0)	A8(SB0)		
SB	B9(SB1)	B2(SB1)	B2(VSP1)	B9(SB1A)	B9(VSP1A)	B9(SB1A)	B9(2W-DATAA)	2W-DATAA(VSP1A) / 2W-DATAA(SB1A)	↔	(SB1A)2W-DATAA(VSP1A)2W-DATAA	A9(2W-DATAA)	A9(SB1A)	A9(VSP1A)	A9(SB1A)	B1(VSP1)	B1(SB1)	A9(SB1)		
SB				B10(SB8A)	B10(VSP8A)	B10(SB8A)	B10(GND)	GND(VSP8A) / GND(SB8A)	↔	(SB8A)GND(VSP8A)GND	A10(GND)	A10(SB8A)	A10(VSP8A)	A10(SB8A)					
SB	B10(SB2)	C2(SB2)	C2(VSP2)	B11(SB2A)	B11(VSP2A)	B11(SB2A)	B11(PERSTA#)	PERSTA#(VSP2A) / GND(SB2A)	→	(SB2A)GND(VSP2A)PERSTA#	A11(PERSTA#)	A11(SB2A)	A11(VSP2A)	A11(SB2A)	C1(VSP2)	C1(SB2)	A10(SB2)	E5 (PERST#)	
SB	B11(SB6)	D2(SB6)	D2(VSP6)	B12(SB6A)	B12(VSP6A)	B12(SB6A)	B12(CPRSNTA#)	CPRSNTA#(VSP6A) / CNTRLR_TYPEA(SB6A)	↔	(SB6A)CNTRLR_TYPEA(VSP6A)CPRSNTA#	A12(CPRSNTA#)	A12(SB6A)	A12(VSP6A)	A12(SB6A)	D1(VSP6)	D1(SB6)	A11(SB6)		
GND	B12	D6	D6	B13	B13	B13	B13	GROUND	GROUND	A13	A13	A13	A13	B6	B6	A12		
HS	B13	D7	D7	B14	B14	B14	B14	PET(TX)p2	→	PER(RX)p2	A14	A14	A14	A14	B7	B7	A13	S23 (PETp2)	S17 (RX2+)
HS	B14	D8	D8	B15	B15	B15	B15	PET(TX)n2	→	PER(RX)n2	A15	A15	A15	A15	B8	B8	A14	S24 (PETn2)	S18 (RX2-)
GND	B15	D9	D9	B16	B16	B16	B16	GROUND	GROUND	A16	A16	A16	A16	B9	B9	A15		
HS	B16	C7	C7	B17	B17	B17	B17	PET(TX)p3	→	PER(RX)p3	A17	A17	A17	A17	A7	A7	A16	E17 (PETp3)	S23 (RX3+)
HS	B17	C8	C8	B18	B18	B18	B18	PET(TX)n3	→	PER(RX)n3	A18	A18	A18	A18	A8	A8	A17	E18 (PETn3)	S24 (RX3-)
GND	B18	C9	C9	B19	B19	B19	B19	GROUND	GROUND	A19	A19	A19	A19	A9	A9	A18		
RSV					B20(RSV0)	B20(RSV0)	B20(RSV0)	RESERVED	NC	RESERVED	A20(RESERVED)	A20(RSV0)							
RSV					B21(RSV0)	B21(RSV0)	B21(RSV0)	RESERVED	NC	RESERVED	A21(RESERVED)	A21(RSV0)							
GND	B1	D3	D3		B22	B22	B22	GROUND	GROUND	A22	A22			B3	B3	A1		
HS	B2	D4	D4	B20	B20	B23	B23	PET(TX)p4	→	PER(RX)p4	A23	A23	A20	A20	B4	B4	A2	E10 (PETp0)	S2 (RX0+)
HS	B3	D5	D5	B21	B21	B24	B24	PET(TX)n4	→	PER(RX)n4	A24	A24	A21	A21	B5	B5	A3	E11 (PETn0)	S3 (RX0-)
GND	B4	C3	C3	B22	B22	B25	B25	GROUND	GROUND	A25	A25	A22	A22	A3	A3	A4		
HS	B5	C4	C4	B23	B23	B26	B26	PET(TX)p5	→	PER(RX)p5	A26	A26	A23	A23	A4	A4	A5	S17 (PETp1)	S9 (RX1+)
HS	B6	C5	C5	B24	B24	B27	B27	PET(TX)n5	→	PER(RX)n5	A27	A27	A24	A24	A5	A5	A6	S18 (PETn1)	S10 (RX1-)
GND	B7	C6	C6	B25	B25	B28	B28	GROUND	GROUND	A28	A28	A25	A25	A6	A6	A7		
SB	B8(SB0)	A2(SB0)	A2(VSP0)	B26(SB0B)	B26(VSPOB)	B29(SB0B)	B29(2W-CLKB)	2W-CLKB(VSPOB) / 2W-CLKB(SB0B)	↔	(SB0B)2W-CLKB(VSPOB)2W-CLKB	A29(2W-CLKB)	A29(SB0B)	A26(VSPOB)	A26(SB0B)	A1(VSP0)	A1(SB0)	A8(SB0)		
SB	B9(SB1)	B2(SB1)	B2(VSP1)	B27(SB1B)	B27(VSP1B)	B30(SB1B)	B30(2W-DATAB)	2W-DATAB(VSP1B) / 2W-DATAB(SB1B)	↔	(SB1B)2W-DATAB(VSP1B)2W-DATAB	A30(2W-DATAB)	A30(SB1B)	A27(VSP1B)	A27(SB1B)	B1(VSP1)	B1(SB1)	A9(SB1)		
SB				B28(SB8B)	B28(VSP8B)	B31(SB8B)	B31(GND)	GND(VSP8B) / GND(SB8B)	↔	(SB8B)GND(VSP8B)GND	A31(GND)	A31(SB8B)	A28(VSP8B)	A28(SB8B)					
SB	B10(SB2)	C2(SB2)	C2(VSP2)	B29(SB2B)	B29(VSP2B)	B32(SB2B)	B32(PERSTB#)	PERSTB#(VSP2B) / GND(SB2B)	→	(SB2B)GND(VSP2B)PERSTB#	A32(PERSTB#)	A32(SB2B)	A29(VSP2B)	A29(SB2B)	C1(VSP2)	C1(SB2)	A10(SB2)	E5 (PERST#)	
SB	B11(SB6)	D2(SB6)	D2(VSP6)	B30(SB6B)	B30(VSP6B)	B33(SB6B)	B33(CPRSNTB#)	CPRSNTB#(VSP6B) / CNTRLR_TYPEB(SB6B)	↔	(SB6B)CNTRLR_TYPEB(VSP6B)CPRSNTB#	A33(CPRSNTB#)	A33(SB6B)	A30(VSP6B)	A30(SB6B)	D1(VSP6)	D1(SB6)	A11(SB6)		
GND	B12	D6	D6	B31	B31	B34	B34	GROUND	GROUND	A34	A34	A31	A31	B6	B6	A12		
HS	B13	D7	D7	B32	B32	B35	B35	PET(TX)p6	→	PER(RX)p6	A35	A35	A32	A32	B7	B7	A13	S23 (PETp2)	S17 (RX2+)
HS	B14	D8	D8	B33	B33	B36	B36	PET(TX)n6	→	PER(RX)n6	A36	A36	A33	A33	B8	B8	A14	S24 (PETn2)	S18 (RX2-)
GND	B15	D9	D9	B34	B34	B37	B37	GROUND	GROUND	A37	A37	A34	A34	B9	B9	A15		
HS	B16	C7	C7	B35	B35	B38	B38	PET(TX)p7	→	PER(RX)p7	A38	A38	A35	A35	A7	A7	A16	E17 (PETp3)	S23 (RX3+)
HS	B17	C8	C8	B36	B36	B39	B39	PET(TX)n7	→	PER(RX)n7	A39	A39	A36	A36	A8	A8	A17	E18 (PETn3)	S24 (RX3-)
GND	B18	C9	C9	B37	B37	B40	B40	GROUND	GROUND	A40	A40	A37	A37	A9	A9	A18		