SFF-TA-1002

Specification for

Protocol Agnostic Multi-Lane High Speed Connector

Rev 1.5 April 29, 2024

SECRETARIAT: SFF TA TWG

There are multiple use cases based on electrical performance.
- 2.5 GT/s NRZ to 112 GT/s PAM4.
- 2.5 GT/s NRZ to 32 GT/s NRZ for orthogonal connectors only.

This specification provides a common reference for systems manufacturers, system integrators, and suppliers.

This specification is made available for public review at https://www.snia.org/sff/specifications. Comments may be submitted at https://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

The description of a connector in this specification does not assure that the specific component is actually available from connector suppliers. If such a connector is supplied it must comply with this specification to achieve interoperability between suppliers.

ABSTRACT: This specification defines an unshielded, Input/Output, card edge connector and mating card interface capable of operation up to 112GT/s PAM4. The connector has 56, 84, or 140 contacts based on bandwidth needs and is configurable for straight, right angle, straddle mount, and orthogonal applications.

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Intellectual Property
The user's attention is called to the possibility that implementation to this Specification may require use of an invention covered by patent rights. By distribution of this specification, no position is taken with respect to the validity of a claim or claims or of any patent rights in connection therewith.. This specification is considered SNIA Architecture and is covered by the SNIA IP Policy and as a result goes through a request for disclosure when it is published. Additional information can be found at the following locations:

- Results of IP Disclosures: https://www.snia.org/sffdisclosures
- SNIA IP Policy: https://www.snia.org/ippolicy

Suggestions for revisions should be directed to https://www.snia.org/feedback/.

Foreword
The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/sff/join.

Revision History

Rev 1.0 (December 2017)
- Initial release

Rev 1.0a (June 14, 2018)
- Corrected header error

Rev 1.0b (June 19, 2018)
- Corrected date error on title page
- Updated Intellectual Property Statement and Foreword to match new template

Rev 1.1 (January 2018)
- Intermediate draft revision

Rev 1.2 (April 3, 2019)
- Added the following connector variations
  - Straight 4C+ variation
  - Right angle height variation of 4.05mm and 4C+ variations
  - Straddle mount connector variations for 1C, 2C, 4C, 4C+ variations and respective SI requirements
  - Press fit and SMT orthogonal 1C & 2C variations
- Added clarification on differential pair counts in Section 3
- Clarified impedance requirements in Section 5.3
- Added Section 5.5 for manufacturability common requirements
- Relaxed insertion and un-mating force requirements.
- Added Section 6 to define pin geometry placement requirements
- Corrected minor drawing errors and editorials

Rev 1.3 (February 19, 2020)
- Updated Table 5-8 LLCR, Shock, and Vibration test requirements
- Added references to SI test specifications

Rev 1.4 (May 9, 2023)
- Updated to new template.
- Updated Figures 5-40 and 5-41 pin tolerance and added solder mask note
- Added 32GT/s NRZ signal integrity requirements to Table 6-5
- Updated Table A-1
- Editorial update to caption for Figure 4-1
- Added Appendix E
- Added additional Host PCB thickness and offset to Table 5-2.
- Clarified Mechanical shock requirement in Table 6-9.
- Additional editorial fixes

Rev 1.5 (April 29, 2024)
- Modified Test Reliability sequence in Table 6-8
- Added new Table 6-6 to signal integrity requirements for straight, right-angle, and straddle mount PCIe applications up to 64GT/s PAM4. Added iRL and ccICN values. Other tables renumbered.
- Added additional Host PCB thickness (2.55mm) and offset to Table 5-2.
- Changed Host PCB thickness tolerance for 3.05mm in Table 5-2.
- Replaced vertical with straight for document consistency.
- Defined Type 1 (original) and Type 2 (ground tied) connectors with changes in Section 4 and 7.

CONTENTS

FIGURES

TABLES

EQUATIONS

1. Scope

This specification defines the mechanical and connector performance requirements for a card edge connector system. This connector system is designed to support high speed signals, power, and side bands on different contacts within the same housing.

1.1 Application Specific Criteria

This connector is capable of supporting a range of protocols. This specification does not list specific supported protocols, but instead details the supported signaling rates and the signal integrity requirements met by the connector. The connector supports signaling rates from 2.5 GT/s NRZ to 112 GT/s PAM4. This includes but is not limited to 16, 28, 32, and 56 GT/s NRZ, and 56 and 112 GT/s PAM4. Only the orthogonal version of the connector is limited to signaling rates from 2.5 GT/s NRZ to 32 GT/s NRZ.

2. References

2.1 Industry Documents

– ASME Y14.5-2009	Dimensioning and Tolerancing
– EIA-364-1000	Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Controlled Environment
– EIA-364-05	Contact Insertion, Release and Removal Force Test Procedure for Electrical Connectors
– EIA-364-13	Mating and Un-mating Force Test Procedure for Electrical Connectors and Sockets
– EIA 364-23	Low Level Contact Resistance Test Procedures for Electrical Connectors and Sockets
– EIA-364-27	Shock Test Procedure for Electrical Connectors
– EIA-364-28	Vibration Test Procedure for Electrical Connectors and Sockets
– EIA-364-29	Contact Retention Test Procedure for Electrical Connectors
– EIA-364-31	Humidity Test Procedure for Electrical Connectors and Sockets
– EIA-364-32	Thermal Shock Test Procedure for Electrical Connectors and Sockets
– EIA 364-70	Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets
– JEDEC J-STD-002D	Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
– JEDEC J-STD-001	Requirements for Soldered Electrical and Electronic Assemblies
– JEDEC JS709A	Defining “Low-Halogen” Electronic Products
– JEDEC PS-002A	DDR4 288 Pin U/R/LR DIMM Connector Performance Standard
– IEEE 802.3	Standard for Ethernet (Clause 92.11.3.2)
– IPC-7711/7721	Rework, Repair and Modification of Electronic Assemblies
– OIF-CIE-3.1	OIF Common Electrical I/O (CEI): Electrical and Jitter Interoperability Agreements for 6G+ bps, 11G+ bps and 25G+ bps I/O
– SFF-TA-1017	Test Board Specification for SFF-TA-1002 Straight Connectors
– SFF-TA-1018	Test Board Specification for SFF-TA-1002 Right Angle Connectors
– SFF-TA-1019	Test Board Specification for SFF-TA-1002 Straddle Mount Connectors
– SFF-TA-1020	Cables and Connector Variants Based on SFF-TA-1002
– REF-TA-1012	Pin Assignment Reference for SFF-TA-1002 Connectors

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifciations. Suggestions for improvement of this specification are welcome and should be submitted to .

Copies of ASME documents may be obtained at https://www.asme.org.

Copies of EIA specifications may be obtained from the Electronic Components

Industry Association (ECIA) manages Electronic Industries Alliance (EIA) standards (https://www.ecianow.org).

Copies of IEEE documents may be obtained from the Institute of Electrical and Electronics Engineers (IEEE) (https://standards.ieee.org).

The International Committee for Information Technology Standards managed ANSI standards-see https://www.techstreet.com/incitsgate.html.

Copies of OIF-CEI specifications may be obtained from the Optical Internetworking Forum (OIF) (https://www.oiforum.com).

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

DIMENSIONING CONVENTIONS: The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May or may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Defines the signal on a connector contact when its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies the restricted designation, then the restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word, or field (e.g., a restricted byte uses the same value as defined for a reserved byte).

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

NRZ: Non-Return-to-Zero
PAM4: Pulse Amplitude Modulation 4-level

3.3 Definitions

For the purpose of SFF Specifications, the following definitions apply:

Advanced grounding contacts: Connector contacts that make first and break last and are capable of carrying power ground return currents and performing electrostatic discharge. Other terms sometimes used to describe these features are: grounding pins, ESD contacts, grounding contacts, static drain, and pre-grounding contacts.

Add in card (AIC): The free half of the connector mating interface defined by this specification. The AIC typically includes more functionality than the physical mechanical interface.

Asymmetric (transmission): Bi-directional interface where the maximum rate of transfer for each direction may be independently specified.

Alignment guides: Connector features that preposition insulators prior to electrical contact. Other terms sometimes used to describe these features are: guide pins, guide posts, blind mating features, mating features, alignment features, and mating guides

Board Termination Technologies: Surface mount single row, surface mount dual row, through hole, hybrid, straddle mount, press fit.

Chiclet: A building block for use in naming convention defined as 8 differential pairs of data signals.

Contact mating sequence: Order of electrical contact during mating/unmating process. Other terms sometimes used to describe this feature are: contact sequencing, contact positioning, make first/break last, EMLB (early make late break) staggered contacts, and long pin / short pin.

Discrete pin connector: Connector where no pins are bussed together.

Fixed: Used to describe the gender of the mating side of the connector that accepts its mate upon mating. This gender is frequently, but not always, associated with the common terminology "receptacle". Other terms commonly used are "female" and "socket connector". The term "fixed" is adopted from EIA standard terminology as the gender that most commonly exists on the fixed end of a connection, for example, on the board or bulkhead side. In this specification "fixed" is specifically used to describe the mating side gender illustrated in Figure 2-1.

Fixed Board: A connector that uses a fixed gender mating side and a termination side suitable for any of the printed circuit board termination technologies.

Free: Used to describe the gender of the mating side of the connector that penetrates its mate upon mating. This gender is frequently, but not always, associated with the common terminology "plug". Other terms commonly used are "male" and "pin connector". The term "free" is adopted from EIA standard terminology as the gender that most commonly exists on the free end of a connection, for example, on the cable side. In this specification "free" is specifically used to describe the mating side gender illustrated in Figure 2-1.

Free Board: A connector that uses a free gender mating side and a termination side suitable for any of the printed circuit board termination technologies

Height: Distance from board surface to farthest overall connector feature

Mating side: The side of the connector that joins and separates from the mating side of a connector of opposite gender. Other terms commonly used in the industry are mating interface, separable interface and mating face.

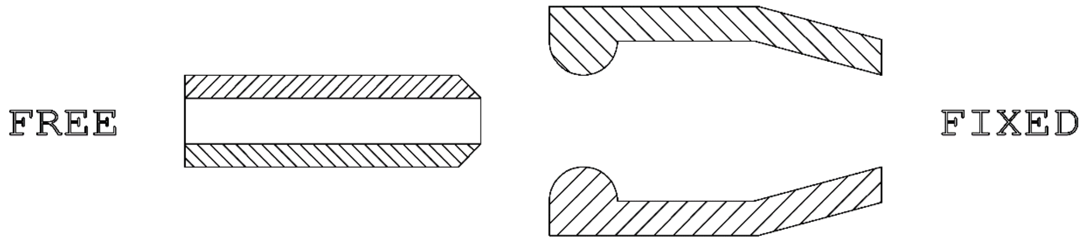


FIGURE 3-1. MATING SIDE GENDER DEFINITION

nC: Connector naming (1C, 2C, 4C) convention that indicates the number of Chiclets. This convention is used because common naming such as “x4, x8” etc. implies symmetrical data transfer in each direction.

Offset: An alignment shift from the center line of the connector

Optional: This term describes features which are not required by the SFF Specification. However, if any feature defined by the SFF Specification is implemented, it shall be done in the same way as defined by the Specification. Describing a feature as optional in the text is done to assist the reader. If there is a conflict between text and tables on a feature described as optional, the table shall be accepted as being correct.

Orthogonal: A connector design for use with printed circuit board assembly technology where the mating direction is parallel to the plane of the printed circuit board while the drive is perpendicular to it.

Reserved: Where this term is used for defining the signal on a connector contact its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields and code values; the bits, bytes, fields and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Right Angle: A connector design for use with printed circuit board assembly technology where the mating direction is parallel to the plane of the printed circuit board

Single row: A connector design for use with surface mount printed circuit board assembly technology where the termination side points are arranged in one line

Straddle mount: A connector design style and a printed circuit board design style that uses surface mount termination points on both sides of the board. The connector is frequently centered between the top and bottom surfaces of the board.

Straight: A connector design for use with printed circuit board assembly technology where the mating direction is perpendicular to the plane of the printed circuit board

Surface mount: A connector design and a printed circuit board design style where the connector termination points do not penetrate the printed circuit board and are subsequently soldered to the printed circuit board

Through hole: A connector design and a printed circuit board design style where the connector termination points penetrates the printed circuit board and are subsequently soldered to the printed circuit board.

Wipe (Contact Location): The contact location has two components: direction of mating and direction of contact pitch. In the direction of mating, the Free contact location shall be a minimum of 0.05 mm from either end of the Fixed contact mating interface after mating and latching.

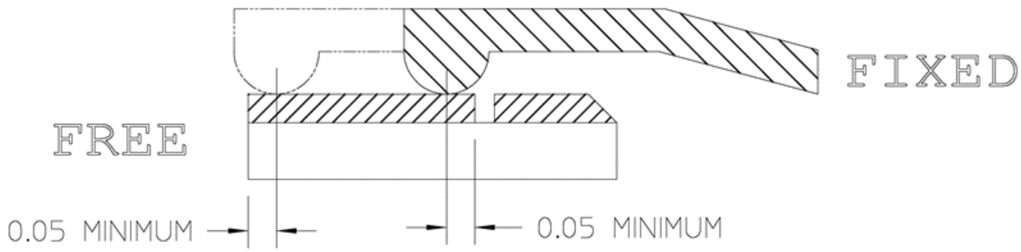


FIGURE 3-2. DIRECTION OF MATING

In the direction of contact pitch, the Free contact shall have no less than 50% of the available mating width in contact with the Fixed contact and there shall be a minimum clearance to the adjacent Fixed contact. The minimum clearance to the adjacent Fixed contact shall be 0.075 mm for interfaces with a pitch of at least 0.70 mm. For pitches less than 0.70 mm, the minimum clearance should be reviewed on a case by case basis to insure that a shorting condition does not exist.

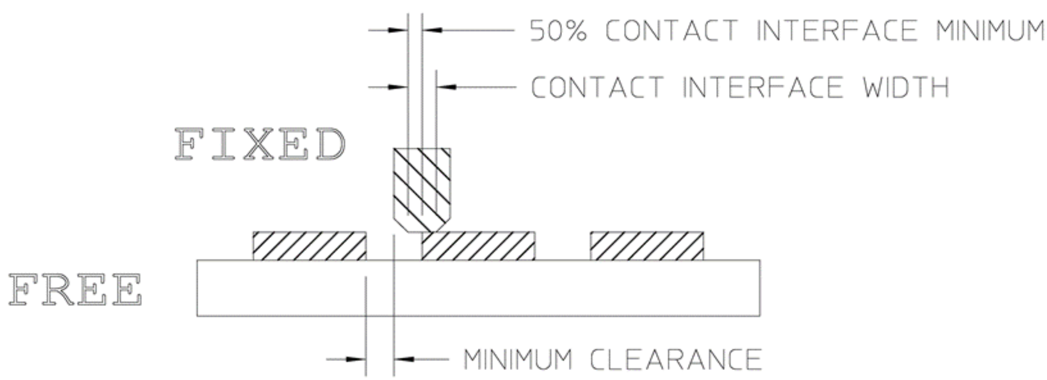


FIGURE 3-3. DIRECTION OF CONTACT

Wipe (Minimum Effective Contact): The distance that the Free contact moves along the Fixed contact without losing electrical connection.

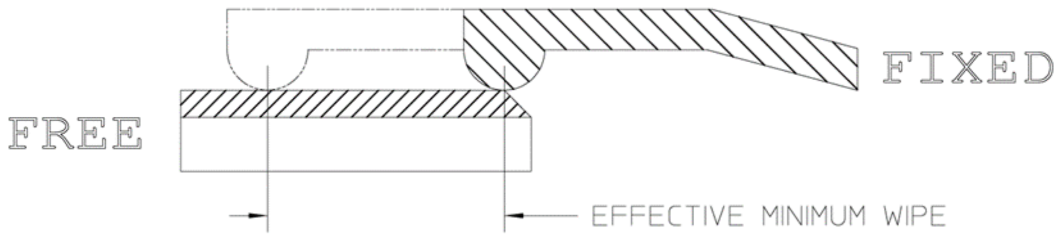


FIGURE 3-4. CONTINUOUS CONTACT

A split or interrupted contact surface (i.e. a contact interface with a pre-pad) is allowable so long as the gap does not allow for the Free contact to make contact with a non-conductive surface.

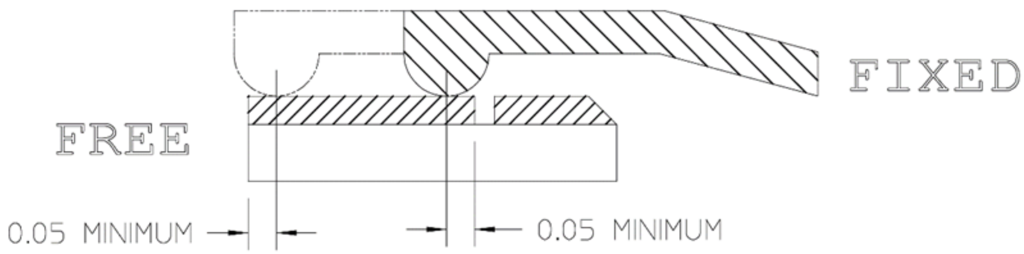


FIGURE 3-5. SPLIT CONTACT

The minimum effective wipe is dependent on the finish of the contact interface. Tin-Tin interfaces shall have a minimum effective wipe of 2.00 mm. Gold-Gold interfaces shall have a minimum effective wipe of 0.40 mm.

4. General Description

This specification defines a card edge connector and add in card interface. Refer to SFF-TA-1020 for cable application details. This connector is deployable in a variety of applications and maintains interoperability between cards of different sizes. The connector supports signaling rates from 2.5 GT/s NRZ to 112 GT/s PAM4. This includes but is not limited to 16, 28, 32, and 56 GT/s NRZ, and 56, 64, and 112 GT/s PAM4. Only the orthogonal version of the connector is limited to signaling rates from 2.5 GT/s NRZ to 32 GT/s NRZ.

This specification describes four different connector orientations, straight, right angle, orthogonal and straddle mount, and four connector sizes as follows.

1. 1C Connector: A connector with 56 contacts with up to 18 differential pairs of data signals in a GSSGSSG configuration.
2. 2C Connector: A connector with 84 contacts with up to 26 differential pairs of data signals in a GSSGSSG configuration.
3. 4C Connector: A connector with 140 contacts with up to 44 differential pairs of data signals in a GSSGSSG configuration as defined in.
4. 4C+ Connector: A connector with 168 contacts with up to 52 differential pairs of data signals in a GSSGSSG.

In addition to differential pairs of data signals, each connector provides a number of contacts to supply power and management signals. To balance connector flexibility with higher signaling rates, the following connector types are defined.

Type 1: The connector uses a discrete pin interface that allows repurposing for other applications and supports asymmetric transmission. The connector supports repurposing of power and management pins for high speed differential pairs in a GSSGSSG configuration and vice versa.

Type 2: The connector uses a mix of defined high speed data signals in a GSSGSSG configuration, power, and management signals. In this connector type, the defined grounds may be joined together within the connector.

Connector type 2 shall be clearly labeled on the connector that it is a Type 2 connector. Connector type 1 may be labeled on the connector. See Section 7 for the pin geometry pattern for each type.

2C, 4C, and 4C+ connectors provide keys to provide fine alignment and prevent 180 degree insertion. 1C connectors use the internal side walls of the connector for fine alignment and are keyed by the form factor and host. Refer to specific application specifications for pin functions and assignments. For a reference list of applications and pin assignments in the industry refer to REF-TA-1012: Pin Assignment Reference for SFF-TA-1002 Connectors.

Figure 4-1 represents a typical mating configuration of this connector. Figure 4-3 show the three connector sizes

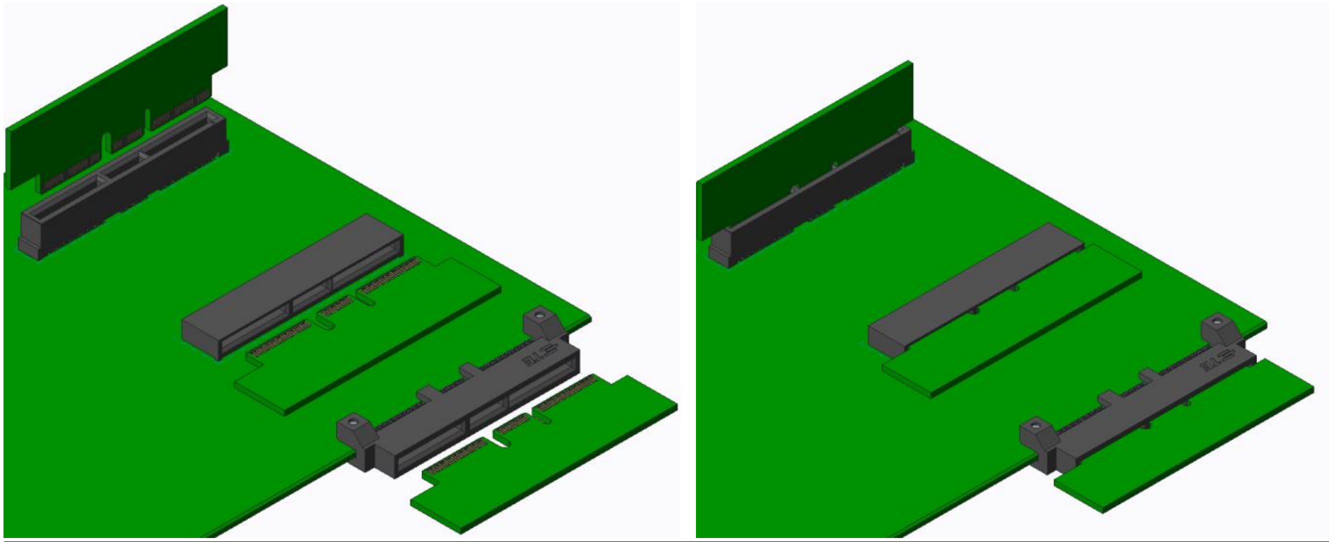


FIGURE 4-1. TYPICAL MATING CONFIGURATION FOR STRAIGHT AND RIGHT ANGLE CONNECTORS

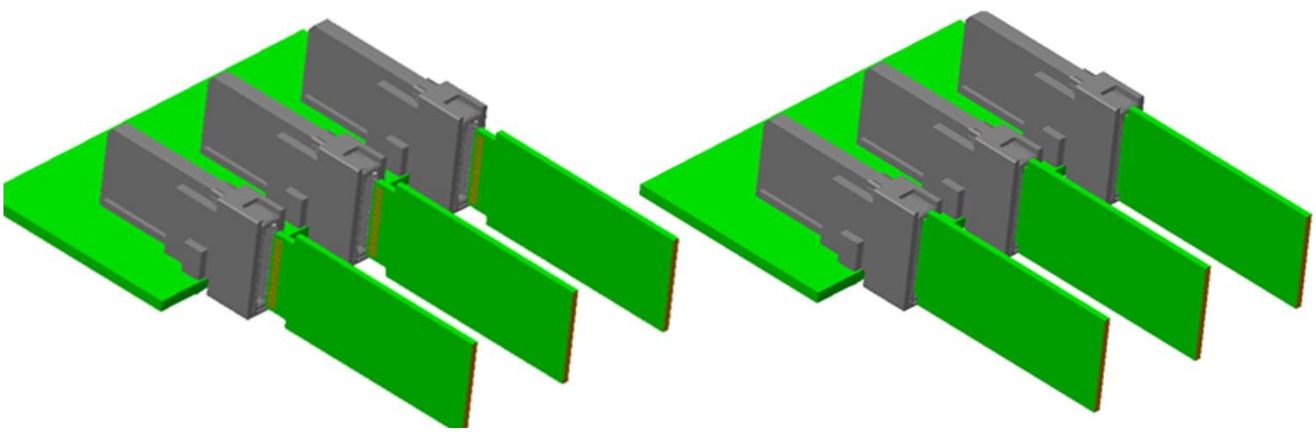


FIGURE 4-2. TYPICAL MATING CONFIGURATION FOR ORTHOGONAL CONNECTORS

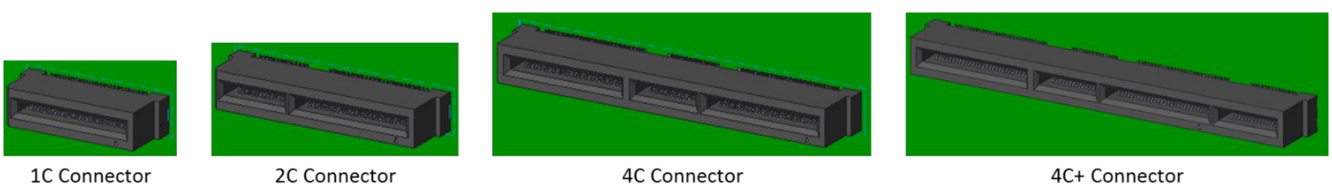


FIGURE 4-3. CONNECTOR SIZES

The connector allows complete upward and downward interoperability as follows and as indicated in Table 4-1 and shown in Figure 4-4 and Figure 4-5:

TABLE 4-1. INTEROPERABILITY MATRIX REQUIREMENTS

	Add-in Cards (AICs)				
Connectors		1C	2C	4C	4C+*
	1C	✓	✓	✓	✓
	2C	✓	✓	✓	✓

	4C	✓	✓	✓	✓
	4C+*	✓	✓	✓	✓

*Note: 1C, 2C, and 4C connectors/AICs must be aligned through the mating form factor and host with the 4C+ connector/AICs to ensure interoperability as shown in Figure 4-4.

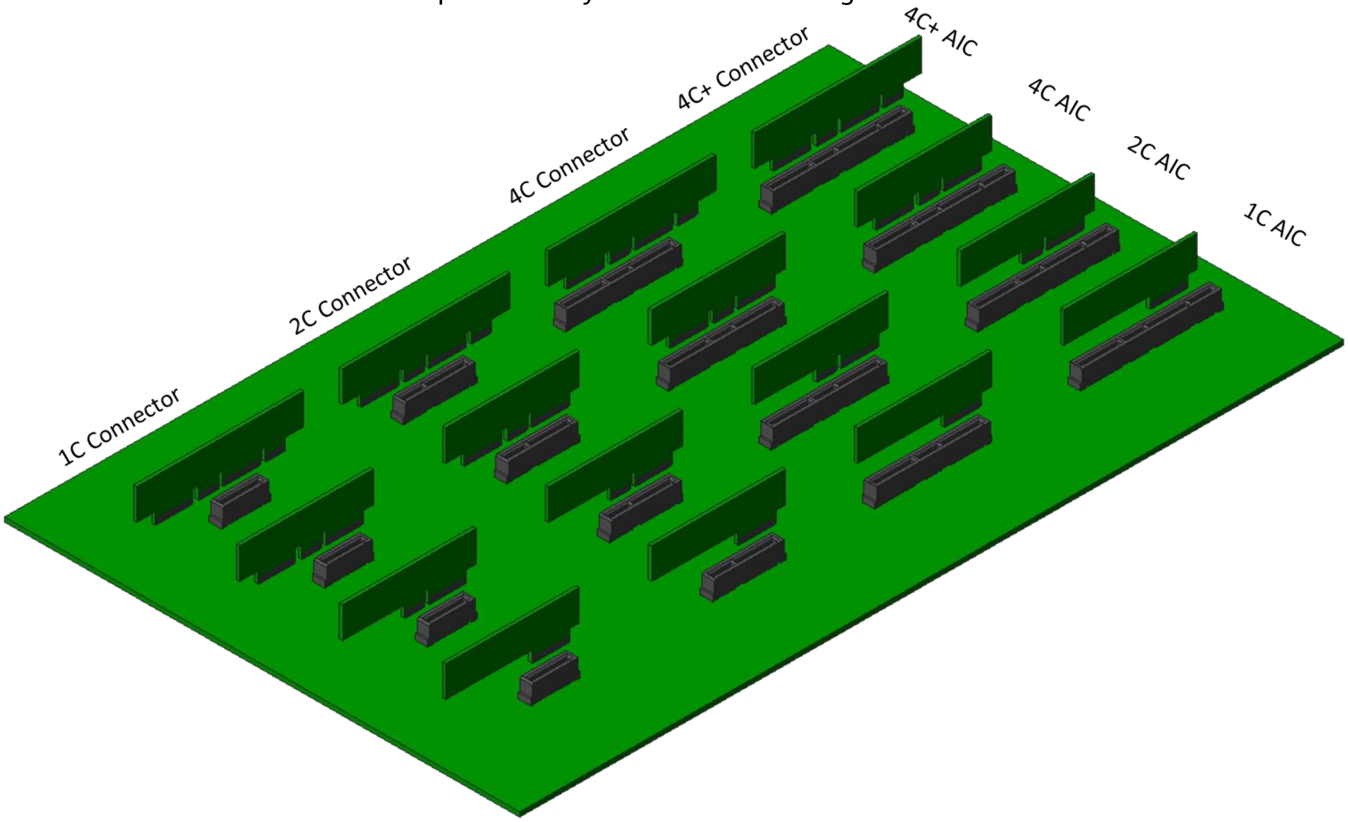


FIGURE 4-4. STRAIGHT CONNECTOR AND AIC INTEROPERABILITY

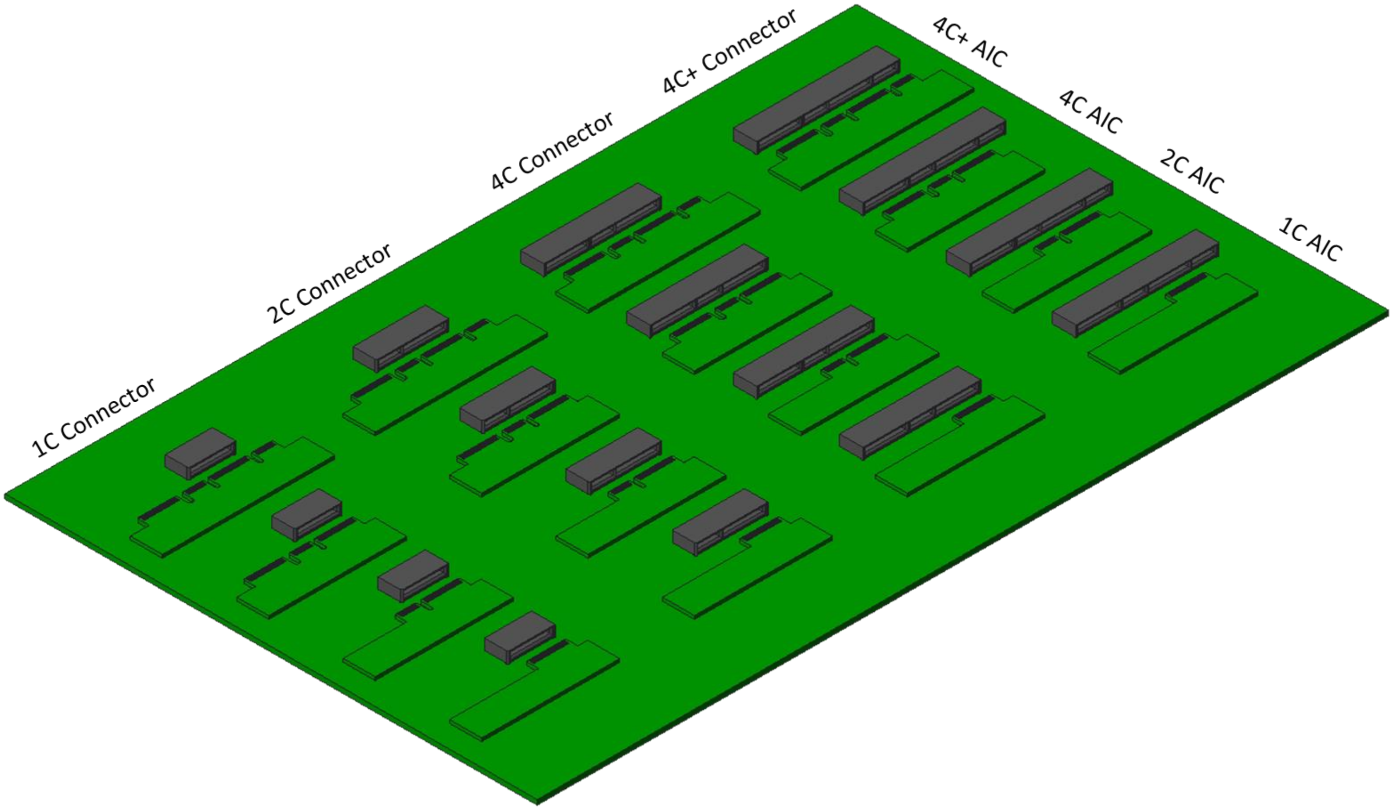


FIGURE 4-5. RIGHT ANGLE CONNECTOR AND CARD INTEROPERABILITY

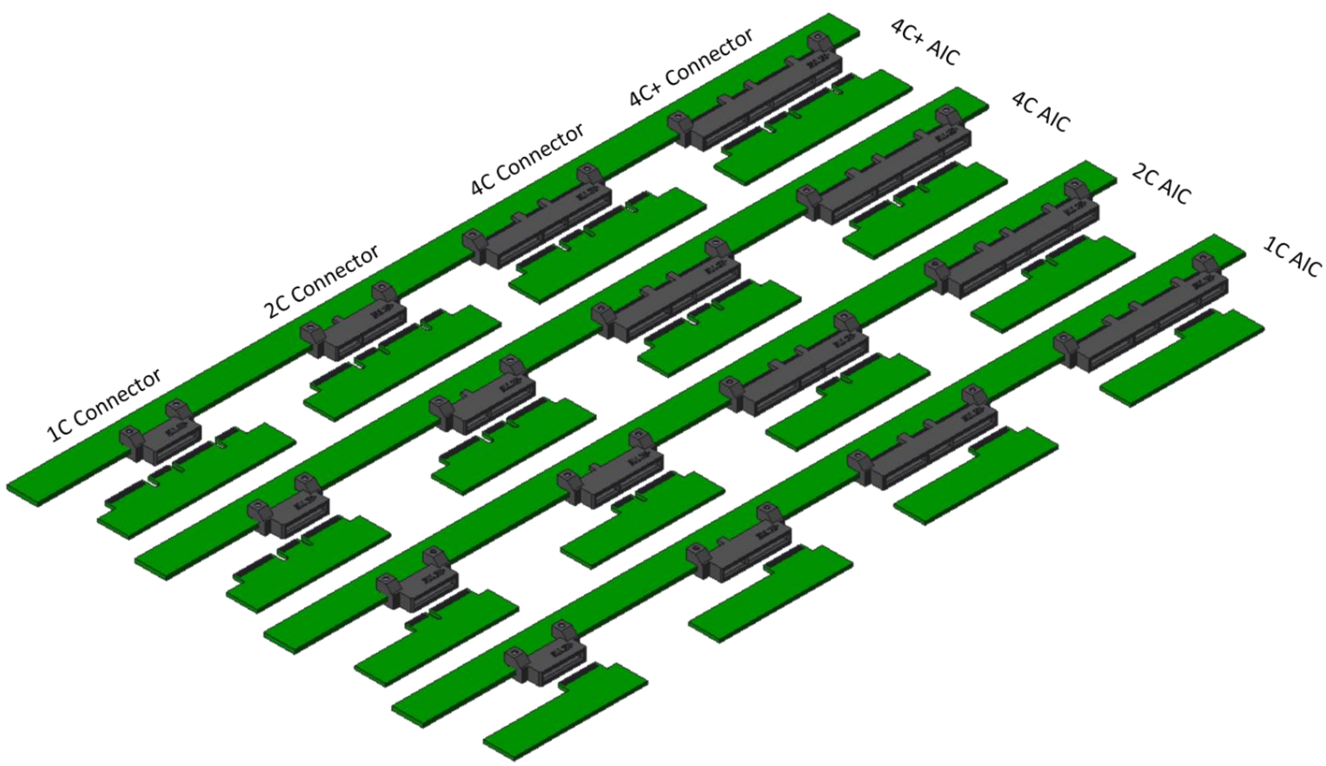


FIGURE 4-6. STRADDLE MOUNT CONNECTOR AND CARD INTEROPERABILITY

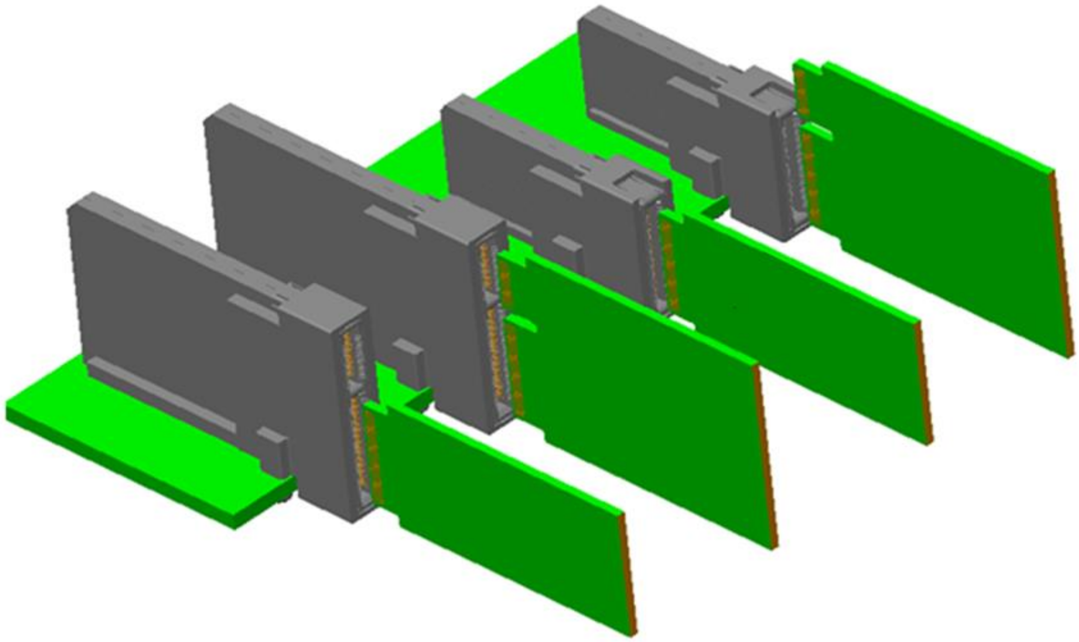


FIGURE 4-7. ORTHOGONAL CONNECTOR AND CARD INTEROPERABILITY

This specification defines the contact range that the retention scheme must provide to assure acceptable connector performance.

5. Connector Interface Dimensions

5.1 General Requirements

All dimensional requirements for the connector and mating card within this specification shall be met in order to provide interoperability between connector and add in card and to fit within the physical boundaries required by the host.

5.2 General Tolerances

Unless otherwise shown, the following tolerances shall apply to the figures:

a. Two-Place dimension = +/- 0.20mm
b. Angular dimension = +/- 3 degrees

5.3 Unshielded Fixed (Receptacle) Connectors

5.3.1 Unshielded Fixed (Receptacle) Straight Connectors

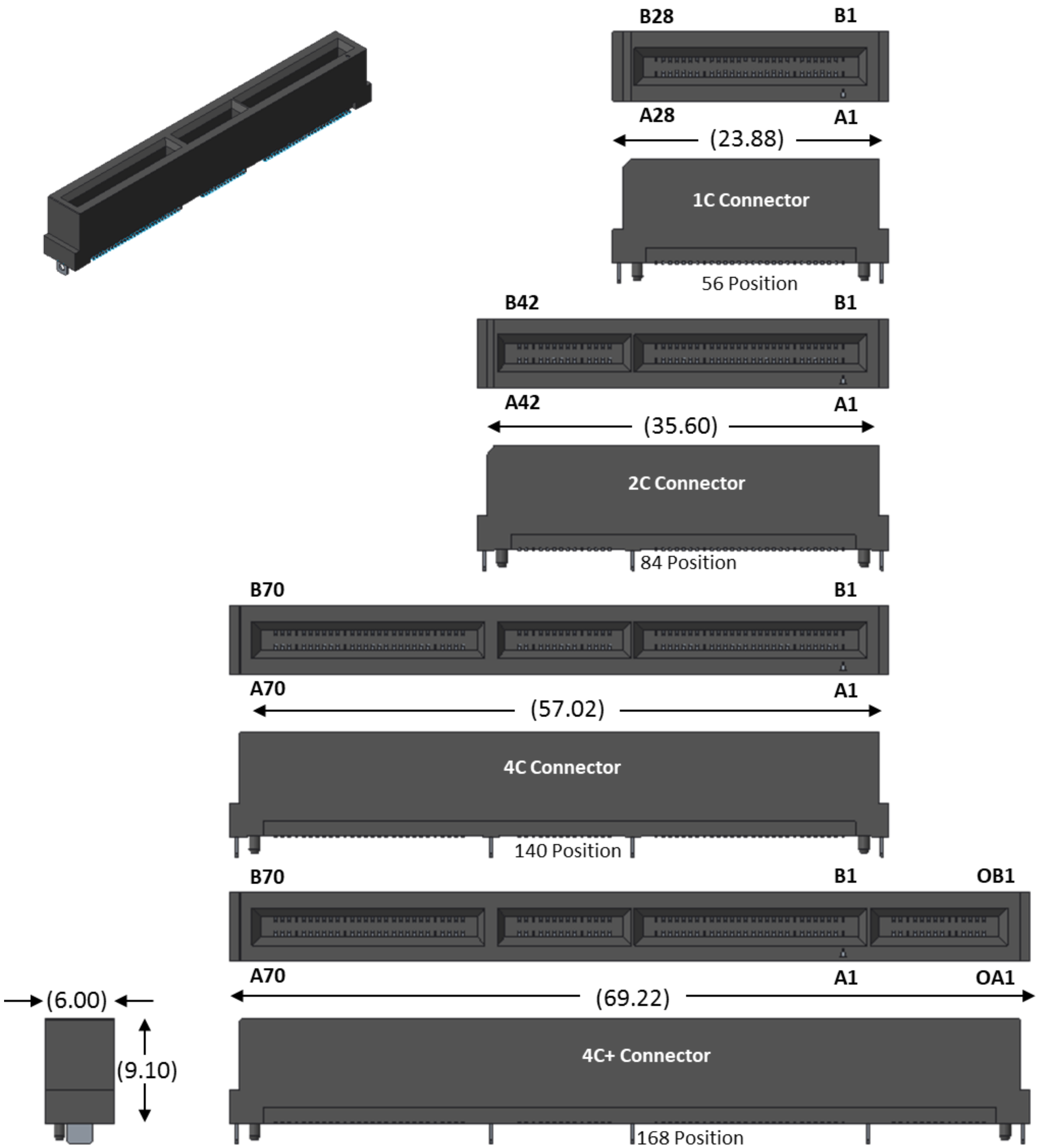


FIGURE 5-1. 1C, 2C, 4C AND 4C+ STRAIGHT CONNECTOR DIMENSIONS OVERVIEW

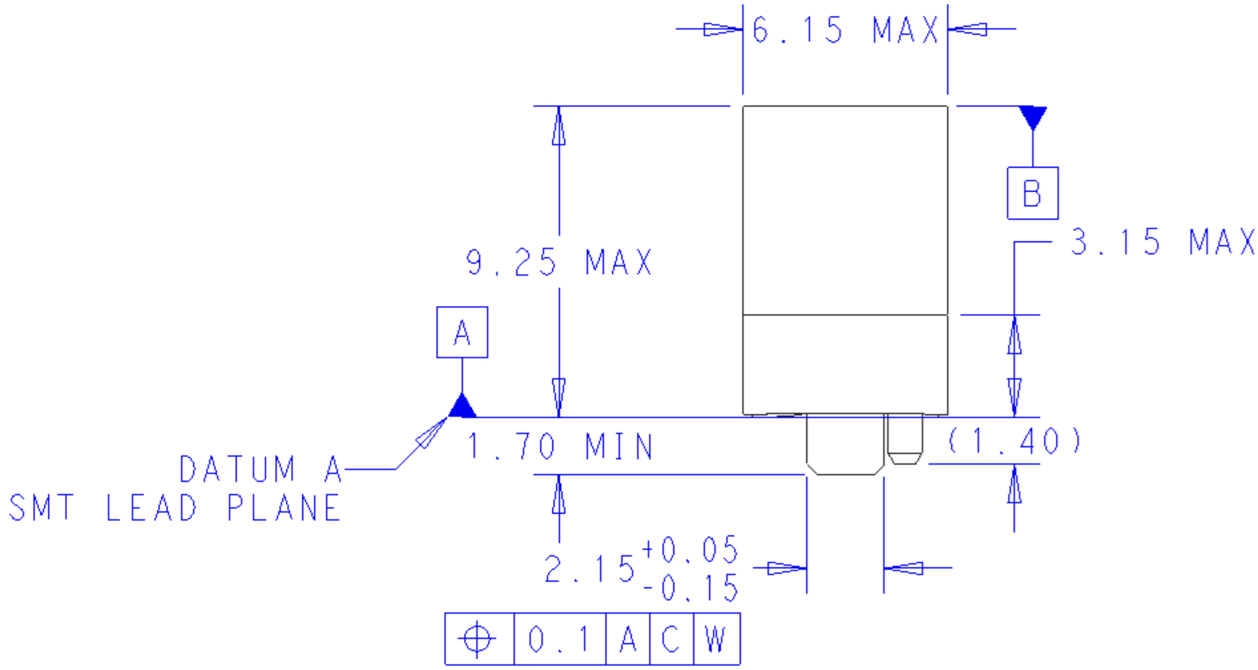


FIGURE 5-2. 1C, 2C, 4C AND 4C+ STRAIGHT CONNECTOR PROFILE DIMENSIONS

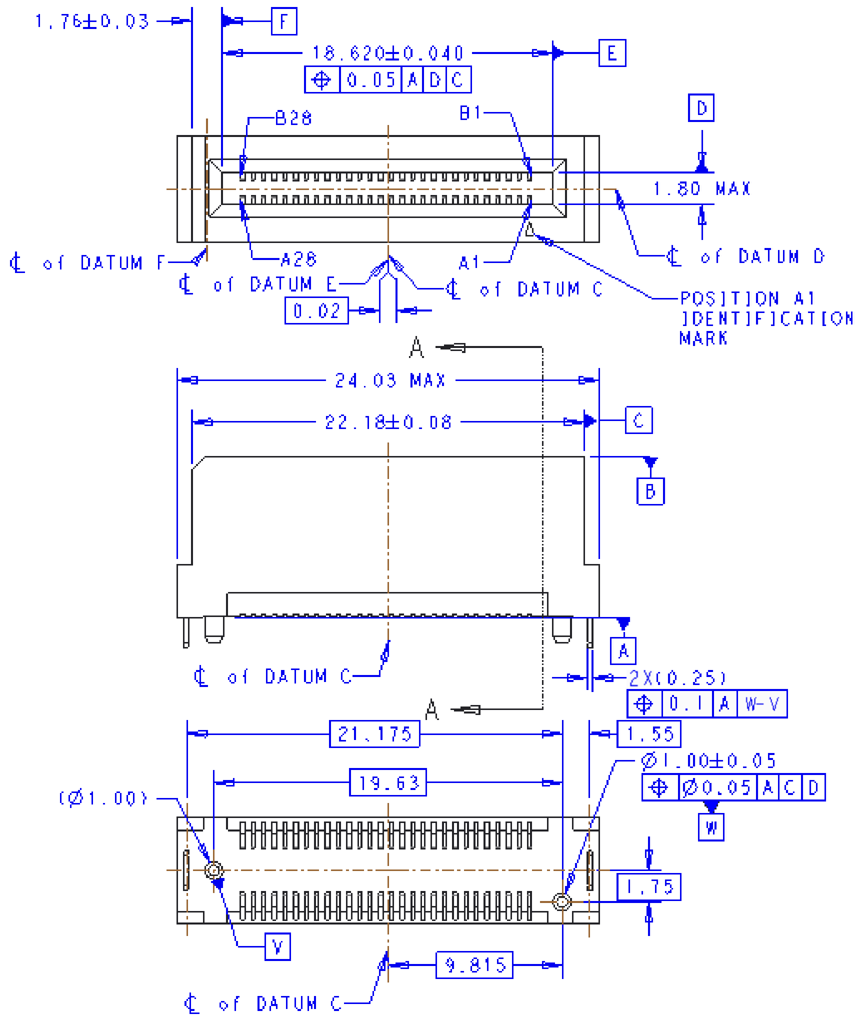


FIGURE 5-3. 1C STRAIGHT CONNECTOR DIMENSIONS

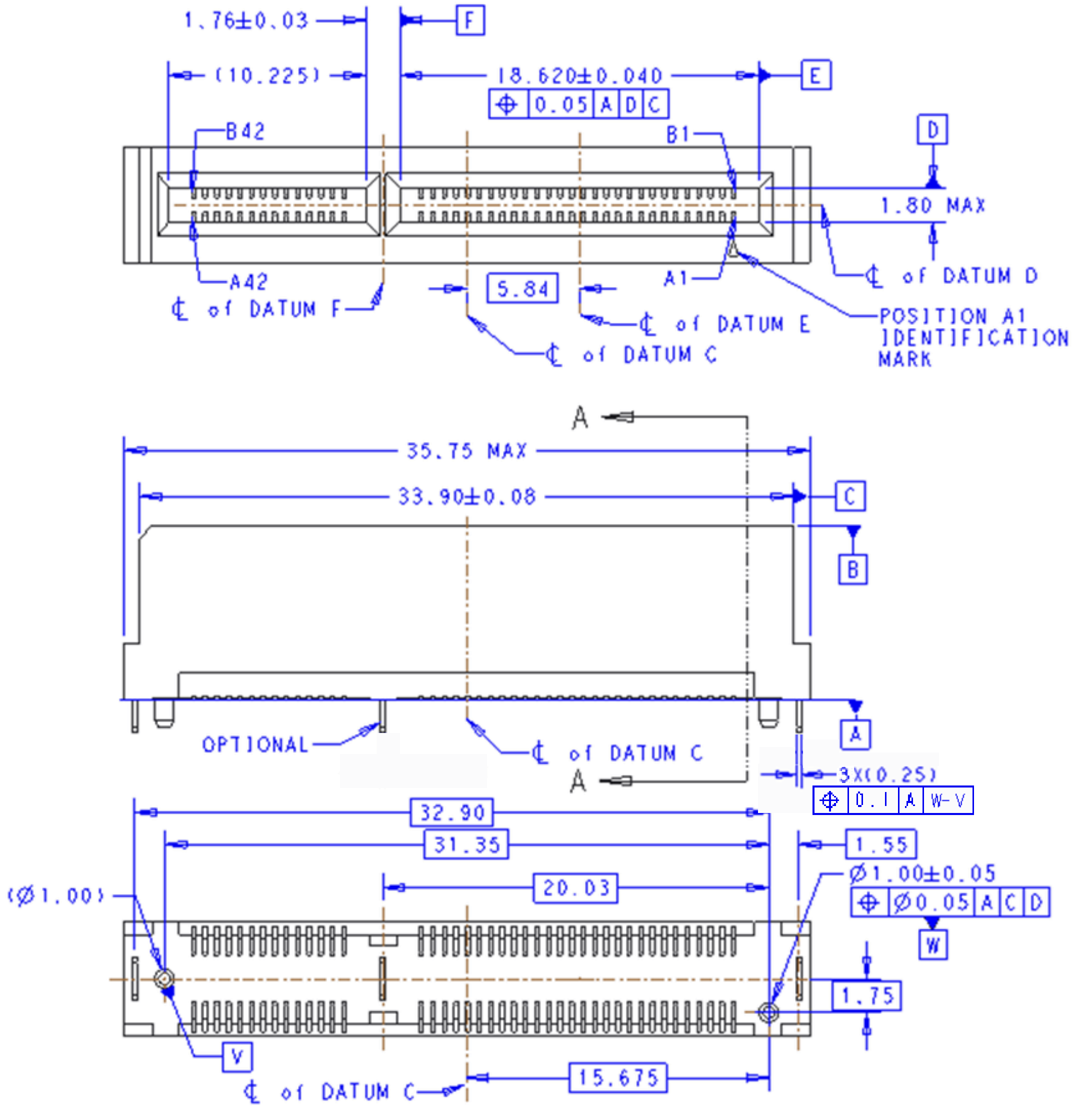


FIGURE 5-4. 2C STRAIGHT CONNECTOR DIMENSIONS

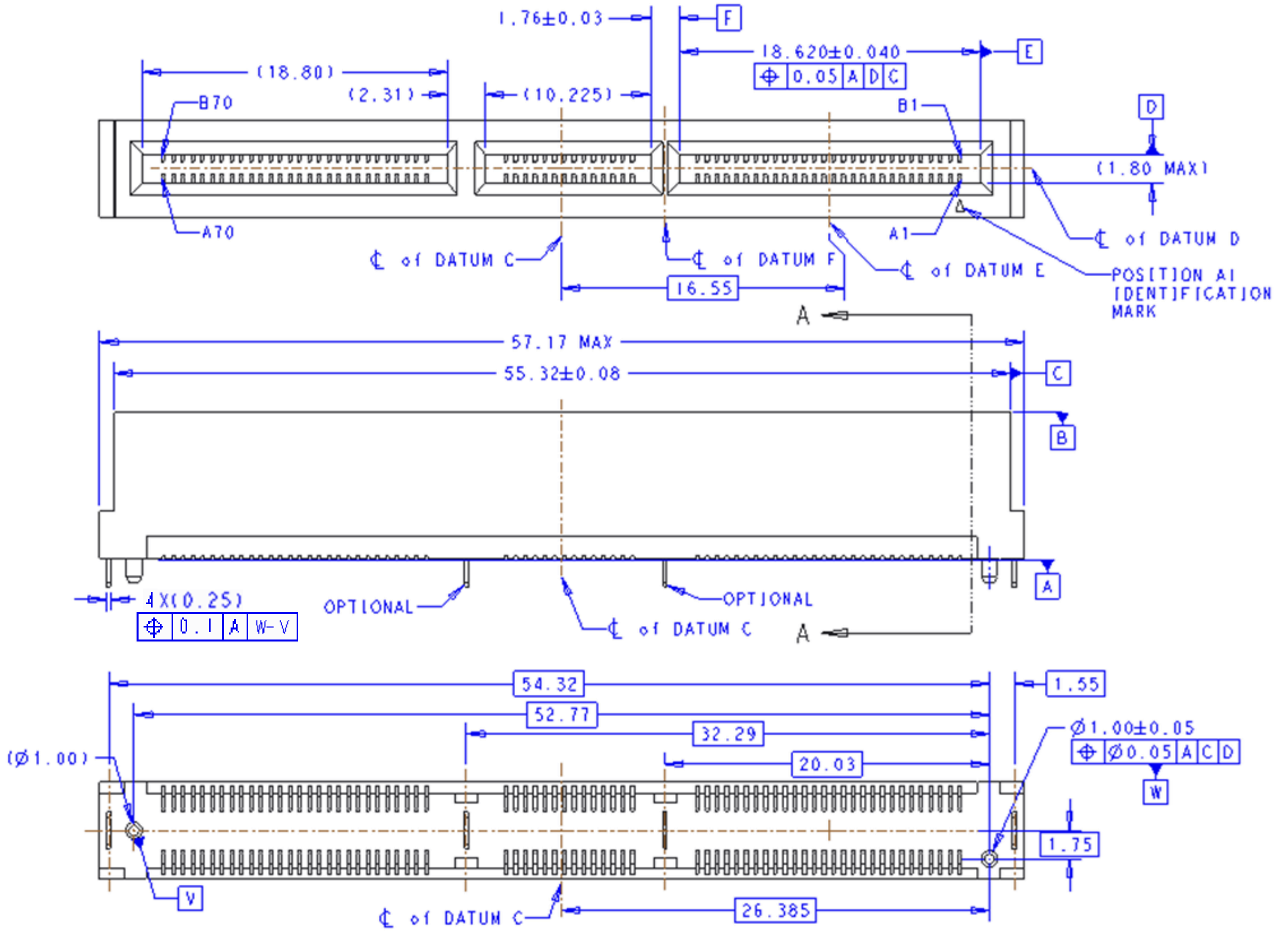


FIGURE 5-5. 4C STRAIGHT CONNECTOR DIMENSIONS

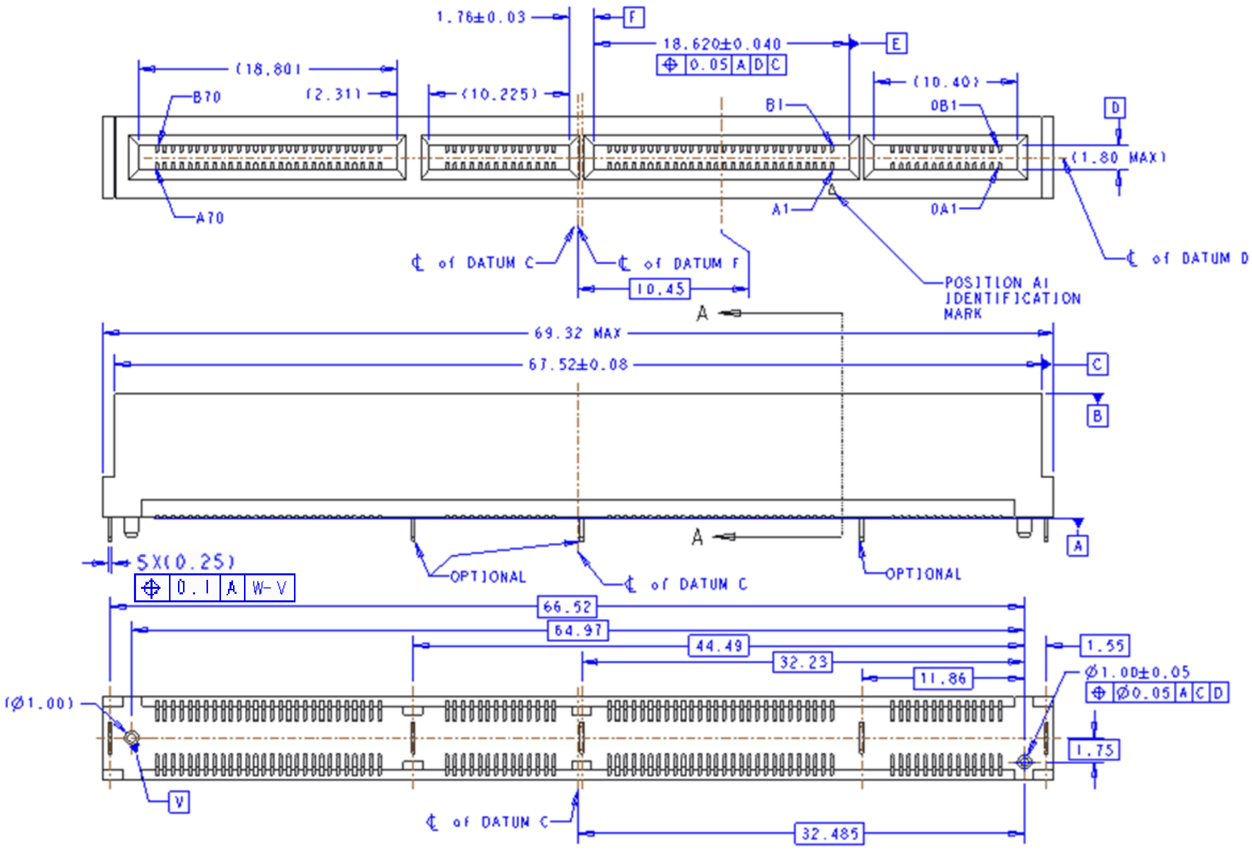


FIGURE 5-6. 4C+ STRAIGHT CONNECTOR DIMENSIONS

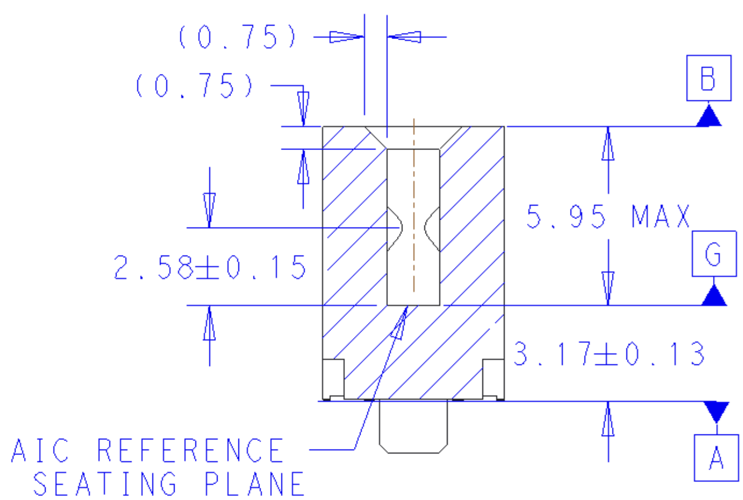


FIGURE 5-7. SECTION A: 1C, 2C, 4C AND 4C+ STRAIGHT CONNECTOR SEATING PLANE

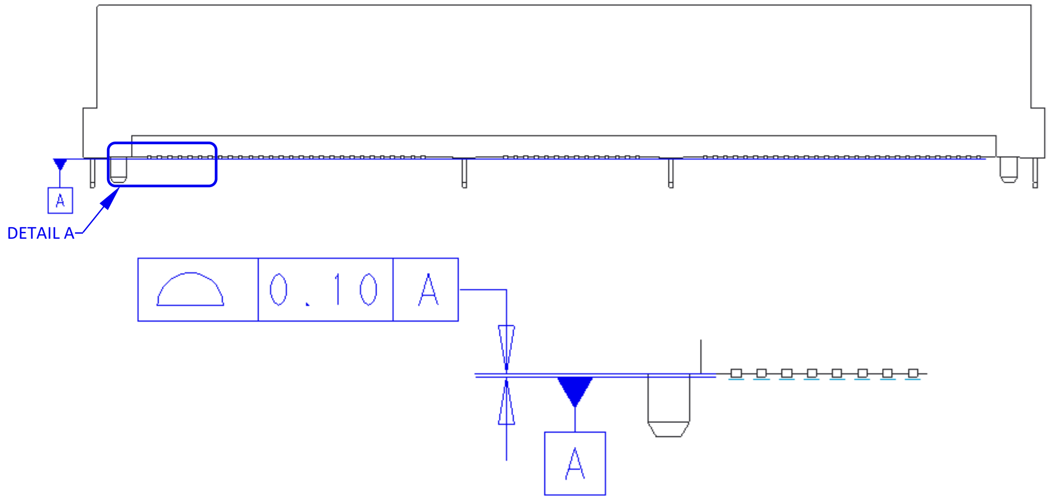


FIGURE 5-8. DETAIL A: STRAIGHT CONNECTOR SMT LEAD CO-PLANARITY

5.3.2 Unshielded Fixed (Receptacle) Right Angle Connectors

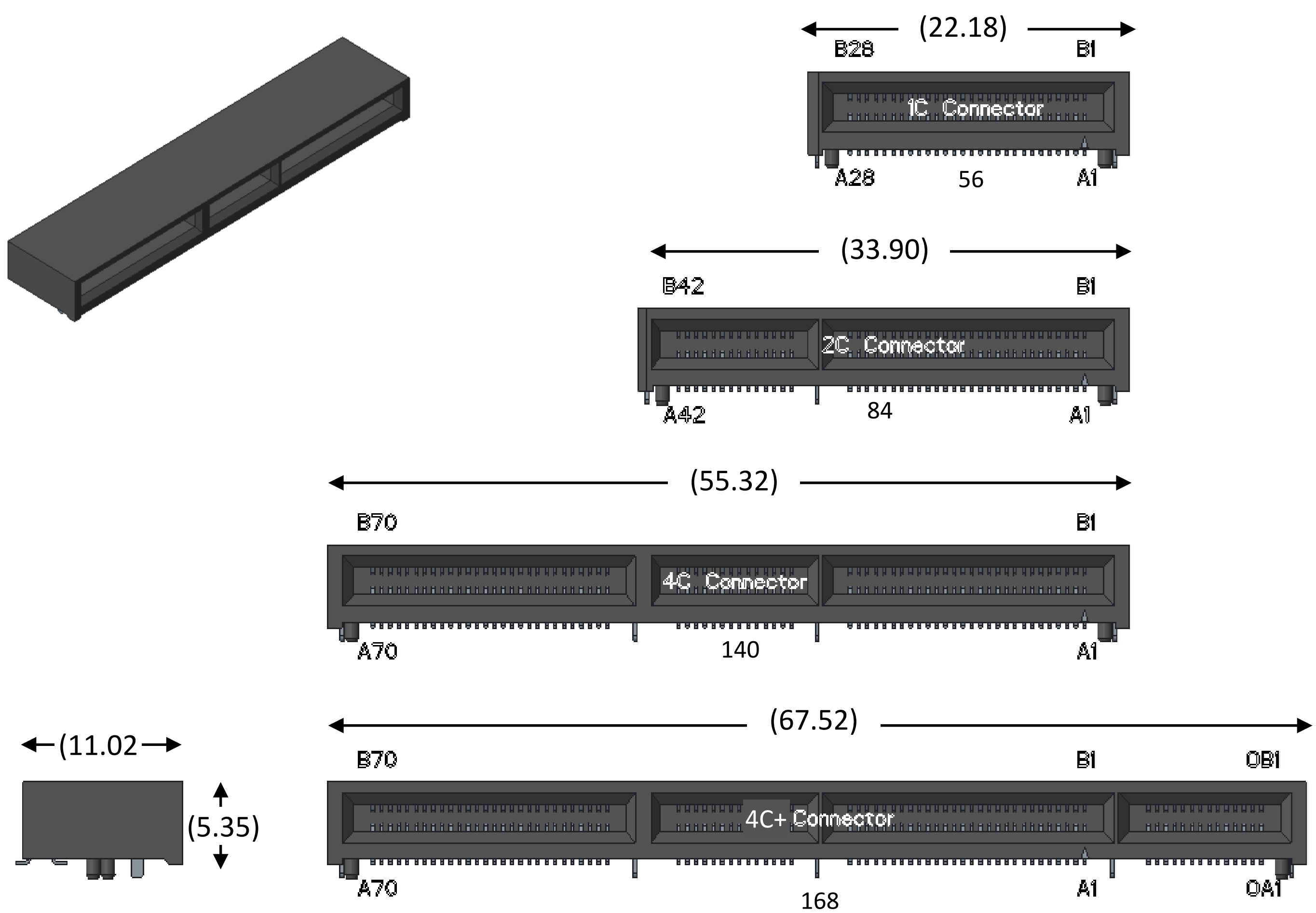


FIGURE 5-9. 1C, 2C, 4C AND 4C+ RIGHT ANGLE CONNECTOR DIMENSIONS OVERVIEW

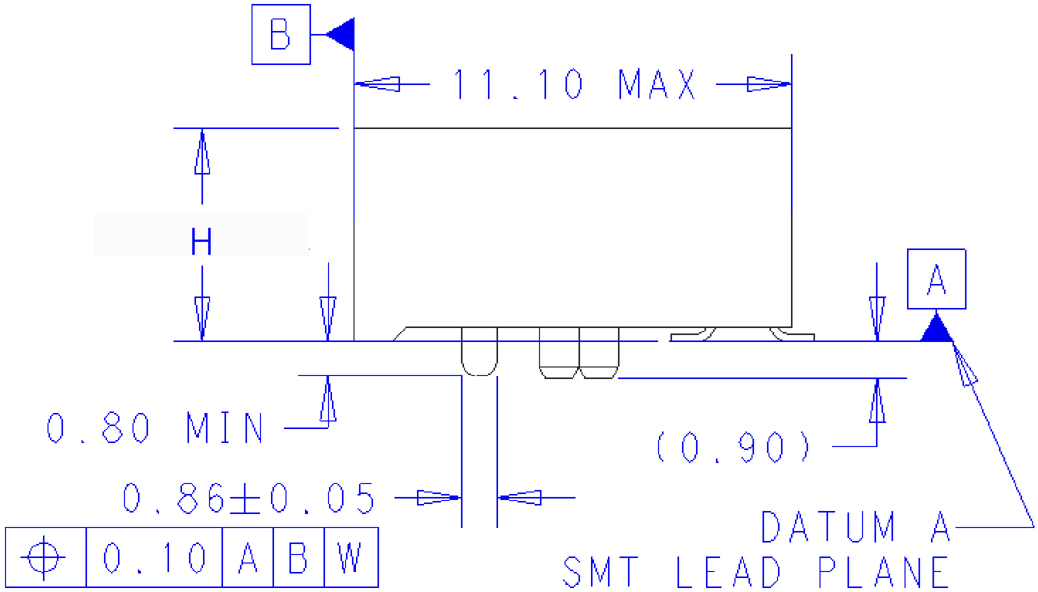


FIGURE 5-10. 1C, 2C, 4C AND 4C+ RIGHT ANGLE CONNECTOR PROFILE DIMENSIONS

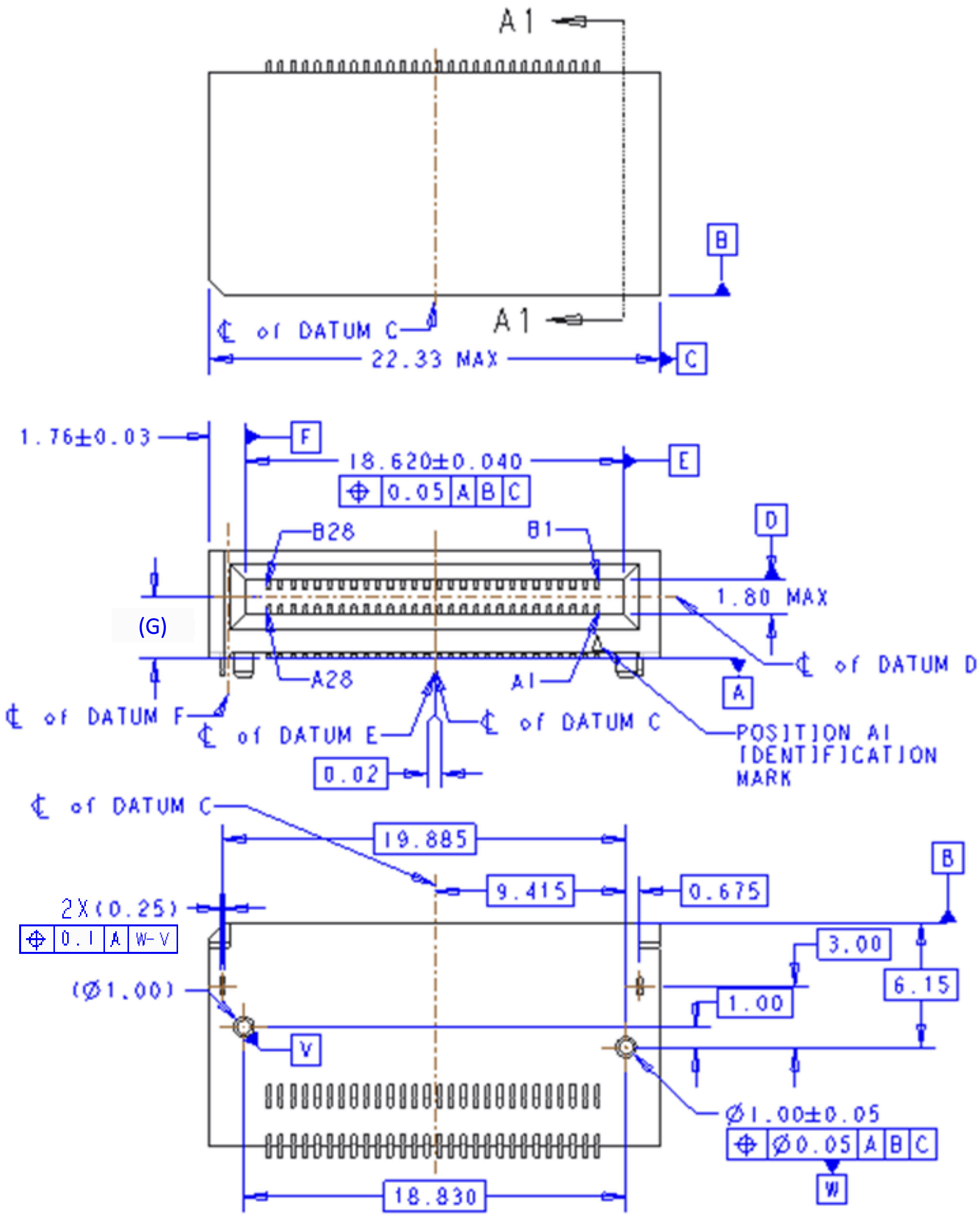


FIGURE 5-11. 1C RIGHT ANGLE CONNECTOR DIMENSIONS

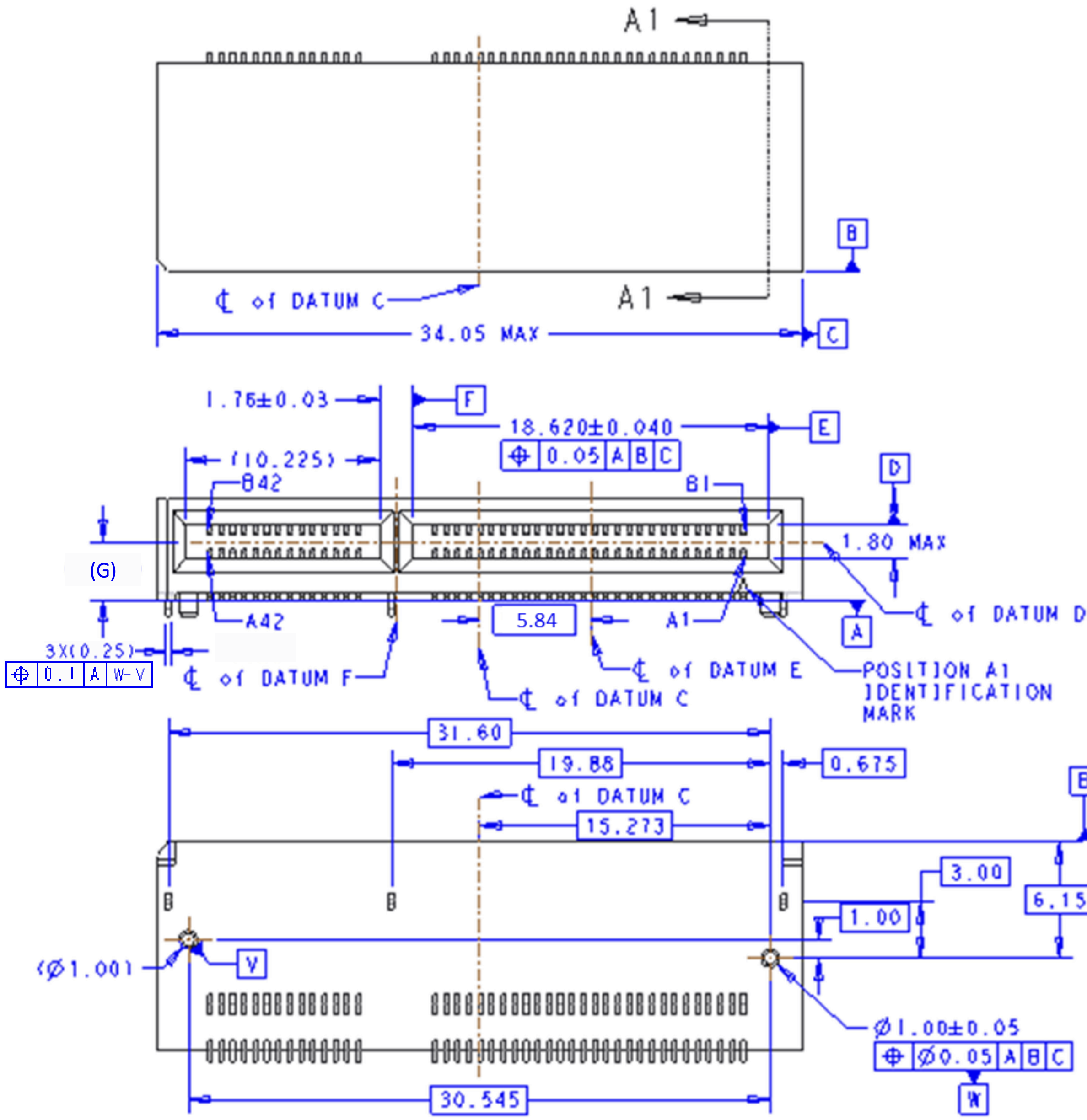


FIGURE 5-12. 2C RIGHT ANGLE CONNECTOR DIMENSIONS

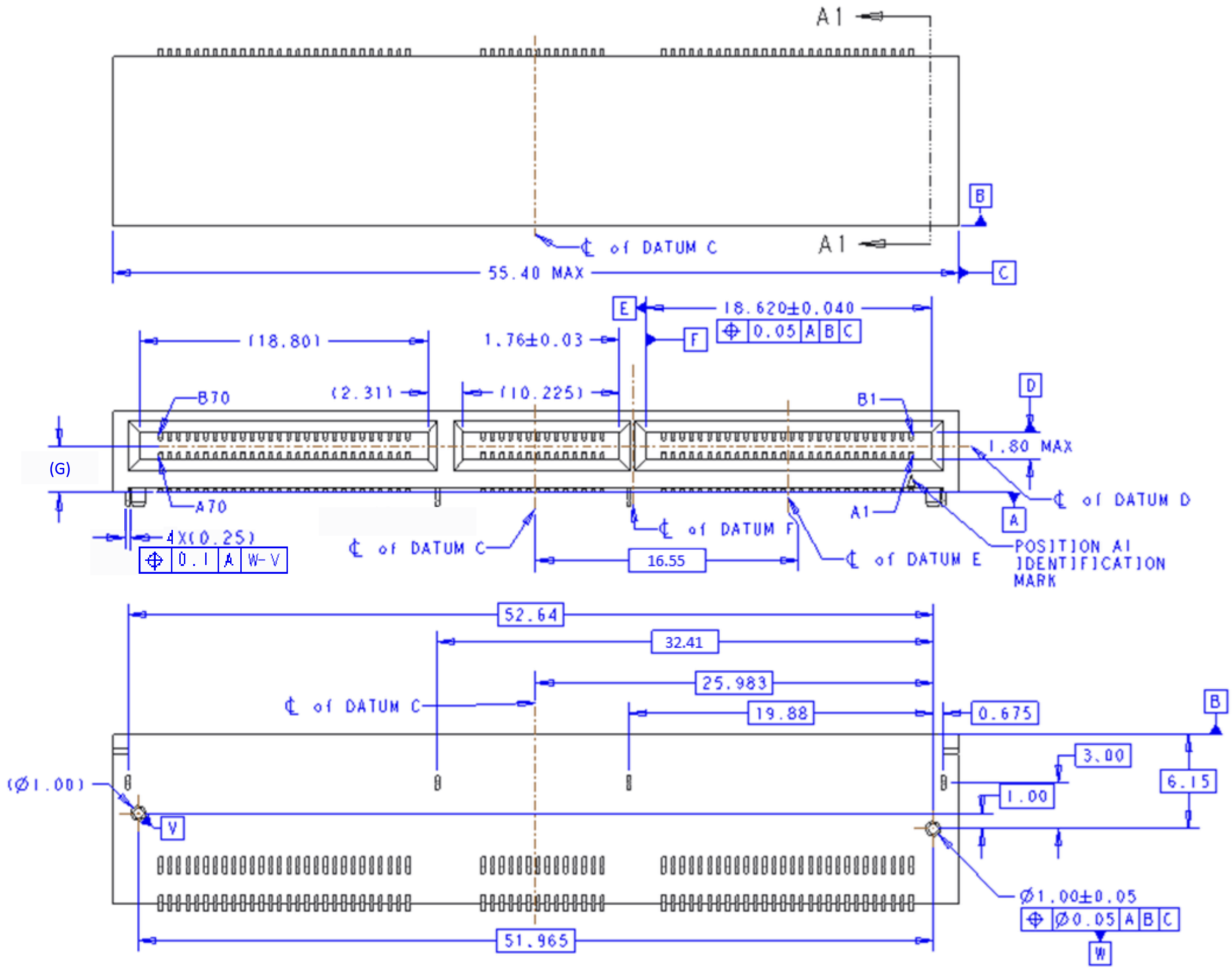


FIGURE 5-13. 4C RIGHT ANGLE CONNECTOR DIMENSIONS

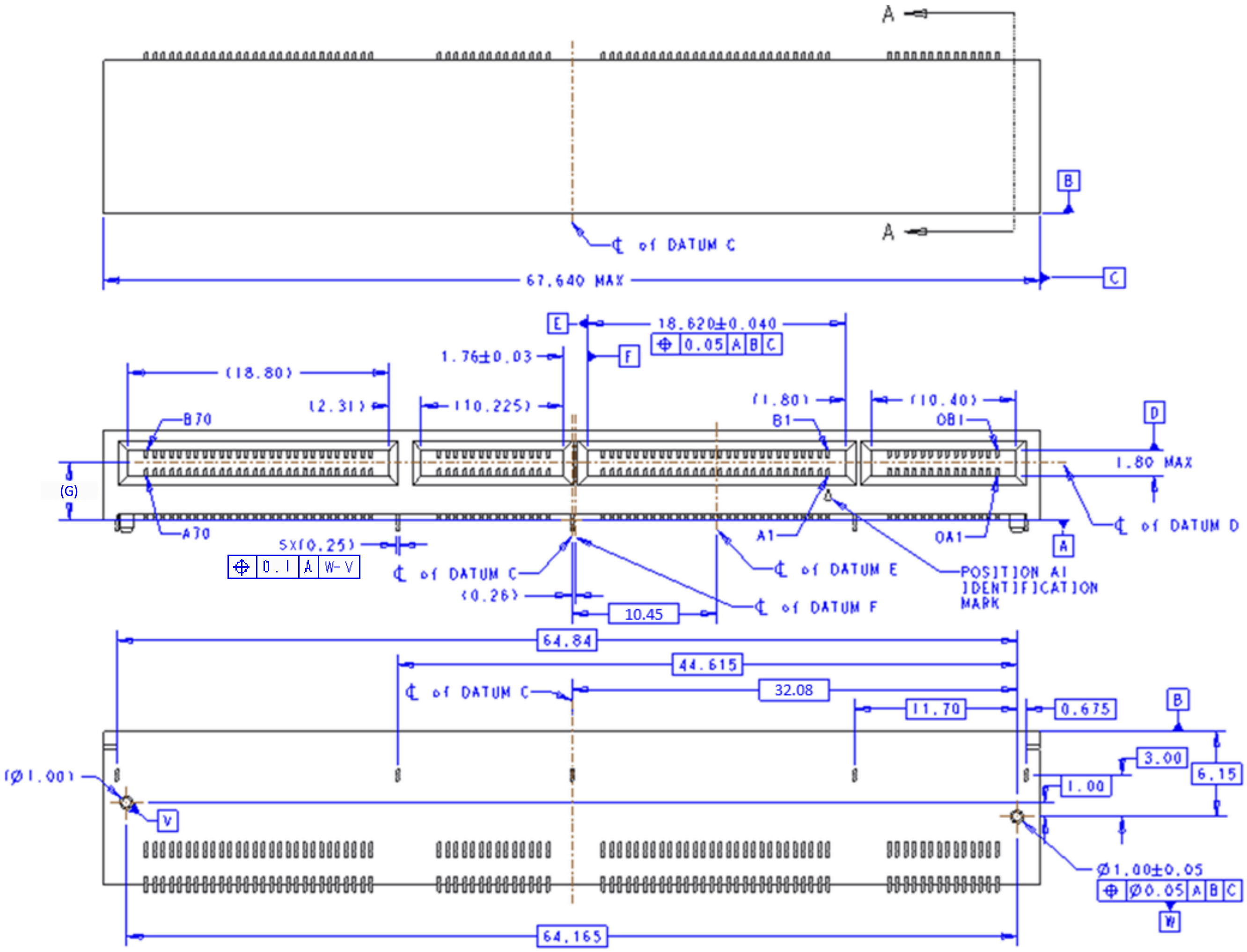


FIGURE 5-14. 4C+ RIGHT ANGLE CONNECTOR DIMENSIONS

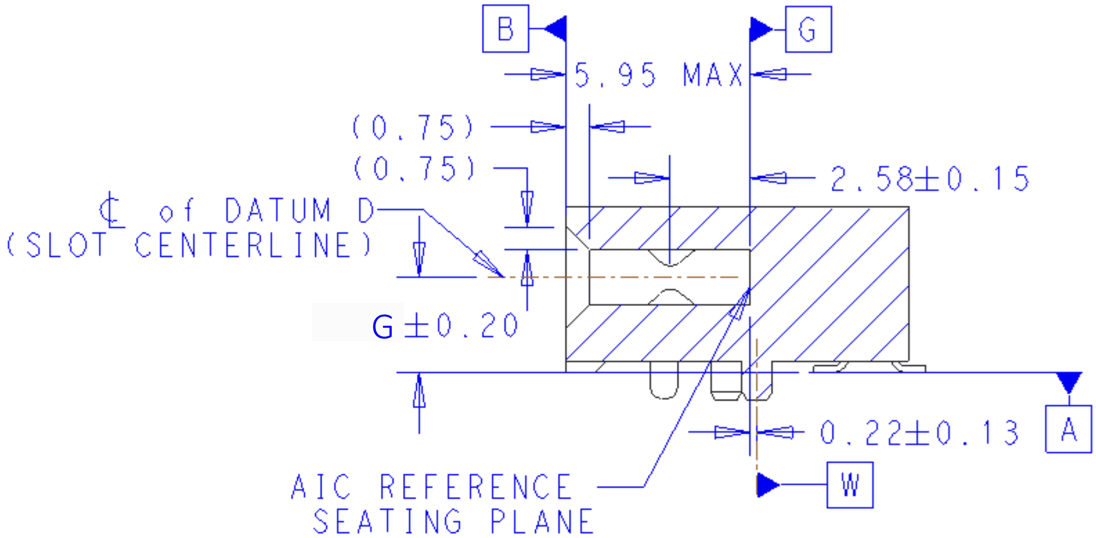


FIGURE 5-15. SECTION A: 1C, 2C, 4C AND 4C+ RIGHT ANGLE CONNECTOR SEATING PLANE

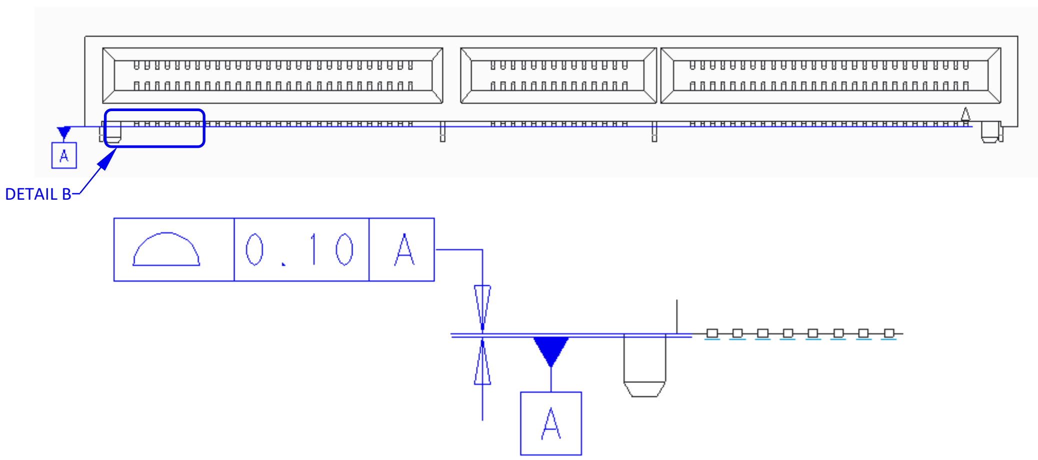


FIGURE 5-16. DETAIL B: RIGHT ANGLE CONNECTOR SMT LEAD CO-PLANARITY

TABLE 5-1. RIGHT ANGLE HEIGHT VARIATIONS

DIM H (mm)	DIM G (mm)
6.55 MAX	4.05
5.55 MAX	3.05

5.3.3 Unshielded Fixed (Receptacle) Straddle Mount Connectors

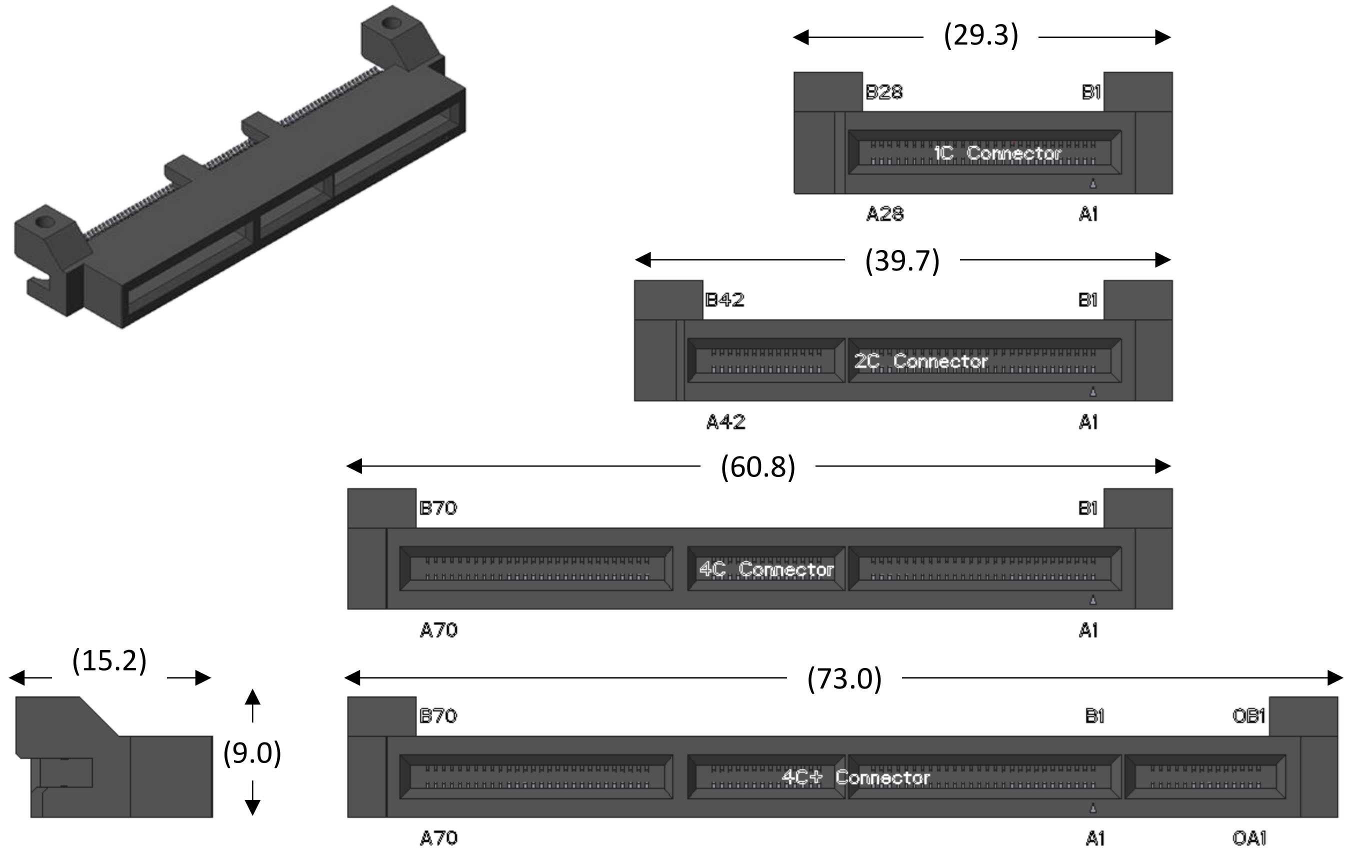


FIGURE 5-17. 1C, 2C, 4C AND 4C+ STRADDLE MOUNT CONNECTOR DIMENSIONS OVERVIEW

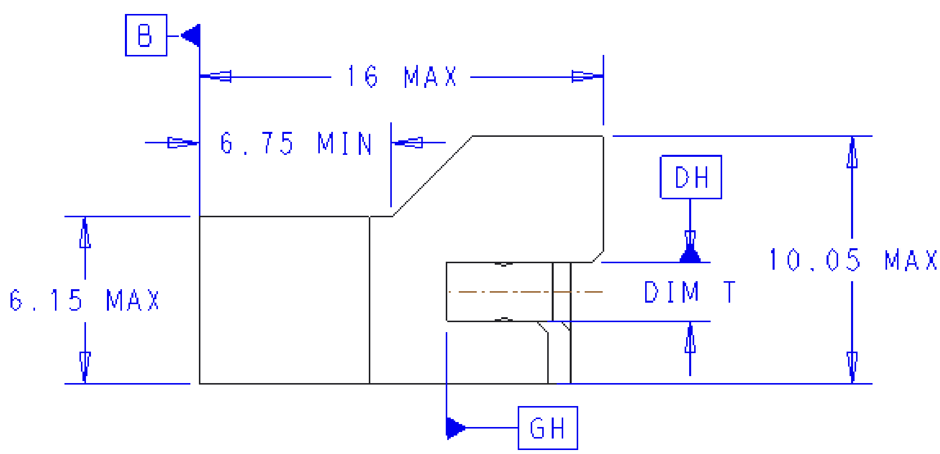


FIGURE 5-18. 1C, 2C, 4C AND 4C+ STRADDLE MOUNT CONNECTOR PROFILE DIMENSIONS (MM)

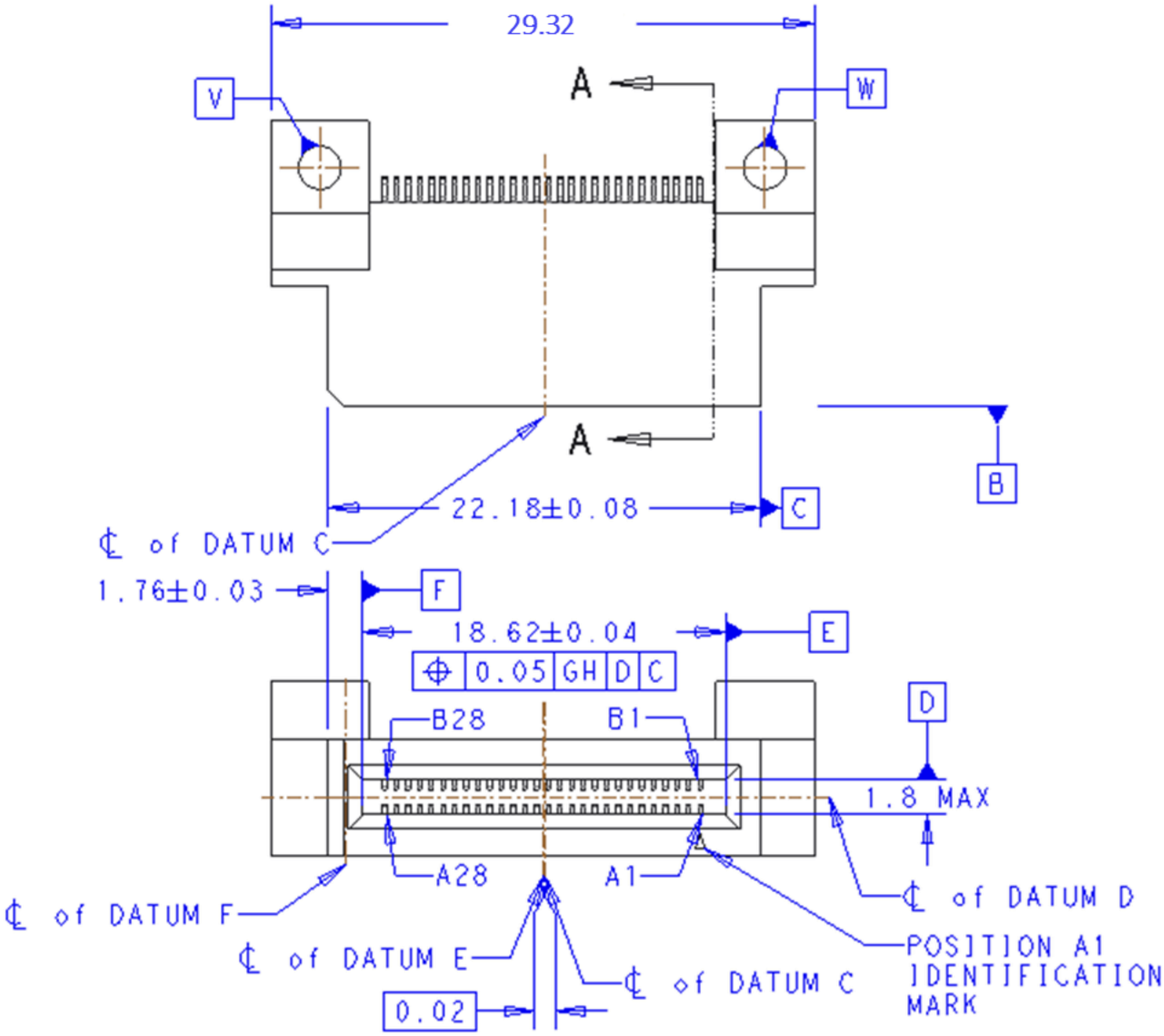


FIGURE 5-19. 1C STRADDLE MOUNT CONNECTOR DIMENSIONS - FRONT VIEW (MM)

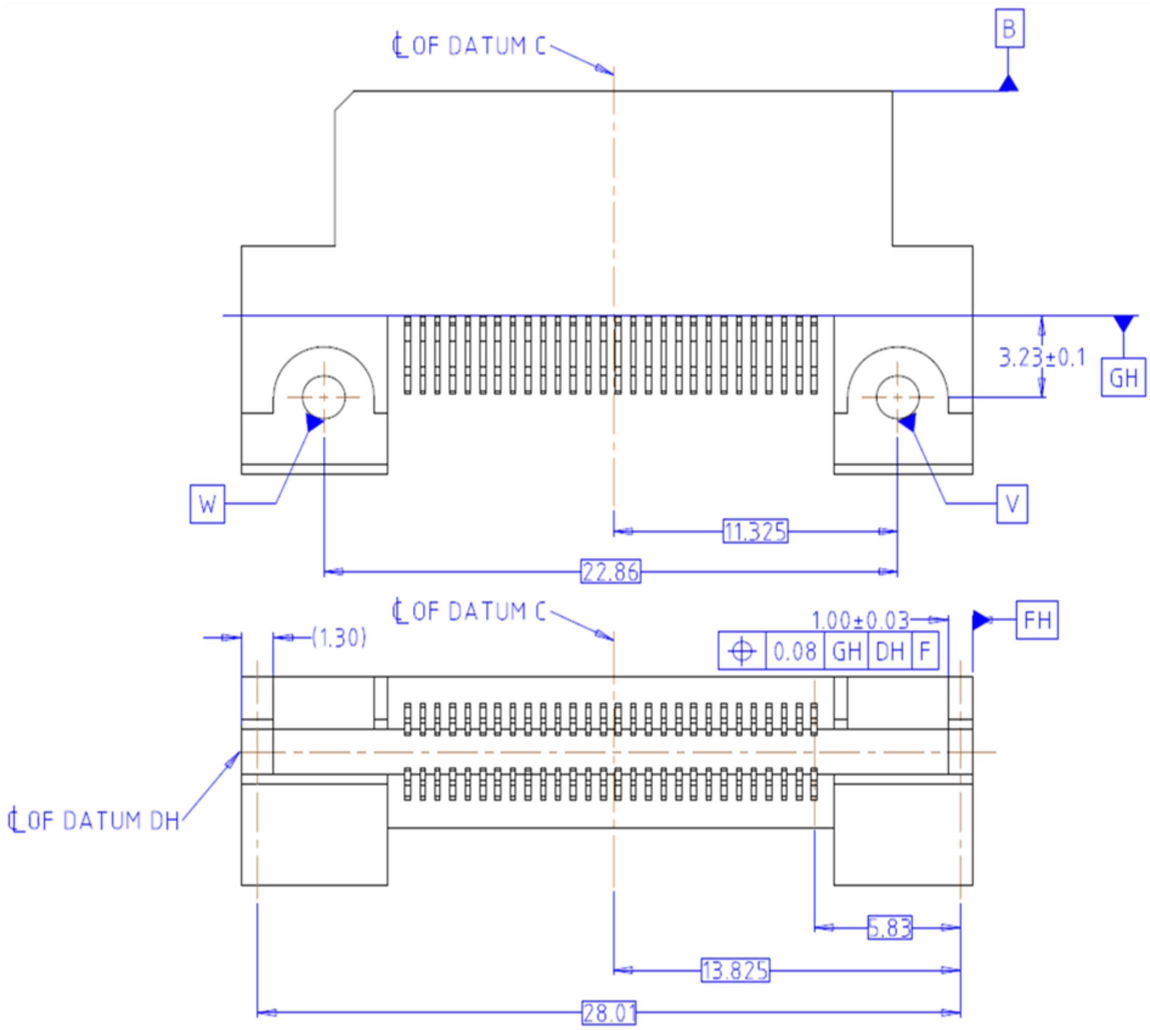


FIGURE 5-20. 1C STRADDLE MOUNT CONNECTOR DIMENSIONS – REAR VIEW (MM)

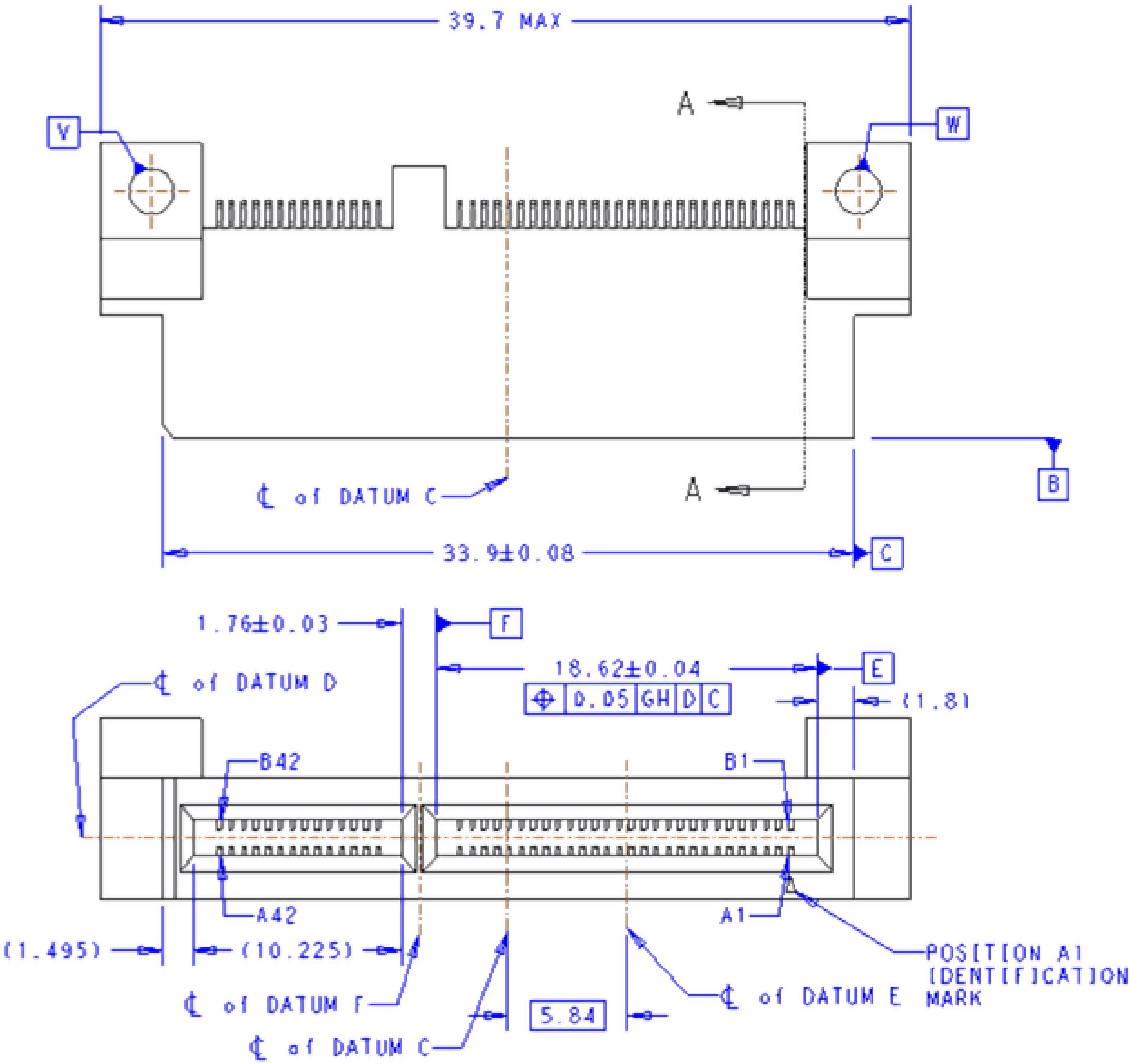


FIGURE 5-21. 2C STRADDLE MOUNT CONNECTOR DIMENSIONS – FRONT VIEW (MM)

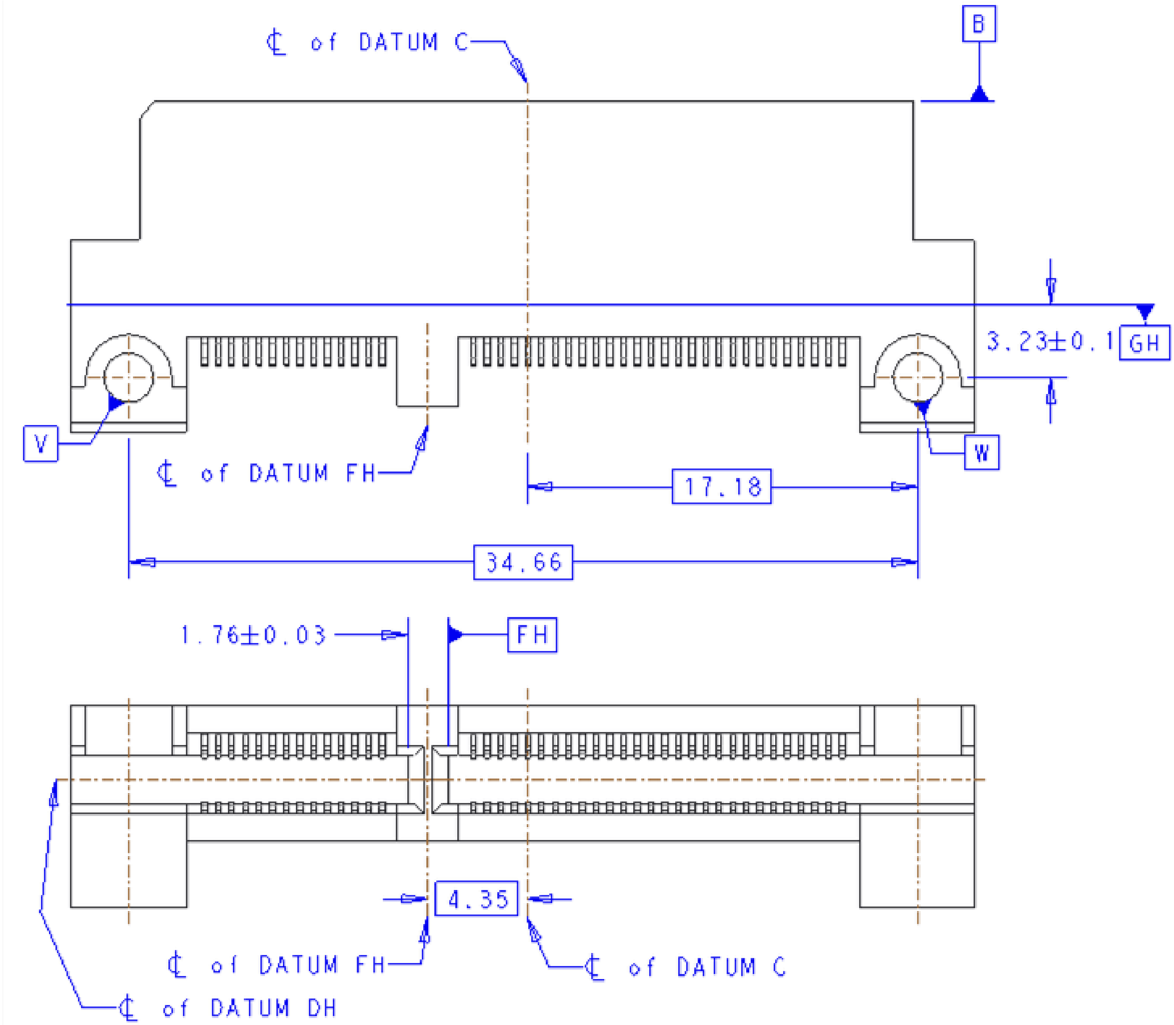


FIGURE 5-22. 2C STRADDLE MOUNT CONNECTOR DIMENSIONS - REAR VIEW (MM)

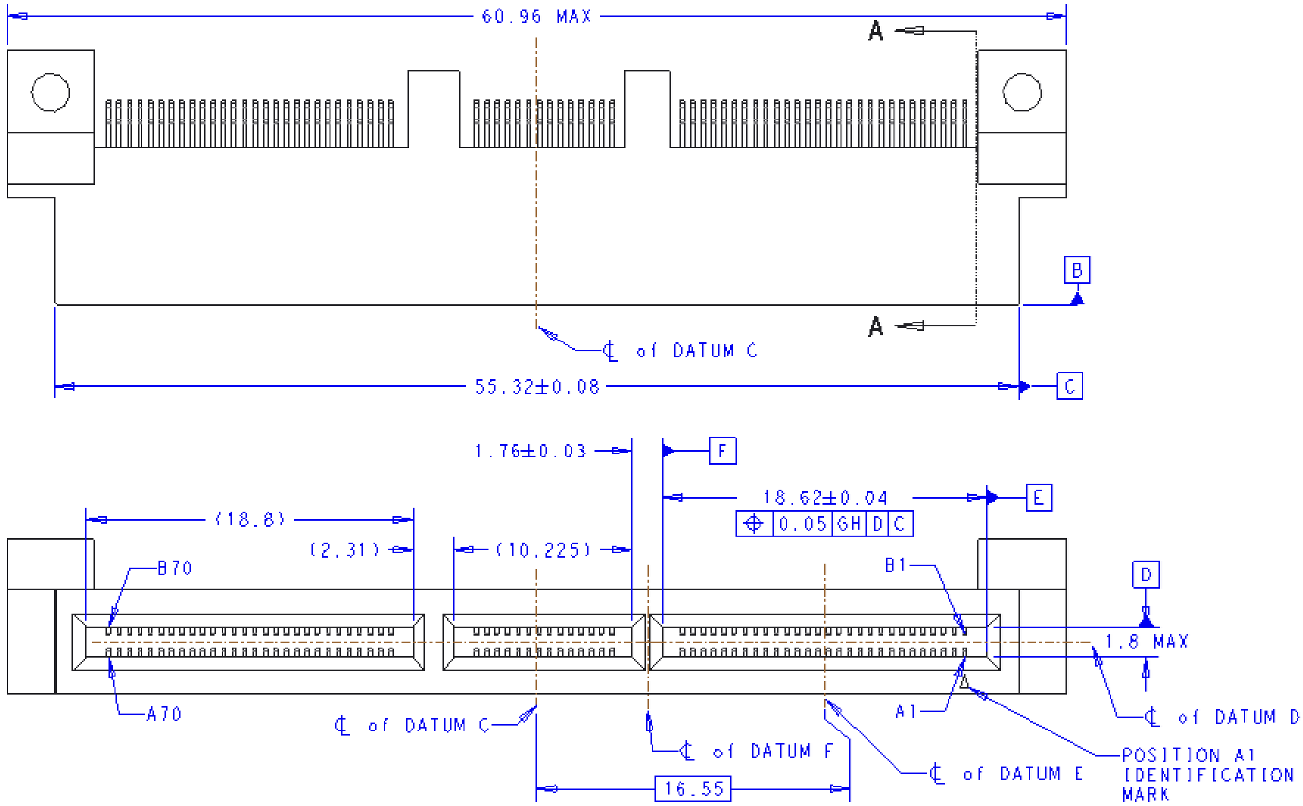


FIGURE 5-23. 4C STRADDLE MOUNT CONNECTOR DIMENSIONS – FRONT VIEW (MM)

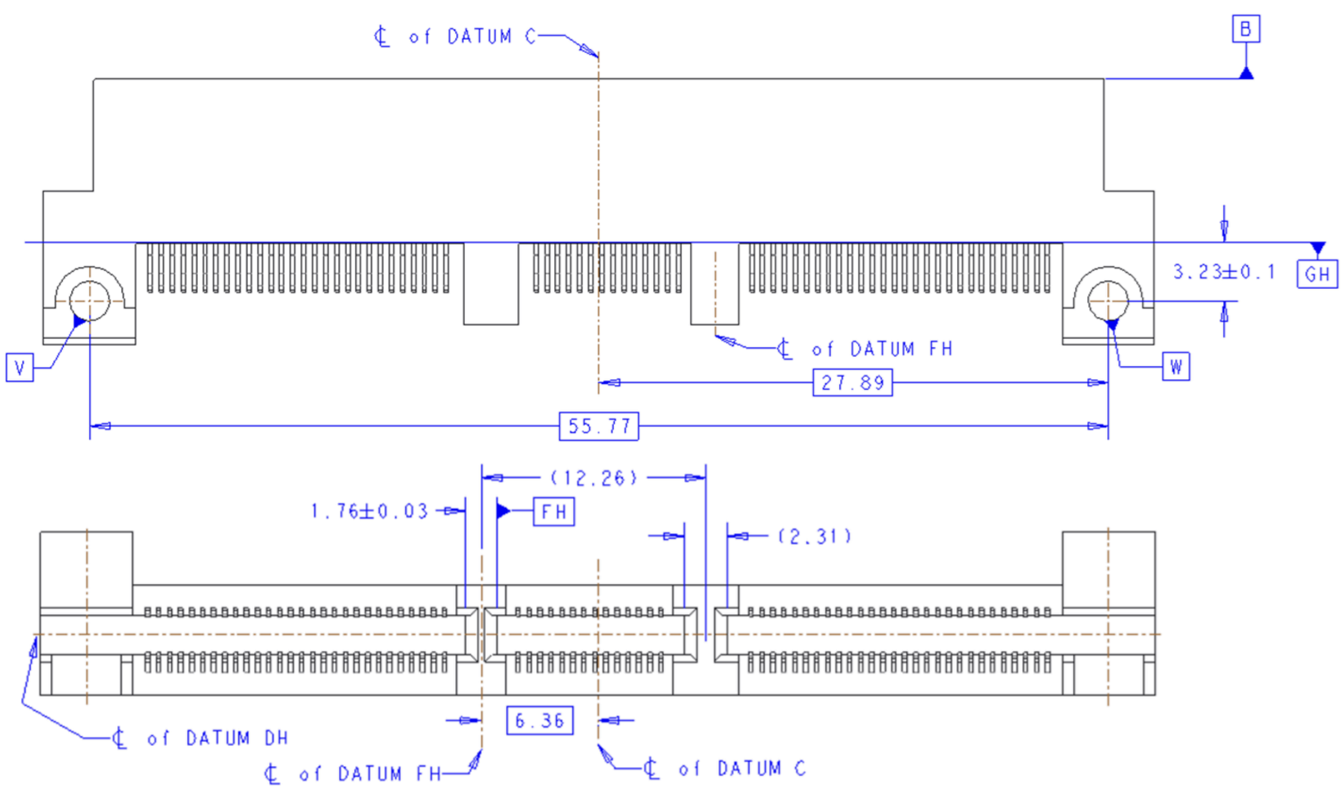


FIGURE 5-24. 4C STRADDLE MOUNT CONNECTOR DIMENSIONS – REAR VIEW (MM)

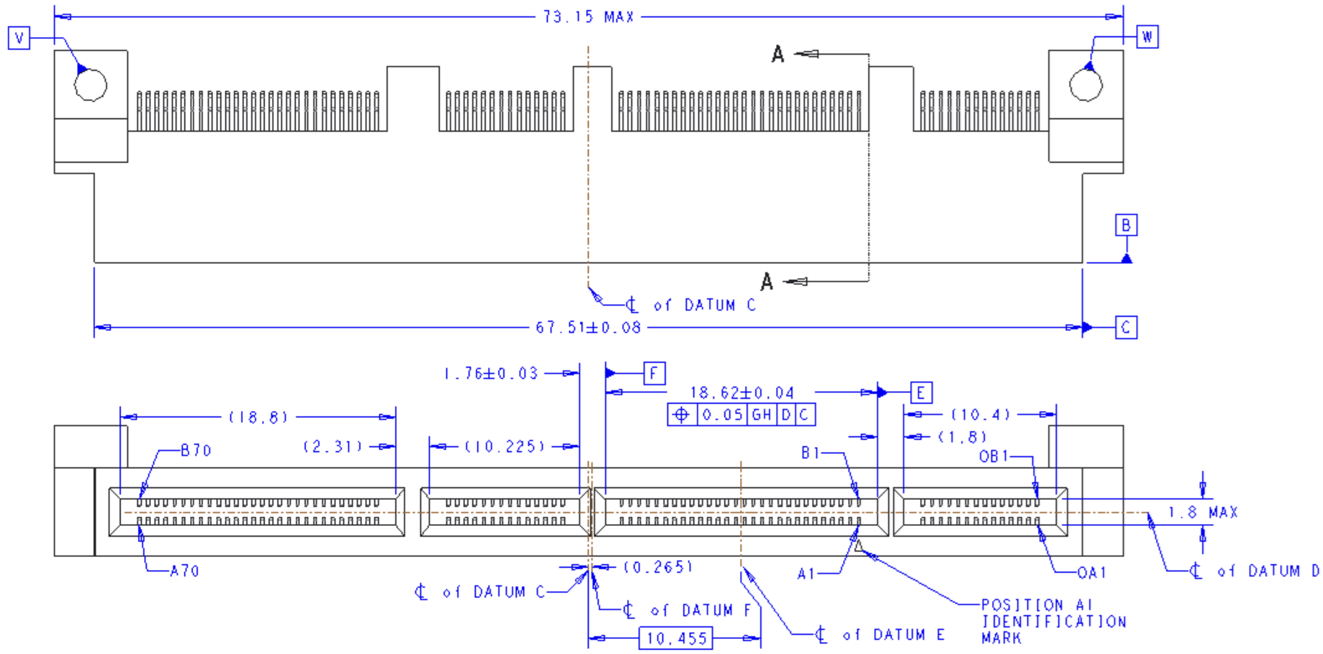


FIGURE 5-25. 4C+ STRADDLE MOUNT CONNECTOR DIMENSIONS – FRONT VIEW (MM)

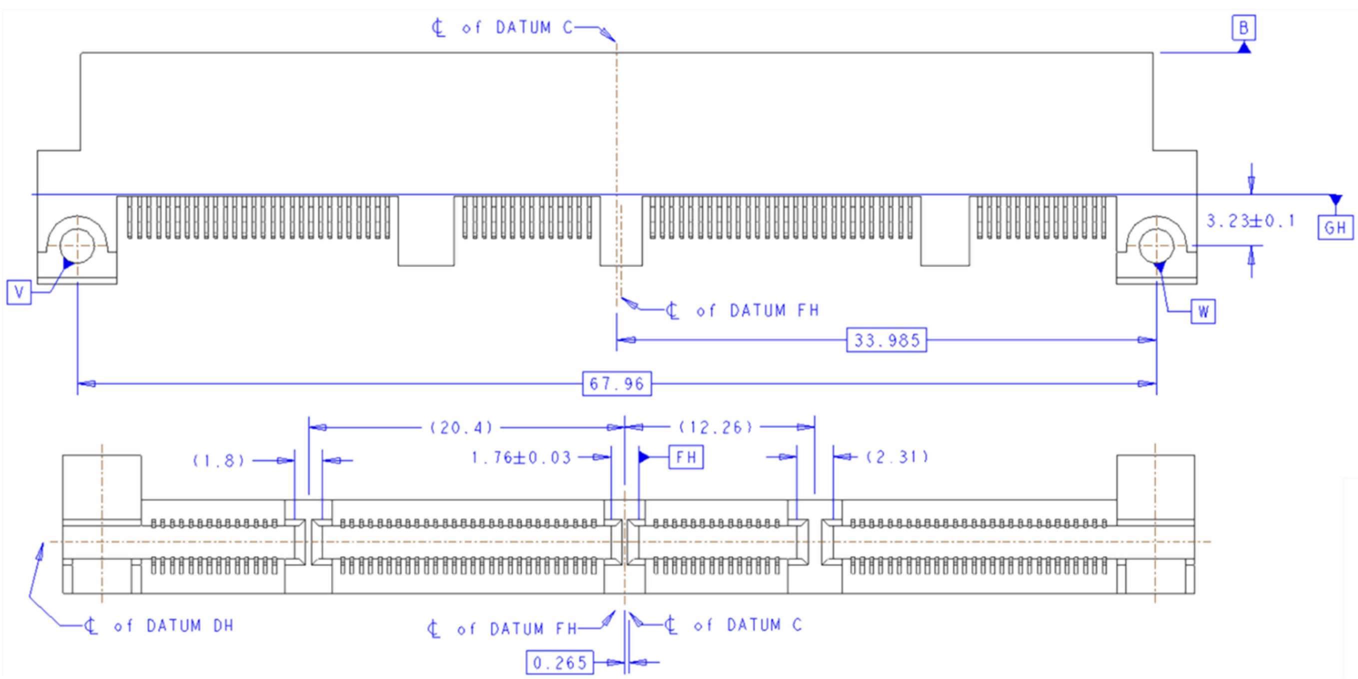


FIGURE 5-26. 4C+ STRADDLE MOUNT CONNECTOR DIMENSIONS – REAR VIEW (MM)

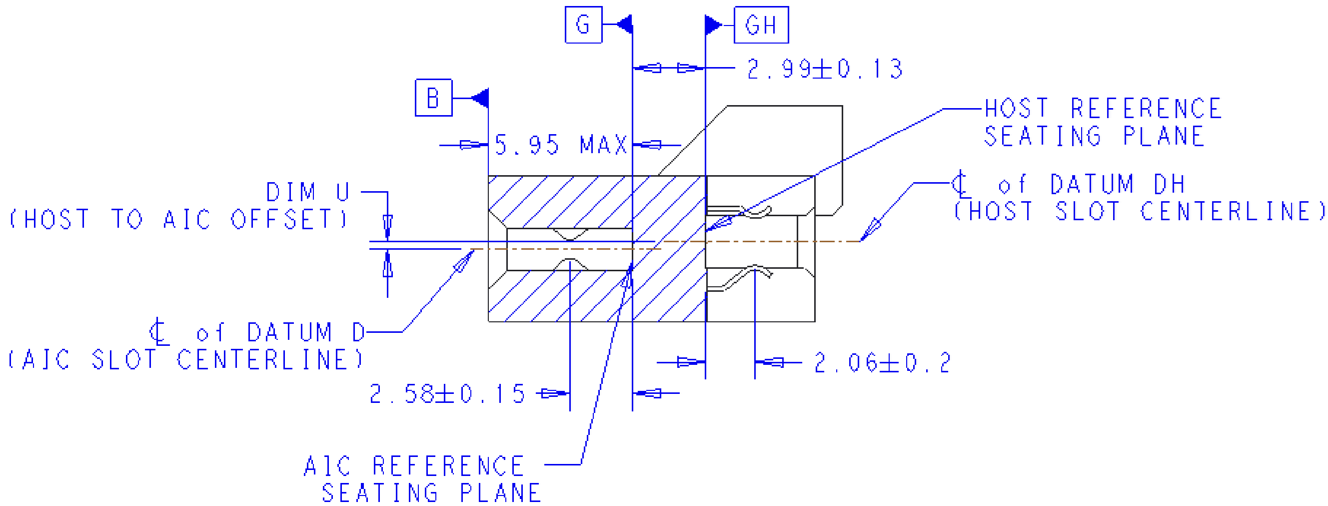


FIGURE 5-27. SECTION A: STRADDLE MOUNT CONNECTOR SEATING PLANE DIMENSIONS (MM)

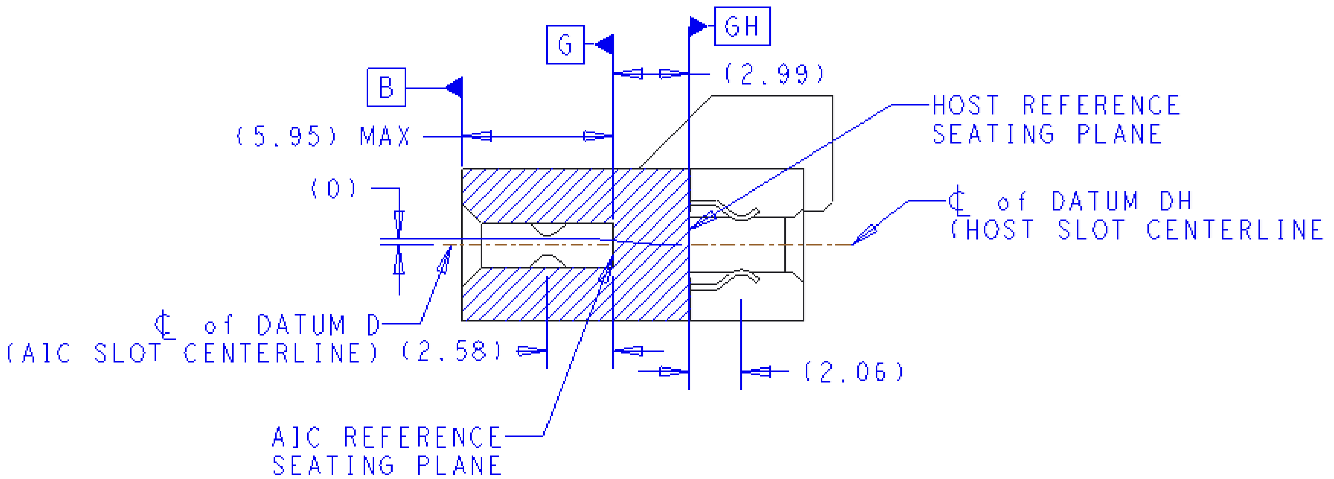
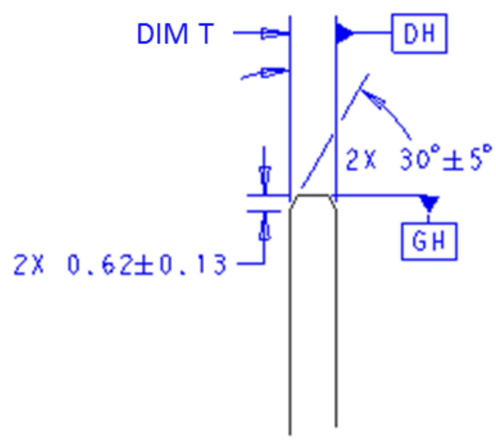


FIGURE 5-28. SECTION A: STRADDLE MOUNT CONNECTOR SEATING PLANE WITH ZERO OFFSET (MM)



Note: Refer to **TABLE 5-2** for DIM T values.

FIGURE 5-29. FIXED SIDE BOARD EDGE PROFILE DIMENSIONS (MM)

TABLE 5-2. STRADDLE MOUNT HOST BOARD THICKNESS AND OFFSET VARIANTS (MM)

DIM T (HOST BOARD THICKNESS)	DIM U (OFFSET)
1.57±0.15 (.062”)	0.00 (.0000”)
1.93±0.19 (.076”)	0.30 (.0118”)
2.36±0.23 (.093”)	0.00 (.0000”)
2.55±0.23 (0.100”)	0.00 (.0000”)
3.05±0.25 (.120”)	0.00 (.0000”)

5.3.4 Unshielded Fixed (Receptacle) Press fit Orthogonal Connectors

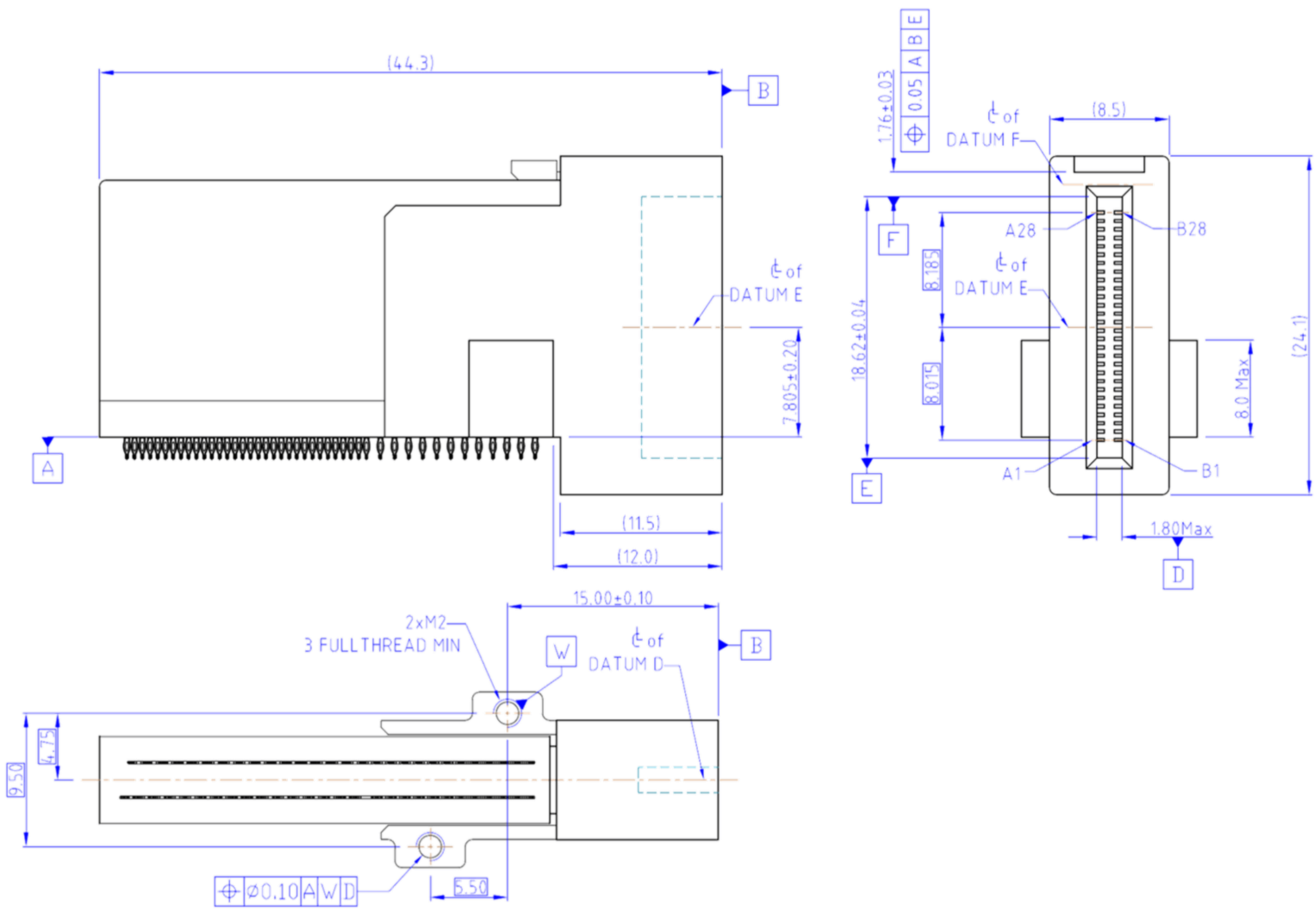


FIGURE 5-30. 1C RIGHT ANGLE ORTHOGONAL CONNECTOR DIMENSIONS (MM)

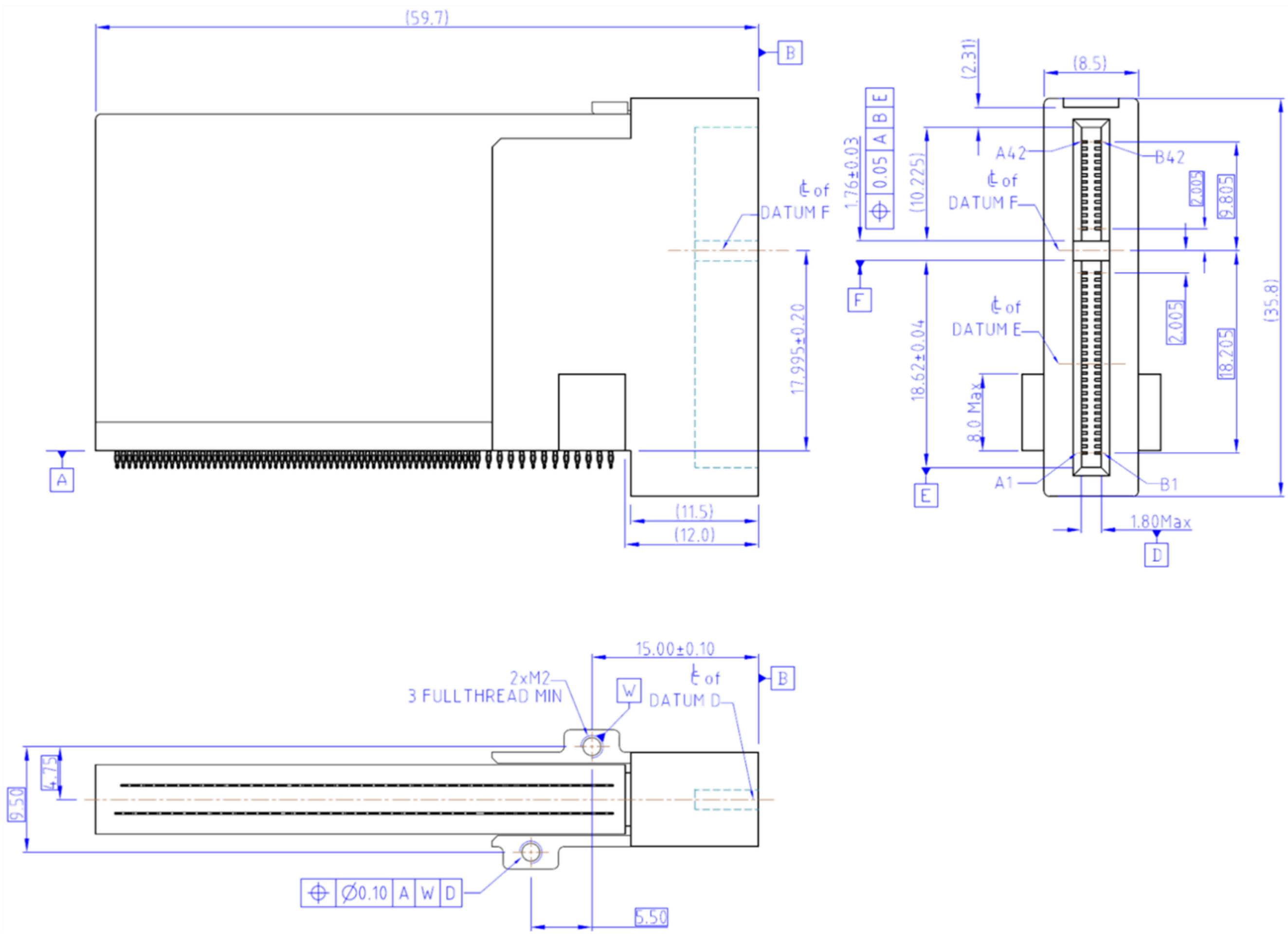


FIGURE 5-31. 2C RIGHT ANGLE ORTHOGONAL CONNECTOR DIMENSIONS (MM)

5.3.5 Unshielded Fixed (Receptacle) Surface Mount Orthogonal Connectors

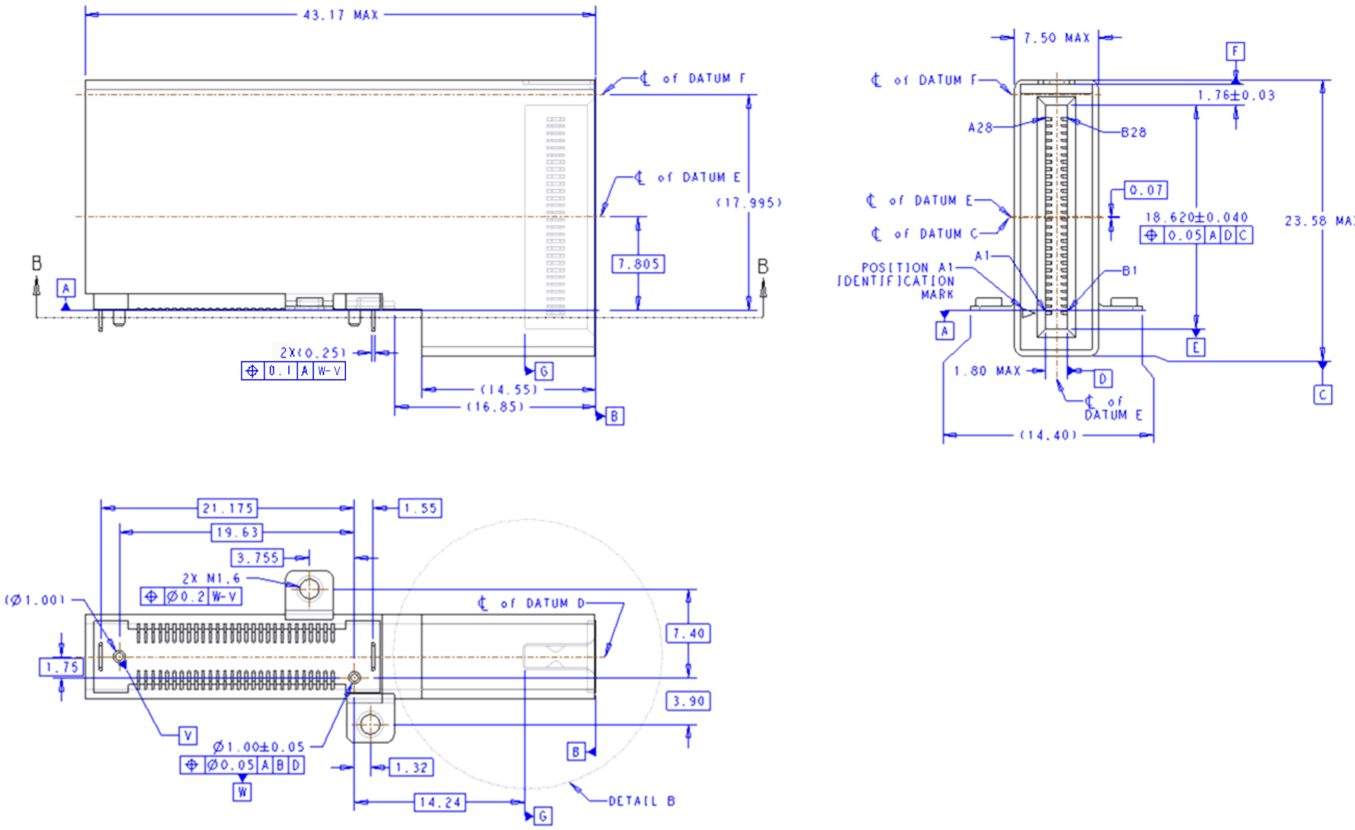


FIGURE 5-32. 1C RIGHT ANGLE ORTHOGONAL SMT CONNECTOR DIMENSIONS (MM)

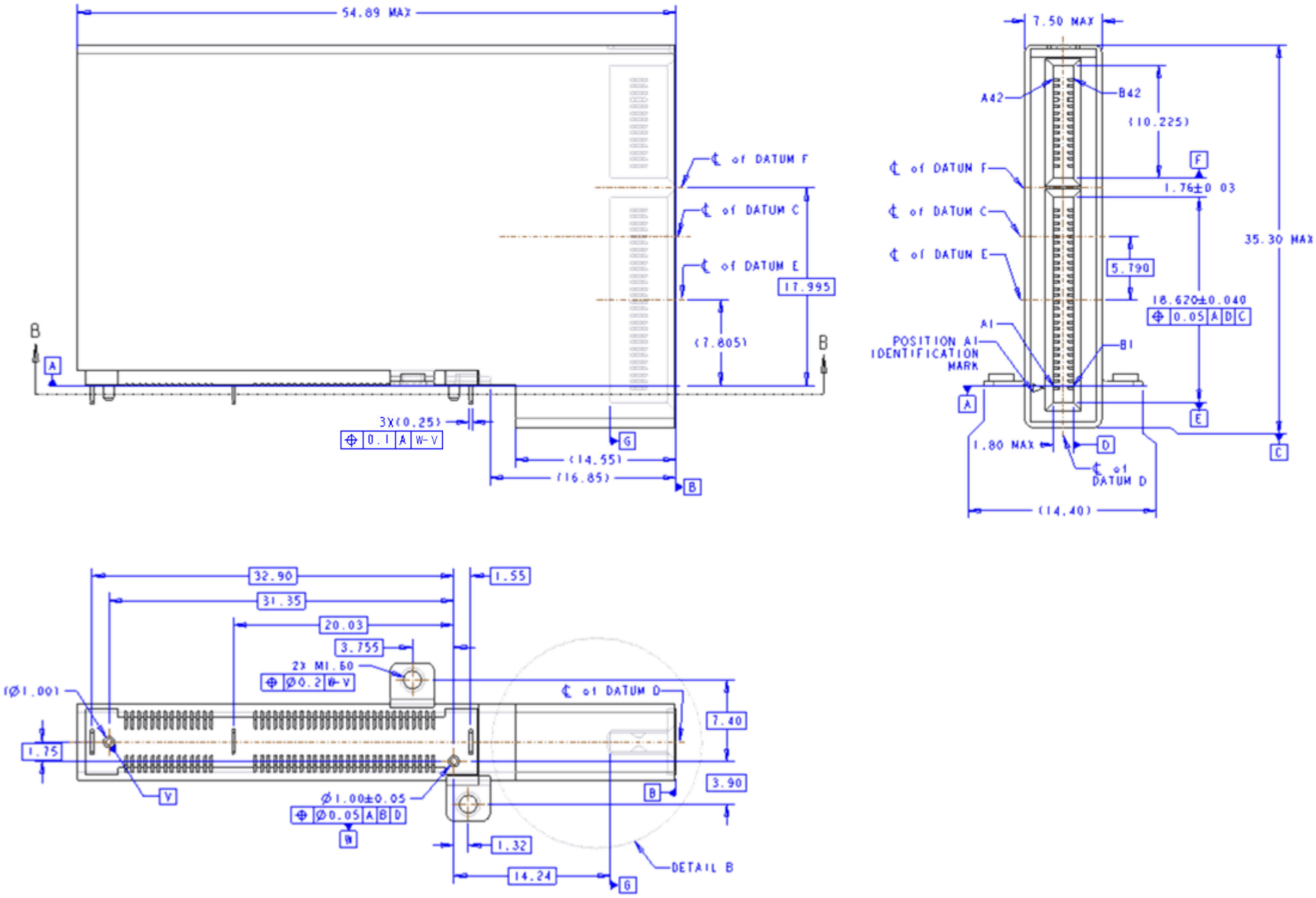
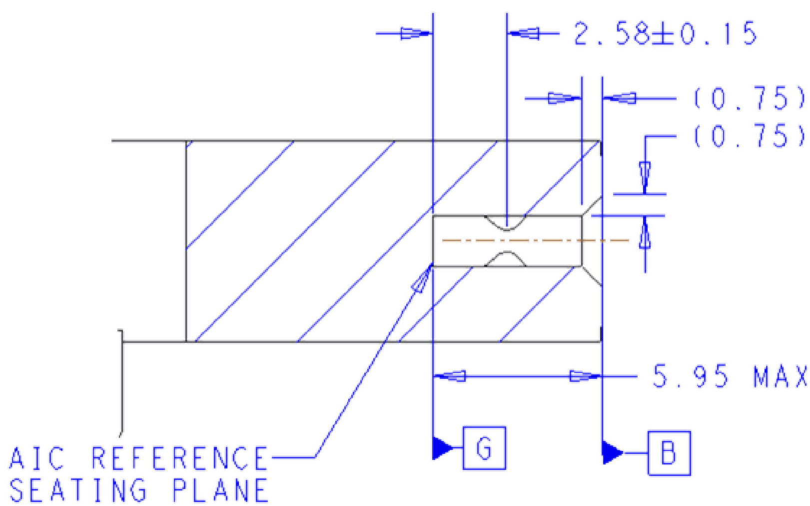


FIGURE 5-33. 2C RIGHT ANGLE ORTHOGONAL SMT CONNECTOR DIMENSIONS (MM)



SECTION B-B

FIGURE 5-34. DETAIL B: RIGHT ANGLE ORTHOGONAL CONNECTOR SEATING PLANE DIMENSIONS (MM)

5.4 Add-In Card Free (Plug) Mechanical Drawings

The Add-In Card (AIC) card outline dimensions are shown in Figure 5-35 through Figure 5-41. If plating tie bars are used for plating purposes, all tie bars shall be removed on the mating AIC. All chamfered edges and edge of pads shall be free of burrs.

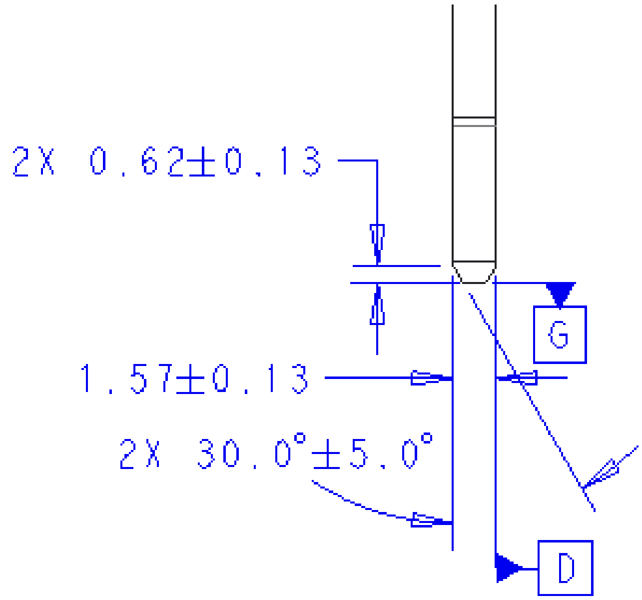
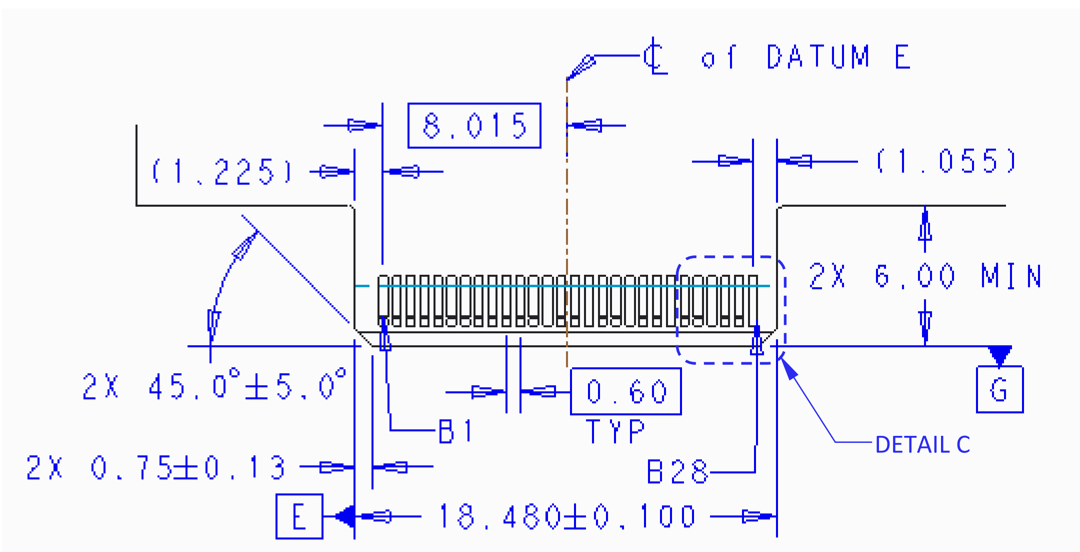
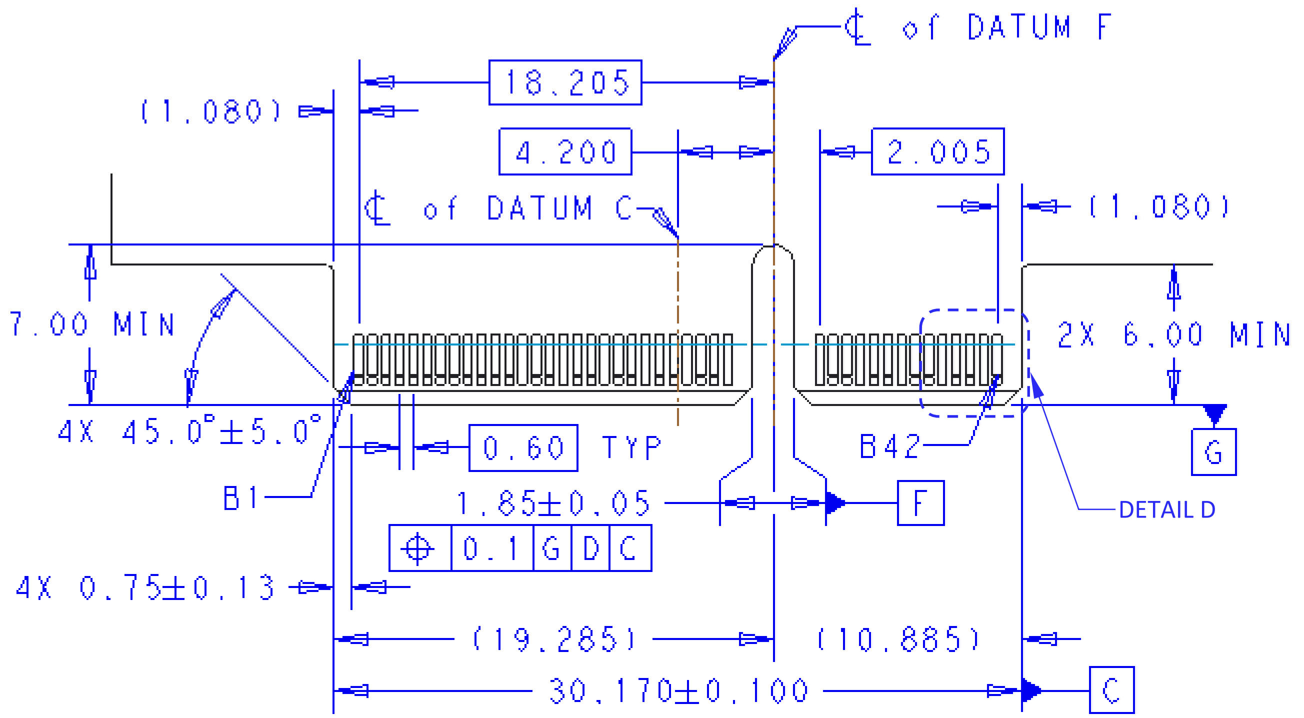


FIGURE 5-35. AIC MATING CARD PROFILE DIMENSIONS



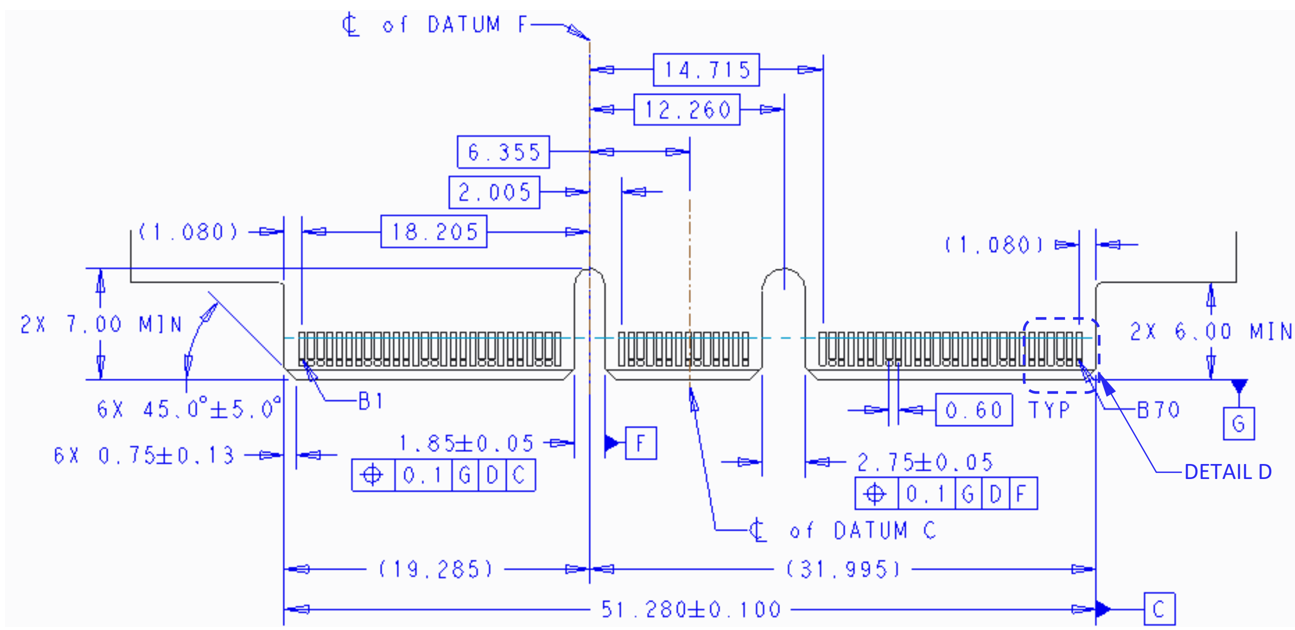
Notes: Position A1 on opposite side of card of B1. Dimensions for pad locations are to center of the pad

FIGURE 5-36. AIC 1C MATING CARD DIMENSIONS



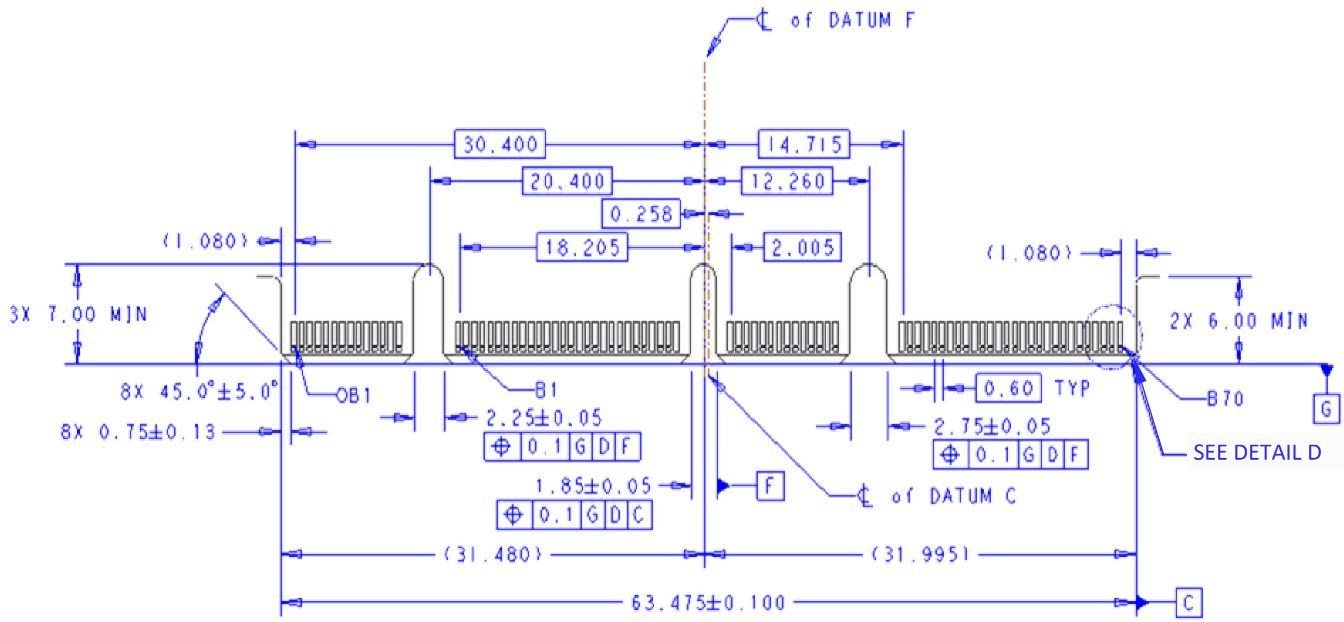
Notes: Position A1 on opposite side of card of B1. Dimensions for pad locations are to center of the pad

FIGURE 5-37. AIC 2C MATING CARD DIMENSIONS



Notes: Position A1 on opposite side of card of B1. Dimensions for pad locations are to center of the pad

FIGURE 5-38. AIC 4C MATING CARD DIMENSIONS

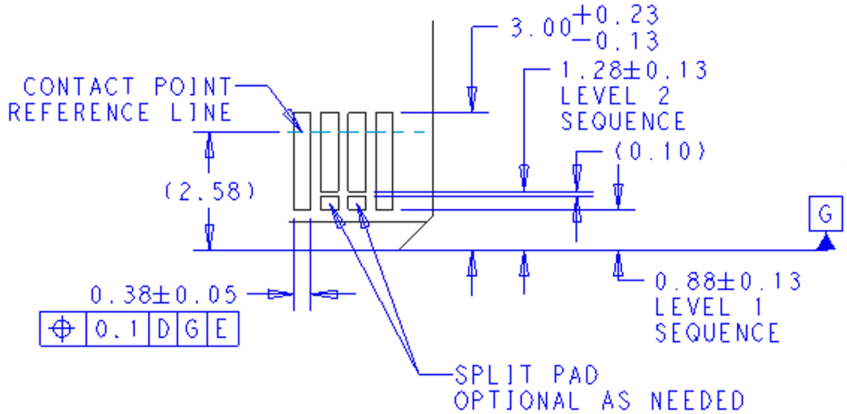


Notes: Position A1 on opposite side of card of B1. Dimensions for pad locations are to center of the pad.

FIGURE 5-39. AIC 4C+ MATING CARD DIMENSIONS (MM)

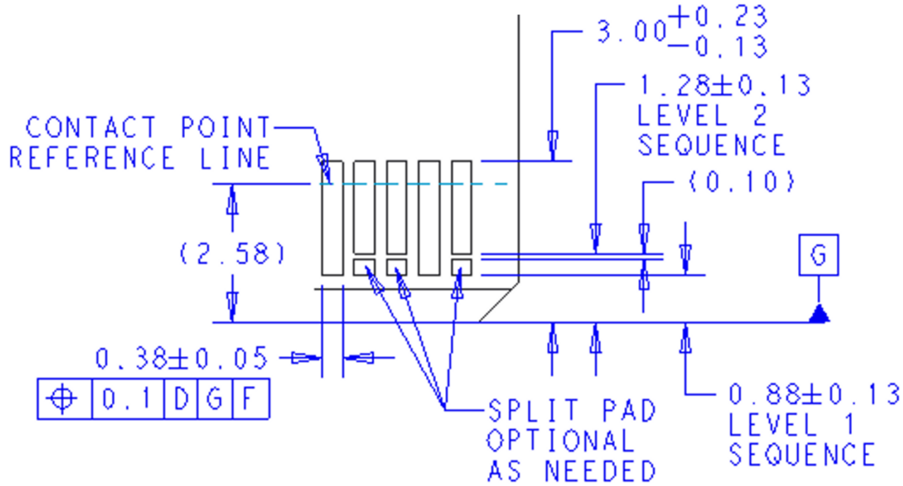
TABLE 5-3. WIPE VALUES FOR LEVEL 1 AND LEVEL 2 SEQUENCING

	Wipe (mm)
Level 1 sequence	1.7 REF
Level 2 sequence	1.3 REF



Notes: PCB Solder Mask should not be less than 2.87 mm from Datum G

FIGURE 5-40. DETAIL C: 1C AIC PAD DIMENSIONS (OPTIONAL SPLIT PAD SHOWN)



Notes: PCB Solder Mask should not be less than 2.87 mm from Datum G

FIGURE 5-41. DETAIL D: 2C, 4C AND 4C+ AIC PAD DIMENSIONS (OPTIONAL SPLIT PAD SHOWN)

5.5 Outer Locus of the Connector Mating Contacts

Figure 5-42 through Figure 5-45 show the outer locus of the connector contacts at the AIC mating interface.

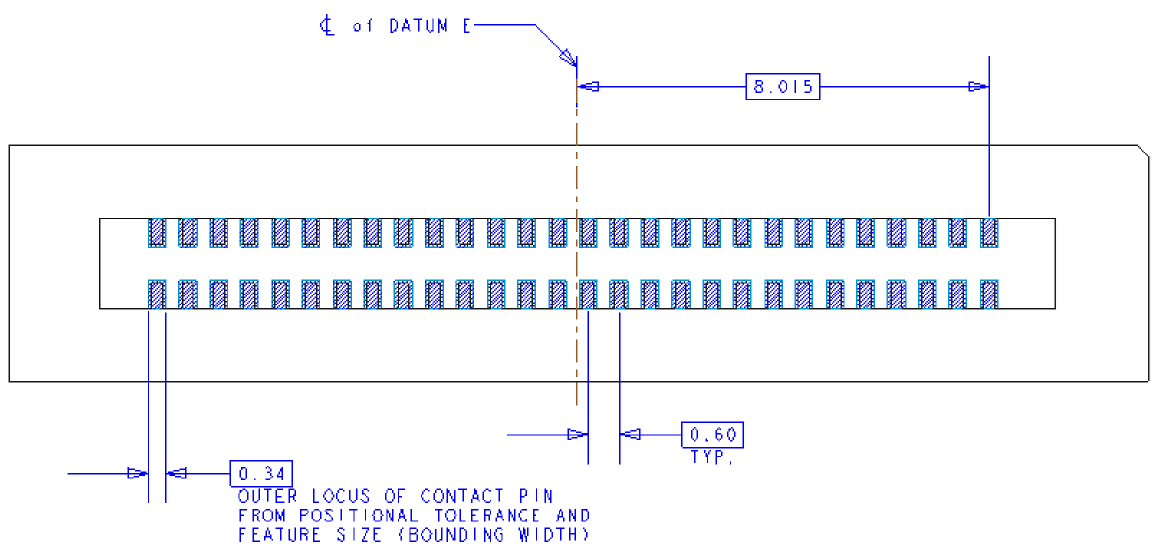


FIGURE 5-42. 1C OUTER LOCUS OF CONNECTOR CONTACT PIN

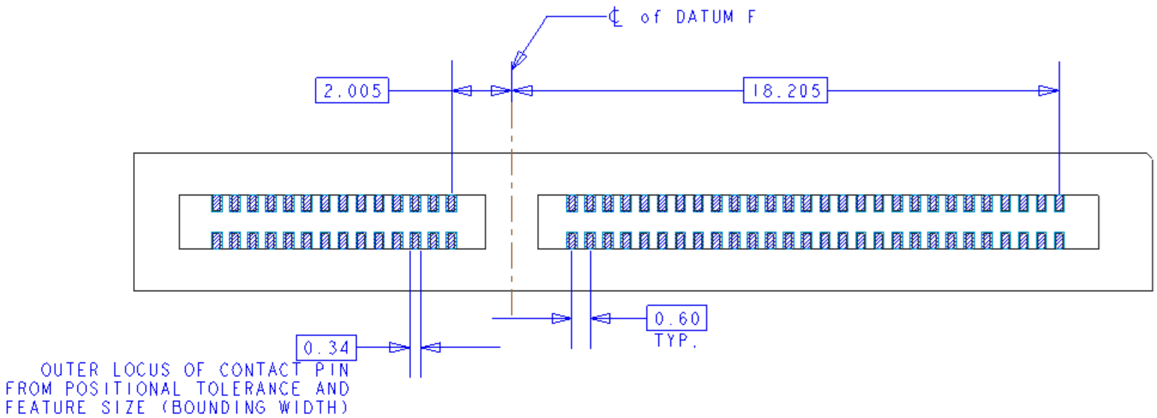


FIGURE 5-43. 2C OUTER LOCUS OF CONNECTOR CONTACT PIN

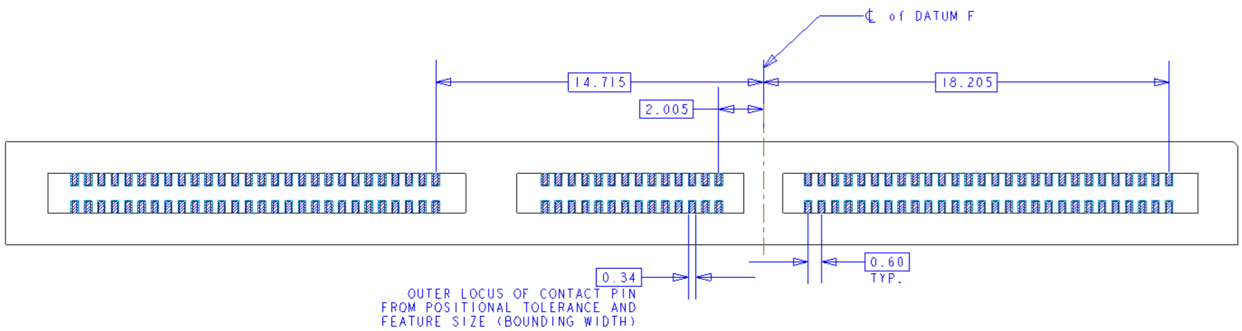


FIGURE 5-44. 4C OUTER LOCUS OF CONNECTOR CONTACT PIN

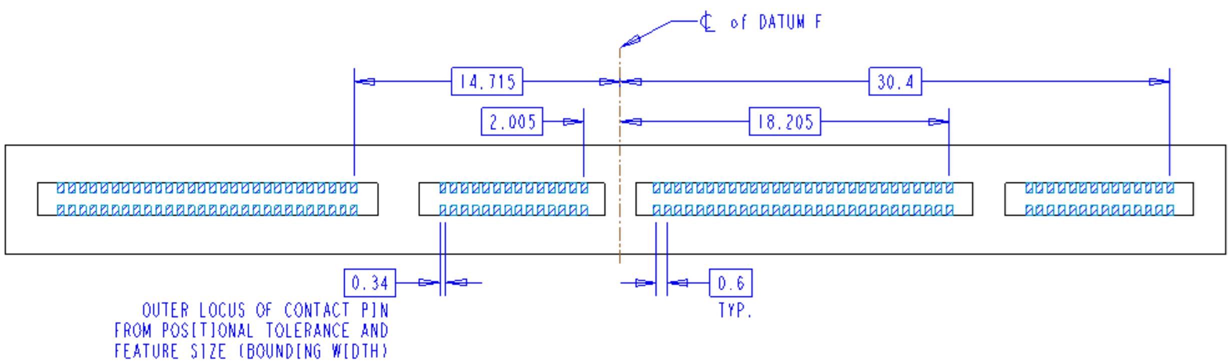


FIGURE 5-45. 4C+ OUTER LOCUS OF CONNECTOR CONTACT PIN

5.6 Outer Locus of SMT Leads

Figure 5-46 through Figure 5-59 show the outer locus of the flat surfaces of the connector SMT leads.

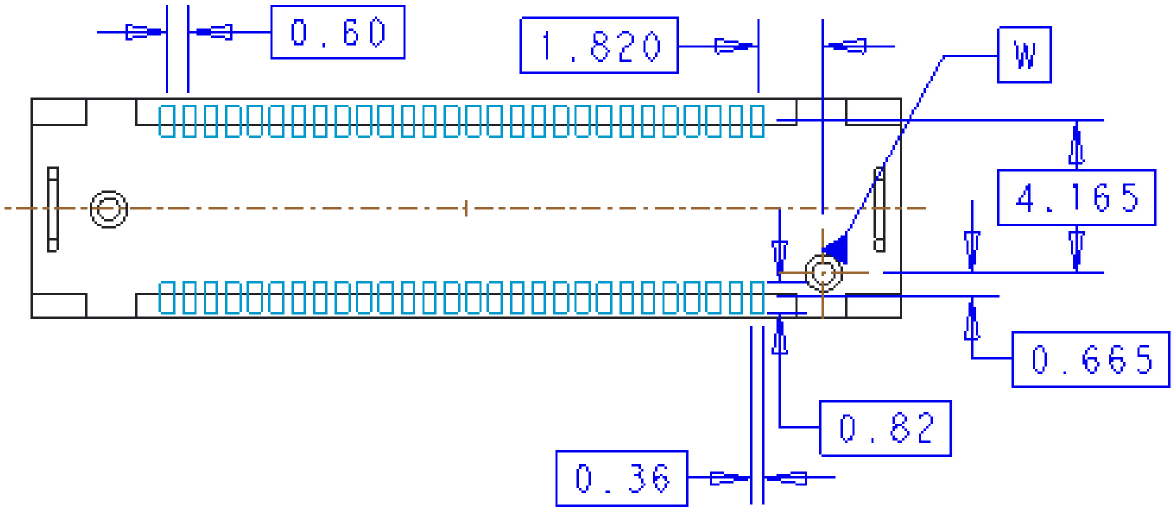


FIGURE 5-46. 1C STRAIGHT OUTER LOCUS OF CONNECTOR SMT LEADS

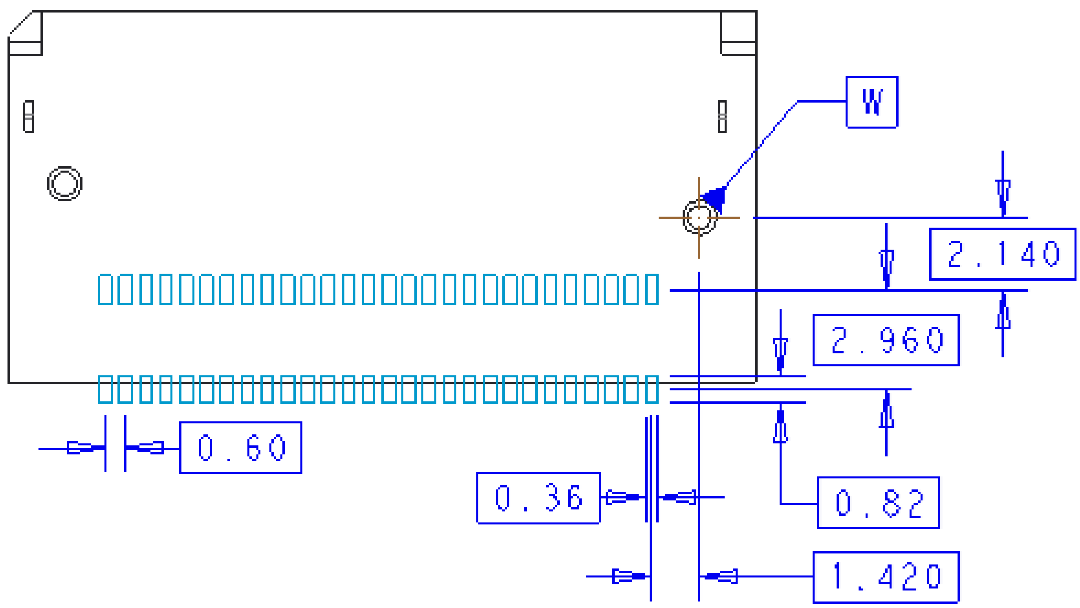


FIGURE 5-47. 1C RIGHT ANGLE OUTER LOCUS OF CONNECTOR SMT LEADS

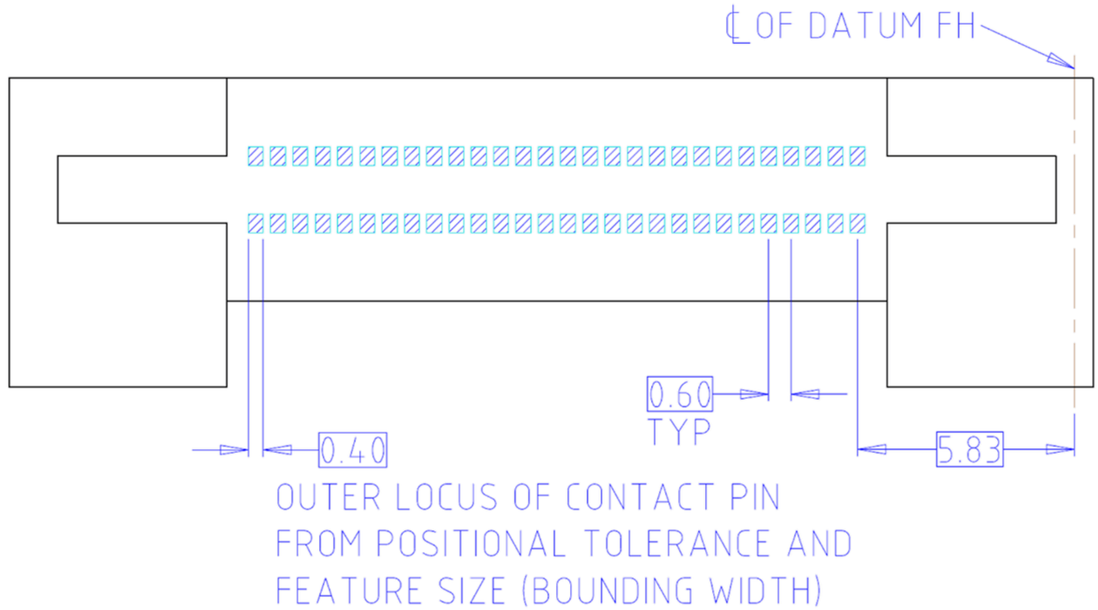


FIGURE 5-48. 1C STRADDLE MOUNT OUTER LOCUS OF CONNECTOR SMT LEADS

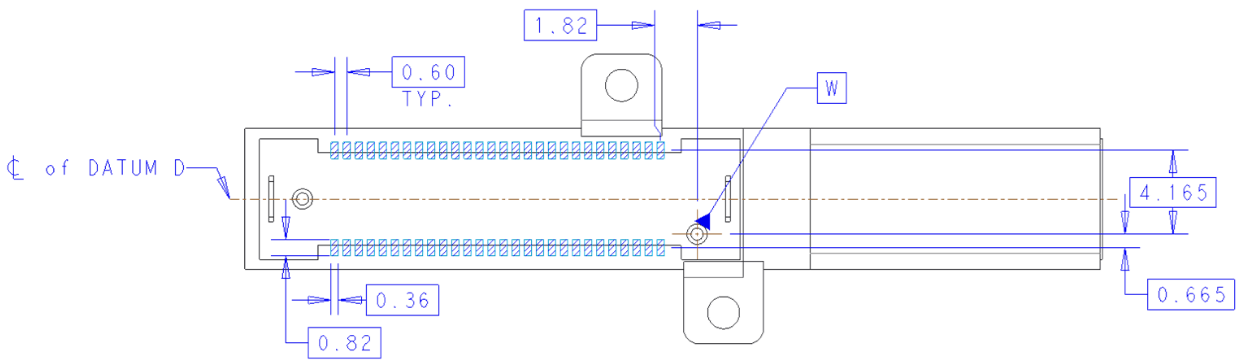


FIGURE 5-49. 1C SMT ORTHOGONAL OUTER LOCUS OF CONNECTOR SMT LEADS

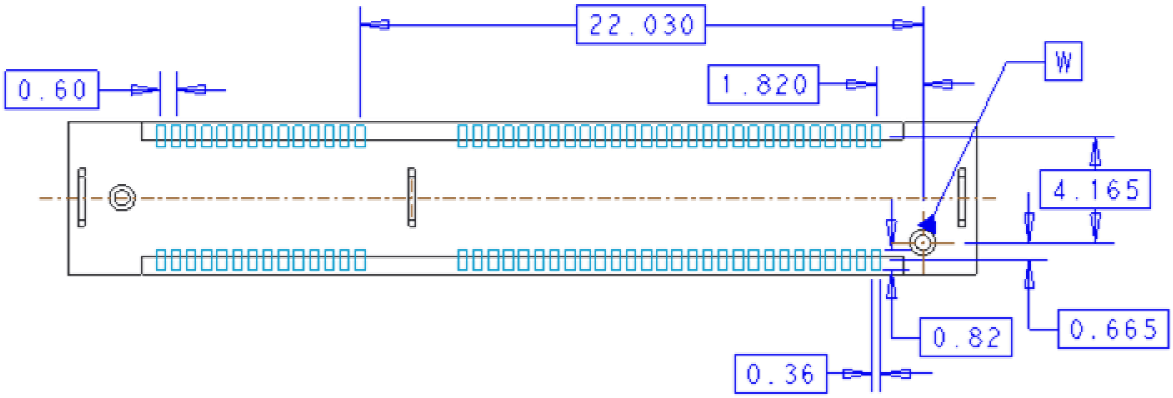


FIGURE 5-50. 2C STRAIGHT OUTER LOCUS OF CONNECTOR SMT LEADS

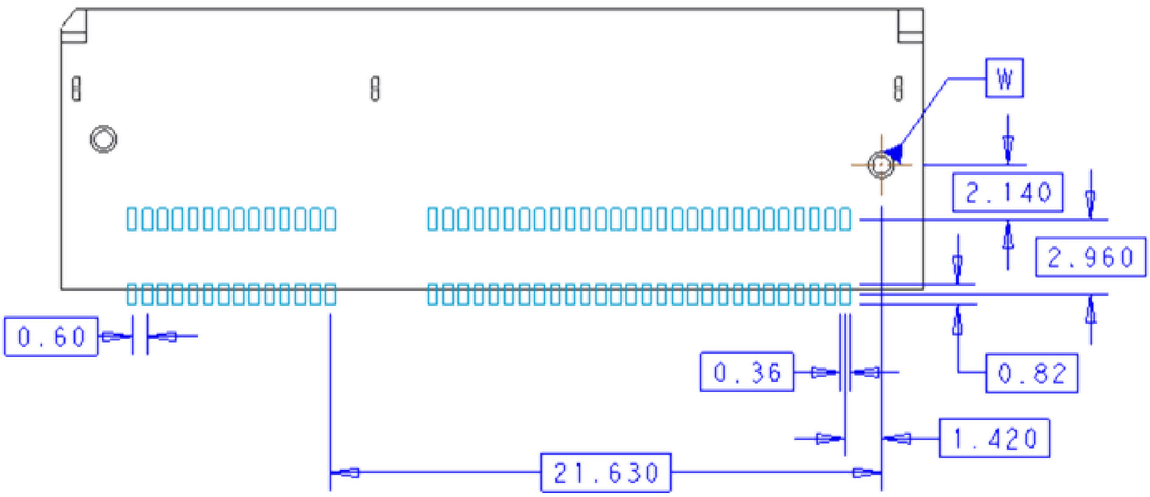


FIGURE 5-51. 2C RIGHT ANGLE OUTER LOCUS OF CONNECTOR SMT LEADS

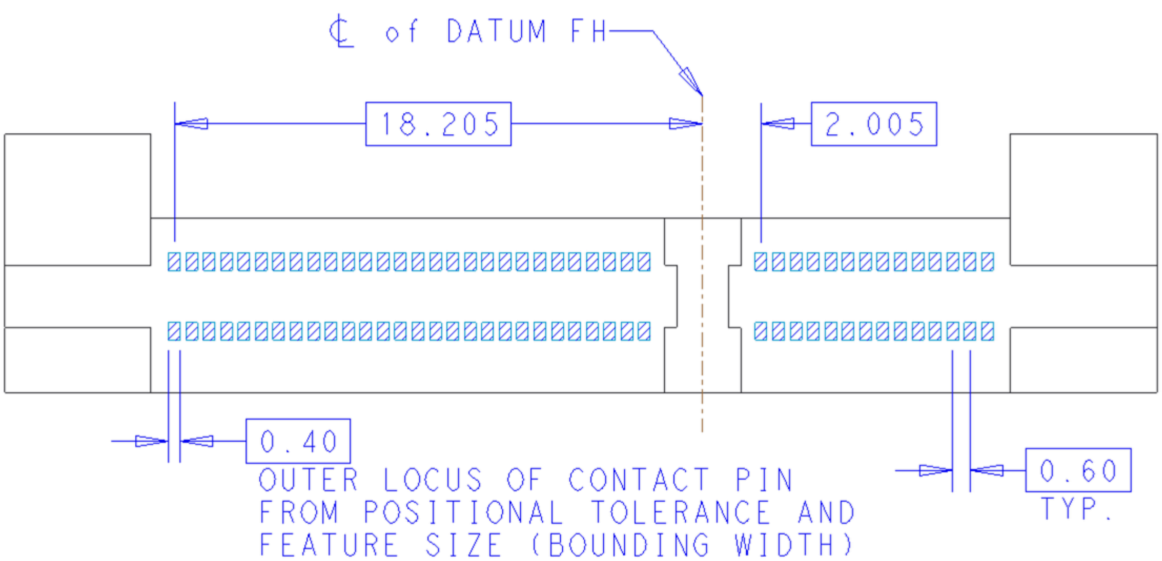


FIGURE 5-52. 2C STRADDLE MOUNT OUTER LOCUS OF CONNECTOR SMT LEADS

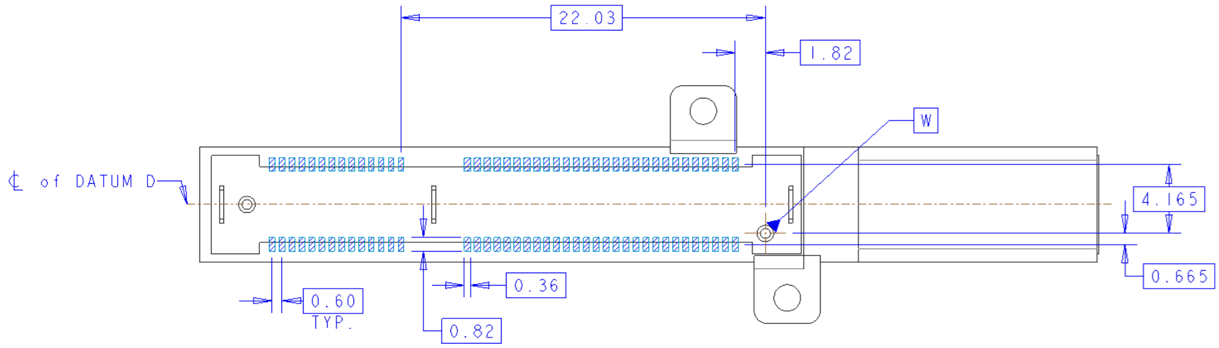


FIGURE 5-53. 2C SMT ORTHOGONAL OUTER LOCUS OF CONNECTOR SMT LEADS

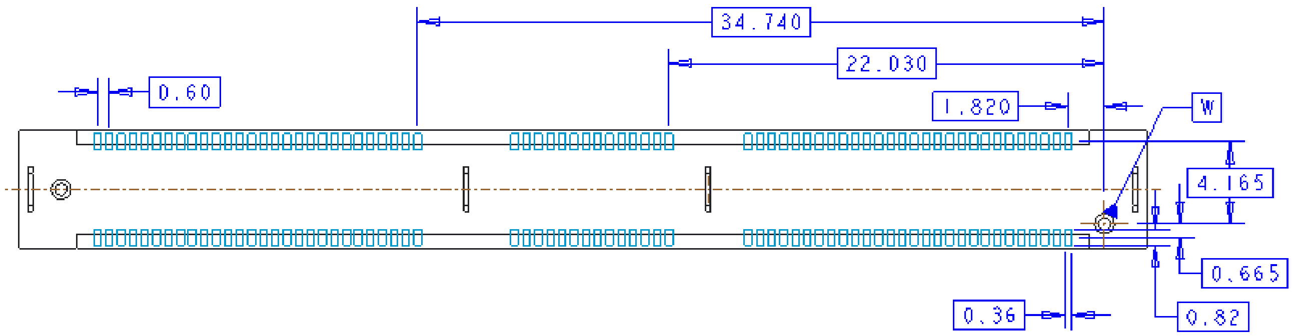


FIGURE 5-54. 4C STRAIGHT OUTER LOCUS OF CONNECTOR SMT LEADS

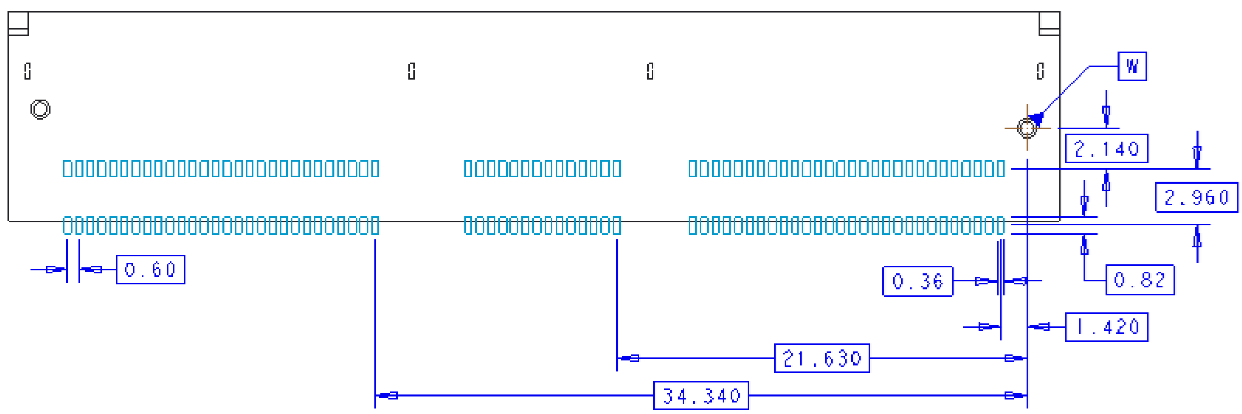


FIGURE 5-55. 4C RIGHT ANGLE OUTER LOCUS OF CONNECTOR SMT LEADS

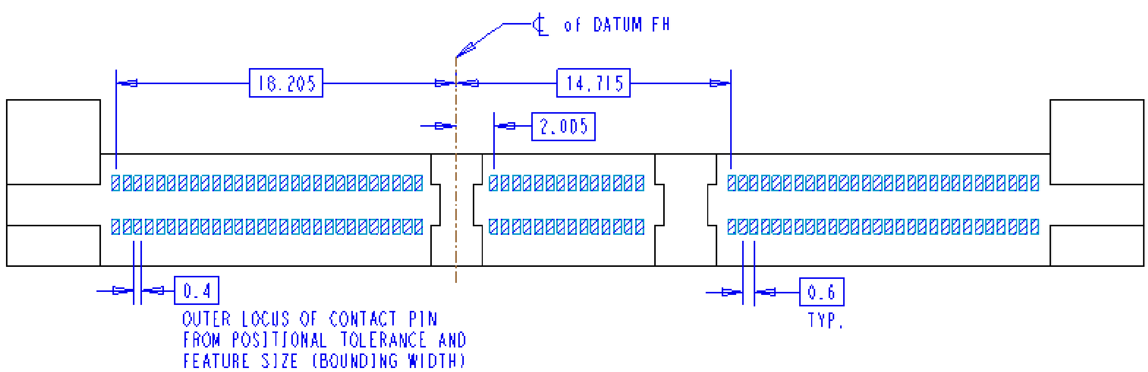


FIGURE 5-56. 4C STRADDLE MOUNT OUTER LOCUS OF CONNECTOR SMT LEADS

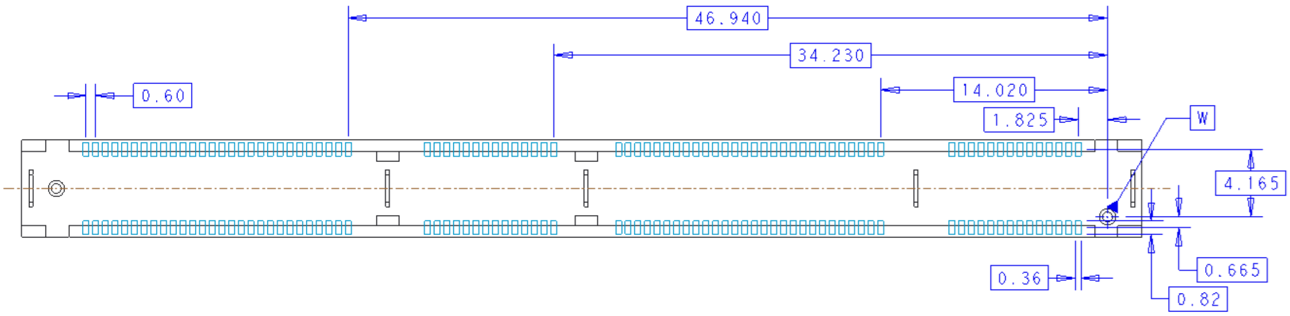


FIGURE 5-57. 4C+ STRAIGHT OUTER LOCUS OF CONNECTOR SMT LEADS

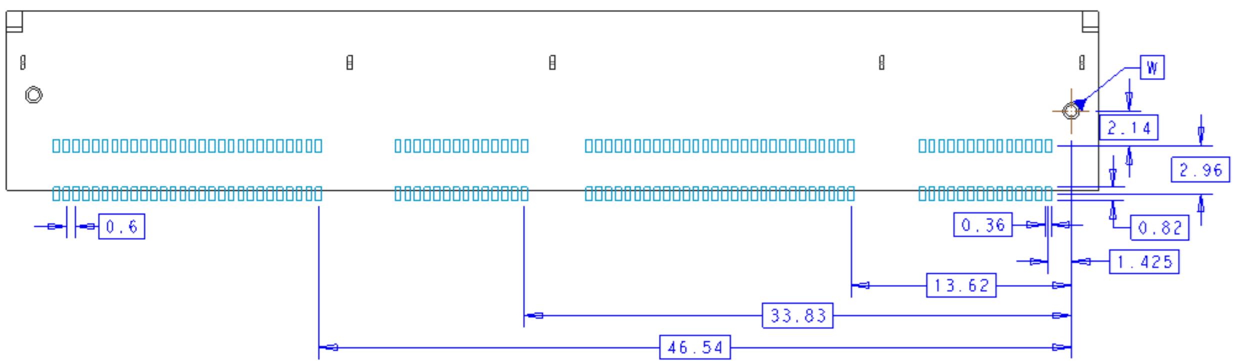


FIGURE 5-58. 4C+ RIGHT ANGLE OUTER LOCUS OF CONNECTOR SMT LEADS

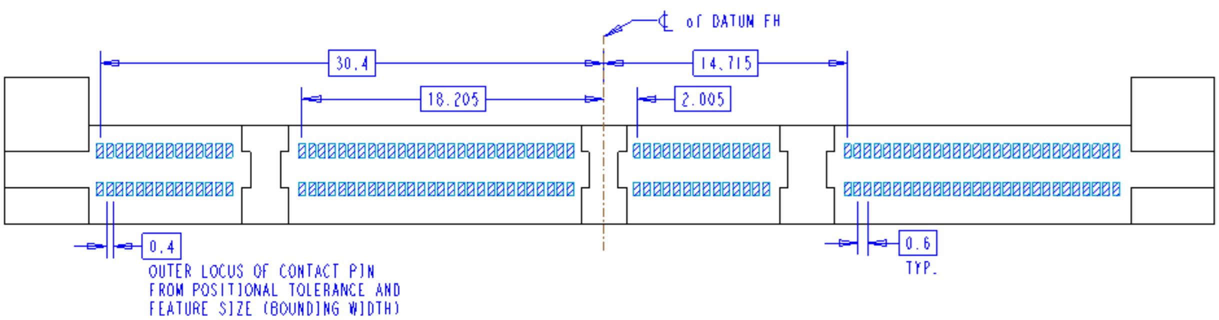


FIGURE 5-59. 4C+ STRADDLE MOUNT OUTER LOCUS OF CONNECTOR SMT LEADS

5.7 Outer Locus of Press fit Leads

Figure 5-60 through Figure 5-61 show the outer locus of the flat surfaces of the orthogonal press fit leads.

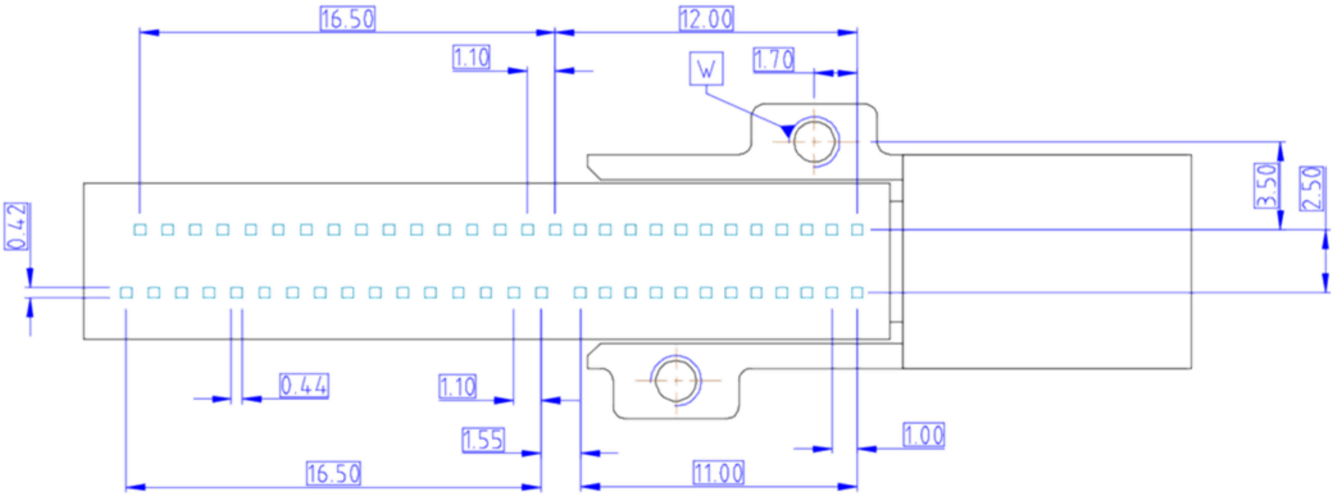


FIGURE 5-60. 1C PRESS FIT ORTHOGONAL OUTER LOCUS OF CONNECTOR LEADS

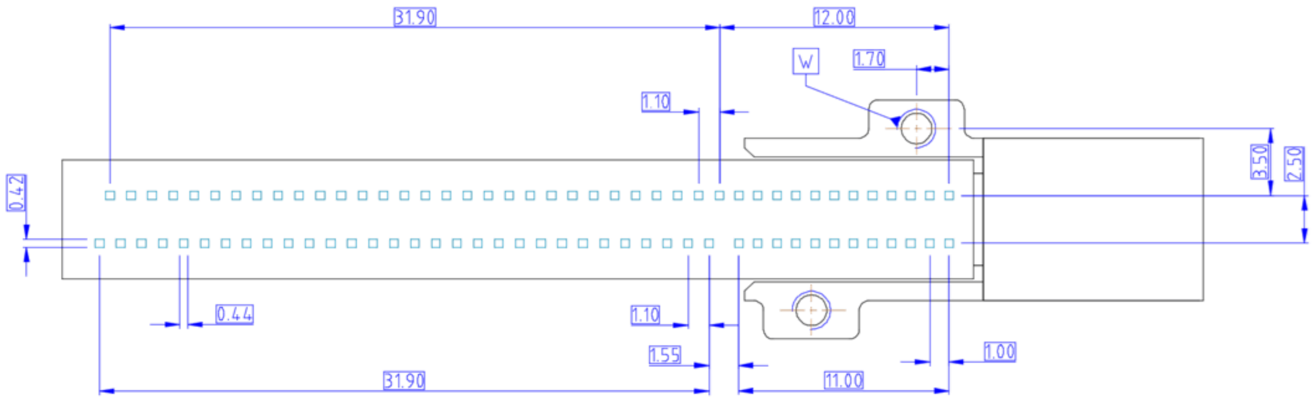


FIGURE 5-61. 2C PRESS FIT ORTHOGONAL OUTER LOCUS OF CONNECTOR LEADS

6. Performance Requirements

6.1 Mechanical Testing and Performance

The connector shall meet the mechanical testing requirements shown in Table 6-1.

TABLE 6-1. MECHANICAL TESTING REQUIREMENTS

Mechanical Test Description	Procedure	Requirement
Insertion Force (AIC to Connector)	EIA-364-13 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 25.4 mm/min. A gauge or AIC manufactured to the maximum thickness shall be used for testing purposes.	1.1 N/pin pair Maximum
Unmating Force (AIC to Connector)	EIA-364-13 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 25.4 mm/min. A gauge or AIC manufactured to the minimum thickness shall be used for testing purposes.	0.10 N/pin pair Minimum
Insertion Force (Connector to Board)	EIA-364-05 Axial Tension/Compression machine such as an Instron Tensile Tester.	SMT: 0-3 N maximum to enable pick and place Press fit: 27 N/pin maximum
Retention Force (Connector to Board, press fit only)	EIA-364-05 Axial Tension/Compression machine such as an Instron Tensile Tester.	2 N/pin minimum to remove
Durability (mating/unmating)	EIA-364-09 Use appropriate AIC. Perform required cycles for connector grade required per the table below. Plug and unplug cycles at a rate of 25.4 mm/minute, replace mating card after 25 cycles	LLCR: Refer to Table 6-9for LLCR requirements. Note: This specification intentionally deviates from EIA-364-09 procedure

TABLE 6-2. MATING CYCLES BY CONNECTOR GRADE

Connector Grade	Total Cycles
A	200
B	100
C	50

Note: To enable high durability cycles, a metal alignment key may be implemented in the connector body.

6.2 Electrical Testing and Performance

Refer to Table 6-3 for connector electrical ratings and Table 6-4 for electrical test requirements and procedures.

TABLE 6-3. CONNECTOR ELECTRICAL AND OPERATING TEMPERATURE RATINGS.

Parameter	Value	Unit	Comment
Voltage Rating per pin	29	V	Refer to Table 6-4 for testing requirements
Current Rating per pin	1.1	A	Tested per EIA 364-70, up to a maximum of 6 adjacent pins per side, 12 pins total
Temperature Rating	-40 to 85˚	C	

TABLE 6-4. ELECTRICAL TEST REQUIREMENTS AND PROCEDURES

Test Description	Requirement	Procedure
Dielectric withstanding voltage.	1 minute hold with no breakdown or flashover	EIA 364-20 Method B Test between adjacent contacts of unmated connector assemblies. Voltage: 300 VAC, Current leakage: 0.5 mA max. Note: This specification intentionally deviates from EIA 364-20 standard procedure.
Insulation resistance	1,000 MΩ minimum.	EIA 364-21 After 100 VDC for 1 minute, measure the insulation resistance between the adjacent contacts of unmated connector assemblies.

6.3 Signal Integrity Testing and Requirements

The connector shall meet the Signal Integrity requirements for all line rates specified in Table 6-5, Table 6-6, and Table 6-7. This specification does not restrict, require or define a specific impedance for the connector. The electrical requirements contained in Table 6-5, Table 6-6, and Table 6-7 are normalized to an 85 Ohm differential simulated or measured environment.   Refer to SFF-TA-1017 for test fixture specifications to measure straight connectors. Refer to SFF-TA-1018 for test fixture specifications to measure right angle connectors. Refer to SFF-TA-1019 for test fixture specifications to measure straddle mount connectors.

TABLE 6-5. STRAIGHT, RIGHT ANGLE AND STRADDLE MOUNT CONNECTOR SIGNAL INTEGRITY REQUIREMENTS (NON PCIE APPLICATIONS)

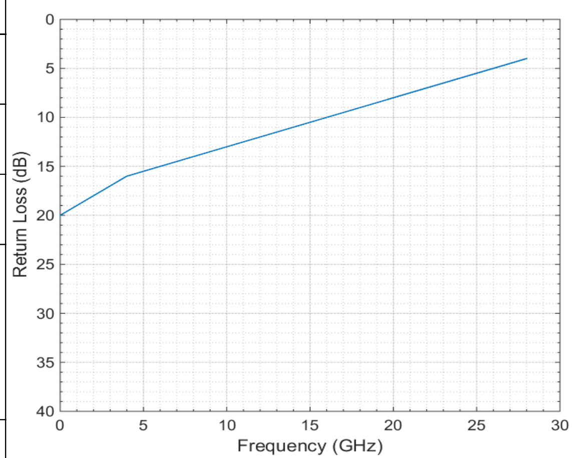
Line Rate	Insertion Loss	Return Loss	Power Sum Near End and Far End Crosstalk
25 GT/s NRZ	Loss up to 16GHz ≤ 1dB		Up to 16GHz ≤ 40dB
28 GT/s NRZ	Loss up to 16GHz ≤ 1dB		Up to 16GHz ≤ 40dB
56 GT/s PAM4	Loss up to 16GHz ≤ 1dB		Up to 16GHz ≤ 40dB
32 GT/s NRZ	Loss up to 16GHz ≤ 1dB		Up to 16GHz ≤ 40dB
56 GT/s NRZ	Loss up to 16GHz ≤ 1dB For frequency >16GHz and ≤ 28GHz. Loss up to 1.5dB		Up to 16GHz ≤ 40dB Frequency >16GHz and ≤ 28GHz. Up to 36dB
112 GT/s PAM4	Loss up to 16GHz ≤ 1dB For frequency >16GHz and ≤ 28GHz. Loss up to 1.5dB		Up to 16GHz ≤ 40dB Frequency >16GHz and ≤ 28GHz. Up to 36dB

TABLE 6-6. STRAIGHT, RIGHT ANGLE AND STRADDLE MOUNT CONNECTOR SIGNAL INTEGRITY REQUIREMENTS (PCIe APPLICATIONS)

Line Rate	Insertion Loss	Return Loss	Power Sum Near End Crosstalk	Power Sum Far End Crosstalk	Intrapair Skew
8 GT/s NRZ (PCIe 3.0)	See 32GT/s NRZ values from Table 6-5				
16 GT/s NRZ (PCIe 4.0)	See 32GT/s NRZ values from Table 6-5				
32 GT/s NRZ (PCIe 5.0)	See 32GT/s NRZ values from Table 6-5				
64 GT/s PAM4 (PCIe 6.0)	≥(-0.1–0.040625*f)dB (0.01≤f≤16 GHz) ≥(1.75-0.15625*f)dB (16<f≤24 GHz)	≤(-25+0.625*f)dB (0.01≤f≤24 GHz) iRL[1,4] ≤ -28 dB	≤(-65+0.625*f)dB (0.01≤f≤24 GHz) ccICN$_{NEXT}$[2] ≤ 149uV	≤(-70+3.75*f)dB (0.01≤f≤4 GHz) ≤(-58+0.75*f)dB (4≤f≤24 GHz) Straight: ccICN$_{FEXT}$[3] ≤ 110uV Right Angle and Straddle mount: ccICN$_{FEXT}$[3] ≤ 125uV	≤0.2 ps[5]

Notes:

1. Integrated Return Loss (iRL) is an excursion allowance that should only be measured if the Return Loss spec is violated. If Return Loss passes then no iRL measurement is needed. If Return Loss fails but iRL passes then Return Loss is considered passing. See Equation 6-1 for how to calculate iRL.
2. ccICN$_{NEXT}$ is an excursion allowance that should only be measured if the Power Sum Near End Crosstalk spec fails. If Power Sum Near End Crosstalk passes then no ccICN$_{NEXT}$ measurement is needed. If Power Sum Near End Crosstalk fails but ccICN$_{NEXT}$ passes then Power Sum Near End Crosstalk is considered passing. See Equation 6-2 for how to calculate ccICN$_{NEXT}$.
3. ccICN$_{FEXT}$ is an excursion allowance that should only be measured if the Power Sum Far End Crosstalk spec fails. If Power Sum Far End Crosstalk passes then no ccICN$_{FEXT}$ measurement is needed. If Power Sum Far End Crosstalk fails but ccICN$_{FEXT}$ passes then Power Sum Far End Crosstalk is considered passing. See Equation 6-3 for how to calculate ccICN$_{FEXT}$. Excursions of PSFEXT shall not deviate PSFEXT by more than 4db with a frequency span less than 2 GHz.
4. Nyquist frequency: 16 GHz for PCIe 6.0
5. Measurement not required. Evaluated through simulation using EIPS method documented in Appendix E.

EQUATION 6-1. INTEGRATED RETURN LOSS (iRL) CALCULATION

$$iRL = \mathrm{dB}\left(\sqrt{\frac{1}{N}\sum_{i=1}^{N} W(f_i) RL_{avg}^2(f_i)}\right)$$

1. $RL_{avg}(fi) = (|RL_{11}(fi)| + |RL_{22}(fi)|)/2$
2. $RL_{11}(f)$, $RL_{22}(f)$ = connector return loss
3. Weighting Function $W(fi) = sinc^2(\frac{f_i}{f_b})\frac{1}{1+(\frac{f_i}{f_t})^4 * (\frac{f_i}{f_r})^8}$
4. f_b = 32 GHz for PCIe 6.0
5. f_t = 9.46 GHz, (where $f_t = \frac{0.2365}{Tr}$; rise time (T_r)=25ps)

6. f_r = 1.5 x Nyquist frequency
7. N = Number of samples, length of frequency array, in 10 MHz steps)

EQUATION 6-2. COMPONENT CONTRIBUTED INTEGRATED CROSSTALK NOISE FOR NEAR END CROSSTALK (ccICN$_{NEXT}$) CALCULATION

$$ccICN_{NEXT} = \sqrt{\frac{1}{2}df\sum_{k=1}^{Nmax}\sigma_x^2\,(\frac{A_{NT}^2}{f_b})sinc^2(k*\frac{df}{f_b})10^{(2\frac{IL_{post-channel}(k)}{10})}\left[\frac{1}{1+(\frac{k*df}{f_t})^4}\right]\left[\frac{1}{1+(\frac{k*df}{f_r})^8}\right]10^{\frac{MDNEXT(k)}{10}}}$$

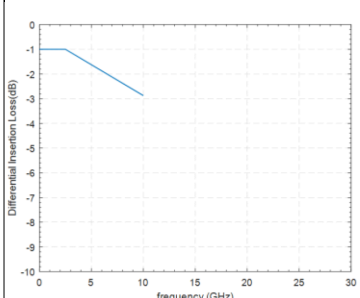
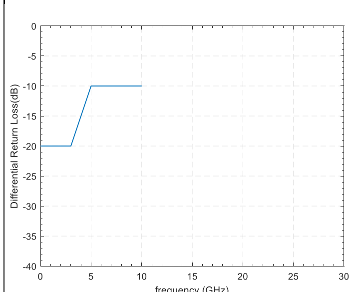
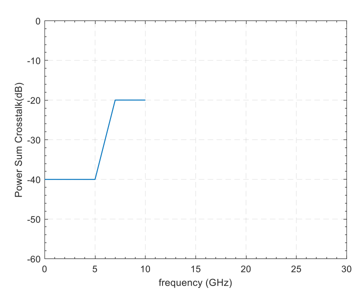
1. $IL_{post-channel}$ = -6dB @ Nyquist frequency, $IL_{post-channel}(f) = -(\frac{6}{f_b/2})f$
2. Frequency sweep for function = 0.01 GHz to 1.5*Nyquist in 0.01 GHz steps (e.g., k = 0.01 GHz, Nmax = 2400 for PCIe 6.0)
3. A_{NT}=1000 mVpp (differential peak to peak voltage)
4. f_t=31.53 GHz, f_r= 1.5*Nyquist (where f_t = 0.2365/ T_r; T_r=7.5ps)
5. $\boldsymbol{\sigma_x^2}$ = scaling factor = 5/9
6. sinc function definition in these equations is normalized sinc function (sinc(x) = sin(pi*x)/(pi*x))
7. $MDNEXT(k) = 10\log_{10}(\sum_{i=1}^{3} 10^{PSNEXT_i/10})$

EQUATION 6-3. COMPONENT CONTRIBUTED INTEGRATED CROSSTALK NOISE FOR FAR END CROSSTALK (ccICN$_{FEXT}$) CALCULATION

$$ccICN_{FEXT} = \sqrt{\frac{1}{2}df\sum_{k=1}^{Nmax}\sigma_x^2\,(\frac{A_{FT}^2}{f_b})sinc^2(k*\frac{df}{f_b})10^{(\frac{IL_{pre-channel}(k)}{10}+\frac{IL_{post-channel}(k)}{10})}\left[\frac{1}{1+(\frac{k*df}{f_t})^4}\right]\left[\frac{1}{1+(\frac{k*df}{f_r})^8}\right]10^{\frac{MDFEXT(k)}{10}}}$$

1. $IL_{pre-channel}$ = -25.25dB @ Nyquist, $IL_{post-channel}(f) = -(\frac{25.25}{f_b/2})f$
2. $IL_{post-channel}$ = -6dB @ Nyquist, $IL_{post-channel}(f) = -(\frac{6}{f_b/2})f$
3. Frequency sweep for function = 0.01 GHz to 1.5*Nyquist in 0.01 GHz steps (e.g., k = 0.01 GHz, Nmax = 2400 for PCIe 6.0)
4. A_{FT}=800 mVpp (differential peak to peak voltage)
5. f_t=31.53 GHz, f_r=1.5*Nyquist (where f_t = 0.2365/ T_r; T_r=7.5ps)
6. $\boldsymbol{\sigma_x^2}$ = scaling factor = 5/9
7. sinc function definition in these equations is normalized sinc function (sinc(x) = sin(pi*x)/(pi*x))
8. $MDFEXT(k) = 10\log_{10}(\sum_{i=1}^{2} 10^{PSFEXT_i/10})$

TABLE 6-7. ORTHOGONAL (SMT AND PRESS FIT) CONNECTOR SIGNAL INTEGRITY REQUIREMENTS ONLY

	Insertion Loss	Return Loss	Power Sum Near End Crosstalk	Power Sum Far End Crosstalk	Intra-pair Skew
Line Rate 16GT/s NRZ					5ps Max

Line Rate 32 GT/s NRZ	-0.8–0.1375*f dB (0≤f≤16 GHz) 3–0.375*f dB (16≤f≤24 GHz)	-20+f dB (0≤f≤4 GHz) -18.2+0.55*f dB (4≤f≤16 GHz) -27+1.1*f dB (16≤f≤20 GHz) -5 dB (20≤f≤24 GHz)	-50+1.25*f dB (0≤f≤8 GHz) -40 dB (8≤f≤16 GHz) -53.3+0.83*f dB (16≤f≤24 GHz)	-50+1.25*f dB (0≤f≤8 GHz) -40 dB (8≤f≤16 GHz) -60+1.25*f dB (16≤f≤24 GHz)	2 ps Max
Procedure	EIA 364-101 The measured differential S parameter shall be referenced to an 85Ω differential impedance.	EIA 364-108 The measured differential S parameter shall be referenced to an 85Ω differential impedance.	EIA 364-90 The measured differential S parameter shall be referenced to an 85Ω differential impedance.	EIA 364-90 The measured differential S parameter shall be referenced to an 85Ω differential impedance.	Intra-pair skew shall be achieved through EIPS measurement method documented in Appendix E

6.4 Reliability Testing and Requirements

Table 6-8 shows the testing order required to validate the connectors developed with this specification per five EIA 364-1000 test groups for 3, 5, or 7-year life cycle requirements. Five samples shall be tested per group.

TABLE 6-8. RELIABILITY TEST SEQUENCE

Test	**Test Group**				
	1	**2**	**3**	**4**	**5**
Low Level Contact Resistance	1,4,6	1,4,6,8	1,3,5,7	1,4,6,8,10	2,4
Dielectric withstanding voltage					1,5
Reseating	5	7		9	
Vibration			4		
Mechanical Shock			6		
Durability (preconditioning)	2	2	2	2	
Temperature Life	3				3
Temperature Life (preconditioning)				3	
Thermal Shock		3			
Cyclic Temp and Humidity		5			
Mixed Flowing Gas				5	
Thermal Disturbance				7	

TABLE 6-9. RELIABILITY TEST CONDITIONS

Reliability Test Description	Procedure	Requirement
Durability (preconditioning)	Refer to EIA 364-1000 for requirements	No evidence of physical damage
Temperature Life Temperature Life (preconditioning)	EIA-364-17, Method A (without electrical load) Test Temperature and Test Duration per EIA 364-1000 Table 8 Test Temperature and Test Duration per EIA 364-1000 Table 9	Electrical, mechanical and environmental criteria
Low Level Contact Resistance (LLCR)	EIA-364-23 (termination of connector to board carrier shall be included in the measurements)	Delta: 15mΩ MAX
Mechanical Shock	EIA-364-27, Test Condition A Alternately, for DIMM applications, Trapezoidal shock 50 G, ± 10% Duration 11 ms Velocity change 170 inch/sec, ± 10% Three drops in each of six directions are applied to each of the samples Shock and Vibration board design should have proper footprint to mate to the connector and test equipment and not produce resonances across the test frequency profile. Further design details are the discretion of the implementer of the test.	Electrical, mechanical and environmental criteria

Reliability Test Description	Procedure	Requirement
Vibration	EIA-364-28 Test Condition D Random profile: 5 Hz @ 0.01 g2/Hz to 20 Hz @ 0.02 g2/Hz (slope up) 20 Hz to 500 Hz @ 0.02 g2/Hz (flat) Input acceleration is 3.13 g RMS 10 minutes per axis for all 3 axes on all samples Random control limit tolerance is ± 3 dB Shock and Vibration board design should have proper footprint to mate to the connector and test equipment and not produce resonances across the test frequency profile. Further design details are the discretion of the implementer of the test.	No discontinuities of ≥ 1 microsecond electrical, mechanical and environmental criteria
Cyclic Temperature and Humidity	EIA-364-31B, Method III without conditioning, initial measurements, cold shock and vibration. Ramp times should be 0.5 hour and dwell times should be 1.0 hour. Dwell times start when the temperature and humidity have stabilized within specified levels, perform 24 cycles in mated condition.	Electrical, mechanical and environmental criteria
Thermal Shock	EIA-364-32, Method A, Table 2, Test Condition 1, -55 ˚C to 85 ˚C, perform 5 cycles in mated condition	Electrical, mechanical and environmental criteria
Thermal Disturbance	EIA-364-1000 Cycle the connector between 15 ±3 ˚C and 85 ±3 ˚C, as measured on the part. Ramps should be a minimum of 2 ˚C/minute. Dwell times should ensure that the contacts reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled; perform 10 cycles in mated condition.	Electrical, mechanical and environmental criteria
Mixed Flowing Gas	EIA-364-65, class IIA, Option 4. Expose all specimens in the mated condition for the total mixed flowing gas exposure duration per Table 4.	Electrical, mechanical and environmental criteria
Reseating	Manually unplug/plug the connector. Perform 3 cycles	No evidence of physical damage

6.5 Manufacturability Testing and Requirements

Table 6-8 shows the testing required to validate the connectors developed with this specification meet common manufacturing criteria in the electronics industry. The test details shown here are for reference. It is recommended that the connector body be narrowed above the SMT leads to allow for visual inspection of solder joints.

TABLE 6-10. RELIABILITY TEST CONDITIONS

Manufacturing Test Description	Procedure	Requirement
Solderability - Lead Free	J-STD-002D; Condition C, 8 hours ± 15 minutes steam precondition.	95% coverage minimum
Lead Free Process ability	260 ˚C, 5 seconds.	No physical damage to connector per visual inspection at 24 inches. No magnification
Electronic Assembly Rework, Repair, and Modification Procedures	IPC-7711/7721: Rework, Repair and Modification of Electronic Assemblies	Meets Class 2, Highest Level of Conformance (section 1.5.1)
Electronic Assembly Materials, Methods, and Acceptance Criteria	IPC J-STD-001: Requirements for Soldered Electrical and Electronic Assemblies	Meets Class 2 Acceptance criteria, Dedicated Service Electronic Products (section 1.3)

7. Pin Geometry Pattern

As stated in section 4, the connector supports multiple types depending on if grounds need to be tied together for improved signal performance. The tables below only describe which pins use a “signal” geometry, which pins use a “GND” geometry, and which pins are Power or Control(“PWRCTL”), if and only if the geometry of those pins is different and does not define a functional pin out.

Type 1 connector is defined in Table 7-1 below. If a connector implementation uses different pin geometry between ground pins and high speed signal pins, the connector shall follow the GSSGSSG pattern defined.

TYPE 2 CONNECTOR WITH GROUNDS TIED TOGETHER IS DEFINED IN TABLE 7-2 BELOW.TABLE 7-1. TYPE 1 PIN GEOMETRY PATTERN FOR 1C, 2C, 4C, AND 4C+ CONNECTORS

Row	Side A	Side B	Connector Variation
O1	GND	GND	4C+ Connector (rows O1–70)
O2	SIGNAL	SIGNAL	
O3	SIGNAL	SIGNAL	
O4	GND	GND	
O5	SIGNAL	SIGNAL	
O6	SIGNAL	SIGNAL	
O7	GND	GND	
O8	SIGNAL	SIGNAL	
O9	SIGNAL	SIGNAL	
O10	GND	GND	
O11	SIGNAL	SIGNAL	
O12	SIGNAL	SIGNAL	
O13	GND	GND	
O14	GND	GND	
KEY			
1	GND	GND	1C Connector (rows 1–28); 2C Connector (rows 1–42); 4C Connector (rows 1–70)
2	SIGNAL	SIGNAL	
3	SIGNAL	SIGNAL	
4	GND	GND	
5	SIGNAL	SIGNAL	
6	SIGNAL	SIGNAL	
7	GND	GND	
8	SIGNAL	SIGNAL	
9	SIGNAL	SIGNAL	
10	GND	GND	
11	SIGNAL	SIGNAL	
12	SIGNAL	SIGNAL	
13	GND	GND	
14	SIGNAL	SIGNAL	
15	SIGNAL	SIGNAL	
16	GND	GND	
17	SIGNAL	SIGNAL	
18	SIGNAL	SIGNAL	
19	GND	GND	
20	SIGNAL	SIGNAL	
21	SIGNAL	SIGNAL	
22	GND	GND	
23	SIGNAL	SIGNAL	
24	SIGNAL	SIGNAL	
25	GND	GND	
26	SIGNAL	SIGNAL	
27	SIGNAL	SIGNAL	
28	GND	GND	
KEY			
29	GND	GND	
30	SIGNAL	SIGNAL	
31	SIGNAL	SIGNAL	
32	GND	GND	
33	SIGNAL	SIGNAL	
34	SIGNAL	SIGNAL	
35	GND	GND	
36	SIGNAL	SIGNAL	
37	SIGNAL	SIGNAL	
38	GND	GND	
39	SIGNAL	SIGNAL	
40	SIGNAL	SIGNAL	
41	GND	GND	
42	GND	GND	
KEY			
43	GND	GND	
44	SIGNAL	SIGNAL	
45	SIGNAL	SIGNAL	
46	GND	GND	
47	SIGNAL	SIGNAL	
48	SIGNAL	SIGNAL	
49	GND	GND	
50	SIGNAL	SIGNAL	
51	SIGNAL	SIGNAL	
52	GND	GND	
53	SIGNAL	SIGNAL	
54	SIGNAL	SIGNAL	
55	GND	GND	
56	SIGNAL	SIGNAL	
57	SIGNAL	SIGNAL	
58	GND	GND	
59	SIGNAL	SIGNAL	
60	SIGNAL	SIGNAL	
61	GND	GND	
62	SIGNAL	SIGNAL	
63	SIGNAL	SIGNAL	
64	GND	GND	
65	SIGNAL	SIGNAL	
66	SIGNAL	SIGNAL	
67	GND	GND	
68	SIGNAL	SIGNAL	
69	SIGNAL	SIGNAL	
70	GND	GND	

TABLE 7-2. TYPE 2 PIN GEOMETRY PATTERN FOR 1C, 2C, 4C, AND 4C+ CONNECTORS

Row	Side A	Side B	Connector Variation			
O1	PWR/CTL	PWR/CTL				4C+ Connector
O2	PWR/CTL	PWR/CTL				
O3	PWR/CTL	PWR/CTL				
O4	PWR/CTL	PWR/CTL				
O5	PWR/CTL	PWR/CTL				
O6	PWR/CTL	PWR/CTL				
O7	PWR/CTL	PWR/CTL				
O8	PWR/CTL	PWR/CTL				
O9	PWR/CTL	PWR/CTL				
O10	PWR/CTL	PWR/CTL				
O11	PWR/CTL	PWR/CTL				
O12	PWR/CTL	PWR/CTL				
O13	PWR/CTL	PWR/CTL				
O14	PWR/CTL	PWR/CTL				
Key						
1	PWR/CTL	PWR/CTL	1C Connector	2C Connector	4C Connector	
2	PWR/CTL	PWR/CTL				
3	PWR/CTL	PWR/CTL				
4	PWR/CTL	PWR/CTL				
5	PWR/CTL	PWR/CTL				
6	PWR/CTL	PWR/CTL				
7	PWR/CTL	PWR/CTL				
8	PWR/CTL	PWR/CTL				
9	PWR/CTL	PWR/CTL				
10	PWR/CTL	PWR/CTL				
11	PWR/CTL	PWR/CTL				
12	PWR/CTL	PWR/CTL				
13	PWR/CTL	PWR/CTL				
14	PWR/CTL	PWR/CTL				
15	PWR/CTL	PWR/CTL				
16	GND	GND				
17	SIGNAL	SIGNAL				
18	SIGNAL	SIGNAL				
19	GND	GND				
20	SIGNAL	SIGNAL				
21	SIGNAL	SIGNAL				
22	GND	GND				
23	SIGNAL	SIGNAL				
24	SIGNAL	SIGNAL				
25	GND	GND				
26	SIGNAL	SIGNAL				
27	SIGNAL	SIGNAL				
28	GND	GND				
Key						
29	GND	GND				
30	SIGNAL	SIGNAL				
31	SIGNAL	SIGNAL				
32	GND	GND				
33	SIGNAL	SIGNAL				
34	SIGNAL	SIGNAL				
35	GND	GND				
36	SIGNAL	SIGNAL				
37	SIGNAL	SIGNAL				
38	GND	GND				
39	SIGNAL	SIGNAL				
40	SIGNAL	SIGNAL				
41	GND	GND				
42	PWR/CTL	PWR/CTL				
Key						
43	GND	GND				
44	SIGNAL	SIGNAL				
45	SIGNAL	SIGNAL				
46	GND	GND				
47	SIGNAL	SIGNAL				
48	SIGNAL	SIGNAL				
49	GND	GND				
50	SIGNAL	SIGNAL				
51	SIGNAL	SIGNAL				
52	GND	GND				
53	SIGNAL	SIGNAL				
54	SIGNAL	SIGNAL				
55	GND	GND				
56	SIGNAL	SIGNAL				
57	SIGNAL	SIGNAL				
58	GND	GND				
59	SIGNAL	SIGNAL				
60	SIGNAL	SIGNAL				
61	GND	GND				
62	SIGNAL	SIGNAL				
63	SIGNAL	SIGNAL				
64	GND	GND				
65	SIGNAL	SIGNAL				
66	SIGNAL	SIGNAL				
67	GND	GND				
68	PWR/CTL	PWR/CTL				
69	PWR/CTL	PWR/CTL				
70	PWR/CTL	PWR/CTL				

Appendix A. Mating Sequence

The connector receptacle has one stage of mating. First mate last break functionality is achieved with the Level 1 and Level 2 Sequencing on the AIC mating pads as indicated in Table A-1. The AIC mating positions below are an example implementation.

TABLE A-1. CONTACT MATING POSITIONS FOR 1C, 2C, 4C AND 4C+ CONNECTORS

Row	AIC Plug (Free)	Receptacle (Fixed)	Row	Row	AIC Plug (Free)	Receptacle (Fixed)	Row
OA1			OA1	OB1			OB1
OA2			OA2	OB2			OB2
OA3			OA3	OB3			OB3
OA4			OA4	OB4			OB4
OA5			OA5	OB5			OB5
OA6			OA6	OB6			OB6
OA7			OA7	OB7			OB7
OA8			OA8	OB8			OB8
OA9			OA9	OB9			OB9
OA10			OA10	OB10			OB10
OA11			OA11	OB11			OB11
OA12			OA12	OB12			OB12
OA13			OA13	OB13			OB13
OA14			OA14	OB14			OB14
KEY		KEY		KEY		KEY	
A1			A1	B1			B1
A2			A2	B2			B2
A3			A3	B3			B3
A4			A4	B4			B4
A5			A5	B5			B5
A6			A6	B6			B6
A7			A7	B7			B7
A8			A8	B8			B8
A9			A9	B9			B9
A10			A10	B10			B10
A11			A11	B11			B11
A12			A12	B12			B12
A13			A13	B13			B13
A14			A14	B14			B14
A15			A15	B15			B15
A16			A16	B16			B16
A17			A17	B17			B17
A18			A18	B18			B18
A19			A19	B19			B19
A20			A20	B20			B20
A21			A21	B21			B21
A22			A22	B22			B22
A23			A23	B23			B23
A24			A24	B24			B24
A25			A25	B25			B25
A26			A26	B26			B26
A27			A27	B27			B27
A28			A28	B28			B28
KEY		KEY		KEY		KEY	

A29			A29	B29			B29
A30			A30	B30			B30
A31			A31	B31			B31
A32			A32	B32			B32
A33			A33	B33			B33
A34			A34	B34			B34
A35			A35	B35			B35
A36			A36	B36			B36
A37			A37	B37			B37
A38			A38	B38			B38
A39			A39	B39			B39
A40			A40	B40			B40
A41			A41	B41			B41
A42			A42	B42			B42
	KEY	KEY			KEY	KEY	
A43			A43	B43			B43
A44			A44	B44			B44
A45			A45	B45			B45
A46			A46	B46			B46
A47			A47	B47			B47
A48			A48	B48			B48
A49			A49	B49			B49
A50			A50	B50			B50
A51			A51	B51			B51
A52			A52	B52			B52
A53			A53	B53			B53
A54			A54	B54			B54
A55			A55	B55			B55
A56			A56	B56			B56
A57			A57	B57			B57
A58			A58	B58			B58
A59			A59	B59			B59
A60			A60	B60			B60
A61			A61	B61			B61
A62			A62	B62			B62
A63			A63	B63			B63
A64			A64	B64			B64
A65			A65	B65			B65
A66			A66	B66			B66
A67			A67	B67			B67
A68			A68	B68			B68
A69			A69	B69			B69
A70			A70	B70			B70

Appendix B. Gatherability

Figure B-1 and Figure B-2 show the linear and angular gatherability of the connector. Figure B-3 shows the mechanical keying for the 4C connector.

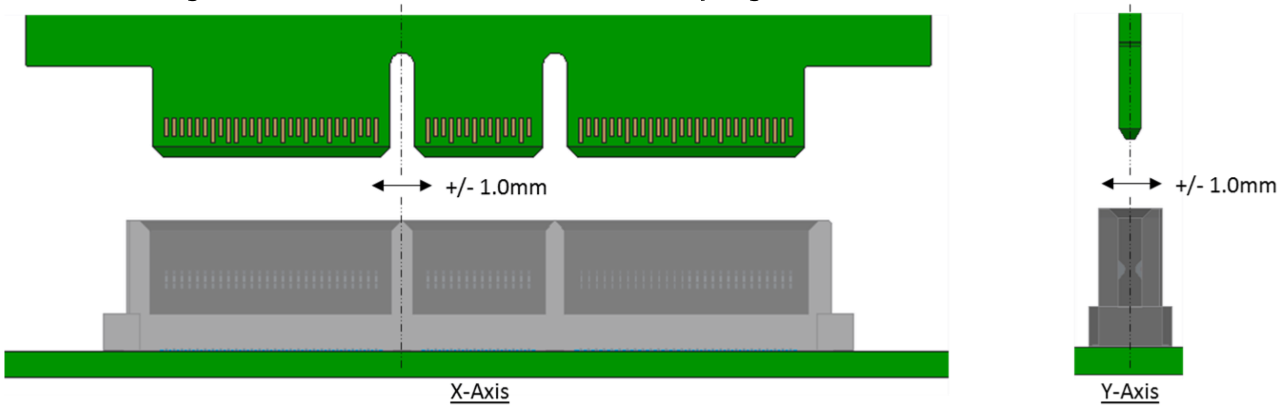


FIGURE B-1. LINEAR GATHERABILITY.

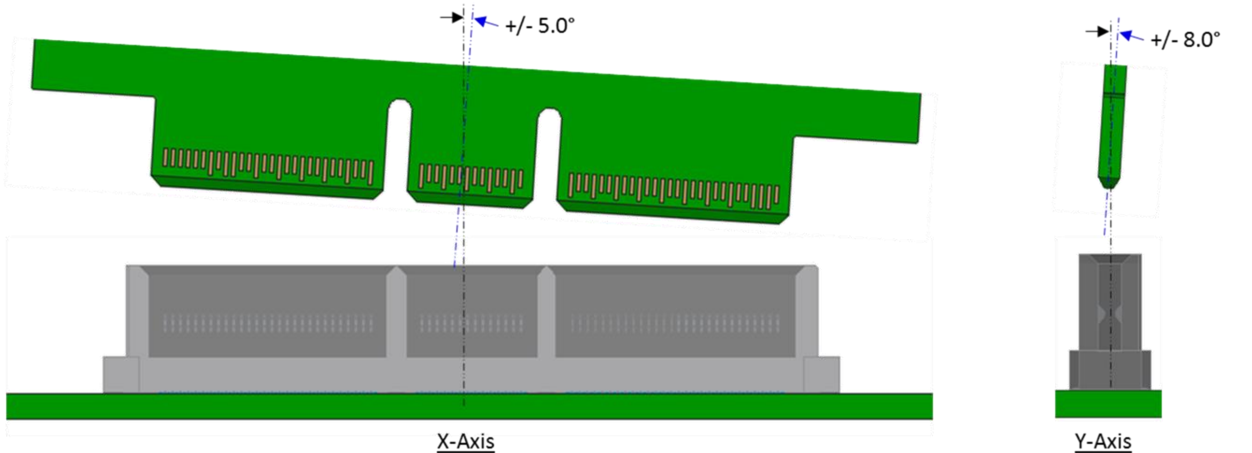


FIGURE B-2. ANGULAR GATHERABILITY.

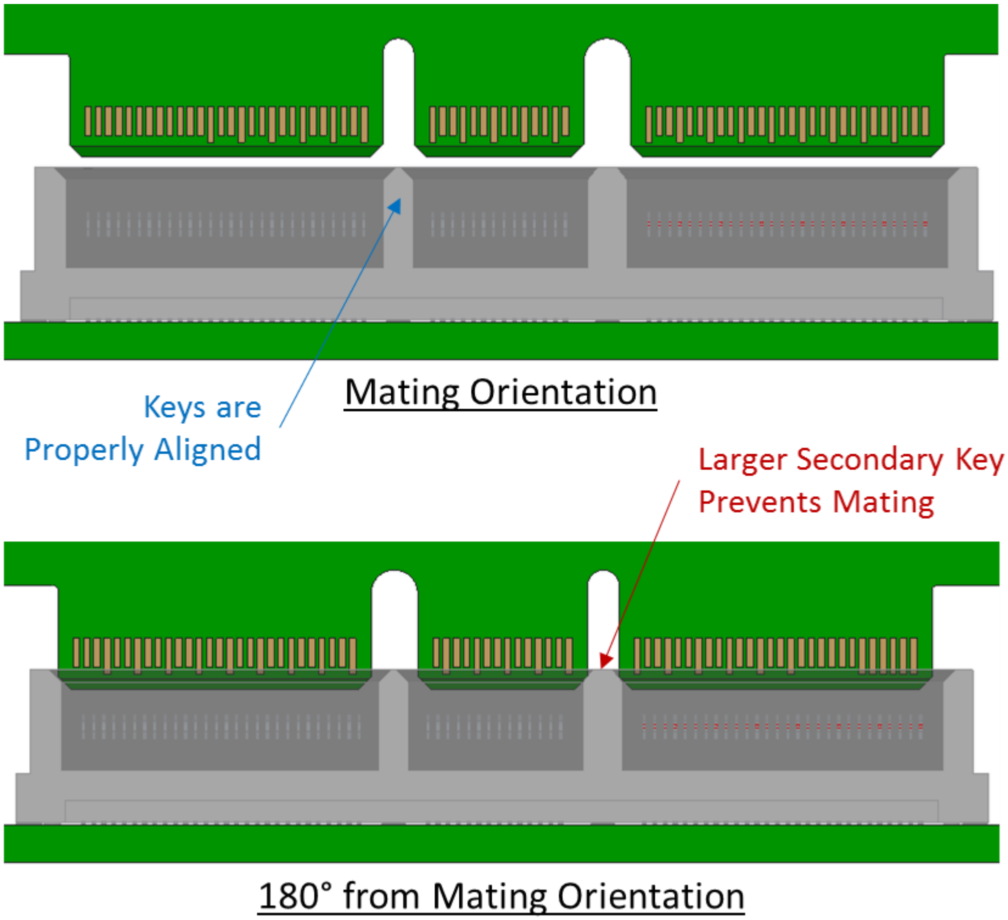


FIGURE B-3. MECHANICAL KEYING.

Appendix C. Printed Circuit Board Footprints

Included PCB layouts are informative to provide a common connector mounting interface to the host board to enable multi-sourcing of the connector while ensuring electrical performance.

This specification is not intended to address the electrical performance characteristics of the host Printed Circuit Board (PCB) material and construction used in these applications. The PCB thickness, number of layers, layer stack up, trace layer location(s), copper plane anti-pads, etc., are all major contributors to the final electrical characteristics of each unique application of the connector.

FIGURE C-1 THROUGH FIGURE C-16 SHOW THE RECOMMENDED PCB FOOTPRINTS.

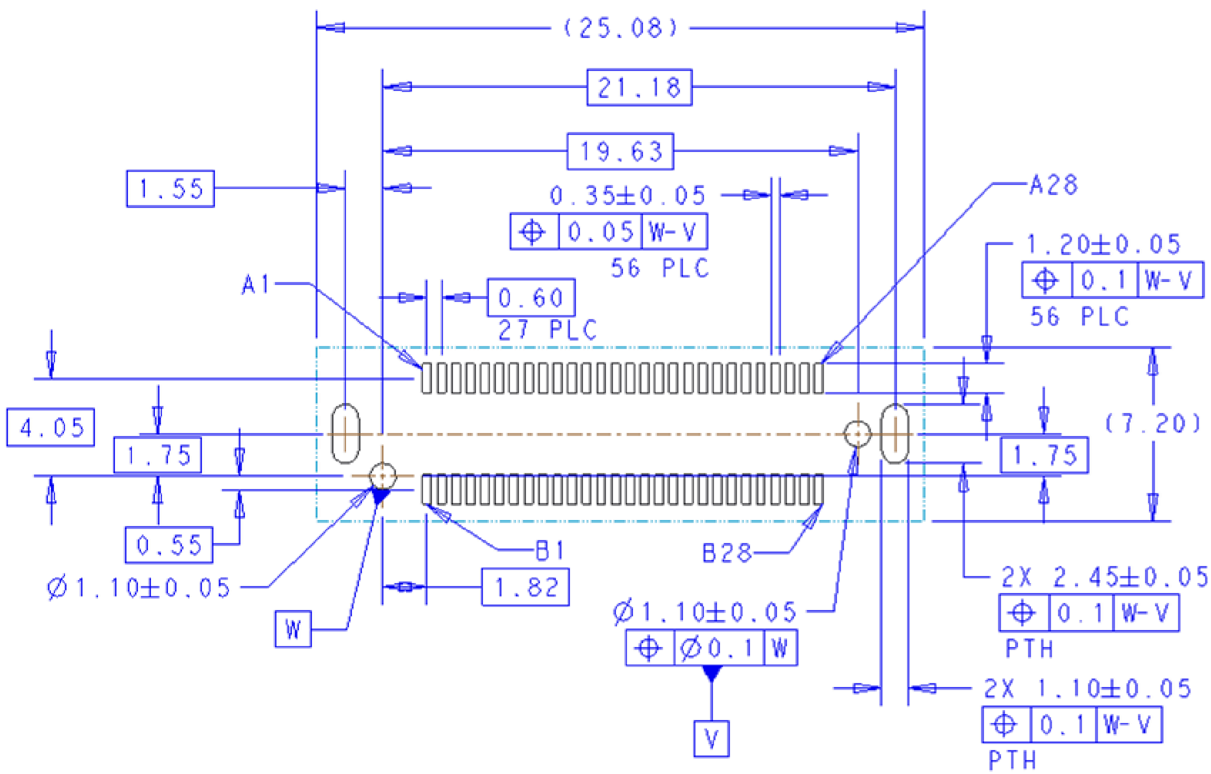


FIGURE C-1. 1C STRAIGHT CONNECTOR FOOTPRINT

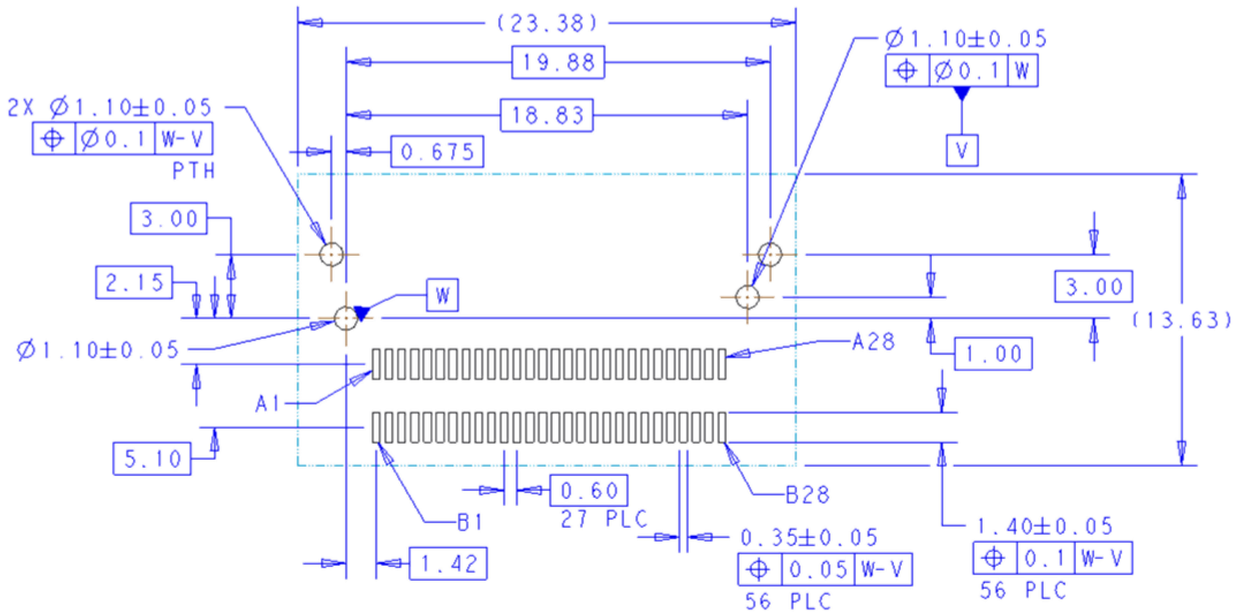


FIGURE C-2. 1C RIGHT ANGLE CONNECTOR FOOTPRINT

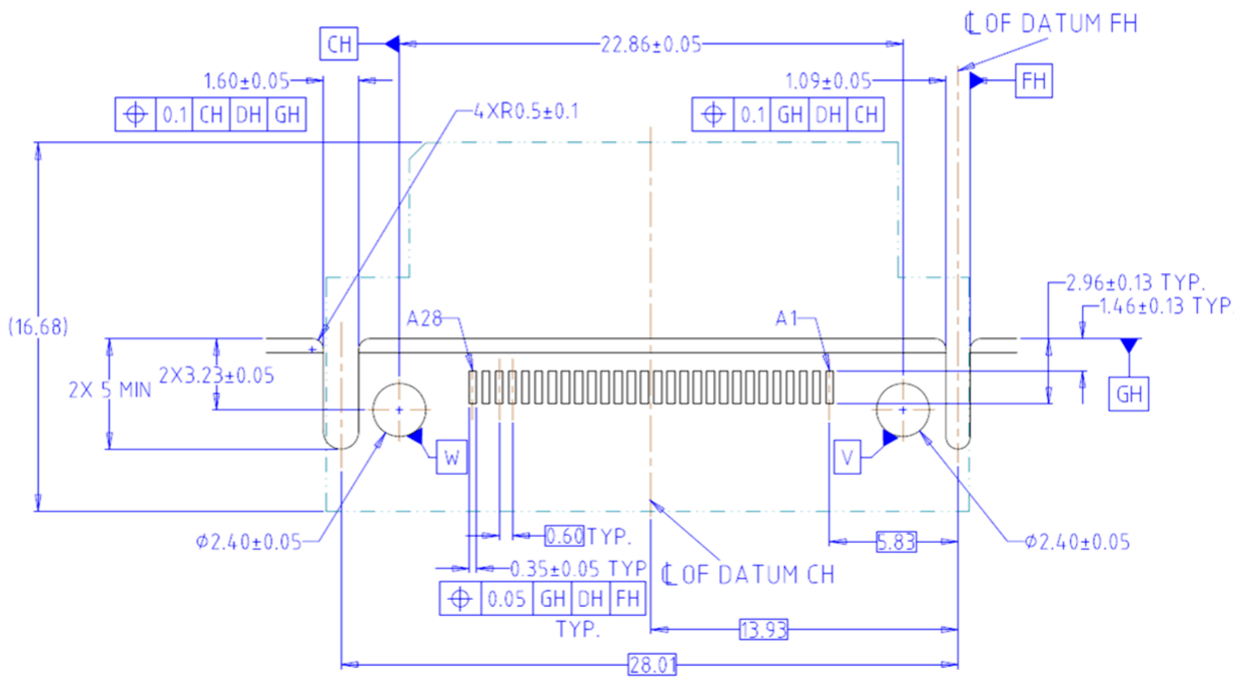


FIGURE C-3. 1C STRADDLE MOUNT CONNECTOR FOOTPRINT

NOTE: POSITION B1 ON THE OPPOSITE SIDE OF CARD OF A1

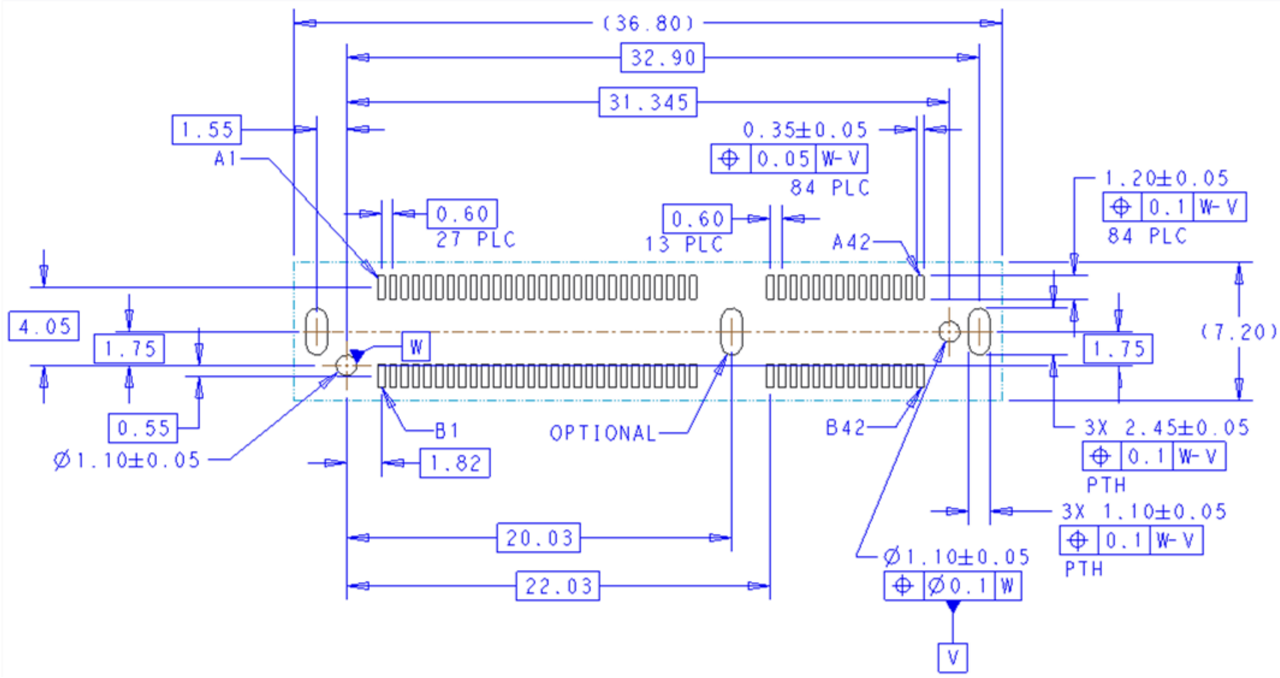


FIGURE C-4. 2C STRAIGHT CONNECTOR FOOTPRINT

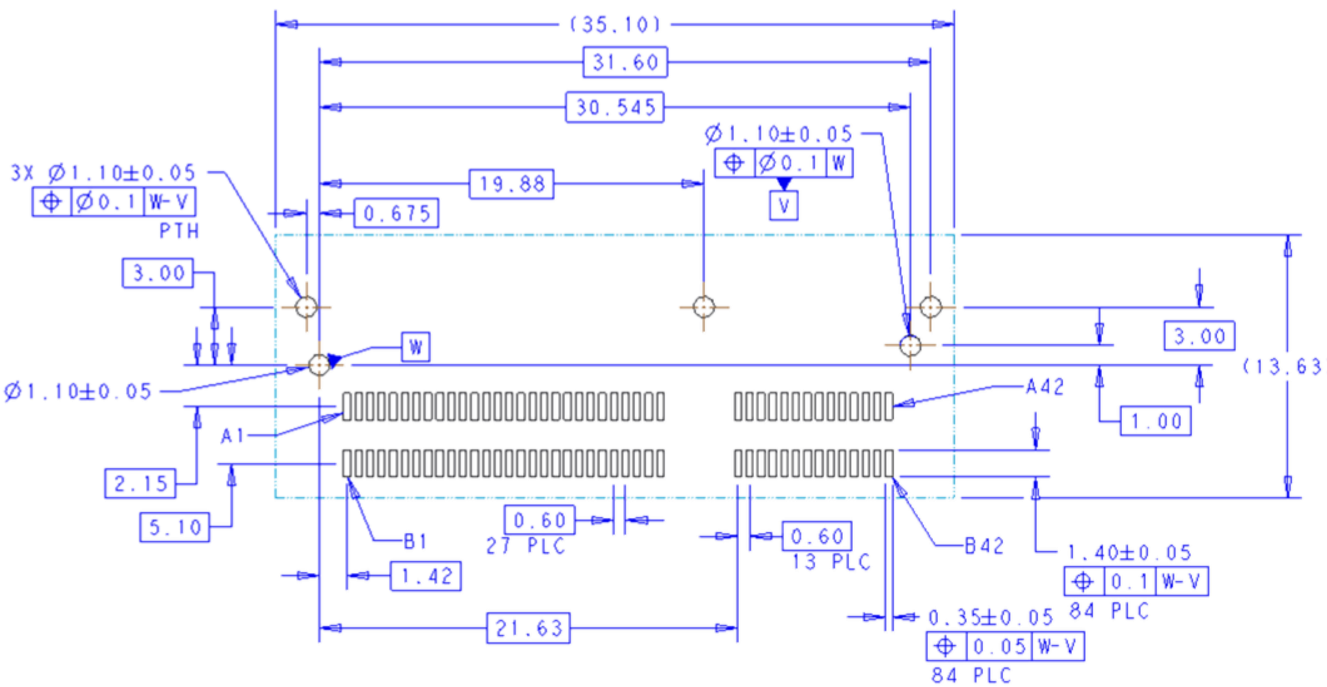


FIGURE C-5. 2C RIGHT ANGLE CONNECTOR FOOTPRINT

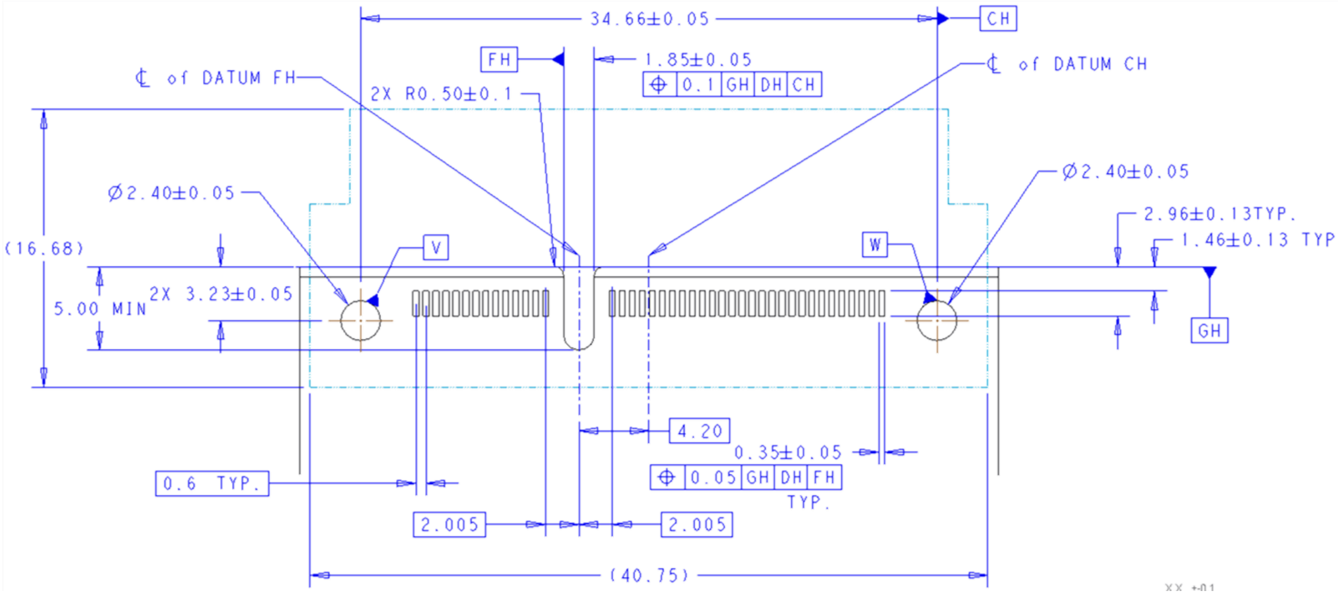


FIGURE C-6. 2C STRADDLE MOUNT CONNECTOR FOOTPRINT

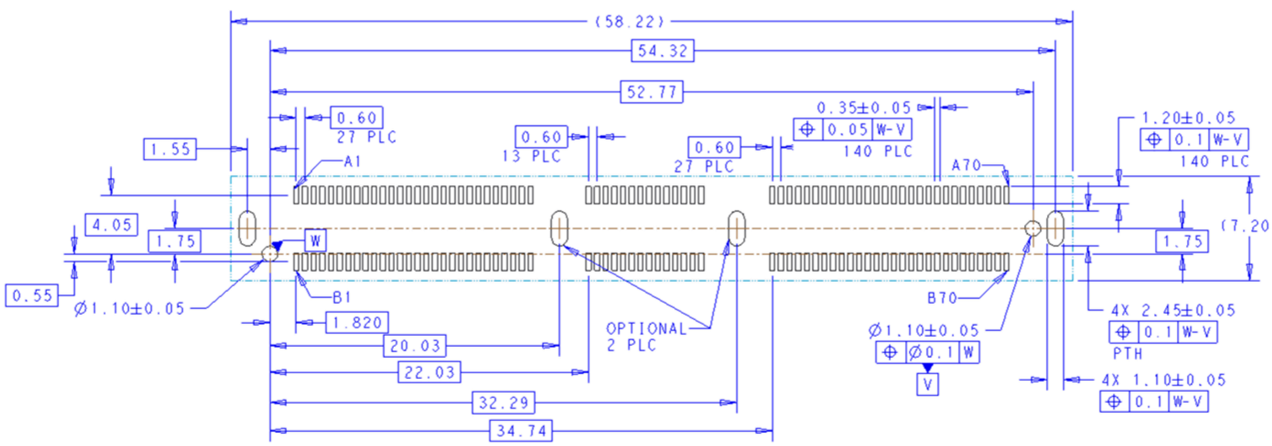


FIGURE C-7. 4C STRAIGHT CONNECTOR FOOTPRINT

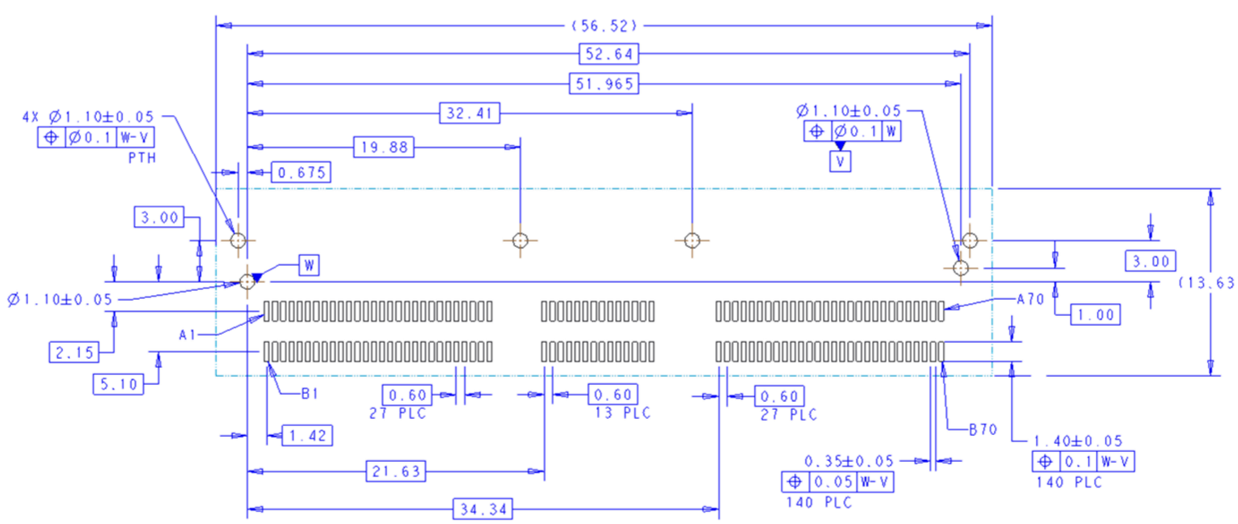


FIGURE C-8. 4C RIGHT ANGLE CONNECTOR FOOTPRINT

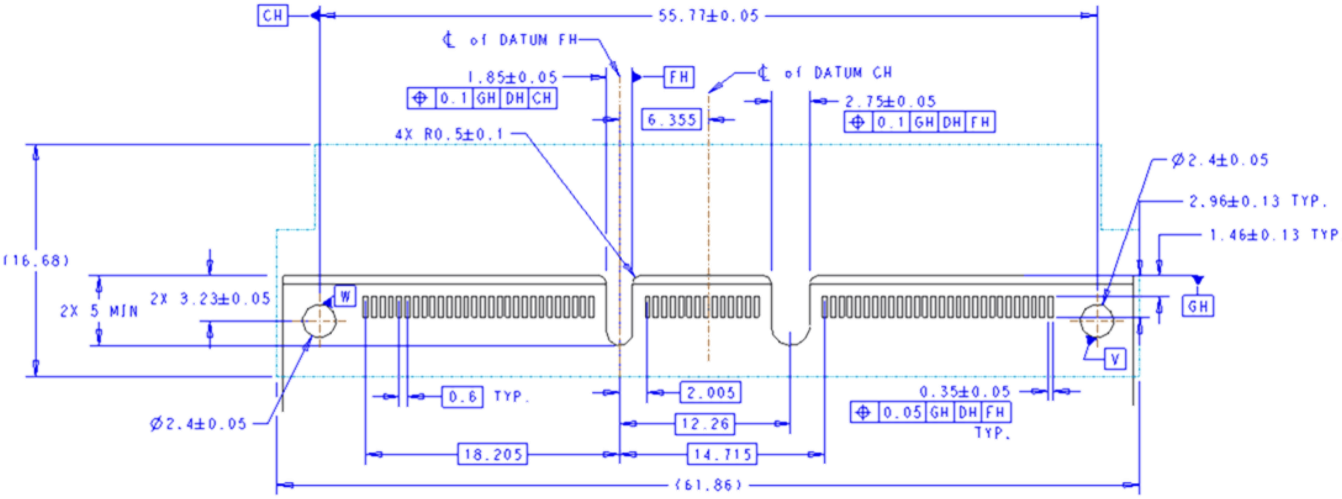


FIGURE C-9. 4C STRADDLE MOUNT CONNECTOR FOOTPRINT (MM)

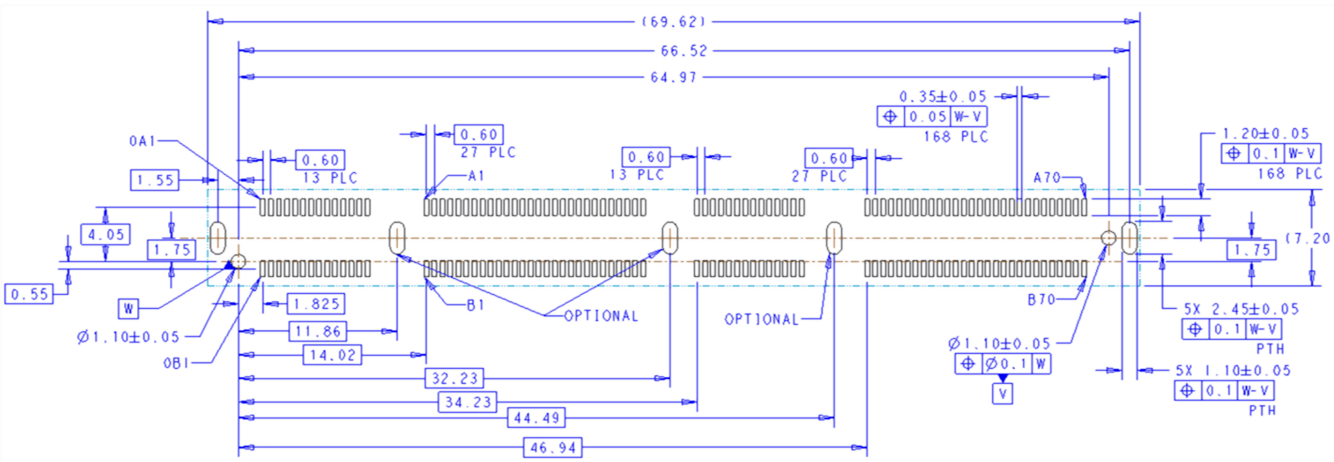


FIGURE C-10. 4C+ STRAIGHT CONNECTOR FOOTPRINT (MM)

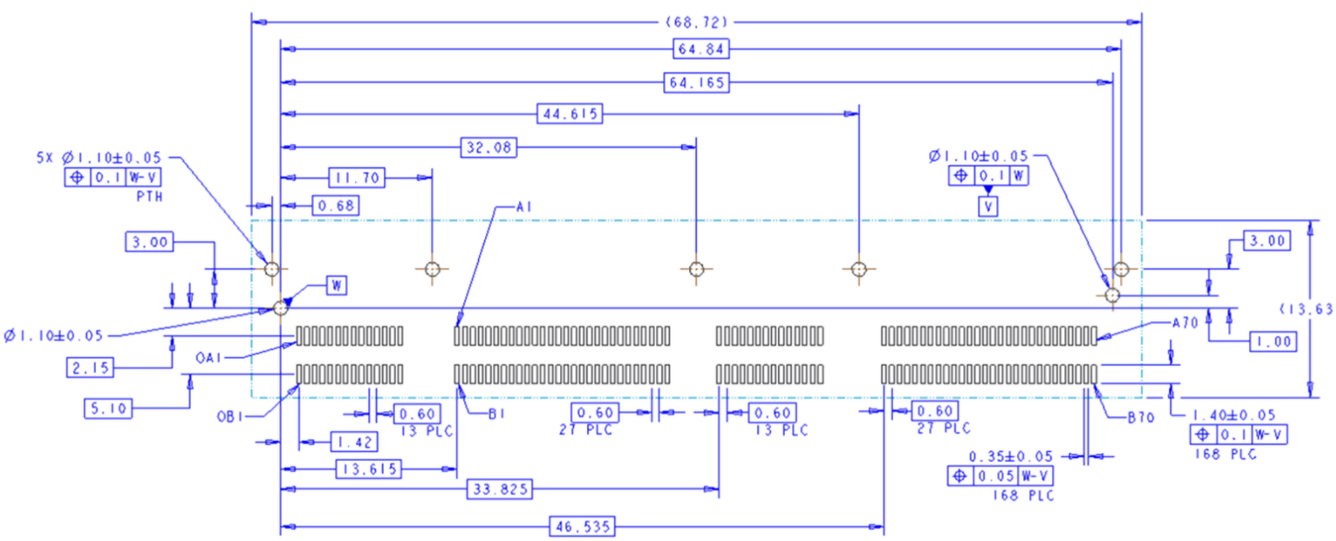


FIGURE C-11. 4C+ RIGHT ANGLE CONNECTOR FOOTPRINT (MM)

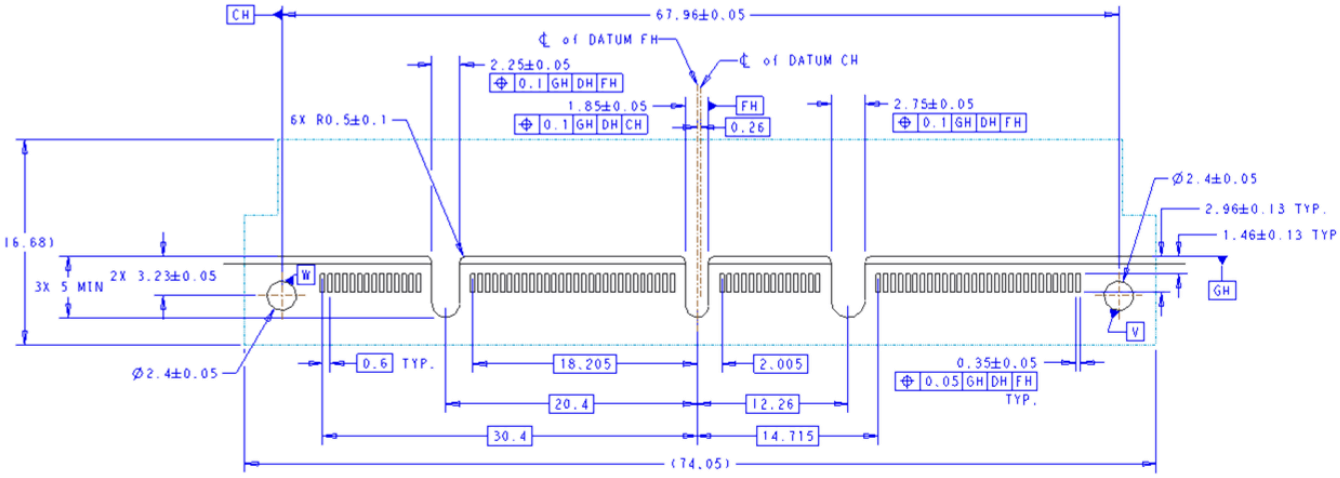


FIGURE C-12. 4C+ STRADDLE MOUNT CONNECTOR FOOTPRINT (MM)

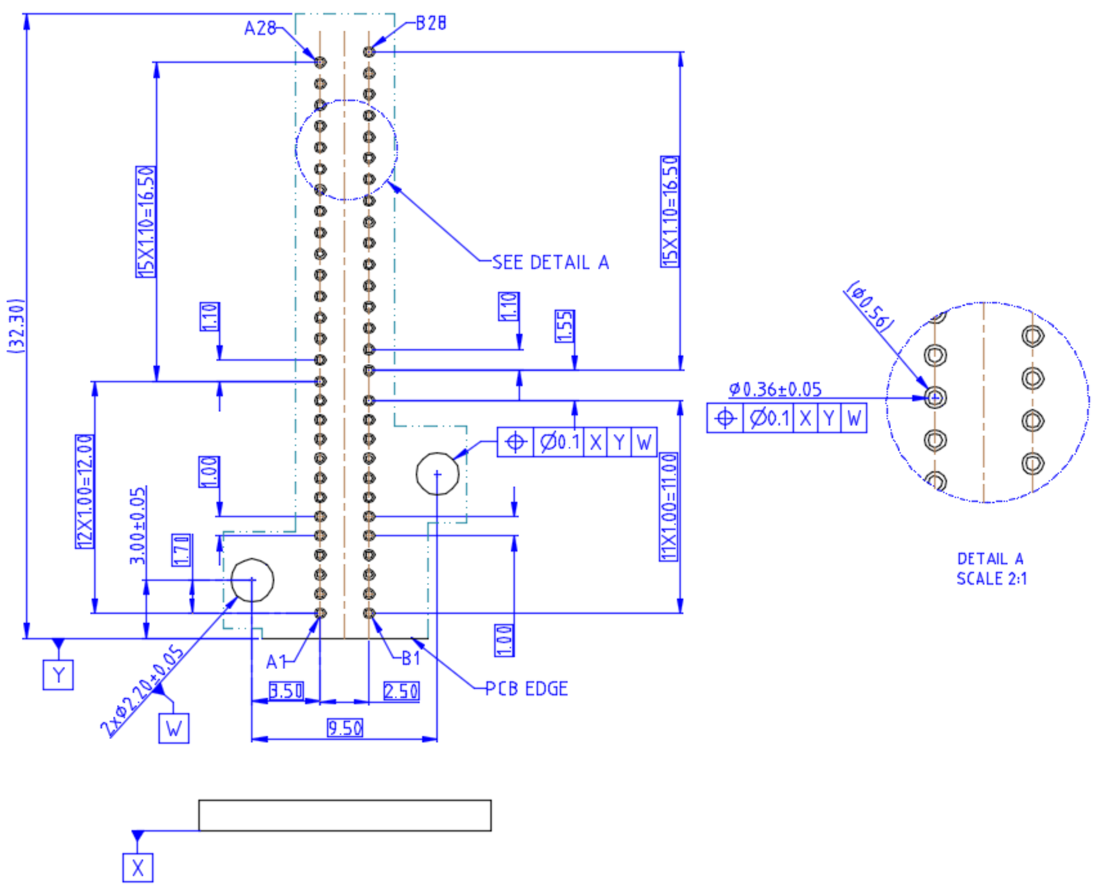


FIGURE C-13. 1C PRESS FIT ORTHOGONAL CONNECTOR FOOTPRINT (MM)

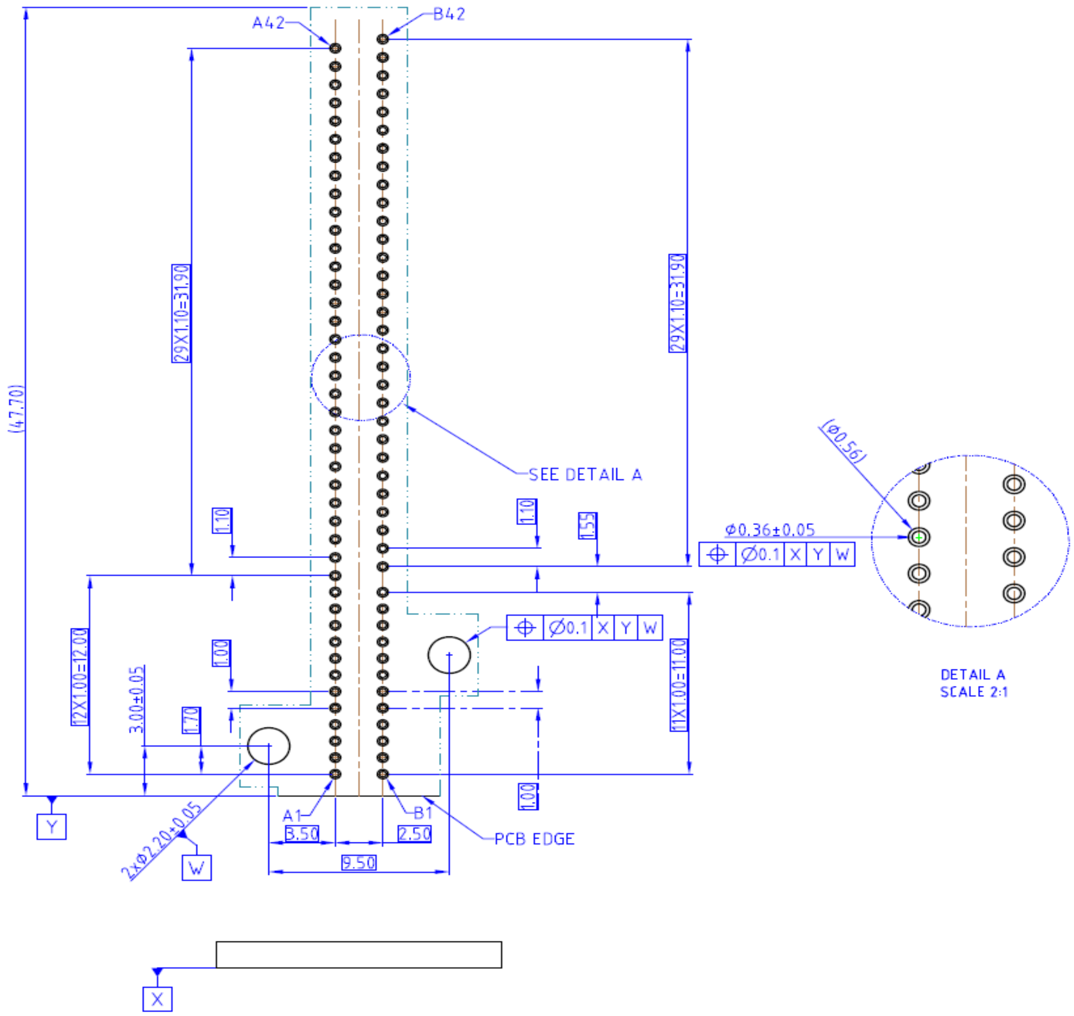


FIGURE C-14. 2C PRESS FIT ORTHOGONAL CONNECTOR FOOTPRINT (MM)

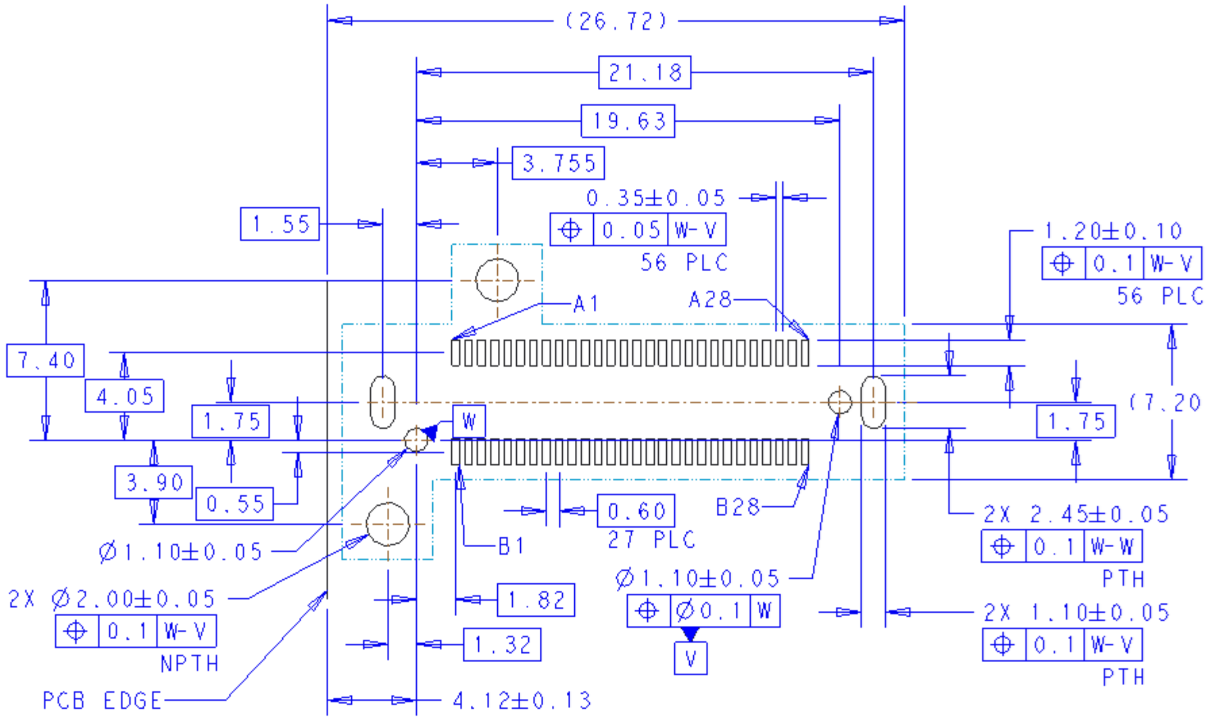


FIGURE C-15. 1C RIGHT ANGLE ORTHOGONAL SMT CONNECTOR FOOTPRINT

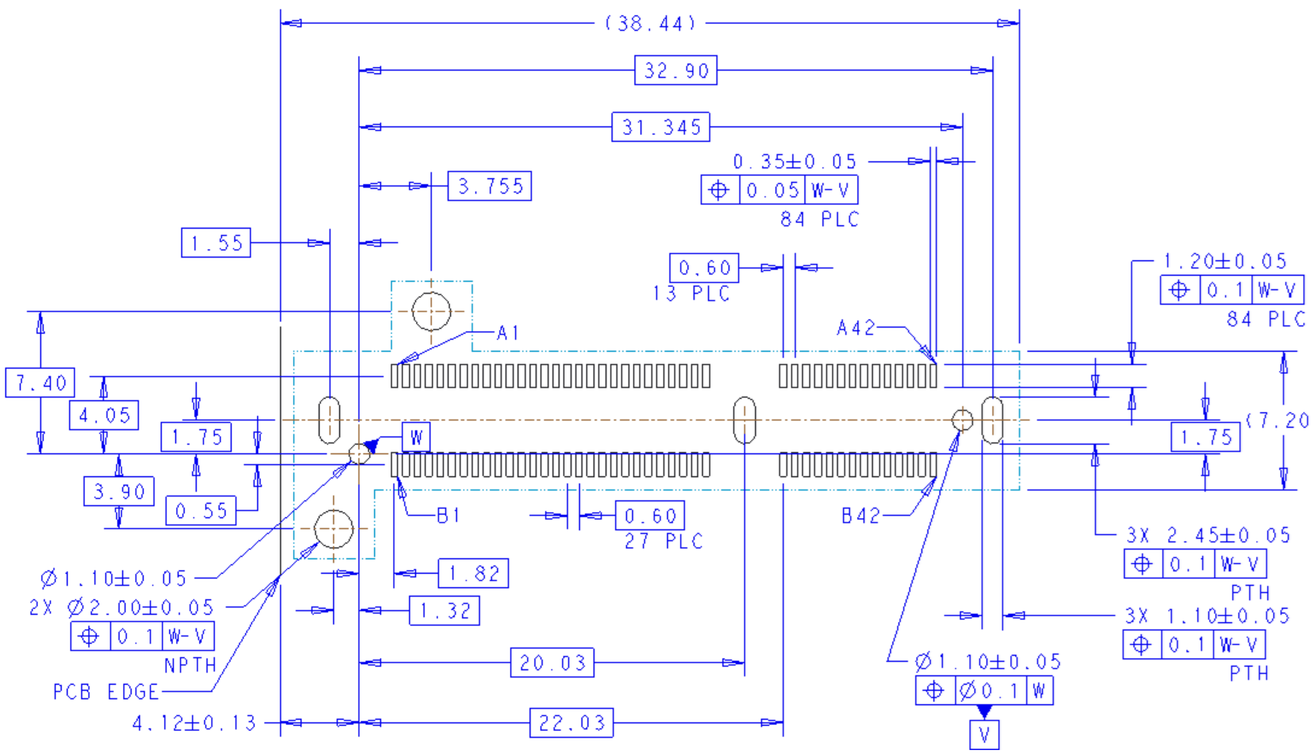


FIGURE C-16. 2C RIGHT ANGLE ORTHOGONAL SMT CONNECTOR FOOTPRINT

Appendix D. Connector Solder Lead Geometry

Refer to Table D-1 and Figure D-1 for informative solder lead geometry for the connector.

TABLE D-1. SMT LEAD GEOMETRY DIMENSIONS

Variable	Description	Straight	Right Angle
A	Pad Width	0.35	0.35
B	Lead Thickness	0.20	0.20
C	Lead Length on Pad	0.76	1.12
D	Lead Tip to Footprint Centerline	2.75	1.79
E	Pad Length	1.20	1.40
F	Distance Between Inside Edges of Pads	3.40	1.56
W	Lead Width	0.24	0.24

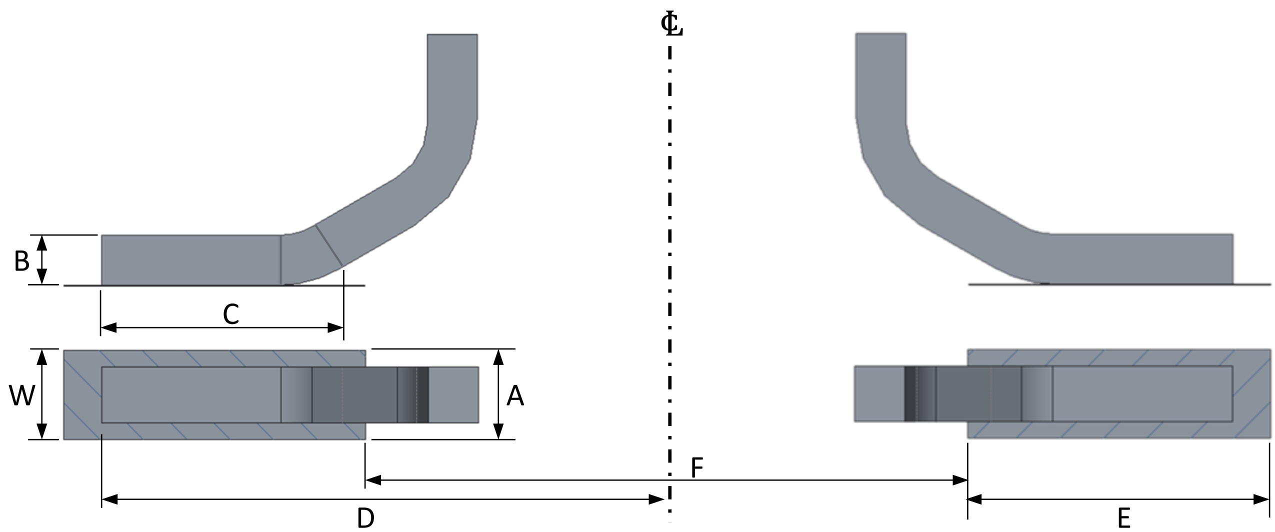


FIGURE D-1. SMT LEAD GEOMETRY

Appendix E. Effective Intra-Pair Skew (EIPS)

The effective skew calculation starts from the frequency domain skew, which is captured from the modified mixed-mode insertion loss. The modified mixed-mode insertion loss relates the differential input to the single-ended output while accounting for the coupling within a differential pair properly. The modified mixed-mode insertion loss, S2d1, and S4d1, which relate the differential input to the single-ended outputs within a 4-port system, are depicted in Figure E-1. The intra-pair skew addition mechanism is illustrated in Figure E-2.

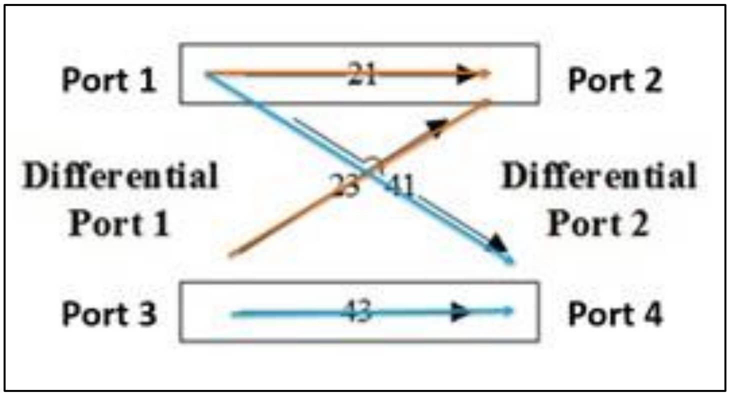


FIGURE E-1. MODIFIED MIXED-MODE INSERTION LOSS, S2D1 AND S4D1

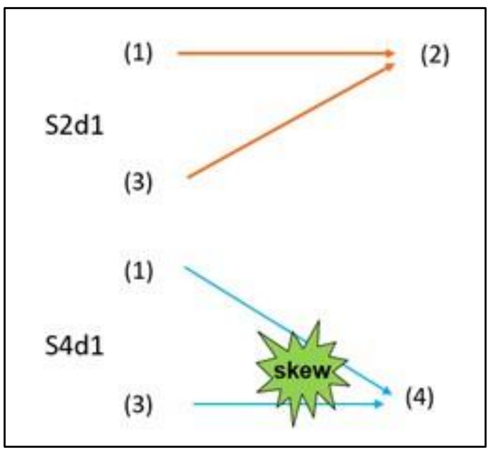


FIGURE E-2. INTRA-PAIR SKEW INTRODUCTION TO A 4-PORT SYSTEM

The modified mixed-mode insertion loss can be represented by the single-ended S-parameter equations as shown in Equation E-1.

EQUATION E-1. CALCULATIONS FOR S2D1 AND S4D1

$$S2d1 = \frac{1}{\sqrt{2}} \times (S21 - S23)$$

$$S4d1 = \frac{1}{\sqrt{2}} \times (S43 - S41)$$

The frequency domain skew, skew(f) is obtained by calculating the difference between two phase delays as shown in Equation E-2.

EQUATION E-2. CALCULATIONS FOR SKEW

$$\Delta t_1 = -{unwrap(phase(S2d1))}/{2\pi f}$$
$$\Delta t_2 = -{unwrap(phase(S4d1))}/{2\pi f}$$
$$skew(f) = \Delta t_1 - \Delta t_2$$

The calculated frequency domain skew is multiplied by a weighting function, which is the product of power spectral density of the random binary sequence and skew impact on the normalized mode conversion. EIPS is the weighted frequency domain skew and is integrated over the frequency region up to 1.5×(Nyquist frequency) where f_{max} is set at 1.5×(Nyquist frequency, f_N) as shown in Equation E-3. $Skew_{avg}$ is the mean of the magnitude of the frequency domain skew over the frequency region of [f_{min}, f_{max}]. F_b is the baud rate. F_r is the Rx rise time and F_t is the TX rise time of a Butterworth filter.

EQUATION E-3. CALCULATIONS FOR EFFECTIVE INTRA-PAIR SKEW

$$EIPS = \int_{f_{min}}^{f_{max}} W(f) \cdot |skew(f)| df$$

$$W(f) = \frac{\left|db\left(S_{cd21,avg\ skew}\right) - db\left(S_{cd21,0skew}\right)\right| \times PSD}{\int_{f_{min}}^{f_{max}} \left|db\left(S_{cd21,avg\ skew}\right) - db\left(S_{cd21,0skew}\right)\right| \times PSD\ df}$$

$$S_{cd21,avg\ skew} = \frac{1}{2} \times (S21 - S23 + S41) \times\ e^{j2\pi f\ \times (skew(f) - skew_{avg})} - S43\ \times\ e^{j2\pi f\ \times (skew(f) - skew_{avg})}$$

$$S_{cd21,0\ skew} = \frac{1}{2} \times (S21 - S23 + S41) \times\ e^{j2\pi f\ \times skew(f)} - S43\ \times\ e^{j2\pi f\ \times skew(f)}$$

$$PSD = sinc(\frac{f}{f_b})^2 \times \frac{1}{1 + (\frac{f}{f_r})^8} \times \frac{1}{1 + (\frac{f}{f_t})^4}$$

To test EIPS, the following should be done:

1. Test Set (Mated Connector + Fixture) Intra-Pair Skew
   a. Insert the DUT into test fixtures for the full channel measurement.
   b. Capture the test set intra-pair skew from IL measurement of each differential pair in the test plan using VNA.
   c. The test set skew is calculated using the Effective Intra-pair Skew per method described in this section.

2. Device Under Test (DUT) Intra-Pair Skew
   a. Calculate DUT skew by subtracting absolute value of rounded fixture skew from absolute value of the test set skew.
   b. Round fixture skew to the nearest ps
   c. Calculate DUT skew by subtracting absolute value of rounded fixture skew from absolute value of the test set skew Figure .

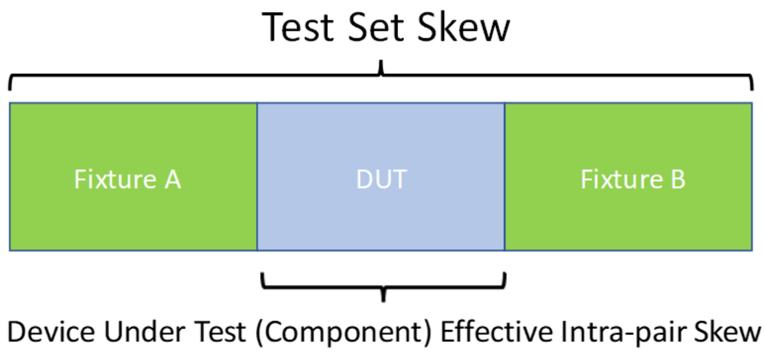


FIGURE E-3. DUT SKEW