SFF-8667

Former Specification for

Module with High Density Connector for Enclosure Applications

Rev 2.0 November 12, 2021

SECRETARIAT: SFF TA TWG

ABSTRACT: This specification formerly defined the system considerations and the high density connector pin assignment for PCI Express® (PCIe®) data signals, power, and enclosure services for the module. Environmental and electrical characteristics are defined for features that are unique to this application or not included in other applicable specifications.

REASON FOR EXPIRATION: Obsolete
This specification is no longer relevant to the industry because this module was not implemented.

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SFF specifications are available at http://www.snia.org/sff/specifications

SFF-8667

Specification for

Module with High Density Connector for Enclosure Applications

Rev 1.0 June 6, 2018

Secretariat: SFF TA TWG

Abstract: This specification defines system considerations and the high density connector pin assignment for PCI Express® (PCIe®) data signals, power, and enclosure services for the module. Environmental and electrical characteristics are defined for features that are unique to this application or not included in other applicable specifications.

This specification provides a common reference for systems manufacturers, system integrators, and suppliers.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

The description of a connector in this specification does not assure that the specific component is actually available from connector suppliers. If such a connector is supplied it must comply with this specification to achieve interoperability between suppliers.

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Intellectual Property

The user's attention is called to the possibility that implementation of this Specification may require the use of an invention covered by patent rights. By distribution of this specification, no position is taken with respect to the validity of a claim or claims or of any patent rights in connection therewith. This specification is considered SNIA Architecture and is covered by the SNIA IP Policy and as a result goes through a request for disclosure when it is published. Additional information can be found at the following locations:

- Results of IP Disclosures: http://www.snia.org/sffdisclosures
- SNIA IP Policy: http://www.snia.org/ippolicy

Change History

Rev 0.0 April 25, 2016
- Initial posting of abstract.

Rev 0.1 May 4, 2016
- Revision posting with first draft of content.

Rev 0.2 May 3, 2017
- Substantial rewrite of entire specification without changes tracked.

Rev 0.3 July 6, 2017
- Corrected signal names in Table 4-1 and 4-2, changed 3.3V_AUX current to 20 mA max, updated dual port configuration, and PWRBRK# and PWRDIS definitions.

Rev 0.4 October 10, 2017
- Updated signal names, replaced DRIVEFAULT with SMBRST#, removed LED and associated requirements.

Rev 0.5 November 2, 2017
- Updated 3.3 Vaux current in Table 4-5 and changed Vcc3.3 to 3.3 Vaux in Table 4-12.

Rev 0.6 April 20, 2018
- Added support for REFCLK and tri-mode host implementation.

Rev 0.7 April 25, 2018
- Added x8 versus x16 mating details and changed PRSNT0# to PRSNT# in Table 4-1.

Rev 1.0 June 6, 2018
- Publication date.

- **Foreword**

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors. The SFF Committee provided a forum for system integrators and vendors to define the form factor of disk drives.

During their definition, other activities were suggested because participants in SFF faced more challenges than the form factors. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

In July 2016, the SFF Committee transitioned to SNIA (Storage Networking Industry Association), as a TA (Technology Affiliate) TWG (Technical Work Group).

Industry consensus is not a requirement to publish a specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF meets during the T10 (see www.t10.org) and T11 (see www.t11.org) weeks, and SSWGs (Specific Subject Working Groups) are held at the convenience of the participants. Material presented to SFF becomes public domain, and there are no restrictions on the open mailing of the presented material by Members.

Many of the specifications developed by SFF have either been incorporated into standards or adopted as standards by ANSI, EIA, JEDEC and SAE.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at:

http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee is contained in the document SFF-8000 which can can be found at:

http://www.snia.org/sff/specifications

Suggestions for improvement of this specification will be welcome, they should be submitted to:

http://www.snia.org/feedback

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FIGURES

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1. Scope

This SFF Specification defines system electrical and environmental characteristics for applications utilizing the HDSFF module defined herein.

1.1 Application Specific Criteria

The environment for the HDSFF module is a computer, cabinet, or enclosure connecting to one or more modules in a restricted packaging environment.

The HDSFF module provides system electrical definition of the connector signals, and environmental requirements to assist manufacturers in the systems integration.

1.2 Copyright

1.3 Disclaimer

The information contained in this publication is subject to change without notice. The SNIA makes no warranty of any kind with regard to this specification, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The SNIA shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this specification.

Suggestions for revisions should be directed to http://www.snia.org/feedback/

2. References

2.1 Industry Documents

- PCI Express Base Specification Revision 4.0
- PCI Express Card Electromechanical Specification Revision 3.0
- SFF-8351 - Specification for 3.5” Form Factor Drive with High Density Connector
- SFF-8631 - Specification for Serial Attachment X8/X16 Unshielded Connector
- SFF-TA-1000 - Specification for 2.5” Form Factor Drive with High Density

Connector
- System Management Bus (SMBus) Specification, Version 2.0

2.2 Sources

There are several projects active within the SFF TWG. The complete list of specifications which have been completed or are still being worked on is contained in the document SFF-8000 which can be found at http://www.snia.org/sff/specifications.

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://www.techstreet.com/incitsgate.tmpl).

2.3 Conventions

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

2.4 Definitions

For the purpose of SFF Specifications, the following definitions apply:

Advanced grounding contacts: Connector contacts that make first and break last and are capable of carrying power ground return currents and performing electrostatic discharge. Other terms sometimes used to describe these features are: grounding pins, ESD contacts, grounding contacts, static drain, and pre-grounding contacts.

Backplane: The components of the enclosure that mechanically support the HDSFF module, and create or route the required signals and power to the HDSFF module from the enclosure. The backplane may be a true multi-module backplane, a paddle card inserted in a host computer, a paddle card attached to an appropriately designed cable, or any component with similar capabilities.

Dual port mode: When enabled, the lane assignments defined in Table 4-7 or Table 4-8 are supported. Lanes form two ports, an A side and a B side. The A and B side PCI Express interfaces must operate independently with any combination of active / inactive states possible. Any other interaction between the A side and B side interfaces is outside the scope of this specification. When the Dual port mode is disabled, all lanes form a single port.

HDSFF module: The storage peripheral that plugs into the backplane using the HDSFF connector. The HDSFF module may be removable from the enclosure through an external port or may be permanently installed in the enclosure. The storage peripheral may be any storage module of any type that meets one of the standards defined form factors and establishes its connection to the backplane through the HDSFF connector.

Module circuitry: Active electrical components on the HDSFF module powered by 12 V and/or 3.3 Vaux not associated with the distribution of supply voltages within the module.

Optional: This term describes features which are not required by the SFF Specification. However, if any feature defined by the SFF Specification is implemented, it shall be done in the same way as defined by the Specification.

Describing a feature as optional in the text is done to assist the reader. If there is a conflict between text and tables on a feature described as optional, the table shall be accepted as being correct.

Reserved: Where this term is used for defining the signal on a connector pin its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields and code values; the bits, bytes, fields and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

VU (Vendor Unique): This term is used to describe bits, bytes, fields, pins, signals, code values and features which are not described in this SFF Specification, and may be used in a way that varies between vendors.

3. General Description

This SFF Specification provides the characteristics that an OEM supplier requires to design an enclosure that uses the HDSFF module, utilizing the high speed multi-lane, multi-function plug and receptacle connector that is designed for use as a common connector system. Two modules are defined in this specification, a x8 and a x16. The x8 module is able to mate with a x8 receptacle or x16 receptacle; the x16 module is only able to mate with a x16 receptacle.

4. Signals

4.1 Signal conventions

Signal names are shown in all upper case letters. Signal names including a lower case n or lower case p followed by a number indicates the polarity of a differential signal (i.e., n for negative or p for positive) and the lane number. Signals may be asserted (active, true) in either a high (more positive voltage) or low (less positive voltage) state. A dash character (-) or hash (#) at the beginning or end of a signal name indicates it is asserted at the low level (active low). No character or a plus character (+) at the beginning or end of a signal name indicates it is asserted high (active high). An asserted signal may be driven high or low by an active circuit, or it may be allowed to be pulled to the correct state by the bias circuitry. Details of the requirements are included in the signal definitions.

Unless noted otherwise, tables specify the voltage and/or current requirements at the HDSFF module connector. Current flow into the HDSFF module is positive and current flow out of the HDSFF module is negative.

4.2 Signal Connector Pin Assignment

The SFF-8631 x8 signal pin assignments are shown in Table 4-1.

TABLE 4-1 SFF-8631 SIGNAL PIN ASSIGNMENTS FOR x8

PIN NUMBER	SIGNAL NAME	DRIVEN BY BACKPLANE/MODULE		SIGNAL NAME	PIN NUMBER
A1	GROUND (12 V)	B	B	12 V	B1
A2	GROUND (12 V)	B	B	12 V	B2
A3	GROUND (12 V)	B	B	12 V	B3
A4	GROUND (12 V)	B	B	12 V	B4
A5	GROUND (12 V)	B	B	12 V	B5
A6	SMBRST#	B	B	12V-PRECHARGE	B6
A7	3.3 Vaux	B	B	REFCLKn1	B7
A8	SMDAT	B	B	REFCLKp1	B8
A9	SMCLK	B	B	PERST0#	B9
A10	PWRDIS	B	B	PERST1#	B10
A11	PWRBRK#	B	M	IFDET1	B11
A12	ACTIVITY#	M	M	PRSNT#	B12
A13	GROUND (12 V)	B	B	REFCLKn0	B13
A14	PERp0	M	B	REFCLKp0	B14
A15	PERn0	M	B	GROUND (12 V)	B15
A16	GROUND (12 V)	B	B	PETp0	B16
A17	GROUND (12 V)	B	B	PETn0	B17
A18	PERp1	M	B	GROUND (12 V)	B18
A19	PERn1	M	B	GROUND (12 V)	B19
A20	GROUND (12 V)	B	B	PETp1	B20
A21	GROUND (12 V)	B	B	PETn1	B21
A22	PERp2	M	B	GROUND (12 V)	B22
A23	PERn2	M	B	GROUND (12 V)	B23
A24	GROUND (12 V)	B	B	PETp2	B24
A25	GROUND (12 V)	B	B	PETn2	B25
A26	PERp3	M	B	GROUND (12 V)	B26
A27	PERn3	M	B	GROUND (12 V)	B27

PIN NUMBER	SIGNAL NAME	DRIVEN BY BACKPLANE/MODULE		SIGNAL NAME	PIN NUMBER
A28	GROUND (12 V)	B	B	PETp3	B28
A29	GROUND (12 V)	B	B	PETn3	B29
A30	PERp4	M	B	GROUND (12 V)	B30
A31	PERn4	M	B	GROUND (12 V)	B31
A32	GROUND (12 V)	B	B	PETp4	B32
A33	GROUND (12 V)	B	B	PETn4	B33
A34	PERp5	M	B	GROUND (12 V)	B34
A35	PERn5	M	B	GROUND (12 V)	B35
A36	GROUND (12 V)	B	B	PETp5	B36
A37	GROUND (12 V)	B	B	PETn5	B37
A38	PERp6	M	B	GROUND (12 V)	B38
A39	PERn6	M	B	GROUND (12 V)	B39
A40	GROUND (12 V)	B	B	PETp6	B40
A41	GROUND (12 V)	B	B	PETn6	B41
A42	PERp7	M	B	GROUND (12 V)	B42
A43	PERn7	M	B	GROUND (12 V)	B43
A44	GROUND (12 V)	B	B	PETp7	B44
A45	DUALPORTEN#	B	B	PETn7	B45
A46	IFDET2	M	B	GROUND (12 V)	B46

The SFF-8631 x16 signal pinout includes the signal assignments shown in Table 4-2 in addition to the signal assignments shown in Table 4-1.

TABLE 4-2 SFF-8631 SIGNAL PIN ASSIGNMENTS FOR x16

PIN NUMBER	SIGNAL NAME	DRIVEN BY BACKPLANE/MODULE		SIGNAL NAME	PIN NUMBER
A47	GROUND (12 V)	B	B	DUALPORTEN16#	B47
A48	PERp8	M	B	GROUND (12 V)	B48
A49	PERp8	M	B	GROUND (12 V)	B49
A50	GROUND (12 V)	B	B	PETp8	B50
A51	GROUND (12 V)	B	B	PETn8	B51
A52	PERp9	M	B	GROUND (12 V)	B52
A53	PERn9	M	B	GROUND (12 V)	B53
A54	GROUND (12 V)	B	B	PETp9	B54
A55	GROUND (12 V)	B	B	PETn9	B55
A56	PERp10	M	B	GROUND (12 V)	B56
A57	PERp10	M	B	GROUND (12 V)	B57
A58	GROUND (12 V)	B	B	PETp10	B58
A59	GROUND (12 V)	B	B	PETn10	B59
A60	PERp11	M	B	GROUND (12 V)	B60
A61	PERn11	M	B	GROUND (12 V)	B61
A62	GROUND (12 V)	B	B	PETp11	B62
A63	GROUND (12 V)	B	B	PETn11	B63
A64	PERp12	M	B	GROUND (12 V)	B64
A65	PERn12	M	B	GROUND (12 V)	B65
A66	GROUND (12 V)	B	B	PETp12	B66
A67	GROUND (12 V)	B	B	PETn12	B67
A68	PERp13	M	B	GROUND (12 V)	B68
A69	PERn13	M	B	GROUND (12 V)	B69
A70	GROUND (12 V)	B	B	PETp13	B70
A71	GROUND (12 V)	B	B	PETn13	B71
A72	PERp14	M	B	GROUND (12 V)	B72
A73	PERn14	M	B	GROUND (12 V)	B73
A74	GROUND (12 V)	B	B	PETp14	B74

PIN NUMBER	SIGNAL NAME	DRIVEN BY BACKPLANE/MODULE		SIGNAL NAME	PIN NUMBER
A75	GROUND (12 V)	B	B	PETn14	B75
A76	PERp15	M	B	GROUND (12 V)	B76
A77	PERn15	M	B	GROUND (12 V)	B77
A78	GROUND (12 V)	B	B	PETp15	B78
A79	RSVD		B	PETn15	B79
A80	RSVD		B	GROUND (12 V)	B80
A81	RSVD			RSVD	B81
A82	RSVD			RSVD	B82
A83	IFDET3	M		RSVD	B83

4.3 Signal Descriptions

4.3.1 Overview

Signal names are maintained from PCIe specifications wherever possible and are defined similarly within this specification. This section provides a reference to where signals are defined in other specifications or provides a definition of the signals when necessary.

4.3.2 Signal Function, Voltage, and Characteristics

Table 4-3 provides a list of the general function, signal names, voltage, and reference to the section number within this specification or the industry specification location of characteristics.

TABLE 4-3 SIGNAL FUNCTION AND VOLTAGE

Function	Signal	Voltage	Reference
Power and Ground	12 V	12 V	See 4.3.3
	12V-PRECHARGE	12 V	See 4.3.4
	3.3 Vaux	3.3 V	See 4.3.5
	GROUND (12 V)	0 V	
Activity indication	ACTIVITY_n		See 4.3.6
Host request for dual port operation	DUALPORTEN_n	3.3 V	See 4.3.7
Interface supported	IFDET1/IFDET2/IFDET3	3.3 V	See 4.3.8
PCIe data signals	PERp0 through PERp15		See 4.3.9
	PERn0 through PERn15		
	PETp0 through PETp15		
	PETn0 through PETn15		
Reset	PERST0#	3.3 V	See 4.3.10
Reset	PERST1#	3.3 V	See 4.3.11
Present indication	PRSNT#	3.3 V	See 4.3.12
Power brake	PWRBRK#	3.3 V	See 4.3.13
Power disable	PWRDIS	3.3 V	See 4.3.14
Reference clock	REFCLKn0, REFCLKp0		See 4.3.15
	REFCLKn1, REFCLKp1		
SMBus clock	SMBCLK	3.3 V	See 4.3.16
SMBus data	SMBDATA	3.3 V	See 4.3.17
SMBus reset	SMBRST#	3.3 V	See 4.3.18

4.3.3 12 V

The module supply rail provided by the system to the module. The voltage, power, and current requirements are defined in Table 4-4.

TABLE 4-4 12 V ELECTRICAL REQUIREMENTS

Characteristic	Value	Comment
Voltage	12 V	Tolerance is vendor specific
Maximum continuous power (3.5”) (2.5”)	50 W 25 W	Highest averaged power value over any 1 sec period
Maximum peak current	12.5 A	Maximum period of 1.5 sec
Maximum initial current load	2 A	Maximum current load presented by the module 12 V supply rail to the system receptacle during the initial power-up ramp to 90% of the minimum module operating voltage.
Initial module power limit	25 W	Configured by the Slot Capabilities register (see PCIe)

4.3.4 12V-PRECHARGE

The first mate supply voltage contact that allow the system to implement voltage supply surge reduction for hot plug applications. The pre-charge pin is shorted to the other supply voltage pins (second mate) on the module.

4.3.5 3.3 Vaux

Mandatory for module; optional for backplane.
3.3 Vaux allows the system to provide power for SMBus on the module. The voltage, current, and capacitive load requirements are defined in Table 4-5. Removal of 3.3 Vaux from the module shall reset the SMBus circuitry.

TABLE 4-5 3.3 VAUX ELECTRICAL REQUIREMENTS

Characteristic	Value	Comment
Voltage	3.3 V ± 15%	Measured at the connector
Maximum continuous current	1 mA (SMBus inactive) 20 mA	Highest averaged current value over any 1 sec period
Maximum capacitive load	5 µF	Presented by the module to the system connector

4.3.6 ACTIVITY#

Driven by module.
This signal is an open-drain output driven low by the module to indicate module activity. The electrical requirements are defined in Table 4-6. Use of this signal is outside the scope of this specification.

TABLE 4-6 ACTIVITY# ELECTRICAL REQUIREMENTS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low voltage	15.0 mA		0.2	V

4.3.7 DUALPORTEN#

Driven by backplane.
Optional for the module and the backplane.
Open drain pulled high by the module.
Static implementation by the system of either:
   a) connecting the pin to ground to enable dual port mode; or
   b) leaving not connected for single port configuration.
For lane port assignment, see Table 4-7 and Table 4-8.

TABLE 4-7 X8 DUAL PORT LANE ASSIGNMENTS

DUALPORTEN#	A side	B side
Asserted	PCIe data signals 0,1,4, and 5	PCIe data signals 2, 3, 6, and 7
De-asserted	PCIe data signals 0 - 7	N/A

TABLE 4-8 X16 DUAL PORT LANE ASSIGNMENTS

DUALPORTEN#	A side	B side
Asserted	PCIe data signals 0, 1, 4, 5, 8, 9, 12, and 13	PCIe data signals 2, 3, 6, 7, 10, 11, 14 and 15
De-asserted	PCIe data signals 0 - 15	N/A

4.3.8 IFDET1/IFDET2/IFDET3

Driven by module.
The module configures each pin as not connected or connected to ground to identify the interface supported by the module. The configuration truth table is defined in Table 4-9.

TABLE 4-9 INTERFACE IDENTIFICATION

Interface	IFDET3 (A83)	IFDET2 (A46)	IFDET1 (B11)	PRSNT#(B12)
No module present	Don't care	Don't care	Don't care	N/C
SAS x8	N/C	N/C	N/C	GROUND
PCIe x8	N/C	N/C	GROUND	GROUND
Not defined	N/C	GROUND	N/C	GROUND
Gen-Z x8	N/C	GROUND	GROUND	GROUND
SAS x16	GROUND	N/C	N/C	GROUND
PCIe x16	GROUND	N/C	GROUND	GROUND
Not defined	GROUND	GROUND	N/C	GROUND
Gen-Z x16	GROUND	GROUND	GROUND	GROUND

4.3.9 PERpX, PERnX, PETpX, and PETpX

See PCIe for signal descriptions and characteristics except for AC coupling capacitor requirements. Due to AC coupling capacitor incompatibilities between the various SFF-8631 mechanically compatible systems and devices, the AC coupling capacitor values, tolerances, and locations and defined in Table 4-10 shall be used.

TABLE 4-10 DECOUPLING CAPACITOR REQUIREMENTS

Signal Name	Location	Nominal Value	Tolerance
PERp0 through PERp15	Host	220 nF	±10%
PERn0 through PERn15	Host	220 nF	±10%
PETp0 through PETp15	Host	220 nF	±10%
PETn0 through PETn15	Host	220 nF	±10%
PERp0 through PERp15	Device	220 nF	±10%
PERn0 through PERn15	Device	220 nF	±10%
PETp0 through PETp15	Device	2.2 µF	±20%
PETn0 through PETn15	Device	2.2 µF	±20%

4.3.10 PERST0#

Driven by backplane.
Asserted when main power is applied and not within specified tolerance or stable. Goes inactive after a delay of TPVPERL time from the power rails achieving specified tolerance on power up.
Also is asserted by root complex to reset associated PCIe interface.
For electrical characteristics, see Table 4-13. For full functional description, see PCIe.

4.3.11 PERST1#

Driven by backplane.
Optional for the module and the backplane.
PERST1# is only valid when DUALPORTEN# or DUALPORTEN16# is asserted.
For electrical characteristics, see Table 4-13. For full functional description, see 4.3.10.

4.3.12 PRSNT#

Driven by module.

Connected to Ground on the module. This signal indicates that the module is present.

4.3.13 PWRBRK#

Driven by backplane.
Optional for the module and the backplane. If the PWRBRK# function is not supported by the module, this pin may still be connected with the electrical characteristics defined in this subsection.
Emergency fail-safe to prevent system damage.
Not intended for dynamic power management.
An open-drain (approximately 100 kohm pull up resistor is required on the module), active low signal driven low by external enclosure. When asserted, a module that supports Emergency Power Reduction shall quickly reduce its power consumption. When de-asserted, the module is permitted to resume normal power consumption.
External enclosure should control how it asserts and de-asserts this signal to avoid thrashing the system with rapid transitions in and out of the Emergency Power Reduction State. The amount of power consumed in the Emergency Power Reduction state is communicated through the Power Budgeting extended capability as defined in the PCI Express Base Specification. The time allowed to achieve power reduction (TPWRBRK-AIC-ENTER-LP-MODE) is defined in the PCI Express CEM Specification.
For electrical characteristics, see Table 4-13.

4.3.14 PWRDIS

Driven by backplane.
Mandatory for module; optional for backplane.
Used by the host to reset an unresponsive module.
Causes module to initiate power down sequence when asserted. Results in 12 V being disabled to module circuitry.
The HDSFF module shall:
A. allow 12 V power to be applied to the module circuitry if the PWRDIS signal is not connected on the backplane connector;
B. allow 12 V power to be applied to the module circuitry if the PWRDIS signal is negated as defined in Table 4-11;
C. disable 12 V power applied to the module circuitry if:
   1. the minimum negated hold time in Table 4-11 is met; and
   2. the PWRDIS signal is asserted as defined in Table 4-11;
D. perform the actions defined for power on reset if:
   1. the minimum negated hold time in Table 4-11 is met;
   2. the PWRDIS signal is asserted as defined in Table 4-11; and
   3. the PWRDIS signal transitions from asserted to negated; and
E. not respond to a change of the PWRDIS signal from negated to asserted or asserted to negated until the PWRDIS signal is held at the asserted or negated level for a minimum of 1 µs.
F. The SMBus device memory map shall provide access to vital product data accessible with the application of only 3.3 Vaux power, independent of PWRDIS being in an active or negated state; and extended management capabilities with the application of both 3.3 Vaux and 12 V power with PWRDIS negated.

TABLE 4-11 PWRDIS ELECTRICAL REQUIREMENTS

Parameter	Min	Max	Units	Notes
Absolute input voltage	-0.5	3.6	V	
Negated voltage (power enabled)	-0.5	0.7	V	1
Asserted voltage (power disabled)	2.1	3.6		2
Driver sink/source current capability	1		mA	1 and 2
PWRDIS asserted hold time	5.0		s	3 and 4
PWRDIS negated hold time	30.0		s	3 and 4

Notes:
1. The PWRDIS signal should be actively negated. If the PWRDIS signal is not actively negated (e.g. open), then the specified values for the PWRDIS signal negated voltage and driver sink current capability applied to the HDSFF module do not apply.
2. The PWRDIS signal shall be actively asserted.
3. The hold time is the length of time the PWRDIS signal is asserted or negated. The length of time after the PWRDIS signal is asserted or negated until the disabling or allowing of power application to the HDSFF module circuitry is vendor specific.
4. The PWRDIS signal should not transition from negated to asserted or asserted to negated for the negated hold time:
   a) after power is applied to the backplane receptacle; or
   b) after the detection of a hot plug event.

4.3.15 REFCLK

Driven by backplane.
Mandatory for module; optional for backplane.
Reference clock signal.

There are two sets of reference clock differential pairs. In the single port mode (i.e., DUALPORTEN# de-asserted), only REFCLKp0 and REFCLKn0 are used. In the dual port mode (i.e., DUALPORTEN# asserted), REFCLKp0 and REFCLKn0 support Port A; REFCLKp1 and REFCLKn1 support port B.

If SRIS (Separate Ref-clock Independent SSC) or SRNS (Separate Ref-clock No SSC) is supported by both the backplane and the module, then the reference clock may not be connected on the backplane. The reference clock shall be the default configuration on the module. If the reference clock is not detected after PERST# de-assertion, then the module shall switch into SRIS/SRNS mode. The device shall only enter the SRNS mode if the device is configured for this mode through a method outside the scope of this specification.

It is recommended that the backplane terminates the reference clock signals at the connector with a pull-down resistor if the clocks are not provided by the backplane.

For electrical characteristics, see the PCI Express Base Specification.

4.3.16 SMBCLK

Driven by backplane.
Mandatory for module; optional for backplane.
SMBus clock signal.
For electrical characteristics, see the SMBus Specification.

4.3.17 SMBDATA

Driven by backplane.
Mandatory for module; optional for backplane.
SMBus data signal.
For electrical and timing characteristics, see the SMBus Specification.

4.3.18 SMBRST#

Driven by backplane.
Mandatory for module; optional for backplane.
The SMBRST# signal is intended to reset the module management interface to an initial state without interrupting the PCIe link or losing NVMe controller data. When SMBRST# is low, the device shall keep the SMBCLK and SMBDATA in a high impedance state and ignore any communication on SMBCLK and SMBDATA. For electrical characteristics, see Table 4-13.

4.3.19 Signal common electrical characteristics

Unless otherwise stated in the signal description, the signal electrical characteristics are referenced to comply with one of the following tables.

TABLE 4-12 MODULE OUTPUT SIGNAL ELECTRICAL REQUIREMENTS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low voltage	4.0 mA		0.2	V
V_{HMAX}	Output high voltage			3.8	V
I_{lkg}	Output leakage current	0 V to +3.3 V	-50	+50	µA
C_{out}	Output pin capacitance			30	pF

TABLE 4-13 INPUT TO MODULE SIGNAL ELECTRICAL REQUIREMENTS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}	Input low voltage		-0.5	0.8	V
V_{IH}	Input high voltage		2.0	3.3 Vaux + 0.5	V
I_{in}	Input leakage current	0 V to +3.3 V	-10	+10	µA
C_{in}	Input pin capacitance			7	pF

5. Design Considerations

There are no additional design considerations to those described in SFF-8351 and SFF-TA-1000 unless otherwise specified in this specification.

5.1 Form Factor Airflow Considerations for 3.5” HDSFF Modules

5.1.1 Introduction

To properly enable High Density Solid State Form Factor (HDSFF) modules in the storage ecosystem, there is a need to define the system thermal solution for maintaining a safe temperature range for all system components.

5.1.2 Related Documents

Refer to the document, “Data Center Storage Equipment - Thermal Guidelines, Issues and Best Practices” published by ASHRAE Technical Committee 9.9 and available at: http://tc99.ashraetcs.org/documents/ASHRAE_Storage_White_Paper_2015.pdf

5.1.3 Thermal Specification

The HDSFF thermal specification is dependent upon the complete storage system. Typically, HDSFF modules are deployed in enclosures, which may also contain system fans, CPUs, DRAMs, power supply units, and networking components.
To enable a dense storage system, twenty four HDSFF modules may be installed in a 3U enclosure, as shown in Figure 5-1.

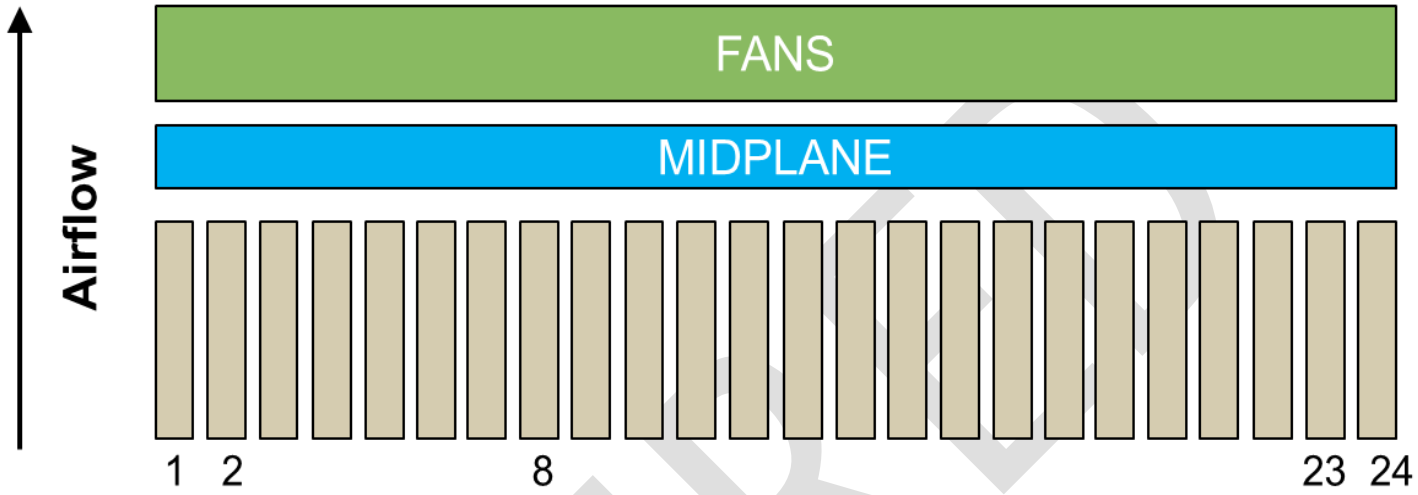

FIGURE 5-1 - TOP VIEW OF 3U STORAGE SUBSYSTEM CONFIGURATION

To physically install up to twenty four HDSFF modules in a standard 3U enclosure, a minimum module pitch of 18 mm shall be used, where the HDSFF module consumes 15 mm and 1.5 mm free space is used on each side of the HDSFF module. System designs that increase the minimum HDSFF module pitch should consider the airflow effects of too much free space surrounding the module. Airflow is needed to pass through or around the module to dissipate heat. Increased spacing may cause the airflow to avoid the module entirely may reduce the module's ability to dissipate heat.

Heatsinks shall be used on HDSFF modules. Differently shaped heatsinks may be used for 50 W and 25 W modules; however, all heatsinks shall support front load bays and top load bays. Pin fin heatsinks may be used to support both load orientations.

The ASHRAE Class A3 temperature limits shall be used for HDSFF modules. A maximum ambient temperature of 40° C shall be enabled for an altitude between 0 m and 950 m. For altitudes between 950 m and 3 050 m, the ASHRAE derating factor of 1° C per 175 m above 950 m shall be used. Operating altitudes beyond 3 050 m shall not be required.

To keep HDSFF modules within suitable temperature ranges, a nominal pressure drop and airflow needs to be established to the module. Beyond the module, storage subsystem components such as midplanes or fans may impact airflow to the HDSFF module. For 50 W HDSFF modules, a minimum pressure drop of 150 Pa and an average minimum airflow of 10 CFM per module shall be supported. For 25 W HDSFF modules, a minimum pressure drop of 75 Pa and an average minimum airflow of 7 CFM per module shall be supported. If multiple modules, such as up to twenty four modules, are used in the enclosure, the aggregate airflow may be used to satisfy the average minimum airflow per module. Selection of fan components and baffle components to ensure adequate pressure drop and airflow to the HDSFF modules and other components in the complete storage solution is vendor unique.

HDSFF modules shall maintain maximum external temperature limits. Any external surface, such as heatsink or case, shall not exceed 70° C. Furthermore, any operator touch point, such as a module carrier or handle, shall not exceed 60° C.

Multiple HDSFF modules in an enclosure may consume a large amount of power and therefore dissipate a large amount of heat. The maximum number of modules operating at maximum power at any one point in time may be limited. See Table 5-1 for the HDSFF thermal specification at 50 W and 25 W modes.

TABLE 5-1 THERMAL SPECIFICATIONS FOR A HDSFF STORAGE MODULE

3U Storage Enclosure Configuration	50 W Module	25 W Module
HDSFF Module Min Gap Space (mm)	1.5	1.5
Heatsink Requirements	Yes, X and Y directions	Yes, X and Y directions
HDSFF Module Max Inlet Air Temperature, 0 m to 950 m (° C)	40	40
HDSFF Module Max Inlet Air Temperature, 950 m to 3 050 m (° C)	40 derated 1° C/175 m	40 derated 1° C/175 m
Fan Pressure Deficit, Min (Pascal)	150	75
Airflow Requirement, Average Min (CFM)	10 CFM/ module	7 CFM/ module
Heatsink Temperature Limit (° C)	70	70
Touch Point Temperature Limit (° C)	60	60