SFF-8472

Specification for

Management Interface for SFP+

Rev 12.4.5 July 7, 2025

SECRETARIAT: SFF TWG

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This document has been released by SNIA. The SFF TWG believes that the ideas, methodologies, and technologies described in this document are technically accurate and are appropriate for widespread distribution.

ABSTRACT: This specification defines an enhanced digital interface (memory map and management interface) for monitoring and control of SFP+ optical transceivers and similar products.

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FOREWORD

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, as well as since SFF's transition to SNIA in 2016, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/join.

Change History

Rev.	Description	Date
1.0	Initial Submission of Document, Preliminary	2001-04-05
2.0	Draft Second Revision, Preliminary	2001-05-18
3.0	Draft Third Revision, Preliminary	2001-06-27
4.0	Draft Fourth Revision, Preliminary	2001-10-08
5.0	Draft Fifth Revision	2001-11-05
6.0	Draft Sixth Revision	2001-11-19
7.0	Draft Revision 7.0	2002-01-09
8.0	Draft Revision 8.0	2002-02-01
9.0	Draft Revision 9.0	2002-03-28
9.0	Revision 9.0 Approved for Technical Content	2002-05
9.2	Revision 9.2 Submitted for Publication	2002-05-30
9.3	Editorial Modifications to rev. 9.2. 9.3 Submitted for Publication	2002-08-01
9.4	Add extensions to include additional technologies. Results of Dec.5 03 discussions. Includes: Support for Multiple Application Selection Reserved values for SFF-8079 in Table 3.1, Table 3.10, Table 3.12, and Table 3.17. Additional transceiver type values in Table 3.5 Additional values in Table 3.1a, 3.5a and 3.5b Additional values in Table 3.12 General editorial modifications.	2004-05-26
9.5	Editorial Modifications to rev. 9.4. 9.5 Submitted for Publication.	2004-06-01
10.0	Add extensions to the following tables: Table 3.1b, 3.2, 3.4, 3.5, 3.5b, 3.7, 3.11, 3.12, 3.21 Editorial changes to the following tables: Table 3.2, 3.3, 3.4, 3.6, 3.7, 3.9, 3.10, 3.17 Add table 3.1a, 3.6a, 3.18a and references to 8079/8431.	2007-02-06
10.2	Editorial updates per ballot feedback. Technical update to Tables 3.1.	2007-06-01
10.3	Edits per SFF-8431	2007-12-07
10.4	Edits per SFF-8431, add bits in Table 3.5 and add Tables 3.6b and 3.6c for SFF-8431 and SFF-8461. Add Table 3.1c.	2009-01-30
11.0	Edits per FC-PI-5 (16GFC) to tables 3.6a,3.12,	2010-05-21
11.1	Table 3-2 Identifier Values and modified to point to SFF-8024 as the reference for later values and codes.	2012-10-26
11.2	Added FC-PI-6 to Table 3.6a Rate Identifier	2013-06-06
11.3	Added OM4 to Table 3.1 and Address A0h, Byte 18. Added 3200 MBytes to Table 3.5 Byte 10 Bit 3.	2013-06-11

Rev.	Description	Date
11.4	Added optional support for: retimer/CDR in transceiver; Variable Receiver Decision Threshold; Rate Select logic for 10G/8G with bypassable CDRs; Table addressing in upper half of address A2h; Laser temperature and TEC current alarms and warnings; Compliance codes for OTN 2 km, 40 km and 80 km profiles in G.959.1.	2014-07-24
11.8	Introduced a major style change. The addition of Section, Figure, and Table numbering makes correlation of previous Change History difficult for readers, so a Cross Reference of Figures and Tables was prepared.	2014-07-31
11.9	Re-defined byte 36 of Table 5-4 Transceiver Compliance Codes to be 'Extended Compliance Codes' Added definitions of the coding formats for optional laser temperature and TEC current to Section 9.2. Added Table 9-3 and Table 9-4 to illustrate the TEC current two's complement format. Corrected Table 10-2 Retimer/CDR Rate Select Logic Table 'Bit 64.1 of A2h' to be 'Bit 64.3 of A0h' Added Byte 64 Bit 5 in Table 8-3 to identify transceivers with Power Level 3 plus: o Renamed t_power_level2 to t_hpower_level in Table 8-7 and modified the contents of the parameter and conditions cells. o Changed the description for bits 1 and 0 in Table 10-1.	2014-08-14
11.9b	Moved CDR unlocked flags from byte A2h 115 to 119. Added Tx input EQ and RX output EMPH to bytes A2h 114-115 Added Tables 9-13 and 9-14 Tx input EQ and Rx output EMPH values.	2014-08-27
12.0	The mix of references to tables and pages was reduced to use only pages Consolidated the two figures in Section 4 into one. Corrected Table 4-4. Byte 12 G.959 value from 0Ah, to 6Bh Removed P1L1-2D1, P1S1-2D2, and P1L1-2D2 from Table 5-6	2014-08-28
12.1	During the review of Rev 12.0 it was recommended that: - the contents of Table 5-3 Connector Values be moved to SFF-8024. - the contents of Table 5-7 Encoding Values be returned to SFF-8024.	2014-09-12
12.2	Further updates to clarify operation of rate select with byte content 0Eh	2014-11-21
12.3	Added bits to support 64GFC speed negotiation Converted to SNIA template. Updated hyperlinks throughout.	2018-07-29

Rev.	Description	Date
12.4	Replaced BR with signaling rate and Gb/s with GBd throughout the document. Modified definition of bytes 14 and 15 in A0h, Table 4-1, to include copper cable attenuation values Added definition in Section 6.1 and 6.2. Modified definition of bytes 56-91 in A0h, Table 4-2, to be used for enhanced features when not used for External Calibration constants. Modified Fig.4-1 to show the new allocation. In Table 5-3 modified description for bit 1, byte 10 to refer to a secondary Fibre Channel Speed register 62. Added byte 62 to the table. Added value 20h in byte 13, Table 5-6 for Rate Select implementation based on PMDs. Modified name and definition of byte 19, in A0h to include cable length in base and multiplier format. Added Table 6-1. Added a High-Power Class declaration bit 6, byte 64 in Table 8-3. Added new value 09h in byte 94, Table 8-8 for SFF-8472, rev 12.4 compliance. Added Section 9.6 on Additional Enhanced Features, Table 9-11 with definitions for all bytes used, Tables 9-12 (Enhanced Control Advertisement), 9-13 (Enhanced Flag Advertisement), 9-14 (Enhanced Signal Integrity Control Advertisement), 9-15 (Enhanced Control). Modified name and definition of bit 0/byte110/A2h to clarify that this status refers to monitor data. Added bit 4, byte 118, A2h Adaptive Input EQ Fault indicator. Added bit 2, byte 118, A2h Enable Power Class 4. Modified definition of A2h, byte 119, bits 0,1,2,3 to be used for 50GE status. Added advertisement bit (A2h, byte 56, bit 4) and control bit (A2h, byte 72, bit 4) for ignoring the state of the HW RS0 and RS1 pins. Moved the RS0/1 ignore control from bit 4/ byte 72 to bit 4/ byte 73. Added bit 4/ byte 72 Rx Output Enhanced EQ Control Override control bit. Added Note 2 to Table 9-15 for recommended use of Tx Squelch Implementation control.	2021-03-31

Rev.	Description	Date
12.5	Section 1. Updated scope text. Section 2. Update References. Section 3. Keywords and Definitions consistent with other SFF documents. Glossary from SFF-8636. Section 4. Refresh figures, tables, corrections. Section 4.1. Update figure clarifying pages and add new pages. Section 4.3. Added page description table. Section 5 to 7. No major technical change. Section 8. Previously reserved bit A0h Byte 65 Bit 0; now used to indicate that other pages may exist that requires the host to perform one or multiple additional operations to determine whether a page exists. Added bit to advertisement for Remote Performance Monitoring Registers, in A0h Byte 92 Table 8-5 Section 9. Clarification on A2h byte 95 check-sum calculations. Section 10. Reorganized and moved description of registers in A2h Page 02h. Section 10.1. A2:118.1 added note for PL4 power level 4. Indicate State 4 once the module has reached Power Level 4. Section 10.4 move to Section 12.2 for RDT. Section 11. Describes paging (paging was previously not clearly defined), clarifying Pg 00h/01h. Section 12. Describes A2h Page 02h management together with SFF-8690. Section 12.1. Define feature advertisement for A2h Page 02h. Section 12.2. Consolidate all RDT registers and define new features for RDT. Previously RDT was in section 10.6 of Revision 12.4. Section 12.3. New Remote Performance Monitoring memory map. Section 13. New High Accuracy Timing Specification, Calibration memory map. Other editorial changes. Change nsec to ns, 0xABCD to ABCDh. Fix inconsistencies. Change TWI to 2-wire.	2025-06-09

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1 Scope

This document defines a memory map and digital management interface for monitoring and control of SFP+ optical transceivers and similar modules.

The interface is an extension of the 2-wire interface ID interface defined in the GBIC specification as well as the SFP MSA. Both specifications define a 256 byte memory map which is accessible over a 2-wire serial interface at the 8 bit address 1010000x (A0h). The enhanced digital management interface makes use of the 8 bit address 1010001x (A2h), so the originally defined 2-wire interface ID memory map remains unchanged. The interface is backward compatible with both the GBIC specification and the SFP MSA.

In order to provide memory space for future extensions, multiple optional pages are defined for the upper 128 bytes of the A2h memory space.

2 References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:

INF-8074	SFP (Small Formfactor Pluggable) 1 Gb/s Transceiver
REF-TA-1011	Reference Guide for Cross Reference to Selected SFF Connectors and Modules
SFF-8024	SFF Module Management Reference Code Tables
SFF-8053	GBIC (Gigabit Interface Converter)
SFF-8079	SFP Rate and Application Selection
SFF-8089	SFP Rate and Application Codes
SFF-8418	SFP+ 10 Gb/s Electrical Interface
SFF-8419	SFP+ Power and Low Speed Interface
SFF-8431	SFP+ 10 Gb/s and Low Speed Electrical Interface
SFF-8690	Tunable SFP+ Memory Map
INCITS FC-PI-4/5/6/7/8	Fibre Channel Physical Interface 4/5/6/7/8
IEEE Std 754	Standard for Floating-Point Arithmetic
IEEE Std 802.3	IEEE Standard for Ethernet
IEEE Std 802.3cx-2023	Improved PTP timestamping accuracy
IEEE Std 1588	IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems
MOPA	Mobile Optical Pluggable Alliance. "MOPA Remote Monitoring Specifications v1.0" https://mopa-alliance.org/papers-and-presentations/
ITU-T G.698.4	Multichannel bi-directional DWDM applications with port agnostic single-channel optical interfaces

H. Peek and P. Jansweijer, "White Rabbit Absolute Calibration", *2018 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control, and Communication (ISPCS)*, Geneva, Switzerland, 2018, pp. 1-5, doi: 10.1109/ISPCS.2018.8543067. https://ieeexplore.ieee.org/document/8543067

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee, can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

NUMBERING CONVENTIONS: The American convention of numbering is used (i.e., the thousands and higher multiples are separated by a comma and a period is used as the decimal point).

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

NUMERALS: Numerals without suffix are understood as numbers in decimal notation (e.g. 16). Hexadecimal literals are marked with a suffix ‘h’ (e.g. 10h), often written with leading zeroes (0010h). Binary literals are marked with a suffix ‘b’ (e.g. 10000b), often written with leading zeroes (00010000b). The suffixes may be omitted for unambiguous cases like 0=0b=0h and 1=1b=1h. Spaces may be inserted to make long hexadecimal or binary digit strings readable (e.g. 0001 0000b).

3 Keywords, Acronyms and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall implemented as defined by the specification. Describing a feature as optional in the text is an informational callout to assist the reader.

Reserved: Where the term is used for a signal on a connector contact, the function is set aside for future standardization. It is not available for vendor-specific use. Where this term is used for bits, bytes, fields, and values; the bits, bytes, fields, and values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies to the restricted designation, then the restricted bit, byte, word, or field shall be treated as a value whose definition is not in scope of this document and is not interpreted by this specification.

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbrevations

B	binary (suffix to preceding binary based number)
ºC	degrees Celsius (thermal unit associated with a value)
CDR	clock and data recovery
COR	clear on read
dB	decibel (base 10 logarithmic unit)
dBm	decibels above one milliwatt
DDM	Digital Diagnostics Monitoring
Gbps	gigabits per second (i.e., 10^9 bits per second)
GHz	gigahertz (i.e., 10^9 cycles per second)
h	hexadecimal (suffix to preceding hexadecimal based number)
HEE	Head End Equipment
Hz	hertz (i.e., cycles per second)
kHz	kilohertz (i.e., 10^3 cycles per second)
km	kilometer (i.e., 10^3 meters)
LSB	least significant bit
m	meter (unit of length)
mA	milliampere (i.e., 10^-3 amperes)
Mbps	megabits per second (i.e., 10^6 bits per second)
MHz	megahertz (i.e., 10^6 cycles per second)
ms	millisecond (i.e., 10^-3 seconds)
MSB	most significant bit
mV	millivolt (i.e., 10^-3 volts)
mW	milliwatt (i.e., 10^-3 watts)
nm	nanometer (i.e., 10^-9 meters)
ns	nanosecond (i.e., 10^-9 seconds)
P-P	peak-to-peak
ps	picosecond (i.e., 10^-12 seconds)
RDDM	Remote Digital Diagnostics Monitoring
RDT	Receiver Decision Threshold
RPM	Remote Performance Monitoring
Rx	receiver
s	second (unit of time)
TC	temperature controller (e.g. thermo-electric cooler)
TEE	Tail End Equipment
Tx	transmitter
µA	microampere (i.e., 10^-6 amperes)
µm	micrometer (i.e., 10^-6 meters)
µV	microvolt (i.e., 10^-6 volts)
µW	microwatt (i.e., 10^-6 watts)
V	volt (unit of electrical potential)
W	watt (unit of electrical power)

3.3 Definitions

Bit Organization

8-bit fields have the most significant bit at bit 7, and 16-bit fields have the most significant bit at bit 15. See Figure 3-1.

								MSB			8-bit Field				LSB
MSB							16-bit Field								LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 3-1 Bit Organization

Big Endian

The default byte order of multi-byte registers representing numerical types is Big Endian, that is the lowest byte address contains the most significant byte of the multi-byte value.

4 Memory Organization

4.1 Introduction

The enhanced digital diagnostic interface is a superset of the MOD_DEF interface defined in the SFP MSA document dated September 14, 2000, later submitted to the SFF Committee as INF-8074. The 2-wire interface pin definitions, hardware, and timing were initially defined there. SFF-8431, later superseded by SFF-8419 define the low speed electrical and management interface specifications for SFP+. Pluggable modules such as SFP+, SFP28 and later SFP form factors that are compliant to SFF-8431 and SFF-8419 hereafter referred to as SFP+ may use this management interface. However, SFP modules capable of 100 Gb/s or more are expected to use CMIS (see SFF-TA-1011).

This document describes an extension to the memory map defined in the SFP MSA (see Figure 4-1). The enhanced interface uses the 2-wire serial bus address 1010001X, commonly referred to as A2h, and where X can be 1 for a read operation or 0 for a write operation. Reads from this address provide diagnostic information about the module's present operating conditions. The transceiver generates this diagnostic data by digitization of internal analog signals. Calibration and alarm/warning threshold data is written during device manufacture.

All bits that are reserved for SFF-8472 shall be set to zero and/or ignored.

Bits labeled as reserved or optional for other usage, such as for SFF-8079, shall be implemented per such other documents, or set to zero and/or ignored if not implemented.

If optional features for SFF-8472 are implemented, they shall be implemented as defined in SFF-8472. If they are not implemented or not applicable to the device, then write bits shall be ignored, and status bits shall be set to zero.

Additional A0h and A2h memory allocations were provided in revision 9.5 to support multi-rate and application selection as defined in the SFF-8079 and SFF-8089 specifications.
Various extensions have been made in revisions since revision 10.4. These include adding new connectors, industry form factors, transceiver codes and controls for transceiver features.

4.2 2-wire Interface Fields

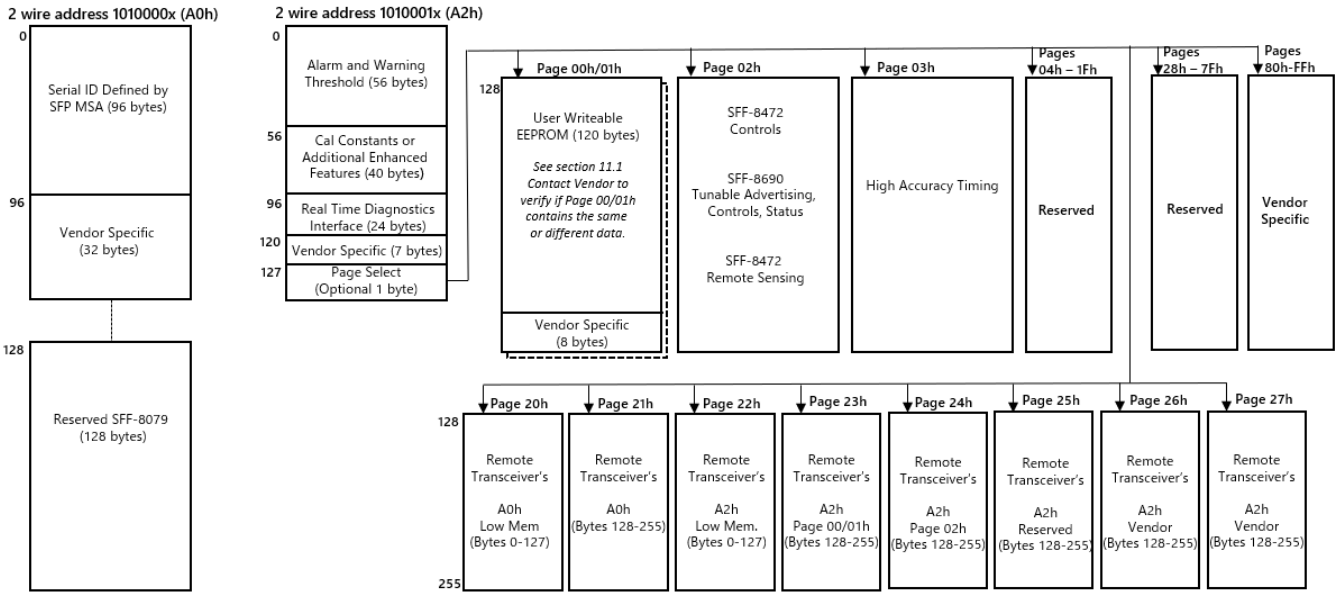

Figure 4-1 2-wire Memory Map Summary

4.3 Pages

The optional Page Select byte expands the range of information that can be provided by the manufacturer. Where used in this specification the Page ID is defined in hexadecimal. Note: Vendor Specific Page IDs may be password-protected. The location of the password is not defined in SFF-8472 and will be defined by the vendor.

The use of Paging System is Optional, and when used the pages shall be used as described in the following table.

In this revision, see Table 8-3, A0h.Byte65.Bit0, which was previously reserved in SFF-8472 Rev 12.4, is now used to indicate that there are additional pages. If this bit is 0b, then the transceiver module has only legacy pages 00/01 and 02h. If this bit is 1b, there are one or more additional pages to be discovered. To discover if a page is supported, the host writes A2h.Byte127 (Page Select) byte, wait momentarily until the page change is complete and then read-back the page select byte. If the page is supported then the page select byte will return what is being written, otherwise it will return 00h. Once the page has been selected, additional validations should be performed to confirm the content of the page, for example for Page 03h, the first 2 bytes, byte 128-129 are format ID as well as the last byte being CC_CALIB, a checksum. This is to ensure that modules that are non-compliant to the additional page description are appropriately managed.

Table 4-1 Page Description

Page	Description of Pages
00h	Contains the legacy unpaged upper memory of A2h.
01h	Both Page 00h and 01h are defined to point to the same information for backward compatibility.
02h	Page used to implement Tunability as per SFF-8690. Page used for RDT control and Remote Performance Monitoring.
03h	High Accuracy Timing Calibrations
04h-1Fh	Reserved
20h	Remote Transceiver SFF-8472 A0h Bytes 0-127
21h	Remote Transceiver SFF-8472 A0h Bytes 128-255
22h	Remote Transceiver SFF-8472 A2h Bytes 0-127
23h	Remote Transceiver SFF-8472 A2h Page 00h/01h Bytes 128-255
24h	Remote Transceiver SFF-8472 A2h Page 02h Bytes 128-255
25h	Remote Transceiver Reserved
26h	Remote Transceiver Vendor Specific
27h	Remote Transceiver Vendor Specific
28h-7Fh	Reserved
80h-FFh	Vendor Specific

4.3.1 Remote Transceiver Pages

In SFF-8472 Rev 12.5 and above, if the optional Remote Performance Monitoring (RPM) feature is supported as described in Section 12.3, a remote transceiver's memory map pages are presented and accessible at the local pages 20h-27h. The content of these pages is identical to the page definition of their respective mapped pages however the host shall account for the time delays for the RPM system to update this content.

As an example, to access the remote transceiver's A2h Page 02h, read from Page 22h. One method of obtaining remote transceivers data is defined by MOPA "Remote Monitoring Specifications v1.0 or later revisions".

4.4 Data Fields

Table 4-2 Data Fields - Address A0h

A0h	# Bytes	Name	Description
BASE ID FIELDS			
0	1	Identifier	Type of transceiver (see Table 5-1)
1	1	Ext. Identifier	Extended identifier of type of transceiver (see Table 5-2)
2	1	Connector	Code for connector type (see SFF-8024 SFF Module Management Reference Code Tables)
3-10	8	Transceiver	Code for electronic or optical compatibility (see Table 5-3)
11	1	Encoding	Code for high speed serial encoding algorithm (see SFF-8024 SFF Module Management Reference Code Tables)
12	1	Signaling Rate, Nominal	Nominal signaling rate, units of 100 MBd. (see details for rates > 25.4 GBd)
13	1	Rate Identifier	Type of rate select functionality (see Table 5-6)
14	1	Length (SMF, km) or Copper Cable Attenuation	Link length supported for single-mode fiber, units of km, or copper cable attenuation in dB at 12.9 GHz
15	1	Length (SMF) or Copper Cable Attenuation	Link length supported for single-mode fiber, units of 100 m, or copper cable attenuation in dB at 25.78 GHz
16	1	Length (50 um, OM2)	Link length supported for 50 um OM2 fiber, units of 10 m
17	1	Length (62.5 um, OM1)	Link length supported for 62.5 um OM1 fiber, units of 10 m
18	1	Length (OM4 or copper cable)	Link length supported for 50 um OM4 fiber, units of 10 m. Alternatively, copper or direct attach cable, units of m
19	1	Length (OM3) or Cable length, additional	Link length supported for 50 um OM3 fiber, units of 10 m. Alternatively, copper or direct attach cable multiplier and base value
20-35	16	Vendor name	SFP vendor name (ASCII)
36	1	Transceiver	Code for electronic or optical compatibility (see Table 5-3)
37-39	3	Vendor OUI	SFP vendor IEEE company ID
40-55	16	Vendor PN	Part number provided by SFP vendor (ASCII)
56-59	4	Vendor rev	Revision level for part number provided by vendor (ASCII)
60-61	2	Wavelength	Laser wavelength (Passive/Active Cable Specification Compliance)
62	1	Fibre Channel Speed 2	Transceiver's Fibre Channel speed capabilities
63	1	CC_BASE	Check code for Base ID Fields (addresses 0 to 62)
EXTENDED ID FIELDS			
64-65	2	Options	Indicates which optional transceiver signals are implemented (see Table 8-3)
66	1	Signaling Rate, max	Upper signaling rate margin, units of % (see details for rates > 25.4 GBd)
67	1	Signaling Rate, min	Lower signaling rate margin, units of % (see details for rates > 25.4 GBd)
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)
84-91	8	Date code	Vendor's manufacturing date code (see Table 8-4)
92	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the transceiver (see Table 8-5)
93	1	Enhanced Options	Indicates which optional enhanced features are implemented (if any) in the transceiver (see Table 8-6)
94	1	SFF-8472 Compliance	Indicates which revision of SFF-8472 the transceiver complies with (see Table 8-8)
95	1	CC_EXT	Check code for the Extended ID Fields (addresses 64 to 94)
VENDOR SPECIFIC ID FIELDS			
96-127	32	Vendor Specific	Vendor Specific EEPROM
128-255	128	Reserved	Reserved (was assigned to SFF-8079)

Table 4-3 Data Fields - Address A2h

A2h	# Bytes	Name	Description
DIAGNOSTIC AND CONTROL/STATUS FIELDS			
0-39	40	A/W Thresholds	Diagnostic Flag Alarm and Warning Thresholds (see Table 9-5)
40-55	16	Optional A/W Thresholds	Thresholds for optional Laser Temperature and TEC Current alarms and warnings (see Table 9-5)
56-91	36	Ext Cal Constants or Additional Enhanced Features	Diagnostic calibration constants for optional External Calibration (see Table 9-6) if External Calibration bit, A0h, byte 92, bit 4 is 1 Additional Enhanced Features advertisement, control and status (see Table 9-11) if External Calibration bit, A0h, byte 92, bit 4 is 0
92-94	3	Reserved	
95	1	CC_DMI	Check code for Base Diagnostic Fields. The range of addresses for this check code depends on the value of the external calibration bit, A0h Byte 92 bit 4. See section 9.7
96-105	10	Diagnostics	Diagnostic Monitor Data (internally or externally calibrated) (see Table 9-16)
106-109	4	Optional Diagnostics	Monitor Data for Optional Laser temperature and TEC current (see Table 9-16)
110	1	Status/Control	Optional Status and Control Bits (see Table 9-16)
111	1	Reserved	Reserved (was assigned to SFF-8079)
112-113	2	Alarm Flags	Diagnostic Alarm Flag Status Bits (see Table 9-17)
114	1	Tx Input EQ control	Tx Input equalization level control (see Table 9-18)
115	1	Rx Out Emphasis control	Rx Output emphasis level control (see Table 9-19)
116-117	2	Warning Flags	Diagnostic Warning Flag Status Bits (see Table 9-17)
118-119	2	Ext Status/Control	Extended module control and status bytes (see Table 10-1)
GENERAL USE FIELDS			
120-126	7	Vendor Specific	Vendor specific memory addresses (see Table 10-3)
127	1	Table Select	Optional Page Select (see Table 10-3)

Table 4-4 Data Fields - Address A2h Page Tables

A2h	# Bytes	Name	Description
Page 00-01h			
128-247	120	User EEPROM	User writable non-volatile memory (see Table 11-1)
248-255	8	Vendor Control	Vendor specific control addresses (see Table 11-2)
Page 02h			
128-255	128	SFF-8472, SFF-8690	Register definitions detailed in this specification and in SFF-8690. See section 12 for a summary of the memory map.

The examples of transceiver and copper cable performance codes below are provided for illustration. Compliance to additional standards and technologies is possible so bits other than those indicated in each row may also be set to indicate compliance to these additional standards and technologies.

Table 4-5 Transceiver Identification/Performance Examples

		Address A0h						
		Rate and Distance Fields						Wave-length Fields
Transceiver Type	**Transceiver Description**	**Byte 12**	**Byte 14**	**Byte 15**	**Byte 16**	**Byte 17**	**Byte 18**	**Bytes 60 & 61**
100-M5-SN-I and 100-M6-SN-I	1062.5 MBd MM 850 nm 500 m / 50 um, 300 m / 62.5 um	0Bh	00h	00h	32h	1Eh	00h	0352h
200-SM-LC-L and 100-SM-LC-L	2125 MBd and 1062.5 MBd 10 km SM 1310 nm	15h[3]	0Ah[3]	64h[3]	00h	00h	00h	051Eh
400-M5-SN-I and 400-M6-SN-I 4	4250 MBd MM 850 nm 150 m / 50 um, 70 m / 62.5 um	2Bh[3]	00h	00h	0Fh[3]	07h[3]	00h	0352h
400-SM-LC-M	4250 MBd SM 1310 nm 4 km "medium" length	2Bh[3]	04h	28h	00h	00h	00h	051Eh
400-SM-LC-L	4250 MBd SM 1310 nm 10 km "long" length	2Bh[3]	0Ah	64h	00h	00h	00h	051Eh
200-SM-LL-V and 100-SM-LL-V	2125 MBd and 1062.5 MBd 50 km SM 1550 nm	15h[3]	32h	FFh	00h	00h	00h	060Eh
ESCON SM	200 MBd 20 km SM 1310 nm	02h	14h	C8h	00h	00h	00h	051Eh
100BASE-LX10	125 MBd 10 km SM 1310 nm	01h	0Ah	64h	00h	00h	00h	051Eh
1000BASE-T	1250 MBd 100 m Cat 5 Cable	0Dh[1]	00h	00h	00h	00h	64h	0000h
1000BASE-SX	1250 MBd 550 m MM 850 nm	0Dh[1]	00h	00h	37h[2]	1Bh[2]	00h	0352h
1000BASE-LX	1250 MBd 5 km SM 1310 nm	0Dh[1]	05h	32h	37h	37h	00h	051Eh
1000BASE-LX10	1250 MBd 10 km SM 1310 nm	0Dh[1]	0Ah	64h	00h	00h	00h	051Eh
1000BASE-BX10-D	1250 MBd 10 km SM 1490 nm downstream TX	0Dh[1]	0Ah	64h	00h	00h	00h	05D2h
1000BASE-BX10-U	1250 MBd 10 km SM 1310 nm upstream TX	0Dh[1]	0Ah	64h	00h	00h	00h	051Eh
OC3/STM1 SR-1	155 MBd 2 km SM 1310 nm	02h	02h	14h	00h	00h	00h	051Eh
OC12/STM4 LR-1	622 MBd 40 km SM 1310 nm	06h[3]	28h	FFh	00h	00h	00h	051Eh
OC48/STM16 LR-2	2488 MBd 80 km SM 1550 nm	19h[3]	50h	FFh	00h	00h	00h	060Eh
G959.1 P1I1-2D1	10709 MBd 2 km SM 1310 nm	6Bh	02h[5]	14h	00h	00h	00h	051Eh
G959.1 P1S1-2D2	10709 MBd 40 km SM 1550 nm	6Bh	28h[5]	FFh	00h	00h	00h	060Eh
G959.1 P1L1-2D2	10709 MBd 80 km SM 1550 nm	6Bh	50h[5]	FFh	00h	00h	00h	060Eh

NOTES:

1. By convention 1.25 GBd should be rounded up to 0Dh (13 in units of 100 MBd) for Ethernet 1000BASE-X.
2. Link distances for 1000BASE-SX variants vary between high and low bandwidth cable types per IEEE Std 802.3 Clause 38. The values shown are 270 m [275 m per 802.3] for 62.5 um / 200 MHz*km cable and 550 m for 50 um / 500 MHz*km cable.
3. For transceivers supporting multiple data rates (and hence multiple distances with a single fiber type) the highest data rate and the distances achievable at that data rate are to be identified in these fields.
4. In this example, the transceiver supports 400-M5-SN-I, 200-M5-SN-I, 100-M5-SN-I, 400-M6-SN-I, 200-M6-SN-I and 100-M6-SN-I.
5. These target distances are for classification and not for specification.

Table 4-6 Copper Cable Identification/Performance Examples

	Address A0h		
	Link Length and Transmitter Technology		Laser wavelength and Cable Specification Compliance
Cable Type	**Byte 7**	**Byte 8**	**Bytes 60 and 61**
Passive Cable compliant to SFF-8431 Appendix E	00h	04h	0100h
Active cable compliant to SFF-8431 Appendix E	00h	08h	0100h
Active cable compliant to SFF-8431 limiting	00h	08h	0400h
Active cable compliant to both SFF-8431 limiting and FC-PI-4 limiting	00h	08h	0C00h

5 Identifiers and Codes

5.1 Physical Device Identifier Values [Address A0h, Byte 0]

The identifier value identifies the physical device described by 2-wire interface information. This value shall be included in the 2-wire interface data.

Table 5-1 Physical Device Identifier Values

A0h	Value	Description
0	00h	Unknown or unspecified
	01h	GBIC
	02h	Module/connector soldered to motherboard (using SFF-8472)
	03h	SFP/SFP+/SFP28 and later form factors using SFF-8472 management interface.
	04-7Fh	Not used by this specification. These values are maintained in the Transceiver References section (Section 4.2) of SFF-8024.
	80-FFh	Vendor specific

NOTE: SFF-8024 Section 4.2 Transceiver References contains the identifier 0Bh DWDM-SFP/SFP+ modules not using SFF-8472 and identifies 20h SFP+ with Common Management Interface Specifications. Not all SFP+ form factor modules use SFF-8472 and the host has to be able to identify the module management interfaces.

5.2 Physical Device Extended Identifier Values [Address A0h, Byte 1]

The extended identifier value provides additional information about the transceiver. The field should be set to 04h for all SFP modules indicating 2-wire interface ID module definition. In many cases, a GBIC elects to use MOD_DEF 4 to make additional information about the GBIC available, even though the GBIC is actually compliant with one of the six other MOD_DEF values defined for GBICs. The extended identifier allows the GBIC to explicitly specify such compliance without requiring the MOD_DEF value to be inferred from the other information provided.

Table 5-2 Physical Device Extended Identifier Values

A0h	Value	Description of connector
1	00h	GBIC definition is not specified or the GBIC definition is not compliant with a defined MOD_DEF. See product specification for details.
	01h	GBIC is compliant with MOD_DEF 1
	02h	GBIC is compliant with MOD_DEF 2
	03h	GBIC is compliant with MOD_DEF 3
	04h	GBIC/SFP function is defined by 2-wire interface ID only
	05h	GBIC is compliant with MOD_DEF 5
	06h	GBIC is compliant with MOD_DEF 6
	07h	GBIC is compliant with MOD_DEF 7
	08-FFh	Reserved

5.3 Connector Values [Address A0h, Byte 2]

The connector value indicates the external optical or electrical cable connector provided as the media interface. This value shall be included in the 2-wire interface data. These values are maintained in the Transceiver or Cable Management section of SFF-8024.

5.4 Transceiver Compliance Codes [Address A0h, Bytes 3 to 10, 36 and 62]

The following bit significant indicators in bytes 3 to 10 and code in byte 36 define the electronic or optical interfaces that are supported by the transceiver. At least one bit shall be set in this field. For Fibre Channel transceivers, the Fibre Channel speed, transmission media, transmitter technology, and distance capability shall all be indicated. SONET compliance codes are completed by including the contents of Table 5-4. Ethernet, ESCON and InfiniBand codes have been included to broaden the available applications of SFP transceivers.

Table 5-3 Transceiver Compliance Codes

A0h	Bit [1]	Description
Extended Specification Compliance Codes		
36	7-0	See SFF-8024 Table 4-4
10G Ethernet Compliance Codes		
3	7	10GBASE-ER
3	6	10GBASE-LRM
3	5	10GBASE-LR
3	4	10GBASE-SR
InfiniBand Compliance Codes		
3	3	1X SX
3	2	1X LX
3	1	1X Copper Active
3	0	1X Copper Passive
ESCON Compliance Codes		
4	7	ESCON MMF, 1310 nm LED
4	6	ESCON SMF, 1310 nm Laser
SONET Compliance Codes		
4	5	OC-192, short reach [2]
4	4	SONET reach specifier bit 1
4	3	SONET reach specifier bit 2
4	2	OC-48, long reach [2]
4	1	OC-48, intermediate reach [2]
4	0	OC-48, short reach [2]
5	7	Reserved
5	6	OC-12, single mode, long reach [2]
5	5	OC-12, single mode, inter. reach [2]
5	4	OC-12, short reach [2]
5	3	Reserved
5	2	OC-3, single mode, long reach [2]
5	1	OC-3, single mode, inter. reach [2]
5	0	OC-3, short reach [2]
Ethernet Compliance Codes		
6	7	BASE-PX [3]
6	6	BASE-BX10 [3]
6	5	100BASE-FX
6	4	100BASE-LX/LX10
6	3	1000BASE-T
6	2	1000BASE-CX
6	1	1000BASE-LX [3]
6	0	1000BASE-SX

A0h	Bit [1]	Description
Fibre Channel Link Length		
7	7	very long distance (V)
7	6	short distance (S)
7	5	intermediate distance (I)
7	4	long distance (L)
7	3	medium distance (M)
Fibre Channel Technology		
7	2	Shortwave laser, linear Rx (SA) [7]
7	1	Longwave laser (LC) [6]
7	0	Electrical inter-enclosure (EL)
8	7	Electrical intra-enclosure (EL)
8	6	Shortwave laser w/o OFC (SN) [7]
8	5	Shortwave laser with OFC (SL) [4]
8	4	Longwave laser (LL) [5]
SFP+ Cable Technology		
8	3	Active Cable [8]
8	2	Passive Cable [8]
8	1-0	Reserved
Fibre Channel Transmission Media		
9	7	Twin Axial Pair (TW)
9	6	Twisted Pair (TP)
9	5	Miniature Coax (MI)
9	4	Video Coax (TV)
9	3	Multimode, 62.5 um (M6)
9	2	Multimode, 50 um (M5, M5E)
9	1	Reserved
9	0	Single Mode (SM)
Fibre Channel Speed		
10	7	1200 MBytes/s
10	6	800 MBytes/s
10	5	1600 MBytes/s
10	4	400 MBytes/s
10	3	3200 MBytes/s
10	2	200 MBytes/s
10	1	See byte 62 "Fibre Channel Speed 2"
10	0	100 MBytes/s
Fibre Channel Speed 2		
62	7-1	Reserved
62	0	64 GFC

NOTES:

1. Bit 7 is the high order bit and is transmitted first in each byte.
2. SONET compliance codes require reach specifier bits 3 and 4 in Table 5-4 to completely specify transceiver capabilities.
3. Ethernet LX, PX and BX compliance codes require the use of the Signaling Rate, Nominal value (byte 12), link length values for single-mode and two types of multimode fiber (Bytes 14-17) and wavelength value for the laser (Bytes 60 and 61) as specified in Table 4-2 to completely specify transceiver capabilities. See Table 4-4 and Table 5-6 for examples of setting values for these parameters.
4. Open Fiber Control (OFC) is a legacy eye safety electrical interlock system implemented on Gigabit Link Module (GLM) type transceiver devices and is not considered relevant to SFP transceivers.
5. Laser type "LL" (long length) is usually associated with 1550 nm, narrow spectral width lasers capable of very long link lengths.

A0h	Bit [1]	Description		A0h	Bit [1]	Description
6. Laser type "LC" (low cost) is usually associated with 1310 nm lasers capable of medium to long link lengths. 7. Classes SN and SA are mutually exclusive. Both are without OFC. SN has a limiting Rx output, SA has a linear Rx output, per FC-PI-4. 8. Refer to bytes 60 and 61 for definitions of the application copper cable standard specification.						

5.4.1 SONET Reach Specifier Bits [Address A0h, Byte 4, bits 3-4]

The SONET compliance code bits allow the host to determine with which specifications a SONET transceiver complies. For each rate defined in Table 5-3 (OC-3, OC-12, OC-48), SONET specifies short reach (SR), intermediate reach (IR), and long reach (LR) requirements. For each of the three rates, a single short reach (SR) specification is defined. Two variations of intermediate reach (IR-1, IR-2) and three variations of long reach (LR-1, LR-2, and LR-3) are also defined for each rate. Byte 4, bits 0-2, and byte 5, bits 0-7 allow the user to determine which of the three reaches has been implemented - short, intermediate, or long. Two additional 'specifier' bits (byte 4, bits 3-4) are necessary to discriminate between different intermediate or long reach variations.

Table 5-4 SONET Reach Specifier Bits

Speed	Reach	Specifier bit 1 (Byte 4 bit 4)	Specifier bit 2 (Byte 4 bit 3)	Description
OC 3/OC 12/OC 48/OC 192	Short	0	0	SONET SR compliant [1]
OC 3/OC 12/OC 48/OC 192	Short	1	0	SONET SR-1 compliant [2]
OC 3/OC 12/OC 48	Intermediate	1	0	SONET IR-1 compliant
OC 3/OC 12/OC 48	Intermediate	0	1	SONET IR-2 compliant
OC 3/OC 12/OC 48	Long	1	0	SONET LR-1 compliant
OC 3/OC 12/OC 48	Long	0	1	SONET LR-2 compliant
OC 3/OC 12/OC 48	Long	1	1	SONET LR-3 compliant
NOTES: 1. OC 3/OC 12 SR is multimode based short reach 2. OC 3/OC 12 SR-1 is single-mode based short reach				

5.4.2 Examples of Transceiver Compliance Codes [Address A0h, Bytes 3-10]

Table 5-5 provides examples of the contents of bytes 3 to 10 for several transceiver types.

Table 5-5 Transceiver Identification Examples

		Address A0h Transceiver Code Fields							
Transceiver Type	**Transceiver Description**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**	**Byte 8**	**Byte 9**	**Byte 10**
100-M5-SN-I and 100-M6-SN-I	1062.5 MBd MM 850 nm 500 m / 50 um, 300 m / 62.5 um	00h	00h	00h	00h	20h	40h	0Ch	01h
200-SM-LC-L and 100-SM-LC-L	2125 MBd 10 km SM 1310 nm	00h	00h	00h	00h	12h	00h	01h	05h
400-M5-SN-I and 400-M6-SN-I [1]	4/2/1 GBd MM 850 nm 150 m / 50 um, 70 m / 62.5 um	00h	00h	00h	00h	20h	40h	0Ch	15h
800-M5-SN-I and 800-M6-SN-I [1]	8/4/2 GBd MM 850 nm 50 um & 62.5 um	00h	00h	00h	00h	20h	40h	0Ch	54h
400-SM-LC-M [1]	4250 MBd SM 1310 nm 4 km "medium" length	00h	00h	00h	00h	0Ah	00h	01h	15h
400-SM-LC-L [1]	4250 MBd SM 1310 nm 10 km "long" length	00h	00h	00h	00h	12h	00h	01h	15h
200-SM-LL-V and 100-SM-LL-V	2125 MBd 50 km SM 1550 nm	00h	00h	00h	00h	80h	10h	01h	05h
1000BASE-T	1250 MBd 100 m Cat 5 Cable	00h	00h	00h	08h	00h	00h	00h	00h
1000BASE-SX	1250 MBd 550 m MM 850 nm	00h	00h	00h	01h	00h	00h	00h	00h
1000BASE-LX	1250 MBd 5 km SM 1310 nm	00h	00h	00h	02h[2]	00h	00h	00h	00h
1000BASE-LX10	1250 MBd 10 km SM 1310 nm	00h	00h	00h	02h[2]	00h	00h	00h	00h
10GBASE-SR	10.3125 GBd 300 m OM3 MM 850 nm	10h	00h	00h	00h	00h	00h	00h	00h
10GBASE-LR	10.3125 GBd 10 km SM 1310 nm	20h	00h	00h	00h	00h	00h	00h	00h
OC3/STM1 SR-1	155 MBd 2 km SM 1310 nm	00h	00h	01h	00h	00h	00h	00h	00h
OC12/STM4 LR-1	622 MBd 40 km SM 1310 nm	00h	10h	40h	00h	00h	00h	00h	00h
OC48/STM16 LR-2	2488 MBd 80 km SM 1550 nm	00h	0Ch	00h	00h	00h	00h	00h	00h
	10GE Passive copper cable with SFP ends [3,4]	00h	00h	00h	00h	00h	04h	00h	00h
	10GE Active cable with SFP ends [3,4]	00h	00h	00h	00h	00h	08h	00h	00h
	8/4/2G Passive copper cable with SFP ends[3]	00h	00h	00h	00h	00h	04h	00h	54h
	8/4/2G Active cable with SFP ends[3]	00h	00h	00h	00h	00h	08h	00h	54h

NOTES:

1. The assumption for this example is the transceiver is "4-2-1" compatible, meaning operational at 4.25 GBd, 2.125 GBd and 1.0625 GBd.
2. To distinguish between 1000BASE-LX and 1000BASE-LX10, A0h Bytes 12 to 18 must be used. See Table 4-2 and Table 4-3 for more information.
3. See A0h Bytes 60 and 61 for compliance of these media to industry electrical specifications.
4. For Ethernet and SONET applications, rate capability of a link is identified in A0h Byte 12 [nominal signaling rate

Transceiver Type	Transceiver Description	Address A0h Transceiver Code Fields							
		Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
identifier]. This is due to no formal IEEE designation for passive and active cable interconnects, and lack of corresponding identifiers in Table 5-3.									

5.5 Encoding [Address A0h, Byte 11]

The encoding value indicates the encoding mechanism that is the nominal design target of the particular transceiver. The value shall be contained in the 2-wire interface data. These values are maintained in the Transceiver or Cable Management section of SFF-8024.

5.6 Signaling rate, nominal [Address A0h, Byte 12]

The nominal signaling rate is specified in units of 100 MBd, rounded off to the nearest 100 MBd. The signaling rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of FFh indicates the signaling rate is greater than 25.4 GBd and addresses 66 and 67 are used to determine the signaling rate. A value of 0 indicates that the signaling rate is not specified and must be determined from the transceiver technology. The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value.

5.7 Rate Identifier [Address A0h, Byte 13]

The rate identifier byte refers to several (optional) industry standard definitions of Rate_Select or Application_Select control behaviors, intended to manage transceiver optimization for multiple operating rates.

Table 5-6 Rate Identifier

A0h	Value	Description
13	00h	Unspecified
	01h	SFF-8079 (4/2/1G Rate_Select & AS0/AS1)
	02h	SFF-8431 (8/4/2G Rx Rate_Select only)
	03h	Unspecified *
	04h	SFF-8431 (8/4/2G Tx Rate_Select only)
	05h	Unspecified *
	06h	SFF-8431 (8/4/2G Independent Rx & Tx Rate_select)
	07h	Unspecified *
	08h	FC-PI-5 (16/8/4G Rx Rate_select only) High=16G only, Low=8G/4G
	09h	Unspecified *
	0Ah	FC-PI-5 (16/8/4G Independent Rx, Tx Rate_select) High=16G only, Low=8G/4G
	0Bh	Unspecified *
	0Ch	FC-PI-6 (32/16/8G Independent Rx, Tx Rate_Select) High=32G only, Low = 16G/8G
	0Dh	Unspecified *
	0Eh	10/8G Rx and Tx Rate_Select controlling the operation or locking modes of the internal signal conditioner, retimer or CDR, according to the logic table defined in Table 10-2, High Bit Rate (10G) =9.95-11.3 Gb/s; Low Bit Rate (8G) = 8.5 Gb/s. In this mode, the default value of bit 110.3 (Soft Rate Select RS(0), Table 9-16) and of bit 118.3 (Soft Rate Select RS(1), Table 10-1) is 1.
	0Fh	Unspecified *
	10h	FC-PI-7 (64/32/16G Independent Rx, Tx Rate Select) High = 32GFC and 64GFC. Low = 16GFC.
	11h	Unspecified *
	12h -1Fh	Reserved
	20h	Rate select based on PMDs as defined by A0h, byte 36 and A2h, byte 67 (Rx, Tx Rate Select) High = A0h, Byte 36 PMD, Low = A2h, Byte 67 PMD
	21h-FFh	Reserved
* To support legacy, the LSB is reserved for Unspecified or INF-8074 (value = 0) or 4/2/1G selection per SFF-8079 (value = 1). Other rate selection functionalities are not allowed to depend on the LSB.		

6 Link Length

6.1 Length (single mode, km) or Copper Cable Attenuation [Address A0h, Byte 14]

Addition to EEPROM data from original GBIC definition. This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using single-mode fiber. The value is in units of kilometers. A value of 255 means that the transceiver supports a link length greater than 254 km. A value of zero means that the transceiver does not support single-mode fiber or that the length information must be determined from the transceiver technology.

For copper cable assemblies, this field is used to record the cable attenuation (or apparent attenuation from the near end of the cable for active cables) at 12.9 GHz in units of 1 dB. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

6.2 Length (single mode, 100s m) or Copper Cable Attenuation [Address A0h, Byte 15]

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using single-mode fiber. The value is in units of 100 meters. A value of 255 means that the transceiver supports a link length greater than 25.4 km. A value of zero means that the transceiver does not support single-mode fiber or that the length information must be determined from the transceiver technology.

For copper cable assemblies, this field is used to record the cable attenuation (or apparent attenuation from the near end of the cable for active cables) at 25.78 GHz in units of 1 dB. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

6.3 Length (50 μm, OM2) [Address A0h, Byte 16]

This value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 50 micron multimode OM2 [500 MHz*km at 850 nm] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 50 micron multimode OM2 fiber or that the length information must be determined from the transceiver technology.

6.4 Length (62.5 μm, OM1) [Address A0h, Byte 17]

This value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 62.5 micron multimode OM1 [200 MHz*km at 850 nm, 500 MHz*km at 1310 nm] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 62.5 micron multimode fiber or that the length information must be determined from the transceiver technology. It is common for a multimode transceiver to support OM1, OM2 and OM3 fiber.

6.5 Length (50 μm, OM4) and Length (Active Cable or Copper) [Address A0h, Byte 18]

For optical links, this value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 50 micron multimode OM4 [4700 MHz*km] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 50 micron OM4 multimode fiber or that the length information must be determined from the transceiver codes specified in Table 5-3.

For copper links, this value specifies link length in meters supported by the transceiver while operating in compliance with applicable standards using copper cable. For active cable, this value represents actual length. The value is in units of 1 meter. A value of 255 means the transceiver supports a link length greater than 254 meters. A value of zero means the transceiver does not support copper or active cables or that the length can be determined from transceiver technology. Further information about cable design, equalization, and connectors is usually required to guarantee meeting a particular length requirement.

6.6 Length (50 μm, OM3) and Length (Active Cable or Copper), additional [Address A0h, Byte 19]

This value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 50 micron multimode OM3 [2000 MHz*km] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver

does not support 50 micron multimode OM3 fiber or that the length information must be determined from the transceiver technology.
For active cable or copper cable, this value specifies the physical interconnect length supported in the following format:

Table 6-1 Cable Length, Additional

A0h	Bit	Name	Description
19	7-6	Length multiplier field (copper or active cable)	Multiplier for value in bits 5-0. 00b – multiplier of 0.1 01b – multiplier of 1 10b - multiplier of 10 11b – multiplier of 100
	5-0	Base length field (copper or active cable)	Link length base value in meters. To calculate actual link length use multiplier in bits 7-6

7 Vendor Fields

7.1 Vendor name [Address A0h, Bytes 20-35]

The vendor name is a 16-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid data.

7.2 Vendor OUI [Address A0h, Bytes 37-39]

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

7.3 Vendor PN [Address A0h, Bytes 40-55]

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

7.4 Vendor Rev [Address A0h, Bytes 56-59]

The vendor revision number (vendor rev) is a 4-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the Vendor's product revision number. A value of all zero in the 4-byte field indicates that the vendor revision is unspecified.

8 Link Characteristics

8.1 Optical and Cable Variants Specification Compliance [Address A0h, Bytes 60-61]

For optical variants, as defined by having zeroes in A0h Byte 8 bits 2 and 3, Bytes 60 and 61 denote nominal transmitter output wavelength at room temperature. 16-bit value with byte 60 as high order byte and byte 61 as low order byte. The laser wavelength is equal to the 16-bit integer value in nm. This field allows the user to read the laser wavelength directly, so it is not necessary to infer it from the Transceiver Codes A0h Bytes 3 to 10 (see Table 5-3). This also allows specification of wavelengths not covered in the Transceiver Codes, such as those used in coarse WDM systems.

For passive and active cable variants, a value of 00h for both A0h Byte 60 and Byte 61 denotes laser wavelength or cable specification compliance is unspecified.

Table 8-1 Passive Cable Specification Compliance (A0h Byte 8 Bit 2 set)

A0h	Bit	Description	A0h	Bit	Description
60	7	Reserved	61	7	Reserved
60	6	Reserved	61	6	Reserved
60	5	Reserved for SFF-8461	61	5	Reserved
60	4	Reserved for SFF-8461	61	4	Reserved
60	3	Reserved for SFF-8461	61	3	Reserved
60	2	Reserved for SFF-8461	61	2	Reserved
60	1	Compliant to FC-PI-4 Appendix H	61	1	Reserved
60	0	Compliant to SFF-8431 Appendix E	61	0	Reserved

Table 8-2 Active Cable Specification Compliance (A0h Byte 8 Bit 3 set)

A0h	Bit	Description	A0h	Bit	Description
60	7	Reserved	61	7	Reserved
60	6	Reserved	61	6	Reserved
60	5	Reserved	61	5	Reserved
60	4	Reserved	61	4	Reserved
60	3	Compliant to FC-PI-4 Limiting	61	3	Reserved
60	2	Compliant to SFF-8431 Limiting	61	2	Reserved
60	1	Compliant to FC-PI-4 Appendix H	61	1	Reserved
60	0	Compliant to SFF-8431 Appendix E	61	0	Reserved

8.2 CC_BASE [Address A0h, Byte 63]

The check code is a one-byte code that can be used to verify that the first 64 bytes of 2-wire interface information in the module is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 0 to byte 62, inclusive.

8.3 Option Values [Address A0h, Bytes 64-65]

The bits in the option field shall specify the options implemented in the transceiver.

Table 8-3 Option Values

A0h	Bit	Description
64	7	Reserved
	6	High Power Level Declaration (see SFF-8431 Addendum) Value of zero identifies standard Power Levels 1 ,2 and 3 as indicated by bits 1 and 5. Value of one identifies Power Level 4 requirement. Maximum power is declared in A2h, byte 66.
	5	High Power Level Declaration (see SFF-8431 Addendum) Value of zero identifies standard Power Levels 1 and 2 as indicated by bit 1. Value of one identifies Power Level 3 or Power Level 4 requirement.
	4	Paging implemented indicator. A value of 1 indicates that paging is implemented and byte 127 of address A2h is used for page selection.
	3	Retimer or CDR indicator. A value of 1 indicates that the transceiver has an internal retimer or clock and data recovery (CDR) circuit.
	2	Cooled Transceiver Declaration (see SFF-8431). Value of zero identifies a conventional uncooled (or unspecified) laser implementation. Value of one identifies a cooled laser transmitter implementation.
	1	Power Level Declaration (see SFF-8431). Value of zero identifies Power Level 1 (or unspecified) requirements. Value of one identifies Power Level 2 requirement. See Table 8-7 and Table 10-1 for control, status, timing. See Bit 5 for Power Level 3 declaration. See Bit 6 for Power Level 4 declaration.
	0	Linear Receiver Output Implemented (see SFF-8431). Value of zero identifies a conventional limiting, PAM4 or unspecified receiver output. Value of one identifies a linear receiver output.
65	7	Receiver decision threshold implemented. A value of 1 indicates that RDT is implemented.
	6	Tunable transmitter technology. A value of 1 indicates that the transmitter wavelength/frequency is tunable in accordance with SFF-8690.
	5	RATE_SELECT functionality is implemented NOTE: Lack of implementation does not indicate lack of simultaneous compliance with multiple standard rates. Compliance with particular standards should be determined from Transceiver Code Section (Table 5-3). Refer to Table 5-6 for Rate_Select functionality type identifiers.
	4	TX_DISABLE is implemented and disables the high speed serial output.
	3	TX_FAULT signal implemented. (See SFF-8419)
	2	Loss of Signal implemented, signal inverted from standard definition in SFP MSA (often called "Signal Detect"). NOTE: This is not standard SFP/GBIC behavior and should be avoided, since non-interoperable behavior results.
	1	Loss of Signal implemented, behavior as defined in SFF-8419 (often called "Rx_LOS").
	0	0b. There are no additional pages besides Page 00/01h and Page 02h. 1b. There are one or more additional pages that need further discovery of features of the module. The discovery procedure is described in section 4.3.

8.4 Signaling Rate, max [Address A0h, Byte 66]

If address 12 is not set to FFh, the upper signaling rate limit at which the transceiver still meets its specifications (Signaling Rate, max) is specified in units of 1% above the nominal signaling rate. If address 12 is set to FFh, the nominal signaling rate (Signaling Rate, nominal) is given in this field in units of 250 MBd, rounded off to the nearest 250 MBd. A value of 00h indicates that this field is not used.

8.5 Signaling Rate, min [Address A0h, Byte 67]

If address 12 is not set to FFh, the lower signaling rate limit at which the transceiver still meets its specifications (Signaling Rate, min) is specified in units of 1% below the nominal bit rate. If address 12 is set to FFh, the limit range of signaling rates specified in units of +/- 1% around the nominal signaling rate. A value of zero indicates that this field is not used.

8.6 Vendor SN [Address A0h, Bytes 68-83]

The vendor serial number (vendor SN) is a 16 byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the Vendor's serial number for the transceiver. A value of all zero in the 16-byte field indicates that the vendor SN is unspecified.

8.7 Date Code [Address A0h, Bytes 84-91]

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory.

Table 8-4 Date Code

A0h	Description
84-85	ASCII code, two low order digits of year (00 = 2000)
86-87	ASCII code, digits of month (01 = Jan through 12 = Dec)
88-89	ASCII code, day of month (01-31)
90-91	ASCII code, vendor specific lot code, may be blank

8.8 Diagnostic Monitoring Type [Address A0h, Byte 92]

"Diagnostic Monitoring Type" is a one-byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the particular transceiver.

Note that if bit 6, address 92 is set indicating that digital diagnostic monitoring has been implemented, received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring must all be implemented. Additionally, alarm and warning thresholds must be written as specified in this document at locations 00 to 55 on 2-wire serial address 1010001x (A2h) (see Table 8-5).

Two calibration options are possible if bit 6 has been set indicating that digital diagnostic monitoring has been implemented. If bit 5, "Internally calibrated", is set, the transceiver directly reports calibrated values in units of current, power etc. If bit 4, "Externally calibrated", is set, the reported values are A/D counts which must be converted to real world units using calibration values read using 2-wire serial address 1010001x (A2h) from bytes 56 to 95. See "Diagnostics" section for details.

Bit 3 indicates whether the received power measurement represents average input optical power or OMA. If the bit is set, average power is monitored. If it is not, OMA is monitored.

8.9 Addressing Modes

Bit 2 indicates whether or not it is necessary for the host to perform an address change sequence before accessing information at 2-wire serial address A2h. If this bit is not set, the host may simply read from either address, A0h or A2h, by using that value in the address byte during the 2-wire communication sequence. If the bit is set, the following sequence must be executed prior to accessing information at address A2h. Once A2h has been accessed, it will be necessary to execute the address change sequence again prior to reading from A0h. The address change sequence is defined as the following steps on the 2-wire serial interface:

1) Host controller generates a Start condition, followed by address of 00000000b.
   Note that the R/W bit of this address indicates transfer from host to device (‘0'b).
2) Device responds with Ack
3) Host controller transfers 00000100b (04h) as the next 8 bits of data
   This value indicates that the device is to change its address
4) Device responds with Ack
5) Host controller transfers one of the following values as the next 8 bits of data:
   xxxxxx00b - specifies 2-wire interface ID memory page
   xxxxxx10b - specifies Digital Diagnostic memory page
6) Device responds with Ack
7) Host controller generates a Stop condition
8) Device changes address that it responds to, based on the Step-5, byte value above:
   xxxxxx00b - address becomes 1010000xb (A0h)
   xxxxxx10b - address becomes 1010001xb (A2h)

Table 8-5 Diagnostic Monitoring Type

A0h	Bit	Description
92	7	Reserved for legacy diagnostic implementations. Must be '0' for compliance with this document.
	6	Digital diagnostic monitoring implemented (described in this document).
	5	Internally calibrated.
	4	Externally calibrated. 0 = Not Externally Calibrated. Page A2h Bytes 56-91 are allocated for enhanced control options, see section 9.6. 1 = Externally Calibrated.
	3	Received power measurement type 0 = OMA, 1 = average power
	2	Address change required see section above, "addressing modes"
	1	Remote Performance Monitoring Registers in Section 12
	0	Reserved

8.10 Enhanced Options [Address A0h, Byte 93]

The Enhanced Options are a one-byte field with 8 single bit indicators which describe the optional digital diagnostic features implemented in the transceiver. Since transceivers do not necessarily implement all optional features described in this document, this field allows the host to determine which functions are available over the 2-wire serial bus. A '1' indicates that the particular function is implemented in the transceiver. Bits 3 and 6 of byte 110 (see Table 9-16) allow the host to control the Rate_Select and TX_Disable functions. If these functions are not implemented, the bits remain readable and writable, but the transceiver ignores them.

Note that "soft" functions of TX_DISABLE, TX_FAULT, RX_LOS, and RATE_SELECT do not meet timing requirements as specified in the SFP MSA section B3 "Timing Requirements of Control and Status I/O" and the GBIC Specification, revision 5.5, (SFF-8053), section 5.3.1, for their corresponding pins. The soft functions allow a host to poll or set these values over the 2-wire interface bus as an alternative to monitoring/setting pin values. Timing is vendor specific but must meet the requirements specified in Table 8-7. Asserting either the "hard pin" or "soft bit" (or both) for TX_DISABLE or RATE_SELECT results in that function being asserted.

Table 8-6 Enhanced Options

A0h	Bit	Description
93	7	Optional Alarm/warning flags implemented for all monitored quantities (see Table 9-17)
	6	Optional soft TX_DISABLE control and monitoring implemented
	5	Optional soft TX_FAULT monitoring implemented
	4	Optional soft RX_LOS monitoring implemented
	3	Optional soft RATE_SELECT control and monitoring implemented
	2	Optional Application Select control implemented per SFF-8079 *This is a legacy Application Select that is not currently used in most SFP Transceivers. It is not recommended for new designs and this bit may be changed to "Reserved" in the future. The upper page of A0h which is presently defined for SFF-8079 may also be defined for other purposes in the future.*
	1	Optional soft Rate Select control implemented per Rate Select Hardware Control Contacts in SFF-8431
	0	Reserved

Table 8-7 I/O Timing for Soft Control and Status Functions

Parameter	Symbol	Min	Max	Units	Conditions
TX_DISABLE assert time	t_off		100	ms	Time from TX_DISABLE bit set [1] until optical output falls below 10% of nominal
TX_DISABLE deassert time	t_on		100	ms	Time from TX_DISABLE bit cleared [1] until optical output rises above 90% of nominal
Time to initialize, including reset of TX_FAULT	t_init		300	ms	Time from power on or negation of TX_FAULT using TX_DISABLE until transmitter output is stable [2]
TX_FAULT assert time	t_fault		100	ms	Time from fault to TX_FAULT bit set
RX_LOS assert time	t_loss_on		100	ms	Time from LOS state to RX_LOS bit set
RX_LOS deassert time	t_loss_off		100	ms	Time from non-LOS state to RX_LOS bit cleared
Rate select change time [3]	t_rate_select		100	ms	Time from change of state of Rate Select bit [1] until module is in conformance with the appropriate specification for the new rate
2-wire interface Clock rate	f_serial_clock		100	kHz	n/a
2-wire interface Diagnostic data ready time	t_data		1000	ms	From power on to data ready, bit 0 of byte 110 set
2-wire interface bus hardware ready time	t_serial		300	ms	Time from power on until module is ready for data transmission over the 2-wire bus
Optional. High Power Level assert time (per SFF-8431)	t_hpower_level		300	ms	Time from High Power Level enable bit set until module operation is stable. See Table 10-1 for control bit.

NOTES:
1. Measured from falling clock edge after stop bit of write transaction.
2. See SFF-8053 GBIC (Gigabit Interface Converter)
3. The T11.2 committee, as part of its FC-PI-2 standardization effort, has advised that a 1 ms maximum is required to be compatible with auto-negotiation algorithms documented in the FC-FS specification. For 64GFC this time is required to be 4 ms maximum.

8.11 SFF-8472 Compliance [Address A0h, Byte 94]

Byte 94 contains an unsigned integer that indicates which feature set(s) are implemented in the transceiver.

Table 8-8 SFF-8472 Compliance

A0h	Value	Interpretation
94	00h	A code of 00h indicates that the Revision Compliance to SFF-8472 is undefined. This value should not be used for modules with Rev 9.3 and later.
	01h	Includes functionality described in Rev 9.3 of SFF-8472.
	02h	Includes functionality described in Rev 9.5 of SFF-8472.
	03h	Includes functionality described in Rev 10.2 of SFF-8472.
	04h	Includes functionality described in Rev 10.4 of SFF-8472.
	05h	Includes functionality described in Rev 11.0 of SFF-8472.
	06h	Includes functionality described in Rev 11.3 of SFF-8472.
	07h	Includes functionality described in Rev 11.4 of SFF-8472.
	08h	Includes functionality described in Rev 12.3 of SFF-8472.
	09h	Includes functionality described in Rev 12.4 of SFF-8472.
	0Ah	Includes functionality described in Rev 12.5 of SFF-8472.
	0Bh - FFh	Reserved

8.12 CC_EXT [Address A0h, Byte 95]

The check code is a one-byte code that can be used to verify that the first 32 bytes of extended 2-wire interface information in the module is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 64 to byte 94, inclusive.

9 Diagnostics

9.1 Overview [Address A2h]

2-wire serial bus address 1010001X (A2h) is used to access measurements of transceiver temperature, internally measured supply voltage, TX bias current, TX output power, received optical power, and two optional DWDM quantities: laser temperature, and TEC current.

The values are interpreted differently depending upon the option bits set at address 92. If bit 5 "internally calibrated" is set, the values are calibrated absolute measurements, which should be interpreted according to the section "Internal Calibration" below. If bit 4 "externally calibrated" is set, the values are A/D counts, which are converted into real units per the subsequent section titled "External Calibration". The optional DWDM quantities are defined for internal calibration only.

Measured parameters are reported in 16-bit data fields, i.e., two concatenated bytes. The 16-bit data fields allow for wide dynamic range. This is not intended to imply that a 16-bit A/D system is recommended or required in order to achieve the accuracy goals stated below. The width of the data field should not be taken to imply a given level of precision. It is conceivable that the accuracy goals herein can be achieved with less than 16 bits of resolution. It is recommended that any low-order data bits beyond the specified accuracy be fixed at zero. Overall system accuracy and precision is vendor dependent.

To guarantee coherency of the diagnostic monitoring data, the host is required to retrieve any multi-byte fields from the diagnostic monitoring data structure (e.g. Rx Power MSB - byte 104 in A2h, Rx Power LSB - byte 105 in A2h) by the use of a single two-byte read sequence across the 2-wire interface.

The transceiver is required to ensure that any multi-byte fields which are updated with diagnostic monitoring data (e.g. Rx Power MSB - byte 104 in A2h, Rx Power LSB - byte 105 in A2h) must have this update done in a fashion that guarantees coherency and consistency of the data. In other words, the update of a multi-byte field by the transceiver must not occur such that a partially updated multi-byte field can be transferred to the host. Also, the transceiver shall not update a multi-byte field within the structure during the transfer of that multi-byte field to the host, such that partially updated data would be transferred to the host.

Accuracy requirements specified below shall apply to the operating signal range specified in the relevant standard. The manufacturer's specification should be consulted for more detail on the conditions under which the accuracy requirements are met.

9.2 Internal Calibration

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data.

1) Internally measured transceiver temperature. Represented as a 16-bit signed two's complement value in increments of 1/256 ºC, yielding a total range of -128ºC to +128ºC. Temperature accuracy is vendor specific but must be better than +/- 3 ºC over the specified operating temperature and voltage. Please see vendor specification for details on location of temperature sensor. See Table 9-1 and Table 9-2 below for examples of temperature format.
2) Internally measured transceiver supply voltage. Represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0-65535) with LSB equal to 100 μV, yielding a total range of 0 V to +6.55 V. Practical considerations to be defined by transceiver manufacturer tend to limit the actual bounds of the supply voltage measurement. Accuracy is vendor specific but must be better than +/- 3% of the manufacturer's nominal value over specified operating temperature and voltage. Note that in some transceivers, transmitter supply voltage and receiver supply voltage are isolated. In that case, only one supply is monitored. Refer to the device specification for more detail.
3) Measured TX bias current in μA. Represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0-65535) with LSB equal to 2 μA, yielding a total range of 0 to 131 mA. Accuracy is vendor specific but must be better than +/- 10% of the manufacturer's nominal value over specified operating temperature and voltage.
4) Measured TX output power in mW. Represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0-65535) with LSB equal to 0.1 μW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Data is assumed to be based on measurement of laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Accuracy is vendor specific but must be better than +/- 3 dB over the specified temperature and voltage. Data is not valid when the transmitter is disabled.
5) Measured RX received optical power in mW. Value can represent either average received power or OMA depending upon how bit 3 of byte 92 (A0h) is set. Represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0-65535) with LSB equal to 0.1 μW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than +/- 3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.
6) Measured optional laser temperature. For DWDM applications bytes 106-107 report laser temperature. The encoding is the same as for transceiver internal temperature defined in paragraph 1) above. The relative and absolute accuracy are vendor specific but relative laser temperature accuracy must be better than +/- 0.2 ºC. [Relative temperature accuracy refers to the accuracy of the reported temperature changes relative to the actual laser temperature changes].
7) Measured TEC current. For DWDM applications, bytes 108-109 report the measured TEC current. The format is signed two's complement with the LSB equal to 0.1 mA. Thus a range from -3276.8 to +3276.7 mA may be reported with a resolution of 0.1 mA. See Table 9-4 and Table 9-5 for further details. Reported TEC current is a positive number for cooling and a negative number for heating. The accuracy of the TEC current monitor is vendor specific but shall be be better than +/- 15% of the maximum TEC current as stored in the TEC current high alarm threshold (bytes 48-49).

The tables below illustrate the 16-bit signed two's complement format used for temperature reporting. The most significant bit (D7) represents the sign, which is zero for positive temperatures and one for negative temperatures.

Table 9-1 Bit Weights (ºC) for Temperature Reporting Registers

Most Significant Byte (byte 96)								Least Significant Byte (byte 97)							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Sign	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

Table 9-2 Digital Temperature Format

Temperature		Binary		Hexadecimal	
Decimal	Fraction	High Byte	Low Byte	High Byte	Low Byte
+127.996	+127 255/256	01111111	11111111	7F	FF
+125.000	+125	01111101	00000000	7D	00
+25.000	+25	00011001	00000000	19	00
+1.004	+1 1/256	00000001	00000001	01	01
+1.000	+1	00000001	00000000	01	00
+0.996	+255/256	00000000	11111111	00	FF
+0.004	+1/256	00000000	00000001	00	01
0.000	0	00000000	00000000	00	00
-0.004	-1/256	11111111	11111111	FF	FF
-1.000	-1	11111111	00000000	FF	00
-25.000	-25	11100111	00000000	E7	00
-40.000	-40	11011000	00000000	D8	00
-127.996	-127 255/256	10000000	00000001	80	01

The tables below illustrate the 16-bit two's complement format used for TEC current reporting. The most significant bit (D7) represents the sign; zero for positive currents (cooling) and one for negative currents (heating).

Table 9-3 Bit Weights (mA) for TEC current Reporting Registers

Most Significant Byte (byte 108)								Least Significant Byte (byte 109)							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Sign	1638.4	819.2	409.6	204.8	102.4	51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1

Table 9-4 TEC Current Format

Current	Binary		Hexadecimal	
Decimal	High Byte	Low Byte	High Byte	Low Byte
+3276.7	01111111	11111111	7F	FF
+3200.0	01111101	00000000	7D	00
+640.0	00011001	00000000	19	00
+25.7	00000001	00000001	01	01
+25.6	00000001	00000000	01	00
+25.5	00000000	11111111	00	FF
+0.1	00000000	00000001	00	01
0.0	00000000	00000000	00	00
-0.1	11111111	11111111	FF	FF
-25.6	11111111	00000000	FF	00
-640.0	11100111	00000000	E7	00
-1024.0	11011000	00000000	D8	00
-3276.7	10000000	00000001	80	01
-3276.8	10000000	00000000	80	00

9.3 External Calibration

Measurements are raw A/D values and must be converted to real world units using calibration constants stored in EEPROM locations 56-95 at 2-wire serial bus address A2h. Calibration is valid over vendor specified operating temperature and voltage. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data.

After calibration per the equations given below for each variable, the results are consistent with the accuracy and resolution goals for internally calibrated devices.

1) Internally measured transceiver temperature. Module temperature, T, is given by the following equation:

   T(C) = T_slope * T_AD (16 bit signed two's complement value) + T_offset

   The result is in units of 1/256°C, yielding a total range of -128°C to +128°C. See Table 9-6 for locations of T_slope and T_offset. Temperature accuracy is vendor specific but must be better than +/-3 °C over specified operating temperature and voltage. Please see vendor specification sheet for details on location of temperature sensor. Table 9-1 and Table 9-2 give examples of the 16-bit signed two's complement temperature format.

2) Internally measured supply voltage. Module internal supply voltage, V, is given in microvolts by the following equation:

   V(μV) = V_slope * V_AD (16-bit unsigned integer) + V_offset

   The result is in units of 100 μV, yielding a total range of 0 to 6.55 V. See Table 9-6 for locations of V_slope and V_offset. Accuracy is vendor specific but must be better than +/-3% of the manufacturer's nominal value over specified operating temperature and voltage. Note that in some transceivers, transmitter supply voltage and receiver supply voltage are isolated. In that case, only one supply is monitored. Refer to the manufacturer's specification for more detail.

3) Measured transmitter laser bias current. Module laser bias current, I, is given in microamps by the following equation:

   I (μA) = I_slope * I_AD (16 bit unsigned integer) + I_offset

   This result is in units of 2 μA, yielding a total range of 0 to 131 mA. See Table 9-6 for locations of I_slope and I_offset. Accuracy is vendor specific but must be better than +/-10% of the manufacturer's nominal value over specified operating temperature and voltage.

4) Measured coupled TX output power. Module transmitter coupled output power, TX_PWR, is given in μW by the following equation:

   TX_PWR (μW) = TX_PWR_slope * TX_PWR_AD (16-bit unsigned integer) + TX_PWR_offset.

   This result is in units of 0.1 μW yielding a total range of 0 to 6.5 mW. See Table 9-6 for locations of TX_PWR_slope and TX_PWR_offset. Accuracy is vendor specific but must be better than +/-3 dB over specified operating temperature and voltage. Data is assumed to be based on measurement of a laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Data is not valid when the transmitter is disabled.

5) Measured received optical power. Received power, RX_PWR, is given in μW by the following equation:

$$\begin{aligned} \text{Rx\_PWR}(\mu W) = {} & \text{Rx\_PWR}(4) * \text{Rx\_PWR\_AD}^4 \text{ (16 bit unsigned integer) } + \\ & \text{Rx\_PWR}(3) * \text{Rx\_PWR\_AD}^3 \text{ (16 bit unsigned integer) } + \\ & \text{Rx\_PWR}(2) * \text{Rx\_PWR\_AD}^2 \text{ (16 bit unsigned integer) } + \\ & \text{Rx\_PWR}(1) * \text{Rx\_PWR\_AD} \text{ (16 bit unsigned integer) } + \\ & \text{Rx\_PWR}(0) \end{aligned}$$

   The result is in units of 0.1 μW yielding a total range of 0 to 6.5 mW. See Table 9-6 for locations of Rx_PWR(4-0). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified

wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.

9.4 Alarm and Warning Thresholds [Address A2h, Bytes 0-39]

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. The factory preset values allow the user to determine when a particular value is outside of "normal" limits as determined by the transceiver manufacturer. It is assumed that these values vary with different technologies and different implementations. When external calibration is used, data may be compared to alarm and warning threshold values before or after calibration by the host. Comparison can be done directly before calibration. If comparison is to be done after calibration, calibration must first be applied to both data and threshold values.

The values reported in the alarm and warning thresholds area (see below) may be temperature compensated or otherwise adjusted when setting warning and/or alarm flags. Any threshold compensation or adjustment is vendor specific and optional. See Vendor's documentation for addition details regarding alarm and warning thresholds.

Table 9-5 Alarm and Warning Thresholds

A2h	# Bytes	Name	Description
00-01	2	Temp High Alarm	MSB at low address
02-03	2	Temp Low Alarm	MSB at low address
04-05	2	Temp High Warning	MSB at low address
06-07	2	Temp Low Warning	MSB at low address
08-09	2	Voltage High Alarm	MSB at low address
10-11	2	Voltage Low Alarm	MSB at low address
12-13	2	Voltage High Warning	MSB at low address
14-15	2	Voltage Low Warning	MSB at low address
16-17	2	Bias High Alarm	MSB at low address
18-19	2	Bias Low Alarm	MSB at low address
20-21	2	Bias High Warning	MSB at low address
22-23	2	Bias Low Warning	MSB at low address
24-25	2	TX Power High Alarm	MSB at low address
26-27	2	TX Power Low Alarm	MSB at low address
28-29	2	TX Power High Warning	MSB at low address
30-31	2	TX Power Low Warning	MSB at low address
32-33	2	RX Power High Alarm	MSB at low address
34-35	2	RX Power Low Alarm	MSB at low address
36-37	2	RX Power High Warning	MSB at low address
38-39	2	RX Power Low Warning	MSB at low address
40-41	2	Optional Laser Temp High Alarm	MSB at low address
42-43	2	Optional Laser Temp Low Alarm	MSB at low address
44-45	2	Optional Laser Temp High Warning	MSB at low address
46-47	2	Optional Laser Temp Low Warning	MSB at low address
48-49	2	Optional TEC Current High Alarm	MSB at low address
50-51	2	Optional TEC Current Low Alarm	MSB at low address
52-53	2	Optional TEC Current High Warning	MSB at low address
54-55	2	Optional TEC Current Low Warning	MSB at low address

9.5 Calibration Constants for External Calibration Option [Address A2h, Bytes 56-91]

When External Calibration bit 4, byte 92 in A0h is set to 1, Bytes 56-94 are allocated to external calibration values as listed in Table 9-6.

Table 9-6 Calibration Constants for External Calibration Option

A2h	# Bytes	Name	Description
56-59	4	Rx_PWR(4)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 56 is MSB, bit 0 of byte 59 is LSB. Rx_PWR(4) should be set to zero for "internally calibrated" devices.
60-63	4	Rx_PWR(3)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 60 is MSB, bit 0 of byte 63 is LSB. Rx_PWR(3) should be set to zero for "internally calibrated" devices.
64-67	4	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB. Rx_PWR(2) should be set to zero for "internally calibrated" devices.
68-71	4	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB. Rx_PWR(1) should be set to 1 for "internally calibrated" devices.
72-75	4	Rx_PWR(0)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 72 is MSB, bit 0 of byte 75 is LSB. Rx_PWR(0) should be set to zero for "internally calibrated" devices.
76-77	2	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB. Tx_I(Slope) should be set to 1 for "internally calibrated" devices.
78-79	2	Tx_I(Offset)	Fixed decimal (signed two's complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB. Tx_I(Offset) should be set to zero for "internally calibrated" devices.
80-81	2	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB. Tx_PWR(Slope) should be set to 1 for "internally calibrated" devices.
82-83	2	Tx_PWR(Offset)	Fixed decimal (signed two's complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB. Tx_PWR(Offset) should be set to zero for "internally calibrated" devices.
84-85	2	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB. T(Slope) should be set to 1 for "internally calibrated" devices.
86-87	2	T (Offset)	Fixed decimal (signed two's complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB. T(Offset) should be set to zero for "internally calibrated" devices.
88-89	2	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB. V(Slope) should be set to 1 for "internally calibrated" devices.
90-91	2	V (Offset)	Fixed decimal (signed two's complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB, bit 0 of byte 91 is LSB. V(Offset) should be set to zero for "internally calibrated" devices.
92-94	3	Reserved	
95	1	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0-94.

The slope constants at addresses 76, 80,84, and 88, are unsigned fixed-point binary numbers. The slope will therefore always be positive. The binary point is in between the upper and lower bytes, i.e., between the eighth and ninth most significant bits. The most significant byte is the integer portion in the range 0 to +255. The least significant byte represents the fractional portion in the range of 0.00391 (1/256) to 0.9961 (255/256). The smallest real number that can be represented by this format is 0.00391 (1/256); the largest real number that can be represented using this format is 255.9961 (255 + 255/256). Slopes are defined, and conversion formulas found, in

the "External Calibration" section. Examples of this format are illustrated below:

Table 9-7 Unsigned Fixed-Point Binary Format for Slopes

Decimal Value	Binary Value		Hexadecimal Value	
	MSB	LSB	High Byte	Low Byte
0.0000	00000000	00000000	00	00
0.0039	00000000	00000001	00	01
1.0000	00000001	00000000	01	00
1.0313	00000001	00001000	01	08
1.9961	00000001	11111111	01	FF
2.0000	00000010	00000000	02	00
255.9921	11111111	11111110	FF	FE
255.9961	11111111	11111111	FF	FF

The calibration offsets are 16-bit signed two's complement binary numbers. The offsets are defined by the formulas in the "External Calibration" section. The least significant bit represents the same units as described above under "Internal Calibration" for the corresponding analog parameter, e.g., 2 μA for bias current, 0.1 μW for optical power, etc. The range of possible integer values is from +32767 to -32768. Examples of this format are shown below.

Table 9-8 Format for Offsets

Decimal Value	Binary Value		Hexadecimal Value	
	MSB	LSB	High Byte	Low Byte
+32767	01111111	1111111	7F	FF
+3	00000000	00000011	00	03
+2	00000000	00000010	00	02
+1	00000000	00000001	00	01
0	00000000	00000000	00	00
-1	11111111	11111111	FF	FF
-2	11111111	11111110	FF	FE
-3	11111111	11111101	FF	FD
-32768	10000000	00000000	80	00

External calibration of received optical power makes use of single-precision floating-point numbers as defined by *IEEE Standard for Floating-Point Arithmetic*, IEEE Std 754. Briefly, this format utilizes four bytes (32 bits) to represent real numbers. The first and most significant bit is the sign bit; the next eight bits indicate an exponent (base 2) in the range of +126 to -127; the remaining 23 bits represent the mantissa. The 32 bits are therefore arranged as in the following table.

Table 9-9 IEEE Std 754 Single-Precision Floating Point Number Format

Function	Sign	Exponent								Mantissa																			
Bit	31	30							23	22																			0
Byte	3								2								1								0				
← Most Significant																												Least Significant →	

Rx_PWR(4), as an example, is stored as shown in Table 9-10:

Table 9-10 Example of Floating Point Representation

Byte Address	Contents	Significance
56	SEEEEEEE	Most
57	EMMMMMMM	Second Most
58	MMMMMMMM	Second Least
59	MMMMMMMM	Least
where S = sign bit; E = exponent bit; M = mantissa bit.		

Special cases of the various bit values are reserved to represent indeterminate values such as positive and negative infinity; zero; and "NaN" or not a number. NaN indicates an invalid result. As of this writing, explanations of the IEEE single precision floating point format were posted on the worldwide web at https://en.wikipedia.org/wiki/Single-precision_floating-point_format . The actual IEEE standard is available at www.IEEE.org .

9.6 Additional Enhanced Features

When External Calibration bit 4, byte 92 in A0h is set to 0, Bytes 56-94 are allocated to Additional Enhanced Features as listed in Table 9-11.

Table 9-11 Additional Enhanced Features

A2h	# Bytes	Name	Description
		Capabilities	
56-57	2	Enhanced Controls Advertisements	Advertisement for Enhanced Controls Implementation (see Table 9-12)
58-59	2	Enhanced Status Advertisements	Advertisement for Enhanced Status Implementation (see Table 9-13)
60-65	6	Enhanced Signal Integrity Controls Advertisement	Advertisement for Signal Integrity Control Implementation (see Table 9-14)
66	1	Max Power Consumption	See A0, byte 64, bit 6 Max power consumption of the module, unsigned integer with LSB = 0.1 W
67	1	Secondary Extended Spec compliance	Secondary Extended Specification compliance code. See SFF-8024 Table 4-4
68	2	Reserved	Reserved for Future Advertisements
		Status	
69-70	2	Reserved	Reserved for Future Status
		Control	
71-74	4	Enhanced Control	Enhanced Control Registers (see Table 9-15)
75-94	20	Reserved	Reserved
95	1	Checksum	Byte 95 contains the sum of bytes 0-94 at module startup before the enhanced control registers 71-74 are changed. When the enhanced control registers are changed, the module vendor may recalculate this checksum if the enhanced control registers are changed. See also section 9.7.

Table 9-12 Enhanced Control Advertisement

A2h	Bit	Name	Description
56	7-5	Reserved	Reserved
	4	RS0/1 pin status ignore	0b - RS0, RS1 pins status ignore bit not implemented 1b - RS0, RS1 pins status ignore bit implemented (see A2h, byte 72, bit4)
	3-2	Tx Squelch Implemented	00b - Tx Squelch not implemented 01b - Tx Squelch reduces OMA 10b - Tx Squelch reduces Pave 11b - User Control, both OMA and Pave supported
	1	Tx Force Squelch Implemented	0b - Tx Force Squelch not implemented 1b - Tx Force Squelch implemented
	0	Tx Squelch Disable Implemented	0b - Tx Squelch disable not implemented 1b - Tx Squelch disable implemented
57	7-2	Reserved	Reserved
	1	Rx Force Squelch Implemented	0b - Rx Force Squelch not implemented 1b - Rx Force Squelch implemented
	0	Rx Squelch disable Implemented	0b - Rx Squelch disable not implemented 1b - Rx Squelch disable implemented

Table 9-13 Enhanced Flags Advertisement

A2h	Bit	Name	Description
58	7-1	Reserved	Reserved
	0	Tx Adaptive Input EQ Fail Flag Implemented	0b – Tx Adaptive Input EQ Fail Flag not implemented 1b - Tx Adaptive Input EQ Fail Flag implemented
59	7-0	Reserved	Reserved

Table 9-14 Enhanced Signal Integrity Control Advertisement

A2h	Bit	Name	Description
60	7-5	Reserved	Reserved
	4-3	Tx Input EQ Store/Recall	00b - Tx Input EQ Store/Recall not implemented 01b - Tx Input EQ Store/Recall implemented 10b - Reserved 11b - Reserved
	2	Tx Input EQ Freeze Implemented	0b - Tx Input EQ Freeze not implemented 1b - Tx Input EQ Freeze implemented
	1	Adaptive Tx Input EQ Implemented	0b - Adaptive Tx Input EQ not implemented 1b - Adaptive Tx Input EQ implemented
	0	Tx Input EQ Manual Control Implemented	0b - Tx Input EQ manual control not implemented 1b - Tx Input EQ manual control implemented
61	7-0	Max Adaptive Tx Input EQ settling time	Maximum Time needed for adaptive algorithm to converge to appropriate setting, LSB = 100 ms
62	7-5	Reserved	Reserved
	4-3	Rx Output EQ Type	00b - Not Implemented, Constant Rx Amplitude p-p or no information 01b - Constant steady state amplitude 10b - Constant average of Rx Amplitude p-p and steady state amplitude 11b - Reserved
	2-1	Rx Enhanced Output EQ Control Implemented	00b - Rx Enhanced Output EQ control not implemented 01b - Rx Enhanced Output EQ pre-cursor control implemented 10b - Rx Enhanced Output EQ post-cursor control implemented 11b - Rx Enhanced Output EQ pre-cursor and post-cursor control implemented
	0	Rx Output Amplitude Control Implemented	0b - Rx Output Amplitude control not implemented 1b - Rx Output Amplitude control implemented
63	7	Rx Output Amplitude code 0011b Implemented	0b - Rx Out Amplitude code 0011b not implemented 1b - Rx Out Amplitude code 0011b implemented
	6	Rx Output Amplitude code 0010b Implemented	0b - Rx Out Amplitude code 0010b not implemented 1b - Rx Out Amplitude code 0010b implemented
	5	Rx Output Amplitude code 0001b Implemented	0b - Rx Out Amplitude code 0001b not implemented 1b - Rx Out Amplitude code 0001b implemented
	4	Rx Output Amplitude code 0000b Implemented	0b - Rx Out Amplitude code 0000b not implemented 1b - Rx Out Amplitude code 0000b implemented
	3-0	Max Tx Input EQ	Maximum supported value of the Tx Input EQ control for manual/fixed programming
64	7-4	Max Rx Output EQ Post-cursor	Maximum supported value of the Rx Output EQ Post-cursor control
	3-0	Max Rx Output EQ Pre-cursor	Maximum supported value of the Rx Output EQ Pre-cursor control
65	7-0	Reserved	Reserved

Table 9-15 Enhanced Control

A2h	Bit	Name	Description
71	7-4	Reserved	Reserved
	3	Tx Input EQ Adaptation Recall	0b - Do not recall 1b - Recall
	2	Tx Input EQ Adaptation Store	0b - Do not store 1b - Store
	1	Tx Input EQ Adaptation Freeze	0b - Adaptive Tx Input EQ no freeze 1b - Adaptive Tx Input EQ freeze
	0	Tx Input EQ Adaptation Enable	0b - Adaptive Tx Input EQ disable (use manual fixed EQ) 1b - Adaptive Tx Input EQ enable
72	7-5	RX Output EQ Control, pre-cursor	Rx Output EQ pre-cursor
	4	Rx Output Enhanced EQ Control Override	0b – When this bit is set to 0b, the host will use Rx Emphasis control register 115, A2h. See Table 9-17 and Table 9-19. 1b - When this bit is set to 1b, the host will use Rx Enhanced Output EQ control, register 72, A2h, as advertised by the module in register 62, A2h, bits 2-1. Default is 0b .
	3-0	RX Output EQ Control, post-cursor	Rx Output EQ post-cursor
73	7-5	Reserved	Reserved
	4	RS0/RS1 Pin State Ignore	0b - Do not ignore 1b - When this bit is set to 1b the state of the RS0 and RS1 hardware pins and A2h, byte 110, bits 4 and 5 are ignored by the module, rate is determined only by A2h, byte 110, bit 3 and byte 118, bit 3 [1]
	3-0	Output Amplitude Control	Rx Output Amplitude
74	7-6	Reserved	Reserved
	5	Rx Force Squelch	0b - No impact on Rx behavior 1b - Rx Output Squelch
	4	Rx Squelch disable	0b - Rx output squelch permitted 1b - Rx output squelch not permitted
	3	Reserved	Reserved
	2	Tx Squelch control [2]	0b -Tx Squelch reduces OMA 1b - Tx Squelch reduces Pave
	1	Tx Force Squelch	0b - No impact on Tx behavior 1b - Tx Output Squelch
	0	Tx Squelch Disable	0b – Tx output squelch permitted 1b – Tx output squelch not permitted

NOTE:
1. To support legacy modules that do not have the RS0/RS1 Pin State Ignore bit, the host needs to set the hardware rate select pins to a correct state.
2. If both options are supported, as advertised in bits 3-2, register 56, it is recommended that the host sets the squelch method based on knowledge of the relevant interface standard.

9.7 CC_DMI [Address A2h, Byte 95]

The checksum is the sum of Bytes 0-94 at module startup prior to modification of the extended control registers Byte 71-74. This checksum can be updated by the module at the module vendors discretion after the modification of the enhanced control registers Byte 71-74 or can retain the same value as it had at start up.

9.8 Real Time Diagnostic and Control Registers [Address A2h, Bytes 96-111]

Table 9-16 A/D Values and Status Bits

A2h	Bit	Name	Description
Converted analog values. Calibrated 16-bit data.			
96	All	Temperature MSB	Internally measured module temperature
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage in transceiver
99	All	Vcc LSB	
100	All	TX Bias MSB	Internally measured TX Bias Current
101	All	TX Bias LSB	
102	All	TX Power MSB	Measured TX output power
103	All	TX Power LSB	
104	All	RX Power MSB	Measured RX input power
105	All	RX Power LSB	
106	All	Optional Laser Temp/Wavelength MSB	Measured laser temperature or wavelength
107	All	Optional Laser Temp/Wavelength LSB	
108	All	Optional TEC current MSB	Measured TEC current (positive is cooling)
109	All	Optional TEC current LSB	
Optional Status/Control Bits			
110	7	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100 ms of change on pin.
	6	Soft TX Disable Select	Read/write bit that allows software disable of laser. Writing '1' disables laser. See Table 8-7 for enable/disable timing requirements. This bit is "OR"d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0 (low).
	5	RS(1) State	Digital state of SFP input pin AS(1) per SFF-8079 or RS(1) per SFF-8431. Updated within 100 ms of change on pin. See A2h Byte 118, Bit 3 for Soft RS(1) Select control information.
	4	Rate_Select State [aka. "RS(0)"]	Digital state of the module's Rate_Select Input Pin. Updated within 100 ms of change on pin. Note: This pin is also known as AS(0) in SFF-8079 and RS(0) in SFF-8431.
	3	Soft Rate_Select Select [aka. "RS(0)"]	Read/write bit that allows software rate select control. Writing '1' selects full bandwidth operation. This bit is "OR'd with the hard Rate_Select, AS(0) or RS(0) pin value. See Table 8-7 for timing requirements. Default at power up is 0/low, unless specifically redefined by value selected in Table 5-6. If Soft Rate Select is not implemented, the transceiver ignores the value of this bit. Note: Specific transceiver behaviors of this bit are identified in Table 5-6 and referenced documents. See Table 10-1, byte 118, bit 3 for Soft RS(1) Select.
	2	TX Fault State	Digital state of the TX Fault Output Pin. Updated within 100 ms of change on pin.
	1	Rx_LOS State	Digital state of the RX_LOS Output Pin. Updated within 100 ms of change on pin.
	0	Data_Not_Ready	Indicates module does not yet have valid monitor data. The bit remains 1 until valid data can be read at which time the bit goes to 0.
111	7-0	Reserved	Reserved (was assigned to SFF-8079).

The Data_Not_Ready bit is 1 during module power up and prior to the first valid A/D reading. Once the first valid A/D reading occurs, the bit is set to 0 until the device is powered down. The bit must be set "0" within 1 second of power up.

9.9 Alarm and Warning Flag Bits [Address A2h, Bytes 112, 113, 116, 117]

Bytes 112, 113, 116 and 117 contain an optional set of alarm and warning flags. The flags may be latched or non-latched. Implementation is vendor specific, and the Vendor's specification sheet should be consulted for details. It is recommended that in either case, detection of an asserted flag bit should be verified by a second read of the flag at least 100 ms later. For users who do not wish to set their own threshold values or read the values in locations 0-55, the flags alone can be monitored. Two flag types are defined.

1. Alarm flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Alarm flags indicate conditions likely to be associated with an in-operational link and cause for immediate action.
2. Warning flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Warning flags indicate conditions outside the normally guaranteed bounds but not necessarily causes of immediate link failures. Certain warning flags may also be defined by the manufacturer as end-of-life indicators (such as for higher than expected bias currents in a constant power control loop).

Table 9-17 Alarm and Warning Flag Bits

A2h	Bit	Name	Description
Optional Alarm and Warning Flag Bits			
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
	6	Temp Low Alarm	Set when internal temperature is below low alarm level.
	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
	3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
	2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
	1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
	0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
	6	RX Power Low Alarm	Set when Received Power is below low alarm level.
	5	Optional Laser Temp High Alarm	Set when laser temperature or wavelength exceeds the high alarm level.
	4	Optional Laser Temp Low Alarm	Set when laser temperature or wavelength is below the low alarm level.
	3	Optional TEC current High Alarm	Set when TEC current exceeds the high alarm level.
	2	Optional TEC current Low Alarm	Set when TEC current is below the low alarm level.
	1	Reserved Alarm	
	0	Reserved Alarm	
114	7-4	Tx input equalization control RATE=HIGH	Input equalization level control
	3-0	Tx input equalization control RATE=LOW	Input equalization level control
115	7-4	RX output emphasis control RATE=HIGH	Output emphasis level control
	3-0	RX output emphasis control RATE=LOW	Output emphasis level control
116	7	Temp High Warning	Set when internal temperature exceeds high warning level.
	6	Temp Low Warning	Set when internal temperature is below low warning level.

A2h	Bit	Name	Description
	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
	4	Vcc Low Warning	Set when internal supply voltage is below low warning level.
	3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
	2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
	1	TX Power High Warning	Set when TX output power exceeds high warning level.
	0	TX Power Low Warning	Set when TX output power is below low warning level.
117	7	RX Power High Warning	Set when Received Power exceeds high warning level.
	6	RX Power Low Warning	Set when Received Power is below low warning level.
	5	Optional Laser Temp High Warning	Set when laser temperature or wavelength exceeds the high warning level.
	4	Optional Laser Temp Low Warning	Set when laser temperature or wavelength is below the low warning level.
	3	Optional TEC current High Warning	Set when TEC current exceeds the high warning level.
	2	Optional TEC current Low Warning	Set when TEC current is below the low warning level.
	1	Reserved Warning	
	0	Reserved Warning	

1
2

9.10 Equalization and emphasis control [Address A2h, Bytes 114-115]

Bytes 114 and 115 are module electrical input equalization and output emphasis controls.

Table 9-18 Input Equalization (Address A2h Byte 114)

Code	Transmitter Input Equalization	
	Nominal	Units
11xx	Reserved	
1011	Reserved	
1010	10	dB
1001	9	dB
1000	8	dB
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No EQ

Table 9-19 Output Emphasis Control (Address A2h Byte 115)

Code	Receiver Output Emphasis At nominal Output Amplitude	
	Nominal	Units
1xxx	Vendor Specific	
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No emphasis

10 Extended Information

10.1 Extended Module Control/Status Bytes [Address A2h, Bytes 118-119]

Addresses 118 and 119 are defined for extended module control and status functions. Depending on usage, the contents may be writable by the host. See Table 8-3 for power level declaration requirement in Byte 64, bit 1.

Table 10-1 Extended Module Control/Status Bytes

A2h	Bit	Name	Description
118	5-7	Reserved	
	4	Adaptive Input EQ Fail Flag	Tx Adaptive Input EQ fail status. 1b = Tx Adaptive Input EQ fail
	3	Soft RS(1) Select	Read/write bit that allows software Tx rate control. Writing '1' selects full speed Tx operation. This bit is "OR'd with the hard RS(1) pin value. See Table 8-7 for timing requirements. Default at power up is 0/low, unless specifically redefined by value selected in Table 5-6. If Soft RS(1) is not implemented, the transceiver ignores the value of this bit. Note: Specific transceiver behaviors of this bit are identified in Table 5-6 and referenced documents. See Table 9-16 , byte 110, bit 3 for Soft RS(0) Select.
	2	Power Level 4 Enable	Value of 1 enables Power Level 4 if listed in A0h, Byte 64.
	1	Power Level Operation State	Optional. SFF-8431 Power Level (maximum power dissipation) status. Value of zero indicates Power Level 1 operation (1.0 W max). Value of one indicates Power Level 2 or 3 or 4 operation (1.5 W or 2.0 W or > 2.0 W max), depending on the values in byte 64 of A0h. Refer to Table 8-3 for Power Level requirement declaration. Refer to Table 8-7 for timing. In Power Level 4 modules, this bit shall be set when all internal circuits are powered and the module has reached steady state. For example, if TxDIS is asserted (laser off), this bit 118.1 shall be asserted (=1b) when the laser is stabilized by the TEC even there is no optical TX power. If TxDIS is de-asserted, then this bit 118.1 shall be asserted when laser is stabilized by the TEC and optical power output is present.
	0	Power Level Select	Optional. SFF-8431 Power Level (maximum power dissipation) control bit. Value of zero enables Power Level 1 only (1.0 W max). Value of one enables Power Level 2 or 3 (1.5 W or 2.0 W max), depending on the values in byte 64 of A0h. Refer to Table 8-3 for Power Level requirement declaration. Refer to Table 8-7 for timing. If Power Levels 2 or 3 are not implemented, the module ignores the value of this bit.
119	7-5	Reserved	
	4	PAM4 Mode Tx Configured	This status bit indicates the module Tx logic has finished configuring itself to 64GFC mode at 28.9 GBd (if bit 2, 64GFC Mode is set) or 50G Ethernet mode at 26.5625GBd (If this rate is selected through module Rate Select).
	3	PAM4 Mode Rx Configured	This status bit indicates the module Rx logic has finished configuring itself to 64GFC mode at 28.9 GBd (if bit 2, 64GFC Mode is set) or 50G Ethernet mode at 26.5625 GBd (If this rate is selected through module Rate Select).
	2	64GFC Mode	Writing a 1 to this bit selects 64GFC speed of operation at 28.9 GBd. When this bit is set to 1, the rate select settings on the pins or in the registers shall be ignored. Default at power up for this bit is 0.

A2h	Bit	Name	Description
	1	Optional Tx CDR unlocked	Used when bit 64.3 (A0h) is set to 1. If the Tx side CDR is enabled, a value of 0 indicates that the CDR is locked, whereas a value of 1 indicates loss of lock of the CDR. If the CDR is in bypass mode, this bit is set to 0. In 64GFC or 50G Ethernet mode, if bit 4 of this byte is set to 1, a value of 0 indicates that the equalizer has finished adaptation and the CDR is locked to the PAM4 signal.
	0	Optional Rx CDR unlocked	Used when bit 64.3 (A0h) is set to 1. If the Rx side CDR is enabled, a value of 0 indicates that the CDR is locked, whereas a value of 1 indicates loss of lock of the CDR. If the CDR is in bypass mode, this bit is set to 0. In 64GFC or 50G Ethernet mode, if bit 3 of this byte is set to 1, a value of 0 indicates that the equalizer has finished adaptation and the CDR is locked to the PAM4 signal.

If the content of byte 13d of A0h is set 0Eh and bit 64.3 of page A0h is set to 1, bits 110.3 and bits 118.3 control the locking modes of the internal retimer or CDR. The retimer/CDR locking modes are set according to the logic table defined in Table 10-2. The default value of bits 110.3 and 118.3 is 1.

Table 10-2 Retimer/CDR Rate Select Logic Table

When byte 13d of A0h is set to 0Eh and bit 64.3 of A0h is set to 1			
Logic OR of RS0 pin and RS0 bit	**Logic OR of RS1 pin and RS1 bit**	**Receiver retimer/CDR**	**Transmitter retimer/CDR**
Low/0	Low/0	Lock at low bit rate	Lock at low bit rate
Low/0	High/1	Lock at high bit rate	Bypass
High/1	Low/0	Bypass	Bypass
High/1	High/1	Lock at high bit rate	Lock at high bit rate
NOTE: Low and high bit rates are defined in byte 13d of A0h.			

10.2 Vendor Specific Locations [Address A2h, Bytes 120-126]

Addresses 120-126 are defined for vendor specific memory functions. Potential usage includes vendor password field for protected functions, scratch space for calculations or other proprietary content.

10.3 Optional Page Select Byte [Address A2h, Byte 127]

In order to provide memory space for DWDM and CDR control functions and for other potential extensions, multiple Pages can be defined for the upper half of the A2h address space. At startup the value of byte 127 defaults to 00h. This ensures backward compatibility for transceivers that do not implement the optional Page structure. When a Page value is written to byte 127, subsequent reads and writes to bytes 128-255 are made to the relevant Page.

This specification defines functions in Pages 00h-03h and 20h-27h. Pages 04h-1Fh and 28h-7Fh are reserved for future use. Writing the value of a non-supported Page shall not be accepted by the transceiver. The Page Select byte shall revert to 0 and read / write operations shall be to the unpaged A2h memory map (see section 4.3).

Pages 80h-FFh are reserved for vendor specific functions.

Table 10-3 Optional Page Select Byte

A2h	# Bytes	Name	Description
120-126	7	Vendor Specific	Vendor specific memory addresses
127	1	Optional Page Select	Defines the page number for subsequent reads and writes to Address A2h Bytes 128-255

11 Address A2h Page 00h/01h

The upper memory address from 128-247 in page A2h is a legacy page defined before the optional paging byte in A2h byte had been defined. To maintain backward compatibility with existing modules both pages 00h and 01h or a module that does not support paging shall implement the following features described in this section below

- 120 bytes of User EEPROM
- 8 bytes of vendor specific control functions

11.1 User Accessible EEPROM Locations [Address A2h, Page 00h / 01h, Bytes 128-247]

For transceivers that do not support pages, or if the Page Select byte is written to 00h, addresses 128-247 represent 120 bytes of user/host writable non-volatile memory - for any reasonable use. Consult module vendor datasheets for any limits on writing to these locations, including timing and maximum number of writes. Potential usage includes customer specific identification information, usage history statistics, scratch space for calculations, etc. It is generally not recommended this memory be used for latency critical or repetitive uses. For transceivers that support page 01h, when the Page Select byte is written to 01h, addresses 128-247 may address the same data as in page 00h, or may represent an additional 120 bytes of user/host writable non-volatile memory. Consult vendor datasheets to determine which of these options is used.

Table 11-1 User Accessible EEPROM Locations

A2h	# Bytes	Name	Description
128-247	120	User EEPROM	User writable EEPROM

11.2 Vendor Specific Control Function Locations [Address A2h, Page 00h / 01h, Bytes 248-255]

For transceivers that do not support pages, or if the Page Select byte is written to 00h or 01h, addresses 248-255 are defined for vendor specific control functions. Potential usage includes proprietary functions enabled by specific vendors, often managed in combination with addresses 120-127.

Table 11-2 Vendor Specific Control Function Locations

A2h	# Bytes	Name	Description
248-255	8	Vendor Specific	Vendor specific control functions

12 Address A2h Page 02h Tunability, RDT and RPM

The memory map for Address A2h Page 02h in Rev 12.4 of this SFF-8472 specification defined two bytes, specifically bytes 130 and 131; yet it did not mention that Page 02h had been used by SFF-8690 Tunable SFP+ Memory map for many years prior to Rev 12.4. To ensure proper standardization, Table 12-1 now details the full memory map of Page 02h. Remote Performance Monitoring control registers have also been added to this memory map.

Table 12-1 Register Groups for Page 02h

A2h	SFF	Read/Write	Description	Section
128	8690	RO	Feature Advertisement for Tunability	
129	**8472**	RO	Feature Advertisement	12.1.1
130-131	**8472**	RO & RW	RDT and Receiver Controls	12.2
132-141	8690	RO	Advertisement of Module Capabilities.	
142-143	8690	-	Reserved for SFF-8690	
144-147	8690	RW	Channel Tuning, Frequency and wavelength controls.	
144-150	8690	-	Reserved for SFF-8690	
151	8690	RW	Module, Module TX control	
152-155	8690	RO	Diagnostics Frequency or Wavelength Error	
156-167	8690	-	Reserved for SFF-8690 Tunable Section	
168	8690	RO	Current Status	
169-171	8690	-	Reserved for Additional Status	
172	8690	RO	Latched Status	
173	8690	-	Reserved for Additional Latched Status	
174-175	**8472**	RO	Remote PM COR Latched Status.	12.3.2
176-191	**8472**	-	Reserved	
192-255	**8472**	-	Remote PM See Section 12.3	12.3

12.1.1 Feature Advertisement

Table 12-2 defines feature advertisement for Receiver Decision Threshold (RDT) and Remote Performance Monitoring (RPM).

Table 12-2 Page 02h Feature Advertisement

A2h	Bit	Name	Description
129	7	Reserved	
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	RPM supported	RPM (Remote Performance Monitoring) Supported. 0b - Not Supported 1b - Supported
	1	RDTcurrval	RDT (Receiver Decision Threshold) current value readable Advertisement. 0b. Current Value used by RDT is not readable. 1b. Current Value used by RDT value in Byte 131 if Byte 129 bit 0=1b.
	0	RDTmode	This advertises the behavior of RDT of the module. 0b - RDT mode per Rev 12.4 (legacy) 1b - RDT mode per Rev 12.5 See Section 12.2 for details.

12.2 Variable Receiver Decision Threshold [A2h, Page 02h, Bytes 130-131]

Table 12-3 defines the variable receiver decision threshold registers. The availability of this function is indicated in address A0h, byte 65, bit 7. There are two behaviors associated with this function as described in sections 12.2.1 and 12.2.2. For either behavior, byte 131 is a two's complement 7-bit value (-128 to +127), defining the decision threshold as a percentage of receiver eye amplitude given by the following equation:

Decision Threshold = 50% + [Byte (131) / 256] * 100%

Table 12-3 Variable Receiver Decision Threshold Control

Address	Bits #	Name	Description
130	7-1	Reserved	
	0	RDT mode	0b. RDT mode is manual 1b. RDT mode is automatic (module control loop)
131	7-0	Optional RDT Value	Value sets the receiver decision threshold: 10000000b = -128; threshold = 0% 00000000b = 0; threshold = 50% 01111111b = +127; threshold = 99.61%

12.2.1 RDT Behavior prior to and including Rev 12.4

In SFF-8472 revisions prior to and including Rev 12.4, Byte 130 is reserved and does not contain any information and Byte 131 is only a control register and will not reflect the status of current value of RDT used. The module is expected to behave as follows:

- Module powers up with RDT value in Byte 131 = 0. (50%)
- Variable RDT control mode is defined by the module vendor. It may include:
  - No active RDT or undefined active RDT control (default Byte 130.0 = 0)
  - RDT controlled as function of temperature as defined by the module vendor (default Byte 130.0 = 1)
- A write to Byte 131 sets the RDT to the value set in Byte 131. This stops any active control of the RDT value by the module. From this point RDT is in manual control mode.
- Once in RDT manual mode, there is no convenient means of reverting the RDT to automatic mode (or back to default mode of the module). Only a power cycle will revert the module back to module's default control mode.

12.2.2 RDT Behavior post Rev 12.4

RDT post revision 12.4 includes two advertisement bits in Byte 129 Table 12-2.

- Byte 129 Bit 0.
  - If 0b, advertises that RDT mode behaves as prior to revision 12.4 of this document.
  - If 1b, advertises that RDT mode behaves as described in this section.
- Byte 129 Bit 1. This is only applicable if Byte 129 Bit 0 is set to 1b.
  - If 0b, advertises that the module does not return the current RDT value in Byte 131.
  - If 1b, advertises that the module returns the current RDT value in Byte 131.

RDT post revision 12.4 includes a new control bit in Byte 130 bit 0. It also allows Byte 131 to return the current RDT value, when the RDT mode is controlled automatically by the module.

- Byte 130.0
  - 0b. RDT is in manual mode. The RDT value is defined by Byte 131 or a 2-wire write to Byte 131.
  - 1b. RDT is in automatic mode. The RDT value is controlled by the module. Furthermore, if Byte 129 Bit 1 = 1b, the current RDT value used by the module will be reported in Byte 131. If Byte 129 Bit 1 = 0b, the current RDT value will not be reported in Byte 131 and the value of Byte 131 will not be changed by the module.

If Byte 130.0 is changed from 1b to 0b, then the RDT value will freeze at its current value. At the transition, if Byte 129 Bit 1 = 1b, Byte 131 shall display the RDT value used. If Byte 129 Bit 1 = 0b, Byte 131 does not display the current value of the RDT. Since Byte 130.0 has been changed to 0b (manual mode), RDT can now be written by the host to take over control of the RDT.

In this update, RDT Byte 131 value is:

- RO when RDT is in automatic mode. (Byte 130.0=1b)
- RW when RDT is in manual mode. (Byte 130.0=0b)
- Writing to this byte no longer automatically enables RDT mode.

12.2.3 RDT options

Table 12-4 defines the variable receiver decision threshold registers. The availability of this function is indicated in address A0h, byte 65, bit 7. There are two behaviors associated with this function as described in sections 12.2.1 and 12.2.2. For either behavior, byte 131 is a two's complement 8-bit value (-128 to +127).

Table 12-4 RDT Options

Advertisement			Description
129.0	**129.1**	**130.0**	
0	x	x	Legacy Mode (prior and including Rev 12.4) RDT value is not readable in Byte 131. Write to Byte 131 - Will stop module control of RDT - RDT will take the value written to Byte 131.
1	0	0	RDT is in manual mode. - RDT is set by the module to some value defined by the vendor and not changed once set. Write Byte 131 - RDT will take the value written to Byte 131. Read Byte 131 will return the current RDT value used by the module or set by the host on a write to Byte 131.
	0	1	RDT is in automatic mode. - RDT is set by the module - A control loop may be present to continuously set the RDT Write Byte 131 - Byte written will be ignored. - Host shall change Byte 130.0=0b to write to Byte 131. Read Byte 131 will not return the current RDT value used by the module.
	1	0	RDT is in manual mode. - RDT is set by the module to some value defined by the vendor and not changed once set. Write Byte 131 - RDT will take the value written to Byte 131. Read Byte 131 will return the current RDT value used by the module or set by the host on a write to Byte 131.
	1	1	RDT is in automatic mode. - RDT is set by the module - A control loop may be present to continuously set the RDT Write Byte 131 - Byte written will be ignored. - Host shall change Byte 130.0=0b to write to Byte 131. Read Byte 131 will not return the current RDT value used by the module.

12.3 Remote Performance Monitoring (RPM) – Optional Feature

Remote Performance Monitoring (RPM) is a method that allows a transceiver to be remotely managed over its media interface. The detail method is described in "MOPA Remote Monitoring Specifications v1.0". A transceiver with hardware supporting RPM may use registers defined in this section and the additional pages 20h to 27h defined in this document for the management of the remote transceiver. If transceivers at both ends of the link support RPM, the RPM features can be enabled.

The support of RPM requires enhanced hardware and firmware features and is entirely optional.

A transceiver supporting RPM shall be able to transmit and receive digital messages using a low-speed low-modulation signal modulated on top of the primary signal of the media interface, so that a low-bandwidth envelope detector can detect these messages. The signal characteristics of this modulated signal is described in ITU-T G.698.4 with the exception that the transmitted signal is at 5 kbps @ 100,000 ppm (5 kbps +/- 50,000 ppm) absolute accuracy, instead of 50 kbps @ 100 ppm (50 kbps +/- 50 ppm). This means that the rate of the transmitted signal may be between 5 kbps +/- 50,000 ppm or may vary from 4.75 kbps to 5.25 kbps. The choice of 5 kbps has been established to allow firmware only encoding and decoding of RPM messages with minimal hardware support. Implementation with higher transmission frequency e.g. 50 kbps, may require additional hardware, such as an FPGA. Furthermore, the choice of 100,000 ppm instead of 100 ppm is to eliminate the need for a precision clock and allow the use of the internal microcontroller clock.

Other key features of this modulated signal relevant to this specification remain the same as defined in ITU-T G.698.4, including:

- A definition of a message frame consisting of a 48-bit frame starting with a 11-bit TOM (Type Of Message) and a 24-bit MSG (Message Content) fields, with 5-bit and 8-bit Hamming code checksums respectively, as shown in Figure 12-1. These Hamming code checksums, positions and transmission bit-orders are detailed in ITU-T G.698.4.
- Message frames are transmitted back-to-back continuously with no padding bits in between frames.
- Reception of the continuous bit-stream are sent to a "Framer" which will find the boundaries of the 48-bit frame by comparing the checksums.
- The Framer declares Frame lock when 2 consecutive frame matches the expected checksum.
- The Framer declares Frame un-lock when 6 consecutive frames checksum are mismatched.

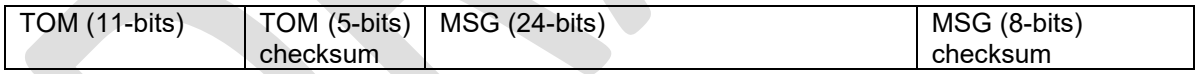

Figure 12-1 G.698.4 Frame Structure

In a typical network, transceivers installed on HEE (Head-End Equipment) are connected over the medium to a transceiver installed on a TEE (Tail-End Equipment). Transceivers connected on TEE may benefit from being managed remotely over the media interface, as the location of the TEE may be remote and hence more difficult to be managed locally. In such a system, it is desirable to have the following features for a transceiver with RPM capabilities.

- Symmetrical. Transceivers on either side of the media link shall have the same firmware.
- Capability to transmit Remote Digital Diagnostics Monitoring (RDDM) over the media interface.
- Capability to transmit Inventory Data within two seconds (2 s) after link is established.
- Capability to transmit Alarms and Warnings.
- RPM channel can be remotely enabled/disabled over the media interface.
- Security features allowing which registers can be transmitted.
- Error counters to measure the quality of the RPM channel and calculate its frame error rates.

The method defined by MOPA and the registers specified here supports all the listed features above. This is achieved by the specification of a transmitter and receiver state machine by "MOPA Remote Monitoring Specification" which defines 5 new TOM (Type Of Message) codes to supplement G.698.4. This facilitates the exchange of data with the remote transceiver with minimum host software intervention and essentially presents the memory map of the remotely managed transceivers at the local transceiver in the pages 20h to 27h. Section

12.4 briefly describes the TOM codes that are used for RPM channel with more details described by the "MOPA Remote Monitoring Specification".

12.3.1 Remote Performance Registers

Remote Performance Registers are the contents of the entire memory map of SFF-8472 registers of the remote transceiver mapped to the local transceiver at pages 20h to 27h (section 4.3). In addition to these pages, memory map registers in A2h Page 02h, listed in Table 12-554, are provided for managing the RPM feature. These registers are applicable if the transceiver supports the RPM feature.

Table 12-5 Register Summary for Remote Performance Monitoring

A2h	Function	Description	Section
129	Adv	Feature Advertise of RPM	12.1.1
174-175	COR latch	COR latched Registers for Remote PM	12.3.2
192-197	Status/Debug	Clock Status and Debug Registers	12.3.3
198-207	Error Counters	Return frame error counters, enables calculation of BER or FER	12.3.4
208-210	Tx Remote Cmd	Allow remote memory map to be written.	12.3.5
211	Tx Mod Index	Tx RPM disable or TX RPM Modulation Index	12.3.6
212-219	Control	Control Registers	12.3.8
220-239	Reserved	Reserved	
240-247	User Remote TX Data	User Data to be transmitted over the RPM channel. A host write to these bytes via the 2-wire interface. Writing to Byte 247 triggers the sending all 8 bytes over the RPM channel. RPM link needs to be established for the data to be successfully sent.	12.3.10
248-255	User Remote RX Data	User Data received from the RPM channel. Read only bytes from 2-wire interface. RPM channel will write to these bytes when "User Remote TX Data" bytes are received by the RPM channel.	12.3.10

12.3.2 Remote Performance Latched Alarms

RPM Latched alarms are listed in Table 12-665. These alarms are latched alarms and Cleared On Read (COR) only if the alarm condition no longer prevails after the read operation. A latched alarm bit is held at 1b while the condition persists and is cleared to 0b on a 2-wire read when the condition no longer persists.

For ease of use, these alarms are placed at Bytes 174-175 in the same group as the latched alarms for Tunability, to allow more efficient reads of COR alarms.

Table 12-6 Page 02h Remote Performance COR Latched Alarms

A2h	Bit	Name	Description
174	7	L-RxUserData	This bit is set to 1 whenever the Remote PM has received a new data frame that consists of content destined for A2h.Pg2 Bytes 248-255 AND the content of these bytes have been updated.
	6	L-RxUserChanged	This bit is set to 1 whenever A2h.Pg2 Bytes 248-255 has been updated by the remote PM data AND the content of the corresponding bytes has changed. That is if any of the byte that was replaced has a different value this latched bit will be set to 1.
	5	L-TxUserSending	This bit is set to 1 when the module receives a write to A2h.Pg2.Byte 247 and has started processing the message to send user data. This bit will be set to 0 when the user data in A2h.Pg2.Byte 247 has been sent. The host will know if the data has been sent once this bit is set to 0.
	4	L-TxUserDataOvrrun	This bit is set to 1 if the host performs a 2-wire write to A2h.Pg2.Bytes 240-247 whilst the RPM channel is still sending user data in A2h.Pg2.Bytes 240-247 . See section 12.3.10.
	3	L-GlobalRxError	Latched-Logical "OR" of bits 2-0. Summary of alarms. "Communication Failure Alarm"
	2	L-MsgError	MSG Hamming code error has been detected in the G.698.4 received 48-bit frame and the frame has been discarded. This bit will be set to 1 only once frame lock has been established. The host may read A2h.Pg2.Byte 206-207 (frameMsgErrCount) to find out how many frames were discarded.
	1	L-TomError	TOM Hamming code error has been detected in the G.698.4 received 48-bit frame and the frame has been discarded. This bit will be set to 1 only after frame lock has been established. The host may read A2h.Pg2.Byte 204-205 (frameTomErrCount) to find out how many frames were discarded.
	0	L-FrameUnlock	This bit is set to 1 as long as the RX framer has not established frame lock. A2h.Pg2.Byte 192 contains the current status of frame lock. NOTE: when frame lock has been established, this bit will be "cleared on read" whereas this bit remains set to 1 if frame lock has not been established. It will take 6 consecutive errored frames to declare a frame unlock state, hence, once frame is locked, it will take at least 57.6 ms for frame unlock to be detected before this alarm is raised again.
175	7	Reserved	
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	L-2ABMsg TX	This bit is set to 1 when the module transmits the security idle message (TOM=2ABh). This is used to indicate that RPM is enabled but the security bit A2h.217.7 is set preventing remote management data to be transmitted.
	2	L-2ABMsg RX	This bit is set to 1 when the module receives security protection IDLE messages (TOM=2ABh is received).
	1	L-CtrlMsg2A0_NACK	This bit is set to 1 when the local module receives a TOM 2A0h msgType = 1b NACK message from the Remote Module via the RPM channel.
	0	L-CtrlMsg2A0_ACK	This bit is set to 1 when the local module receives TOM 2A0h msgType = 1b ACK message from the Remote Module via the RPM channel.

12.3.3 Remote Performance Monitoring Status

A host may read this register described in Table 12-776 to read the status of RPM channel's receiver status. Once the RX framer has locked, then communication from the remote transceiver has been established. Other bits in this register report various states that the RPM receiver to allow trouble shooting of the RPM channel.

Table 12-7 Page 02h Remote Performance Monitoring Status Registers

A2h	Bit	Name	Description
192	7	S1_Data Ready	This bit is raised when all the S1_Data has been received and validated by performing checksum calculations and comparisons.
	6	Reserved	Reserved.
	5	Clk Hi detected	In Manchester Encoded bit-stream, there will be two clock frequencies. Ex. a 5 kbps signal will have 5 kHz and 10 kHz frequencies. This is an optional bit that indicates that the 10 kHz signal "Clk Hi" is detected. The purpose of this bit is to enhance the debugging of the RPM channel.
	4	Clk Lo detected	In Manchester Encoded bit-stream, there will be two clock frequencies. Ex. a 5 kbps signal will have 5 kHz and 10 kHz frequencies. This is an optional bit that indicates that the 5 kHz signal "Clk Lo" is detected. The purpose of this bit is to enhance the debugging of the RPM channel.
	3	RPM Frame Locked	This Flag Bit indicates receiver RPM channel's frame lock state. 1b. The RX "Framer" as described in section 12.3 has locked to the 48-bit G.698.4 frame. 0b. The RX Framer has not locked or has lost lock to the 48-bit frame.
	2	Phase Locked	This Flag Bit indicates if the RX framer has locked to the correct phase boundary of the incoming Manchester Encoded signal. 1b. Indicates that the Receiver has detected the correct phase boundary for the Manchester Encoded Signal. 0b. Indicates that the Receiver is still searching for the correct phase boundary of the Manchester Encoded Signal.
	1	Bits Locked (Transitions)	Bits locked is an intermediate implementation to indicate that the receiver has detected clear transitions of bits going from 0 to 1 or 1 to 0 at the expected frequency. This flag bit indicates that the Receiver has detected the bit boundaries consistent with a Manchester encoded signal. In some systems, depending on the locking mechanism, this may be part of clock locking. If so, simply indicate the bit is 1b (locked). 1b. Locked to bit boundaries. 0b. Still looking for bit boundaries. e.g. if the signal consists of only a clock signal at 5 kbps, then only the clock locked bit will be raised. This bit further indicates that there are transitions at 180 out of phase of the clock for a 50/50 mark space ratio of a Manchester encoded bit-stream, indicating that the clock signal has a clear 5 kHz and 10 kHz tone.
	0	Clock Locked	This Flag Bit indicates that the receiver has extracted the clock frequency and is now locked to the remote transmitter's clock. The frequency difference between the transceivers may be up to 100,000 ppm. Transmitter local oscillator at -50,000 ppm and Receiver local oscillator at +50,000 ppm. 1b. Receiver has detected the clock frequencies for the incoming bit-stream. 0b. Receiver has not detected any expected clock frequencies.

		Special Write Only Function when a value is written to this register, Byte 192.	Writing to this read-only status register with a value of A5h, the module shall reset all the error counters registers (see section 12.3.4). Writing any other value shall have no effect. The only way to verify this write has been accepted is to read the error counter registers before and after the write operation. The error counter registers are provided in the memory map for device characterization and link characterization during production or normal operating conditions. These error counter registers could also be used by a host to dynamically change the modulation index (see 12.3.6.1) to optimize the performance of the RPM channel. If a host is not interested in link performance of the RPM channel, the host can ignore these error counter registers. However, if the host management system is interested in the RPM channel's link performance, it is recommended that the host manages error counters periodically. This is because the error counter register wrap to 0 and it is assumed that the host will accumulate the counters to maintain accurate count.
193-195		Most Recent Rx RPM MSG message value	Debugging register to indicate the value of the most recently received 24-bit MSG content. (Figure 12-1) Byte 193 contains bits 23-16, Byte 194 contains bits 15-8 and Byte 195 contains bits 7-0 of the 24 bit MSG. Once the RX Framer is locked, this register may be updated once every 9.6 ms.
196-197		Most Recent Rx RPM TOM value	Debugging register to indicate the value of the most recently received 11-bit TOM content. The upper 5 bits of byte 196 are reserved and shall be set to 0. Byte 196 contains bits 10-8 and Byte 197 contains bits 7-0 of the TOM. Once the RX framer is locked, this register may be updated once every 9.6 ms.

12.3.4 Remote Performance Monitoring Error Counters

Once the receiver framer has achieved frame lock, the counters shown in Table 12-887 may be read to evaluate the quality of the link and estimate Bit Error Rate or Frame Error Rate. The Hamming codes used in the TOM checksum and the MSG checksum can each detect up to two errors within each of the TOM or MSG. This set of counters is synchronized and maintains data coherency with Bytes 200-203 "Frame Count". Frame Count shall start counting once the frame is locked, and stop counting when a complete frame LOL event has been detected. Once the "Frame Count" has started running the errored frame count will also accumulate if there is an errored frame detected.

The host may also issue a reset by writing A2h Page 2 Byte 192 status register with the value A5h. If a reset is not issued the "Frame Count" will wrap around after 2^{32}-1 frames (or about 477.2 days of operation). Each of the frameTomErrCount or frameMsgErrCount will independently wrap around after 2^{16} -1 errored frames, if these are not reset. Thus if a host is interested in managing the error rates of the link during normal operation, it is recommended that a host resets and accumulate error statistics as needed periodically before these error counters wrap to 0.

Table 12-8 Page 02h Remote Performance Monitoring Error Counters

A2h	Bit	Name	Description
198-199	16	Frame LOL Counter	This is a 16-bit counter indicating the number of LOL events that have occurred. A LOL event is when six (6) consecutive errored frames have been received. An errored frame is when a message frame is received with a Hamming code violation in the G.698.4 header (TOM) or the message (MSG) parts of the frame.
200–203	32	Frame Count	This is a Big Endian 32 bit counter value that counts the total number of frames that has been received. It counts the frames received once frame lock has been achieved. Frames with and without errors are counted, until a complete LOL event has occurred.
204-205	16	frameTomErrCount	This is a counter that counts the number of frame header (TOM) that failed its Hamming code parity (frame has been discarded).
206-207	16	frameMsgErrCount	This is a counter that counts the number of frame message (MSG) that failed its Hamming code check (the frame has been discarded). NOTE: Once a frame TOM message error has been detected, the Hamming code detection for the MSG portion will be skipped.

12.3.5 Remote Performance Monitoring Remote Control Messages

Once the communication link between the local and the remote module has been achieved over the RPM channel, these three registers shown in Table 12-998 allow the local host to send a message that may affect the remote module's memory map. Bytes 208-210 defines the MSG content of the RPM control message which will be sent using TOM=2A0h. Hence the message that is sent is TOM=2A0h MSG=Bytes 208-210 (see Section 12.4.1). This allows any register in the remote memory of SFF-8472 to be written, subject to security settings by receiving module. For example, a control message received over the RPM message link that attempts to change the laser frequency of a tunable module should not be executed, as changing the lasing frequency would take RPM link down.

Table 12-9 Page 02h Remote Performance Monitoring Remote Control Message

A2h	Bit	Name	Description
208	8	Message content to send to remote transceiver	Bits 7-0 of the 24-bit MSG (with TOM=2A0h)
209	8		Bits 15-8 of the 24-bit MSG (with TOM=2A0h)
210	8		Bits 23-16 of the 24-bit MSG (with TOM=2A0h) Writing to this byte on the host 2-wire interface will trigger the module to transmit TOM=2A0h and this 24-bit MSG defined by these three registers.

The TOM and MSG Hamming code can detect two bits in error in the TOM and independently two bits of error in the MSG. A frame is discarded when there is one or more bits in error in the message detected by the Hamming code.

12.3.6 RPM Tx Rx Enable and Tx Modulation Index

Table 12-10109 defines the behavior of byte 211. This register can be used to enable and disable TX RPM and allow the setting of the transmitter's modulation index. Setting the modulation index to 0 will disable the TX RPM.

Table 12-10 Page 02h Remote Performance Monitoring Tx Modulation Index

A2h	Bit	Name	Description
211	7	Reserved	Reserved
	6-0	Tx RPM Enable Tx Mod Index	A value of 0. TX Modulation Index, remote performance monitoring TX is turned off. When TX RPM is turned off, there will be no modulated RPM signal transmitted. A value of 1-9. is Reserved, writing these values will set the modulation index to 1% (same as value of 10). A value between 10-100. This indicates to modulation index of 1-10% respectively. NOTE: a reasonable range for remote performance monitoring to work will be between 3 and 10%. Lower values settings are provided but are not recommended for reliable communications.

12.3.6.1 Dynamic Adjustment of modulation index

Example of Dynamic Adjustment of modulation index of Host Side TX.

Table 12-11 Example Dynamic Adjustment of RPM TX Modulation Index - Host

State	Description
Setup remote Performance Monitoring link	Setup transfer of Page 02h data to remote nodes and digital diagnostics data.
Read Page 22h Error Counters.	Accumulate error counters over time
Write Page 02h Byte 211	Increase or decrease as needed. May need to define what happens when decreasing modulation index in the event that it was decreased too low, to prevent user from setting too low (e.g. Environment conditions)

Example of Dynamically Adjustment of modulation index of Remote Side TX.

Table 12-12 Example Dynamic Adjustment of RPM TX Modulation Index - Media

State	Description
Setup remote Performance Monitoring link	Setup transfer of Page 02h data to remote nodes and digital diagnostics data.
Read Page 22h Byte 211	This is the Remote TX modulation index.
Read Page 02h Error Counters.	Accumulate error counters for this TX modulation index.
Write Page 02h Byte 208-210 to write to Remote Transceiver Page 02h, Byte 211.	If error counters are greater than acceptable, send a message to increase the modulation index. Otherwise, either send a message to slowly reduce the modulation index within limit or maintain the current modulation index.

12.3.7 RPM Enable/Disable

Table 12-131310 describes the RPM control registers bytes 212 and 213 that enable and disable RPM.

Table 12-13 RPM Control Registers

A2h	Bit	Name	Description
212	7-4	TX_RPM state	These 4 bits are read-only bits reflecting the state machine state of the RPM TX state machine. This is mainly to allow the local host to monitor the TX_RPM state.
	3	Enable Local RPM Enable RPM Enable	This bit can be written only from the host 2-wire interface. When set to 1b, the local transceiver will start to send messages to the remote transceiver to enable its RPM channel. If the local RPM channel is disabled, setting this bit will also enable the local RPM transmitter.
	2	RPM Request Send Data	This bit is read-only from the host 2-wire interface and can only be written by a message received over the RPM channel. This bit is set to 1b when the RPM message receives a command message to enable and start transmitting RPM data. It allows the RPM channel to be enable from the media interface (or a remote Transceiver)
	1	Reserved	
	0	TX RPM Enable	This bit can be written only from the host 2-wire interface. This bit will enable RPM transmission. If this bit is set to 1b TX RPM will be enabled. This is independent of the modulation index, which may be optimized, but this bit can be configured to be enabled via a message on the RPM channel. A message TOM:MSG 2A0:905401 (see section 12.4.1.2) is a message to modify the memory map at Pg2 byte 54h (or I2C address 128+84 = 212) with value 01.
213	7-4	RX_RPM state	These 4 bits are read-only bits reflecting the state machine state of the RPM RX state machine. This is mainly to allow the local host to monitor the RX_RPM state.
	3-1	Reserved	
	0	Rx RPM Enable	0b. RX RPM disabled 1b. RX RPM enabled This bit will enable and disable the RX RPM. Everything from clock recovery to framer shall be disabled. All status flags shall indicate clock and framers to be unlocked once disabled. Any RX path related hardware or software processing requirements shall be either powered down or not running respectively. This bit can be written only by the Host 2-wire interface and cannot be set to disable or enable by the RPM channel message.

12.3.8 RPM Data Transmission Control A2h Page 02 Bytes 214-215

These registers control the data being sent over the RPM channel. These can only be set from the 2-wire interface only, irrespective of the security settings in Byte 216 below.

The purpose of the RPM transmission channel is to exchange memory map. Byte 214 as shown in Table 12-141411 defines a bit mask on which group of registers will be sent as data to the remote transceiver. In the group of registers in the table, 3 register groups are not listed. These are:

- A0h:0-95. These contain non-volatile inventory information e.g. SN, PN, etc. that identifies the transceiver.
- A2h:96-119. These contains DDM, alarms and some control registers in the memory map.
- A2h:P2.192-207. These contain RPM controls and statuses.

These groups of registers are considered special registers that are transmitted without the need of any configuration. A0h:0-95 and A2h:96-119 are automatically transmitted whenever the RPM transmitter is enabled, irrespective of whether its receiver is locked or not. Once its receiver is locked, the remote transmitter will send a message indicating that it has received the inventory data A0h:0-95 and once that happens, the transmitter will now send A2h:96-119 and A2h:P2.192-207 and the contents of the register sets defined by bit-mask in Table 12-141411. The hand-shaking mechanism between the transceiver and remote transceiver is via messaging and described in "MOPA Remote Monitoring Specifications".

Table 12-14 RPM Data Transmission Control Registers

A2h	Bit	Len	Name	Description
214	7	-	Reserved	If "bit" is set to 1b then the address range for that bit will be sent as part of remote performance monitored data in State sending S2_Data. A2h.96-119 and A2h:P2.192-207 is always sent once RPM states are locked. A2h.96-119 and A0h:0-95 is always sent prior to local and remote data transfer is not locked.
	6	128	A2h.P03:128-255	
	5	32	A2h.P02.208-239	
	4	64	A2h.P02.128-191	
	3	128	A2h.P00.128-255	
	2	104	A2h.0-95,120-127	
	1	128	A0h.128-255	
	0	32	A0h.96-127	
215	7-0		Reserved	Reserved for vendor pages to be sent in RPM.

12.3.9 RPM Control and Configuration A2h Page 02 Bytes 216-219

Byte 216-217 configures additional security features for the Transmitter to further limit memory map data that can be transmitted. This byte defines a bit mask that when set, will instruct the local host to inhibit sending memory data defined by that bit. The remote receiver has commands to request specific bytes, but this byte will have priority of what can be sent. If the respective bit is set to 1b, the TOM::MSG shall still be sent (if the command to send the messages comes from the RPM channel) but the content shall be set to CCh within the TOM::MSG. This is because the remote receiver is still expected to receive the address of the memory map.

Table 12-15 RPM TX Security Features

A2h	Bit	Name	Description
216	7	A2h.P03.128-255	Inhibit Sending
	6	A2h.P02.208-239	
	5	A2h.P02.128-191	
	4	A2h.P00.128-255	
	3	A2h.120-127	
	2	A2h.0-95	
	1	A0h.128-255	
	0	A0h.96-127	
217	7	Global TX RPM Disable	Inhibit Sending any RPM (only 2ABh Idle messages)
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	Reserved	
	1	Reserved	
	0	Reserved	

Byte 218-219 configures additional security features that limit memory mapped locations writeable from the messages received over the RPM channel. If the bit is set and if the register is writeable, the range of memory defined for the bit will not be writeable from the RPM channel and is only writeable from the 2-wire host interface.

Table 12-16 RPM RX Security Features

A2h	Bit	Name	Description
218	7	Global Write Prot	This protects writing to any Register except TX_RPM_CTRL (PG2.R212)
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	WriteProtTxModIdx	This protects writing to TX Modulation Index Registers.
	1	WriteProtRxCtrls	This protects writing to receiver control registers. A2h.P02.130-131.
	0	WriteProtTunable	This protects writing to Tunable Registers. SFF-8690. A2h.P02.128-171.
219	7	Reserved	
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	Reserved	
	1	Reserved	
	0	Reserved	

12.3.10 Transmitting and Receiving User Data over Remote PM channel.

There are 8 bytes of TX and 8 bytes of RX allocated in the memory map for transmitting and receiving user data. When the host writes to bytes 240-247 of this page, the data in the bytes will be sent over the RPM channel. The write will only be triggered after byte 247 is written. See Table 12-171714 for additional details.

Bytes 248-255 are RO bytes and will reflect the user data RX over the RPM channel. See Table 12-171714 for additional details.

Table 12-17 Page 02h RemotePM TX RX User Data

A2h	Bytes	Name	Description
240-247	RW 8	RemotePM TX User Data	When Byte 247 is written, this will trigger the Remote PM to transmit the data. This shall be sent at the highest priority and should interrupt the transmission of periodic data. Whilst the 8-bytes of data is transmitting, a Latched Alarm Bit will be raised. The host shall restrain writing to these set of registers as long as this alarm is raised. If any of the bytes 240-247 is written prior to all 8-bytes is transmitted, a Latched Alarm Bit indicating "overrun" may be raised, indicating that the transmit data corruption may have occurred or the new data is ignored. This depends on whether the module implements double buffering or not. The recommendation is for the module to **not** use double buffering of these 8 bytes and raise the "overrun" alarm if these bytes are written whilst the user channel is being transmitted. This is because since this message is a higher priority message, it will interrupt the regular transmission of periodic data and hence may affect the timing update performance of periodic data. Hence the host should refrain from sending user data more than once per second to allow regular digital diagnostics message to be transferred. There is no additional indication, no change in hardware pin states, to flag that the user data has been transmitted, beside the L-TX sending alarm.
248-255	RO 8	RemotePM RX User Data	This set of 8 bytes will be updated if any of these bytes are received over the RPM channel. A latched alarm will be raised whenever the framer updates any of the I2C memory map location for bytes 248-255 in this page. In addition, whenever the RX User Data has been received, a latched alarm will be raised whenever the corresponding data byte that has been updated has a value that was changed by the RPM channel.

12.4 TOM (Type Of Message) Summary

Table 12-181815 summarizes the newly defined TOM which will be used for RPM messaging.

Table 12-18 Page 02h RemotePM TX RX User Data

TOM	Name	Purpose/Description
2A0h	CTRL_CMD_RSP See section 12.4.1	This message controls the behavior of the remote transceiver. There are two types of control messages. Type 0b. This is used to request the remote transceiver to send specific areas of the memory map. Type 1b. This is used to alter the memory map of the remote transceiver similar to an I2C write on the host interface.
2A8h	SEND_A0_PG_DATA See section 12.4.2	This message is used to send memory map of page data to the remote transceiver. The SFF-8472 device address A0h lower and A0h upper memory map are sent using this TOM. This TOM is also used to send vendor pages.
2A9h	SEND_A2_PG_DATA See section 12.4.2	This message is used to send memory map of A2h low (bytes 0-127) and A2h upper pages 0 and 2. Page 0/1 are assumed to have the same content.
2AAh	EXT_IDLE	This message is used by the state machine to send IDLE message. This is an extended IDLE message as the MSG field of this TOM consist of a running 24-bit counter. The transmitter will increment the counter each time a message has been sent. This message can also be used as a heartbeat.
2ABh	SECURITY_IDLE	This message is sent instead of the requested data when a local security flag is set by the local host preventing memory map data to be sent over the media interface. When the receiver receives this message, a flag will be raised to indicate that the remote transceiver has prevented data to be sent due to security settings.

12.4.1 TOM: 2A0h. CTRL_CMD / RSP message

This TOM is defined for the sending a message to the remote node. It allows a host to send a command message to the remote host, including writing to the memory map of the remote transceiver (SFF-8472 based transceiver). A command message that is sending commands shall be sent at a higher priority than other messages sending data packets in an application where bi-directional RPM is being continuously sent.

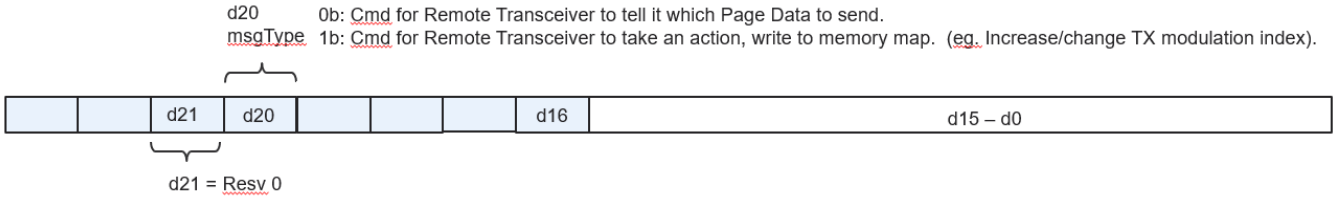

Figure 12-2 TOM 2A0h Generic Message

Figure 12-2 show the 24-bit MSG of the TOM 2A0h. This includes

- 1 bit of message type
  - 0b. Indicating message is sending page data, include Rx DDM

- 1b. Indicating a command message to affect modules memory map.
- 1 bit of reserved
- 22 bits of message content that is dependent on the message type field (d20)

12.4.1.1 TOM 2A0h. msgType = 0b

TOM 2A0h msgType 0b is to be used to command the receiver to transmit page data. When this message is received, the receiver should start transmitting data using TOM 2A8h and 2A9h message. Figure 12-3 show the fields in this message.

The receiver upon reception of this message, shall start sending page data the prescribed number of times per command in the repeatEnc portion of the message or continuously. The data shall be sent using either TOM 2A8h or 2A9h.

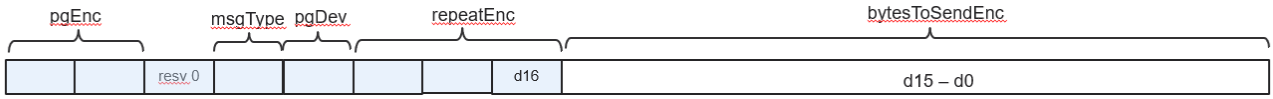

Figure 12-3 TOM 2A0h msgType 0b fields

This message consists of:

- msgType is 0b.
- pgEnc (page Encoding) and pgDev (page Devices) indicates which page data to be transmitted, together with the bytesToSendEnc mask field.
  - pgDev 0 pgEnc 0. Send A0h Low data (Bytes 0 to 127).
  - pgDev 0 pgEnc 1. Send A0h Hi data (Bytes 128 to 255)
  - pgDev 0 pgEnc 2. Resv for Vendor Page
  - pgDev 0 pgEnc 3. Resv for Vendor Page
  - pgDev 1 pgEnc 0. Send A2h Low data (Bytes 0 to 127)
  - pgDev 1 pgEnc 1. Send A2h Page 00h/01h. (Bytes 128-255)
  - pgDev 1 pgEnc 2. Send A2h Page 02h. (Bytes 128-255)
  - pgDev 1 pgEnc 3. Resv. Could be potentially used to send A2h. Page 03h.
- repeatEnc defines how many times the page data shall be sent.
  - Value of 0 mean to stop sending the data.
  - Values between 1 to 6 is to tell the receiver to transmit data set repeatedly 1 to 6 times.
  - Value of 7 mean that the data set requested shall be sent repeatedly (Remote DDM data).
- bytesToSendEnc defines a 16-bit mask. Each bit defines an 8 byte group (octet) of addresses within the page. The start address of the octet in the page = 8*bitpos. (Values are 0,8,16,…,112,120). This is a 7 bit address, so this represents the lower 7 bits address in the upper I2C address space.

12.4.1.2 TOM 2A0h. msgType = 1b

TOM 2A0h msgType 1b is to be used to command the receiver to write to a memory map location or take an action. Upon reception of this message, the receiver shall send an acknowledgement back on the TX. This command and acknowledge message will be sent as higher priority than data message.

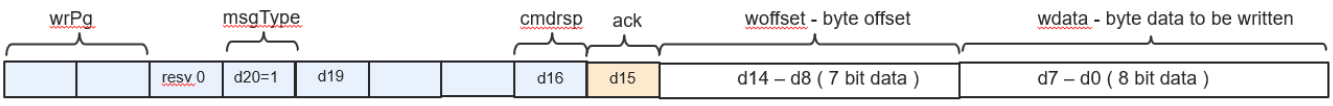

Figure 12-4 TOM 2A0h msgType 1b fields

This message consists of:

- msgType 1b.
- wrPg 2 bit encoded field.
  - wrPg 0. Write to A2h low.
  - wrPg 1. Write to A2h Page 00h/01h.
  - wrPg 2. Write to A2h Page 02h.
  - wrPg 3. Vendor defined.
- cmdRsp flag.
  - 0 bit indicates this is a command.
  - 1 bit indicates this is a response message to the command. In the case of the response message the other bits like wrPg, woffset and wdata of the command shall be echoed.
- Ack or Nack flag.
  - In a CMD message, cmdRsp = 0, this bit shall be set to 0.
  - In a RSP message, cmdRsp = 1, this bit shall indicate 0 (NACK) or 1 (ACK). The NACK mean that the action was not taken. The reason for the NACK is not defined. An ACK mean that the action was taken.
- Woffset
  - This is the 7-bit address within the page to be written. If writing to upper page, then this is the lowest 7 bit of the address.
- Wdata
  - This is the 8-bit data (byte) of the byte to be written.
- All other bits undefined shall be reserved and set to 0.

NOTE: This command allows any I2C memory of the remote transceiver in A2h Pages 00h/01h/02h to be written. The only difference is the memory map is written from a command received in the media channel as opposed to the local I2C interface. Currently it is up to the vendor's firmware to accept or not accept these writes from the media interface or only allow a certain set of registers to be writeable from the media interface.

12.4.2 TOM: 2A8h/02A9h. Sending Page Data

These two message types are used to send page content. Each frame sends only 2 bytes. The frame structure is defined in Figure 12-5. TOM 2A8h is used to send devEnc 0b message (see 12.4.1.1) and TOM 2A9h is used to send devEnc 1b.

- TOM 2A8h
  - Send Data from A0h low
  - Send Data from A0h high
  - Send Data from Vendor specific pages
- TOM 2A9h
  - Send Data from A2h low
  - Send Data from A2h Page 00h/01h.
  - Send Data from A2h Page 02h.

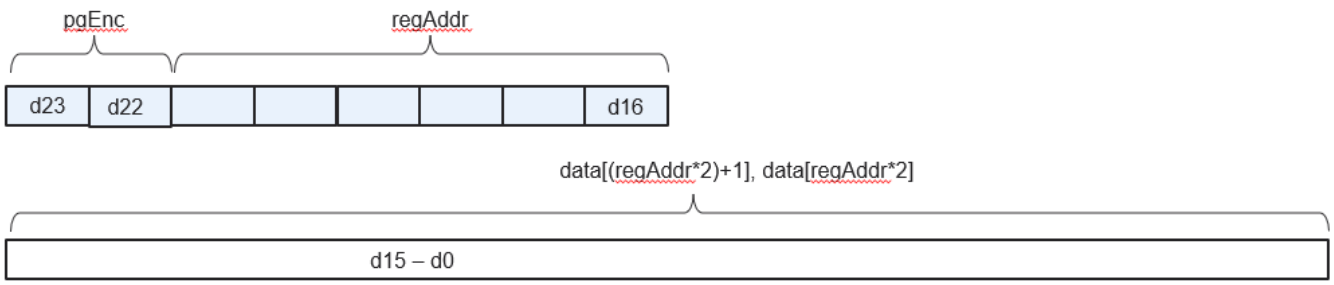

Figure 12-5 TOM 2A8h/2A9h fields

This message consists of

- pgEnc.
  - TOM 2A8h.
    - pgEnc 00b. Send data from Page A0h low
    - pgEnc 01b. Send data from Page A0h high.
    - pgEnc 10b. vendor specific.
    - pgEnc 11b. vendor specific.
  - TOM 2A9h.
    - pgEnc 00b. Send data from Page A2h low.
    - pgEnc 01b. Send data from Page A2h Page 00h/01h.
    - pgEnc 10b. Send data from Page A2h Page 02h.
    - pgEnc 11b. Reserved.
- regAddr
  - This is the top 6 bits of the byte address within a page.
- Page data (2 bytes).

12.4.3 TOM: 2AAh. Extended Idle

This TOM is defined as an extended IDLE message. The receiver does not have to act on the message. This message is can also be used as a heart beat as the MSG content consist of a 24-bit sequence number or counter. The transmitter should increment the counter each time it sends this extended IDLE message.

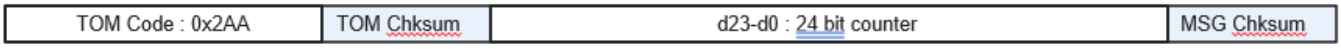

Figure 12-6 TOM 2AAh Extended Idle Fields

12.4.1 TOM: 2ABh. Security Idle

This TOM is defined as a security IDLE message. It is mainly defined to signal to the receiver that due to local security settings, the requested data cannot be sent, hence the data packet which is normally sent by using either TOM of 2A8h or 2A9h has been replaced by this security IDLE message. The MSG payload consist of a 16-bit field reserved for flags and an 8-bit sequence number.

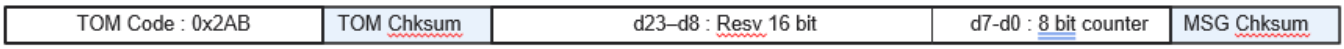

Figure 12-7 TOM 2ABh Security Idle Fields

13 Address A2h Page 03h High Accuracy Timing

Page 03h has been defined for parameters used for enhanced calibration for high accuracy timing. There are two formats depending on the format identifier at the start of the page. The two formats are

- Calibration format for Optical Modules. See Table 13-1 and section 13.4
- Calibration format for Loopback Modules. See Table 13-2 and section 13.5

This specification describes a multi-lane memory map where Lane N is defined to be within (1-8). In SFF-8472 only Lane 1 (N=1) applies.

Format ID (Bytes 128-129)

Format ID determines if page 03h contains a valid entry. One of the following valid values determines the format of the definition. The following formats are defined:

- CA1Bh => 'CALB' Calibration format for Optical Modules (see section 13.4)
- 100Bh => 'LOOB' Calibration format for Loopback Modules (see section 13.5)

CC_CALIB (Byte 255)

This check code is a one-byte code that can be used to verify that the 127 bytes of calibration configuration data are correct. It uses byte 128 to 254 inclusive to calculate the check codes. This method is the same as the CC_* check code computation in other tables in the document.

In the discovery of this page as mentioned in section 4.3, the host shall read and validate the format ID bytes 128-129 as well as a checksum CC_CALIB to be as expected before the data of this page is used.

Table 13-1 Register Summary Page 03h – Calibration format for Optical Modules

A2h	Size Bytes	Name	Description
128-129	2	Format ID	CA1Bh – Indicates page 03h has the calibration format for Optical Modules
130-149	20	Common Header	Common Header, see section 13.3
150	1	Nb_Lanes	Number of lanes for which delays are specified in the module. For SFF-8472 this value is 1.
151	1	Op_Mode_Id	ID of the “Operational mode” associated with the values of the page. For SFF-8472 this value is 0.
152-154	3	Rx_Pwr_Dly(0)	Curve coefficient for RX optical power dependent delay
155-157	3	Rx_Pwr_Dly(1)	Curve coefficient for RX optical power dependent delay
158-160	3	Rx_Pwr_Dly(2)	Curve coefficient for RX optical power dependent delay
161-163	3	Rx_Pwr_Dly(3)	Curve coefficient for RX optical power dependent delay
164-166	3	Rx_Pwr_Dly(4)	Curve coefficient for RX optical power dependent delay
167-168	2	T_Detune_Offset	Temperature dependent laser wavelength de-tuning offset
169-170	2	T_Detune_Slope	Temperature dependent laser wavelength de-tuning slope
171-174	4	Delta_Rx_Max	Largest value of the 3-sigma standard deviations of all (one for SFF-8472) reported Average Receiving delays, in ns
175-178	4	Delta_Tx_Max	Largest value of the 3-sigma standard deviations of all (one for SFF-8472) reported Average Transmitting delays, in ns
179-182	4	Avg_Rx_Lane	Average Receiving delay on Lane, in ns
183-186	4	Avg_Tx_Lane	Average Transmitting delay on Lane, in ns
187-254	68	Reserved 00h	All bytes 00h
255	1	CC_CALIB	Checkcode over bytes 128-254

See 13.4 Calibration format for Optical Modules.

Table 13-2 Register Summary Page 03h – Calibration format for Loopback Modules

A2h	Size Bytes	Name	Description
128-129	2	Format ID	100Bh – Indicates page 03h has the calibration format for Loopback Modules
130-149	20	Common Header	Common Header, see section 13.3
150-153	4	Calibration Inaccuracy	Largest value of the 3-sigma standard deviations of all reported delays.
154	1	Reserved 00h	Byte 00h
155-158	4	Tx_to_Rx Delay	Delay from looped back Tx to Rx port
159	1	Reserved 00h	Byte 00h
160-163	4	Tx_to_Mon Delay	Delay from Tx port to MON monitoring connector
164	1	Reserved 00h	Byte 00h
165-168	4	Rx_to_Mon Delay	Delay from Rx port to MON monitoring connector
169-254	86	Reserved 00h	All bytes 00h
255	1	CC_CALIB	Checkcode over bytes 128-254

See 13.5 Calibration format for Loopback Modules.

This page 03h is read-only by the host application to avoid accidental erasures of the contents of the page. However, the module shall support a method to allow the content of this page to be written via the 2-wire interface. This allows outsourcing of high accuracy calibration to a specialized third party.

The method to write to this page is currently not defined here in this specification and is left to the manufacturer.

13.1 Definition of time reference planes and delays associated

The delay calibration parameters stored in page 03h apply to delays between electrical and optical time reference planes (also called phase planes). These reference planes are:

- **Electrical reference plane:** If connectors are used that specify their reference plane (like many RF connectors) then that reference plane shall be used. Otherwise the electrical reference plane shall be the landing spot of the contact finger.
- **Optical reference plane:** The fiber physical contact plane.

Manufacturers shall specify the reference planes that apply to the calibration of their modules.

13.1.1 Delays associated with Optical Modules

All Rx delays are from optical reference plane to electrical reference plane; all Tx delays are from electrical reference plane to optical reference plane.
The module is characterized (in each direction) by two types of delays:

- Avg_Rx/Tx_LaneN: an average delay, and
- Delta_Rx/Tx_Max: a 3 sigma deviation from the average delay to take into account variations that can occur between different units of the same module type and over the lifetime of the device, and calibration inaccuracies.

IEEE Std 1588 allows for the compensation of known delays and their asymmetries in the ingress and egress paths. The average delay (Avg_Rx/Tx_LaneN) is used by the host of the module as input for this compensation. When a module has multiple lanes, the host will select one of the lanes for sending the PTP messages. Therefore the host needs the average delay value for each lane. The remaining unknown residual delay cannot be compensated for, but the value of Delta_Rx/Tx_Max can be used to estimate the remaining inaccuracy of the module after compensation of the average value. As the choice of the lane for PTP cannot be controlled outside the host, a single value (worst-case, i.e. maximum over all its lanes) is sufficient per module. More details about the role of the host can be found in IEEE 802.3cx-2023.
The actual Receiver delay of a lane "N" (Rx_delay_LaneN) of the module (in a given operational mode) is statistically bounded by the 3 sigma range;

$$\text{Avg\_Rx\_LaneN} - \text{Delta\_Rx\_max} \leq \text{Rx\_Delay\_LaneN} \leq \text{Avg\_Rx\_LaneN} + \text{Delta\_Rx\_max} \quad \text{13.1.1-(1)}$$

Similarly, the actual Transmitter delay of a lane "N" (Tx_Delay_LaneN) of the module (in a given operational mode) is bounded by the 3 sigma range;

13.1.1-(2) Avg_Tx_LaneN – Delta_Tx_max ≤ Tx_Delay_LaneN ≤ Avg_Tx_LaneN + Delta_Tx_max

The number of lanes defined in SFF-8472 is 1.

13.1.2 Delays associated with Loopback Modules

A Calibration Loopback Module (Figure 13-1) provides calibrated access to the electrical reference plane (see 13.1) of the module's connector to enable electrical absolute calibration of equipment that use optical modules.

The module is characterized by:

- Tx_to_Rx, Tx_to_Mon and Rx_to_Mon: average delays between the respective ports of the module, and
- Calibration Inaccuracy: largest value of the 3-sigma standard deviations of all reported delays.

Note: This method originates from H. Peek and P. Jansweijer, "White Rabbit Absolute Calibration."

13.2 Numeric Formats

The calibration parameters in this page use numeric fixed-point arithmetic formats described in sections 13.2.1 to 13.2.6. The fixed-point arithmetic format notation used is: q<Number of bits for integer part>.< Number of bits for fractional part >. The value in this format is obtained by multiplying the original value by $2^{<\text{Number of bits for fractional part}>}$. For example, 2.5 ns is expressed in q48.16 format as 0000 0000 0002 8000h.

NOTE: These numeric formats used for time are similar to the IEEE Std 1588 Time Interval data type (q48.16), which is used to store ingress/ingress latencies, such that conversions and calculations are simple.

13.2.1 Description of the q16.16 format for time delay

Time in ns is represented by a fixed-point unsigned 32-bit integer in q16.16 format. The range of delays that can be represented is from 0 to 65 μs (2^{16} ns) with a granularity of 15 fs ($1/2^{16}$ ns).

13.2.2 Description of the q8.16 format for time correction

Time correction in ns is represented by a fixed-point signed two's complement 24-bit integer in q8.16 format. The range of delays that can be represented is [-128.0000 to +127.9999] ns with a granularity of 15 fs ($1/2^{16}$ ns).

13.2.3 Description of the q8.8 format for temperature

Temperature in ºC is represented by a fixed-point signed two's complement 16-bit integer in q8.8 format. The range of temperature that can be represented is [-128 to +127.996] ºC with a granularity of $1/2^8$ ºC
.

13.2.4 Description of the q8.8 format for wavelength correction

Wavelength correction in $1/10^{th}$ of a nm (0.1 nm) is represented by a fixed point signed two's complement 16-bit integer in q8.8 format. The range of wavelength that can be represented is [-12.8 to +12.7996] nm with a granularity of 0.4 pm ($1/2^8$ * 0.1 nm).

13.2.5 Description of the q8.16 format time correction coefficient

Time correction in ns per dBm^n is represented by a fixed-point signed two's complement 24-bit integer in q8.16 format. The range of coefficient that can be represented is [-128.0000 to +127.9999] ns/dBm^n with a granularity of 15 fs/dBm^n ($1/2^{16}$ ns/dBm^n). The "n" is the order of the coefficient.

13.2.6 Description of the q8.8 format for wavelength correction rate (temperature change)

Wavelength correction in 1/100 of a nm (0.01 nm) per ºC is represented by a fixed point signed two's complement 16-bit integer in q8.8 format. The represented range is [-1.28 to +1.27996] nm/ºC with granularity of 0.04 pm/ºC ($1/2^8$ * 0.01 nm/ºC).

13.3 Common Header Section

Table 13-3 Register Groups for Page 03h

A2h	Size Bytes	Name	Description
130	1	Version	This version number shall be 01h
131-133	3	Calibration Date	
134-139	6	Cal Uniq ID	Calibration Unique Identifier (CUI). Calibration Responsible
140	1	Stratum	Calibration Stratum. 0 is the highest precision.
141-149	9	Reserved	Common header section. Reserved 00h.

13.3.1 Version (Byte 130)

This is the version number that describes this memory map format. It shall be set to 1.

13.3.2 Calibration Date (Bytes 131-133)

The 3 bytes define the "Calibration Date" which is the date at which the calibration for this module was validated. Each field described below cannot be all "1"s. If any field is invalid because the field is set to all 1s bit value, then the Calibration Date is deemed invalid.

Table 13-4 Page 03h High Accuracy Timing Calibration Date Encoding

A2h	Bit	Name	Description
131	7-0	Year encoding	This byte conveys the Year encoding. YEAR = Byte131 + 2000. Byte131 = FFh means this year encoding is not valid/defined.
132	7-4	Month Encoding	These 4 bits define the Month encoding. MONTH = Byte132.7-4.
	3-0	Day Encoding	See Byte133.7. Day encoding is a 5-bit value. These 4 bits are the upper bits of the 5-bit value.
133	7	Day Encoding	This bit defines the least significant bit of the day encoding. DayByte = (Byte132.3-0)<<1) + Byte133.7 DAY = DayByte + 1.
	6-0	Number Encoding	Number in the range 0 to 126 is assigned such that multiple calibrations done in one day can be distinguished. The number value of 127 is considered not valid.

As an example, December 29, 2024 is encoded as follows:

- Byte 131 = 18h (24d). YEAR = 2000 + 24 = 2024.
- Byte 132 = CEh.
  - Month = Ch (12d).
  - Partial Date value = Eh. (see next line below)
- Byte 133 bit 7 = 0b
  - DATE = (Eh<<1) + 0h + 1 = 1Dh. (29d).

Note that one is added to DayByte ('DayByte+1') so that 31 calendar days can be encoded with the value range

from 0 to 30 of DayByte. The value 31 of DayByte (all 1s bit value) is reserved to mean invalid.

13.3.3 Calibration Unique Identifier (CUI) (Bytes 134-139)

The CUI consists of a 48-bit, 6 byte value, representing:

- OUI/CID (Organizational Unique Identifier, assigned by IEEE or Company Identifier). This field identifies the organization that is responsible for the calibration (the Calibration Responsible).
- OSI (Organizational Specific Identifier) assigned by the Calibration Responsible for internal identification (device, version, etc.).

The Calibration Responsible is the organization that performs the calibration which is not necessarily the vendor.

Table 13-5 Page 03h Calibrated Unique ID format

A2h	Size Bytes	Name	Description
134-136	3	OUI/CID	Organization Unique Identifier Company ID (Identifier) - As assigned by IEEE.
137-139	3	OSI	Organization Specific Identifier.

13.3.4 Stratum (Byte 140)

This byte provides stratum value which indicates the length of the calibration chain, i.e. calibrator generation.

Calibration accuracy decreases with each calibrator generation. For example, an SFP calibration performed using proper equipment would render stratum n=0, such SFP can become a calibrator. An SFP calibration performed using a calibrator SFP with stratum n=0 would render SFP with stratum = 1 (next calibrator generation), such SFP can become a calibrator again, and so forth. The n-th generation has Stratum-n (0 being the highest accuracy). When Stratum is unused or undefined this byte should be set to FFh.

NOTE: This value is informative, the inaccuracy of the provided calibration values is provided by calibration inaccuracy bytes (see 13.1.1 and 13.1.2).

13.4 Calibration format for Optical Modules (Bytes 150-254)

Table 13-1 shows the summary of the register definitions when the Format ID is equal to CA1Bh (i.e., the "Calibration format for Optical Modules" is used). The details of the registers are described in this section.

13.4.1 Nb_Lanes (Byte 150)

This unsigned integer value of 1 Byte indicates the number of lanes supported by the module. SFF-8472 supports a single lane so this value is 1. This field is introduced for compatibility of Page 03h with multi-lane modules.

13.4.2 Op_Mode_Id (Byte 151)

This unsigned integer value of 1 Byte indicates the operational mode for which the set of delay values of page 03h are valid.
An operational mode is a given combination of interface speed, DSP algorithms (e.g., FEC schemes), etc… Different operational modes can lead to different delay values. The intention of this field is to identify the operational mode for which the delay values in the page apply. The Id is an arbitrary number set by the module manufacturer. The host is aware of the current operational mode of the module and needs to know the association to the corresponding Id, via configuration. Note that the assumption is that all lanes operate in the same mode, so a single Op_Mode_Id reflects the mode of all lanes.
The module shall support at least one mode and contain at least one page. The default value is 0, which indicates that the module has only a single operational mode it can work in. This is the scope of this document. Modules with multiple operational modes would have one Op_Mode_Id value (different from 0) per mode and one associated page per mode. This is out of scope of this document.

13.4.3 RX Power Dependent Delay (Bytes 152-166)

These bytes provide Rx_Pwr_Dly(4-0) coefficients (see table 13-1) in q8.16 format (see 13.2.5) of an RX power dependent delay curve that is described by a 4th order polynomial (equation 13.4.3-(1)).

$$\text{13.4.3-(1) } Rx\_Pwr\_Dly\_Cor\ (ns) = Rx\_Pwr\_Dly(4) * Rx\_PWR\_dBm^4 + Rx\_Pwr\_Dly(3) * Rx\_PWR\_dBm^3 + Rx\_Pwr\_Dly(2) * Rx\_PWR\_dBm^2 + Rx\_Pwr\_Dly(1) * Rx\_PWR\_dBm + Rx\_Pwr\_Dly(0)$$

Where (see Table 13-1)

- Rx_Pwr_Dly(0) is located in bytes 152-154 in format q8.16 (in ns/dBm^0)
- Rx_Pwr_Dly(1) is located in bytes 155-157 in format q8.16 (in ns/dBm^1)
- Rx_Pwr_Dly(2) is located in bytes 158-160 in format q8.16 (in ns/dBm^2)
- Rx_Pwr_Dly(3) is located in bytes 161-163 in format q8.16 (in ns/dBm^3)
- Rx_Pwr_Dly(4) is located in bytes 164-166 in format q8.16 (in ns/dBm^4)

The resulting Rx_Pwr_Dly_Cor value shall be converted to the q8.16 format (in ns, see 13.2.2). If the result of the equation 13.4.3-(1) yields a value outside the q8.16 range then the result of Rx_Pwr_Dly_Cor shall be bounded to the respective min or max of the q8.16 format.

The input variable RX_PWR_dBm in equation 13.4.3-(1) is calculated using 13.4.3-(2).

$$\text{13.4.3-(2) } Rx\_PWR\_dBm = 10 * \log10(Rx\_PWR)$$

The input variable in equation 13.4.3-(2) is Rx_PWR (see sections 9.2, 9.3 item 5). It is read in 0.1 microwatt units and shall be converted into dBm units, Rx_PWR_dBm as per the 13.4.3-(2) equation, before being used in equation 13.4.3-(1) to calculate the output delay correction (Rx_Pwr_Dly_Cor) for Average Receiving delay (Avg_Rx_LaneN, see section13.1.1) in ns using q16.16 format (see section 13.2.2). The correction shall be applied as follows:

$$\text{13.4.3-(3) } Avg\_Rx\_LaneN\_Corrected = Avg\_Rx\_LaneN + Rx\_Pwr\_Dly\_Cor$$

Where

- Avg_Rx_LaneN is located in bytes (179-182)+(N-1)*8 (see 13.4.6), in unsigned q16.16 (in ns, see 13.2.1)
- Rx_Pwr_Dly_Cor is the result of 13.4.1-(1) in signed q8.16 (in ns, see 13.2.2)

And the resulting Avg_Rx_LaneN_Corrected is in format q16.16 (in ns, see 13.2.1), it is the average delay, corrected for received power, for the module in the receiver direction of lane N.
The result of equation 13.4.3-(3) should be limited within the range of unsigned q16.16 (see 13.2.1) even if it can yield a value outside of this range.

When the Rx_Pwr_Dly(4-0) fields are not used then the bytes 152-166 shall be set to zero.

13.4.4 T_Detune_Offset (Bytes 167-168), T_Detune_Slope (Bytes 169-170)

These bytes provide T_Detune_Offset and T_Detune_Slope coefficients (see table 13-1) in equation 13.4.4-(1) that defines temperature-dependent wavelength de-tuning with respect to the specified laser wavelength. When a module has multiple lanes, it is expected that the lasers will have similar thermal behavior. Therefore the characterization of a single laser is sufficient per module.

The input variable in equation13.4.4-(1) is the temperature in fixed point q8.8 format (see section 13.2.3 and sections 9.2, 9.3 item 1). The output of the equation is the correction to the specified wavelength, expressed as a fixed point q8.8 value (see section 13.2.4). This means that de-tuning can range from -12.8 nm up to +12.7996 nm, from the specified laser wavelength.

$$\text{13.4.4-(1) } T\_Detune\ (0.1\ nm) = T\_Detune\_Slope * T(C) + T\_Detune\_Offset$$

Where:

- T_Detune_Offset is in q8.8 (in 0.1 nm, see 13.2.4)
- T_Detune_Slope is in q8.8 (in 0.01 nm/ ºC, see 13.2.6)

When the T_Detune_Slope and T_Detune_Offset fields are not used then the bytes 167-170 shall be set to zero.

The resulting T_Detune value shall be converted to the q8.8 format (see 13.2.4). If the result of the equation yields a value outside the q8.8 range then the result T_Detune shall be bounded to the respective min or max of the q8.8 format.

13.4.5 Delta_Rx_max (Bytes 171-174), Delta_Tx_Max (Bytes 175-178)

The residual delay is indicated in unsigned q16.16 format (see 13.2.1) in ns units. It represents the maximum over all lanes (for SFF8472 the number of lanes is 1) of the 3-sigma deviations from the average delays in the respective direction (receiving or transmitting). It is an unknown delay introduced by the device and holds for all reported delays. When related to the average values in section 13.4.6 and 13.4.7, it can be used to classify the synchronization inaccuracy performance of the device.

NOTE: The reported values shall take account of the inaccuracy of the calibration process and calibration generation chain that is indicated by the stratum value, see 13.3.4.

13.4.6 Avg_Rx_LaneN with N=1 for SFF-8472 (Bytes (179-182)+(N-1)*8)

The delay is indicated in unsigned q16.16 format (see 13.2.1) in ns units. It represents the average delay characterized for the module in the Receiver direction of lane N. It is the known delay added by the device, and can be compensated for by the host, e.g., for the purpose of synchronization using IEEE Std 1588.
The register of unused or non-existing lanes is filled with 00h Bytes.

13.4.7 Avg_Tx_LaneN with N=1 for SFF-8472 (Bytes (183-186)+(N-1)*8)

The delay is indicated in unsigned q16.16 format (see 13.2.1) in ns units. It represents the average delay characterized for the module in the Transmitter direction of lane N. It is the known delay added by the device, and can be compensated for by the host, e.g., for the purpose of synchronization using IEEE Std 1588.
The register of unused or non-existing lanes is filled with 00h Bytes.

13.5 Calibration format for Loopback Modules (Bytes 150-254)

Table 13-2 shows the summary of the register definitions when the Format ID (see 13) is equal to 100Bh (i.e., the “Calibration format for Loopback Modules” is used). The details of the registers are described in this section.

The Calibration Loopback module connects the TX and RX ports on the electrical SFP connector and probes this electrical loopback connection while forwarding the probed signals with fixed and calibrated delay to the monitor connector (MON, see Figure 13-1). This allows for calibrated access of the electric time reference plane of SFP/SFP+ sockets of network devices. The calibrated delays between TX, RX and MON are provided in the bytes defined below.

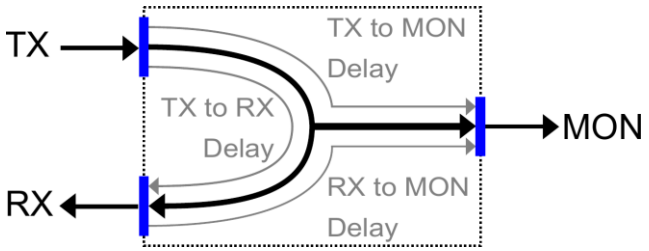

Figure 13-1 Calibration Loopback Module

13.5.1 Calibration Inaccuracy (Bytes 150-153)

The value represents the calibration inaccuracy of the reported delays. It is a 4 byte value in unsigned q16.16 format (see section 13.2.1) in ns units.

NOTE: The reported values shall take account of the inaccuracy of the calibration process and calibration generation chain that is indicated by the stratum value, see 13.3.4.

13.5.2 TX to RX Delay (Bytes 155-158)

Tx-to-Rx Delay is the fixed delay from TX to RX port in ns using q16.16 format (see section 13.2.1).

13.5.3 TX to MON Delay (Bytes 160-163)

Tx-to-Mon Delay is the fixed delay from TX to the MON output connector in ns using q16.16 format (see section 13.2.1).

13.5.4 RX to MON Delay (Bytes 165-168)

Rx-to-Mon Delay is the fixed delay from RX to the MON output connector in ns using q16.16 format (see section 13.2.1).

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