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SFF-TA-1001

Specification for

Universal x4 Link Definition for SFF-8639

Rev 1.1 May 28, 2018

Secretariat: SFF TA TWG

Abstract: This specification defines the Universal x4 Link Definition for SFF-8639.

This specification provides a common reference for systems manufacturers, system integrators, and suppliers.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

The description of a connector in this specification does not assure that the specific component is actually available from connector suppliers. If such a connector is supplied it shall comply with this specification to achieve interoperability between suppliers.

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The user's attention is called to the possibility that implementation to this Specification may require use of an invention covered by patent rights. By distribution of this specification, no position is taken with respect to the validity of a claim or claims or of any patent rights in connection therewith. Members of the SFF Committee which advise that a patent exists are required to provide a statement of willingness to grant a license under these rights on reasonable and non-discriminatory terms and conditions to applicants desiring to obtain such a license.

Change History

Rev 1.0 November 3, 2017
-Public standard

Rev 1.1 May 28, 2018

-All	Changed lane X term to LaneX Added off-page section links and hyperlinks
-Footer	Moved Page # up to same row as the title
-Section 2.2	Updated to latest boilerplate
-Section 2.3	Dropped drawing paragraph
-Figure 3-1	Changed typo of SFF-8630 label to SFF-8639
-Table 4-4 & -Section 4.2.4	Added Manufacturing Mode tolerance.
-Section 4.3.2	Fixed table reference from 4-6 to 4-7
-Section 4.5	Changed all 2.2uF capacitors in the table listings to 20%

Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors. The SFF Committee provided a forum for system integrators and vendors to define the form factor of disk drives.

During their definition, other activities were suggested because participants in SFF faced more challenges than the form factors. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

In July 2016, the SFF Committee transitioned to SNIA (Storage Networking Industry Association), as a TA (Technology Affiliate) TWG (Technical Work Group).

The Members' support of a specification is identified on the second page of each specification. Industry consensus is not a requirement to publish a specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF meets during the T10 (see www.t10.org) and T11 (see www.t11.org) weeks, and SSWGs (Specific Subject Working Groups) are held at the convenience of the participants. Material presented to SFF becomes public domain, and there are no restrictions on the open mailing of the presented material by Members.

Many of the specifications developed by SFF have either been incorporated into standards or adopted as standards by ANSI, EIA, JEDEC and SAE.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at:
http://www.snia.org/sff/join

The complete list of specifications which have been completed or are currently being worked on by SFF can be found at:
http://www.snia.org/sff/specifications

Suggestions for improvement of this specification will be welcome, they should be submitted to: http://www.snia.org/feedback

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1 Scope

This specification defines a Universal x4 Link Definition for an SFF-8639 drive and backplane connection.

This specification does not mandate nor imply any SFF-TA-1001 slot compatibility with Quad PCIe devices.
This specification does mandate that SFF-TA-1001 devices are compatible with both Quad PCIe slots and SFF-TA-1001 slots.

Table 1-1 elaborates on the Quad PCIe/SFF-TA-1001 relationship.

TABLE 1-1 DEVICE/BAY INTEROPERATION

Device Type	SFF-TA-1001 x4 Slot	SFF-TA-1001 x2 Slot	SFF-TA-1001 x1 Slot	Quad PCIe x4 Slot	Quad PCIe x2 Slot	Quad PCIe x1 Slot
SFF-TA-1001 x4 Device	Full x4	Full x2	Full x1	Full x4	Full x2	Full x1
SFF-TA-1001 x2 Device	Full x2	Full x2	Full x1	Full x2	Full x2	Full x1
SFF-TA-1001 x1 Device	Full x1	Full x1	Full x1	Full x1	Full x1	Full x1
Quad PCIe x4 Device	No link*	No link*	No link*	Full x4	Full x2	Full x1
Quad PCIe x2 Device	No link*	No link*	No link*	Full x2	Full x2	Full x1
Quad PCIe x1 Device	No link*	No link*	No link*	Full x1	Full x1	Full x1

*No link instances can be detected by out of band signal (IFDET2) usage.

Note: x2 and x1 fields also applies to dual port drives.

1.1 Application Specific Criteria

SFF-8639 extended SFF-8680 to provide an independent path for a PCIe x4 wide port to be available with an independent backplane connection (wiring and cable receptacle) to accommodate separate host controller connections (separate SAS/SATA and PCIe host connections).

New storage controllers may offer both SAS/SATA and PCIe from the same host, which allows for a given drive slot on the backplane to be wired to a single cable receptacle. This provides for one host connection to a drive slot that will accept a SAS, SATA, or PCIe device leaving a tri-mode host to determine the proper communication protocol.

To enable full compatibility with the current industry established backplanes, SFF-TA-1001 compliant devices shall accommodate backplanes designed for *PCI-SIG PCI Express SFF-8639 Module Specification* (Quad PCIe) devices with slot detection and lane switching circuitry that will allow operation in either a Quad PCIe or SFF-TA-1001 backplane slot at full bandwidth.
Further, this specification creates compatibility with the high speed phys/lanes defined by the SFF-8630 SAS wiring for full x4 and dual port x2 SAS lane usage.

This specification defines the pin usage & slot detection method, and addresses host & backplane wiring issues that occur when designing for a backplane receptacle that accepts both PCIe and SAS/SATA data storage devices.

1.2 Copyright

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Suggestions for revisions should be directed to http://www.snia.org/feedback/

2 References

2.1 Industry Documents

Gen-Z Scalable Connector Specification
Gen-Z SFF 8639 2.5-Inch Compact Specification
INCITS 534/T10 Serial Attached SCSI - 4 (SAS-4)
PCI-SIG PCI Express SFF-8639 Module Specification
Serial ATA International Organization Serial ATA Specification

SFF Committee specifications are available from www.snia.org/sff/specifications
- SFF-8630 Serial Attachment 4X 12 Gb/s Unshielded Connector
- SFF-8639 Multifunction 6X Unshielded Connector
- SFF-8680 Serial Attachment 2X 12 Gb/s Unshielded Connector
- SFF-9402 Multi-Protocol Internal Cables for SAS and/or PCIe
- SFF-9639 Multifunction 6X Unshielded Connector Pinouts

2.2 Sources

There are several projects active within the SFF TWG. The complete list of specifications which have been completed or are still being worked on is contained in the document SFF-8000 which can be found at
http://www.snia.org/sff/specifications

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://www.techstreet.com/incitsgate.tmpl).

Copies of PCI-SIG standards may be downloaded from the PCI-SIG website (http://pcisig.com/specifications).

Copies of Gen-Z specifications can be downloaded from the Gen-Z Consortium's website at https://genzconsortium.org.

2.3 Conventions

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

2.4 Definitions

For the purpose of SFF Specifications, the following definitions apply:

Optional: This term describes features which are not required by the SFF Specification. However, if any feature defined by the SFF Specification is implemented, it shall be done in the same way as defined by the Specification. Describing a feature as optional in the text is done to assist the reader. If there is a conflict between text and tables on a feature described as optional, the table shall be accepted as being correct.

Reserved: Where this term is used for defining the signal on a connector contact its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields and code values; the bits, bytes, fields and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

For the purpose of this specification, the following definitions apply:

Device: A hard drive, solid state drive, or any other data target that plugs into the backplane receptacle.

PCIe: PCI Express

Quad PCIe: Complies with the PCI-SIG *PCI Express SFF-8639 Module Specification*.

Quad PCIe slot: A device slot offering separate (dual) communication paths (2 lanes SAS/SATA, 4 lanes PCIe) to an SFF-8639 connector based slot. The separate communication paths to the slot consists of separate cables, backplane connectors & wiring paths, and pins to the device. Complies with the PCI-SIG *PCI Express SFF-8639 Module Specification*.

Tri-mode phy: A single phy on a storage controller host that may provide connectivity for SAS, SATA, and PCIe devices.

SFF-TA-1001 slot: A device slot offering a single communication path (4 lanes maximum) to an SFF-8639 connector based slot. This single communication path would allow for three storage protocols (SATA, SAS, and PCIe) transmissions based on the type of device installed in the slot. Complies with this specification.

3 General Description

The SFF-TA-1001 system defines pinout and usage for a multi-protocol accepting device connector based on the SFF-8639 connector technology and the SAS defined SFF-8630 wide port pin definition. This technology provides a universal x4 link definition for a drive bay, allowing for a selection of electrically compatible disk drives or SSDs to occupy a given backplane slot where the host is responsible for detection of a compatible protocol for communication. The link width defined may be up to 4 lanes wide and may be to a single host or divided into separate x2 wide host connections.

This connector is suited to drive bays where SAS, SATA, or PCIe drives may be accommodated and attached to a tri-mode host controller for proper detection. Design guidance is offered for slot detection, distinction, and operation between the PCIe standard SFF-8639 pin definition so that a single drive type may be used in both Quad PCIe slots and SFF-TA-1001 slots.

Figure 3-1 represents a typical mating configuration of this connector.

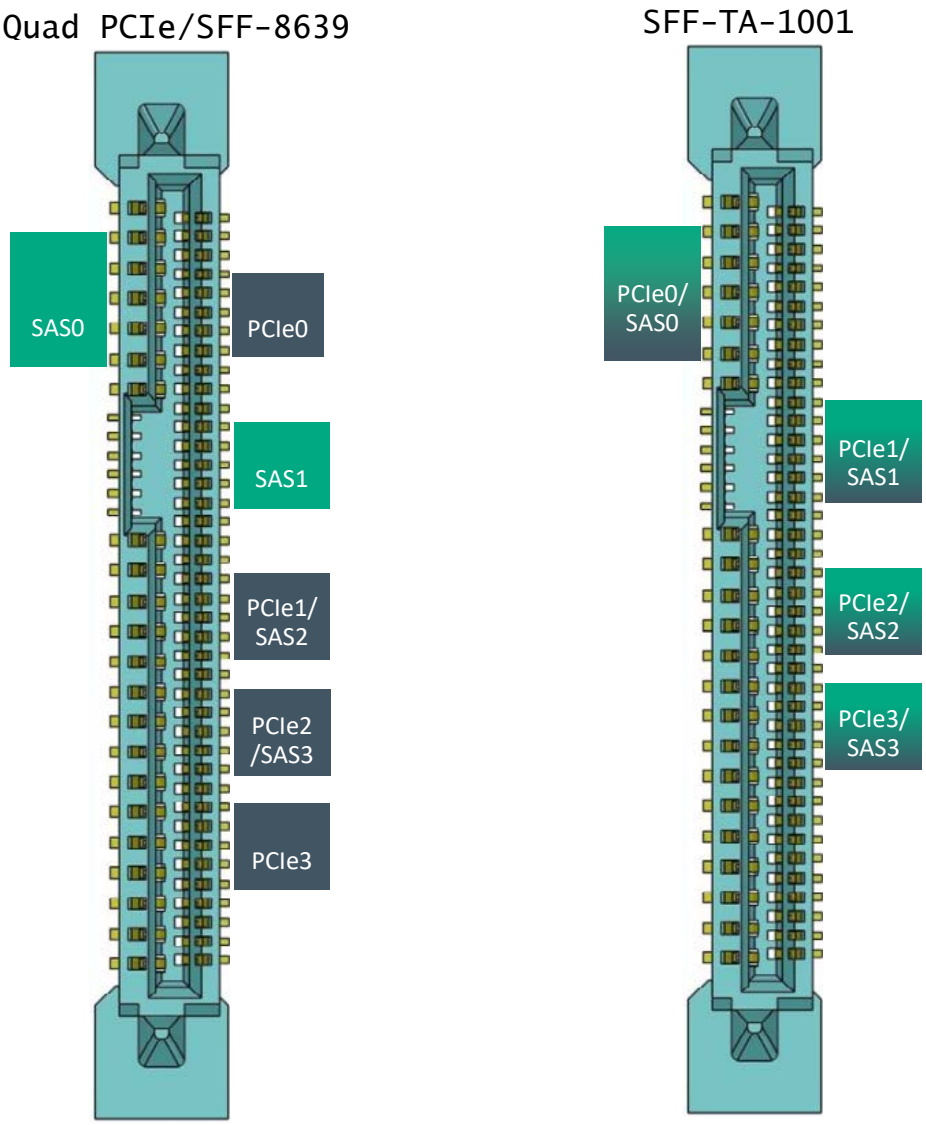

FIGURE 3-1 PORT USAGE OVERVIEW

4 Implementation

This section defines the specific pin functions that enable the SFF-TA-1001 characteristics of a device.

4.1 Pinout

Tables 4-1 through 4.3 specify the pinout for the SFF-TA-1001 connector for both PCIe and SAS devices. Signal descriptions specific to either protocol are found in their respective controlling documents (*INCITS 534/T10 Serial Attached SCSI – 4 (SAS-4)*, *PCI-SIG PCI Express SFF-8639 Module Specification*).

TABLE 4-1 P SERIES SIGNALS

	HOST RECEPTICAL	SFF-TA-1001 DEVICE PLUG
P1	WAKE#	WAKE#
P2		Reserved
P3	PWRDIS	PWRDIS
P4	IfDet#	IfDet#
P5	Ground	Ground
P6	Ground	Ground
P7	+5V	
P8	+5V	
P9	+5V	
P10	PRSNT#	PRSNT#
P11	ACTIVITY LED	ACTIVITY#
P12	Ground	Ground
P13	+12V	+12 V Precharge
P14	+12V	+12 V
P15	+12V	+12 V

TABLE 4-2 S SERIES SIGNALS

	HOST RECEPTICAL	SFF-TA-1001 DEVICE PLUG
S1	Ground	Ground
S2	TX p0	PETp0
S3	TX n0	PETn0
S4	Ground	Ground
S5	RX n0	PERn0
S6	RX p0	PERp0
S7	Ground	Ground
S8	Ground	Ground
S9	TX p1	PETp1
S10	TX n1	PETn1
S11	Ground	Ground
S12	RX n1	PERn1
S13	RX p1	PERp1
S14	Ground	Ground
S15	Ground	HPT0
S16	Ground	Ground
S17	TX p2	PETp2
S18	TX n2	PETn2
S19	Ground	Ground
S20	RX n2	PERn2
S21	RX p2	PERp2
S22	Ground	Ground
S23	TX p3	PETp3
S24	TX n3	PETn3
S25	Ground	Ground
S26	RX n3	PERn3
S27	RX p3	PERp3
S28	Ground	Ground

TABLE 4-3 E SERIES SIGNALS

	Host	PCIe
E1	REFCLKB+	REFCLKB+
E2	REFCLKB-	REFCLKB-
E3	+3.3V Aux	+3.3 Vaux
E4	PERSTB#	PERSTB#
E5	PERST#	PERST#
E6	IfDet2#	Ground
E7	REFCLK+	REFCLK+
E8	REFCLK-	REFCLK-
E9	Ground	Ground
E10		
E11		
E12	Ground	Ground
E13		
E14		
E15	Ground	Ground
E16	HPT1	HPT1
E17		
E18		
E19	Ground	Ground
E20		
E21		
E22	Ground	Ground
E23	SMBCLK	SMBCLK
E24	SMBDAT	SMBDAT
E25	DualPortEn#	DualPortEn#

*1 The PETpx and PETnx pins shall be connected to the PCI Express Receiver differential pair on the PCIe device.
*2 The PERpx and PERnx pins shall be connected to the PCI Express Transmitter differential pair on the PCIe device.

Note: Names the signals on the device from the host perspective i.e. a receiver on the device has a transmitter signal name.

Note: New pins introduced in this specification (HPT0, HPT1, IfDet2# & DualPortEn#) are described in Section 4.2 & 4.3.

Note: See SFF-9639: Multifunction 6X Unshielded Connector Pinouts for a comparison of pin assignments with other specifications, including the PCI-SIG PCI Express SFF-8639 Module Specification defined pinout.

4.2 Host Port Type Operation

Table 4.4 describes the various functions of the three Host Port Type configuration pins. These signals are set by the slot connector and read by the device.

TABLE 4-4 HOST PORT TYPE CONTROL SIGNAL MAP

HPT0	HPT1	DualPortEn#	
S15	E16	E25	Device Operational Mode
Open	Open	Open	Host Port Quad PCIe Single x4
Open	Open	Gnd	Host Port Quad PCIe Dual x2
Gnd	Open	Open	Host Port SFF-TA-1001 Single x4
Gnd	Open	Gnd	Host Port SFF-TA-1001 Dual x2
Open	Gnd	Open	Gen-Z Single x4
Open	Gnd	Gnd	Gen-Z Dual x2
Gnd	Gnd	Open	Undefined Single x4
Gnd	Gnd	Gnd	Manufacturing Mode

4.2.1 Host Port Type 0 Pin Operation

The Host Port Type 0 (HPT0) pin shall be an open drain output from the slot to the device to determine which type of slot the device is mated to. An SFF-TA-1001 compliant slot shall assert this pin low. A Quad PCIe slot defines this pin as Reserved (not connected).

The device shall have the necessary input pull-up resistor (meeting signal parameters described in section 4.4) to ensure the proper value is read for Quad PCIe and shall read this pin at power-on to determine PCIe lane configuration.

TABLE 4-5 HOST PORT TYPE PINS

Host Port Type 0 (S15)	Definition
Open	Host Port Quad PCIe
Gnd	Host Port SFF-TA-1001

4.2.2 Host Port Type 1 Pin Operation

The Host Port Type 1 (HPT1) pin shall be an open drain output from the host to the device to determine which type of host protocol the device is mated to. An SFF-TA-1001 compliant host (or slot) shall either assert this pin low or allow for the signal to float high.

The device shall have the necessary input pull-up resistor (meeting signal parameters described in section 4.4) to ensure the proper value is read for Quad PCIe and shall read this pin at power-on to determine PCIe lane configuration.

TABLE 4-6 HOST PORT TYPE PINS

Host Port Type 1 (E16)	Definition
Open	PCIe host interface
Gnd	See table 4-4

4.2.3 Dual Port Enable Pin

See Quad PCIe specification (PCI-SIG *PCI Express SFF-8639 Module Specification*) for usage.

4.2.4 Manufacturing Mode

Manufacturing mode may be enabled by the device when the HPT0, HPT1, and DualPortEn# signals are set as specified in Table 4-4. Manufacturing mode is vendor specific and shall only be used during device manufacturing. Device suppliers shall disable this mode after manufacturing.

4.3 Device Side Operation

4.3.1 Dual Port Capability

Due to the precedence of SAS devices using SAS phy1 for Domain B, dual port PCIe SFF-TA-1001 devices need to swap PCIe Lane1 and Lane2 to allow for contiguous lanes to be associated within the same host port domain. In this configuration PCIe Lane2 and Lane3 become Domain B Lane0 and Lane1. This lane switch only applies to devices that enable a dual port configuration.

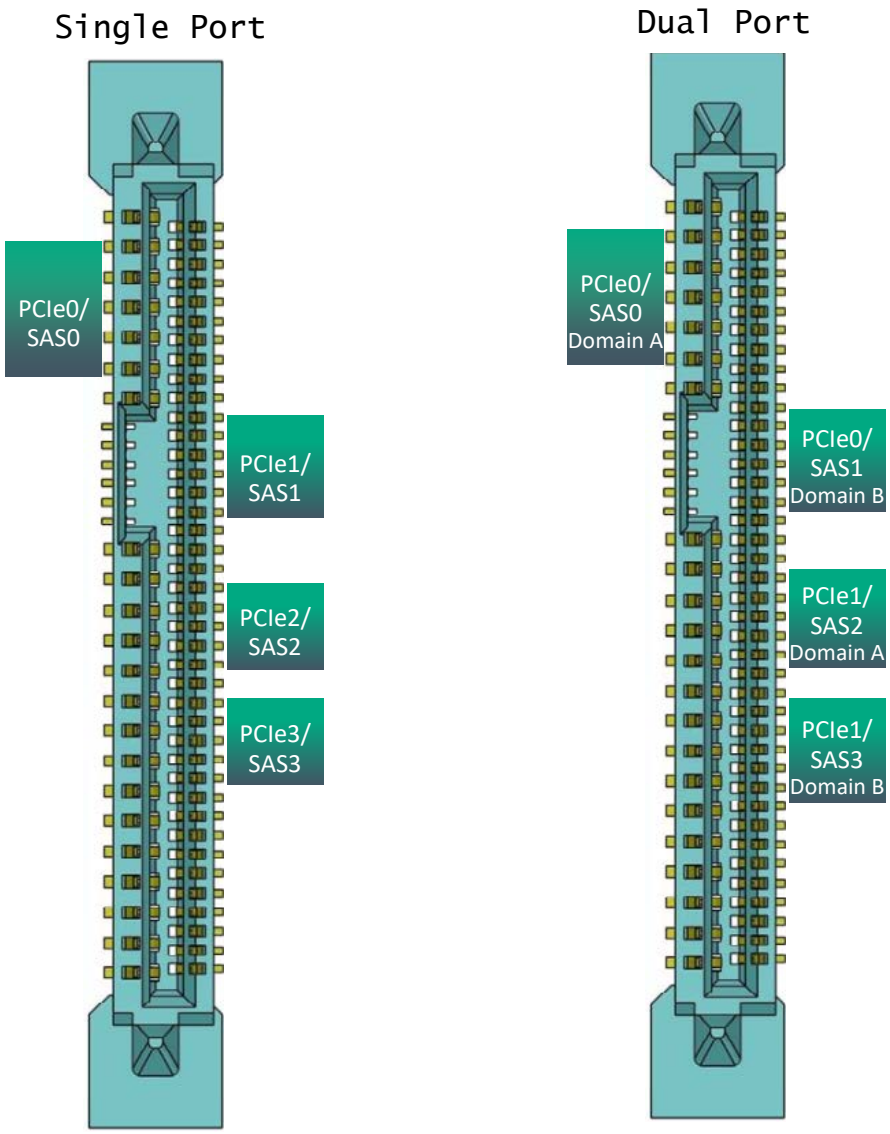

FIGURE 4-1 DUAL PORT LANE CONFIGURATION

4.3.2 Device Side Phy Routing to Connector Pins

Table 4-7 lists the device lane assignments for the three variations. A SFF-TA-1001 compliant device shall support full compatibility (i.e. support the same number of lanes in SFF-TA-1001 or Quad PCIe mode) with *PCI-SIG PCI Express SFF-8639 Module Specification* (Quad PCIe) slots by sensing the S15 (HPT0) pin. The device input for HPT0 shall default to high such that when mated to the Quad PCIe Reserved pin will default to Quad PCIe lane assignments as defined in the Quad PCIe column in the table.

TABLE 4-7 HOST SET PINS

PCIe Lane		SFF-TA-1001 Single Port S15=0, E25=1	SFF-TA-1001 Dual Port S15=0, E25=0	Quad PCIe S15=1
PortA Lane0		S[2-6]	S[2-6]	E[10-14]
PortA Lane1		S[9-13]	S[17-21]	S[17-21]
PortA Lane2	PortB Lane0	S[17-21]	S[9-13]	S[23-27]
PortA Lane3	PortB Lane1	S[23-27]	S[23-27]	E[17-21]

Note: Single port x2 usage shall use Lane0 & Lane1. Single port x1 usage shall use Lane0.

4.3.3 Device Type Encoding

The IfDet2# pin on the device side shall be asserted low by the SFF-TA-1001 device. This signal may be used as an open drain input to the host (via the slot) to determine the type of device connected in the slot. This pin is marked Reserved by the SAS, SATA, & PCIe SFF-8639 standards, therefore the slot shall implement a weak pull-up so that the host's input will default to the proper level when devices other than SFF-TA-1001 are installed.

TABLE 4-8 DEVICE TYPE ENCODING

PRSNT#	IfDet#	IfDet2#	
P10	P4	E6	Device Type Installed
Gnd	Gnd	Open	SAS / SATA
Gnd	Open	Open	Undefined
Open	Gnd	Open	Quad PCIe
Open	Open	Open	Bay Empty
Gnd	Gnd	Gnd	Undefined
Gnd	Open	Gnd	Undefined
Open	Gnd	Gnd	SFF-TA-1001 PCIe
Open	Open	Gnd	Gen-Z

4.4 Additional Signal Parametric Specifications

The DC specifications for HPT0, HPT1, and IfDet2# are given in the following table.

TABLE 4-9 ADDITIONAL SIGNAL DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage		-0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V	1
V_{OL}	Output Low Voltage	4.0mA		0.2	V	2
V_{OH}	Max High Voltage			V_{CC} + 0.5	V	1
I_L	Output High Leakage Current	0V to V_{CC}	-50	+50	µA	3

Notes:
*1 V_{CC} represents the nominal +3.3V supply voltage of the driver circuitry for an output and the nominal +3.3V supply voltage of the receiver for an input.

*2 Open-drain output.

*3 Leakage at the pin when the output is not active (high impedance).

4.5 AC Coupling Capacitor Usage

Due to AC coupling capacitor incompatibilities between the various SFF-8639 mechanically compatible systems and devices, the following AC coupling capacitor values, tolerances and locations shall be used. In order to minimize DC wander, in-line AC coupling capacitors shall not be added for those locations identified as "not required". Table 4-10 specifies the coupling capacitors that shall be on the host, table 4-11 specifies the coupling capacitors that shall be on the device when in SFF-TA-1001 mode, and table 4-12 specifies the coupling capacitors that shall be on the device when in Quad PCIe mode.

TABLE 4-10 HOST AC COUPLING CAPACITOR LOCATIONS AND VALUES

Signal Name	Pin	Nominal	Tolerance	Notes
L0 (Xmtr+)	S2	220 nF	10%	
L0 (Xmtr-)	S3	220 nF	10%	
L0 (Rcvr-)	S5	220 nF	10%	
L0 (Rcvr+)	S6	220 nF	10%	
L1 (Xmtr+)	S9	220 nF	10%	
L1 (Xmtr-)	S10	220 nF	10%	
L1 (Rcvr-)	S12	220 nF	10%	
L1 (Rcvr+)	S13	220 nF	10%	
L2 (Xmtr+)	S17	220 nF	10%	
L2 (Xmtr-)	S18	220 nF	10%	
L2 (Rcvr-)	S20	220 nF	10%	
L2 (Rcvr+)	S21	220 nF	10%	
L3 (Xmtr+)	S23	220 nF	10%	
L3 (Xmtr-)	S24	220 nF	10%	
L3 (Rcvr-)	S26	220 nF	10%	
L3 (Rcvr+)	S27	220 nF	10%	

TABLE 4-11 DEVICE (SFF-TA-1001 MODE) AC COUPLING CAPACITOR LOCATIONS AND VALUES

Signal Name	Pin	Nominal	Tolerance	Notes
L0 (Rcvr+)	S2	2.2 uF	20%	Needed for circuit protection
L0 (Rcvr-)	S3	2.2 uF	20%	Needed for circuit protection
L0 (Xmtr-)	S5	-	10%	Not required
L0 (Xmtr+)	S6	-	10%	Not required
L1 (Rcvr+)	S9	2.2 uF	20%	Needed for circuit protection
L1 (Rcvr-)	S10	2.2 uF	20%	Needed for circuit protection
L1 (Xmtr-)	S12	-	10%	Not required
L1 (Xmtr+)	S13	-	10%	Not required
L2 (Rcvr+)	S17	2.2 uF	20%	Needed for circuit protection
L2 (Rcvr-)	S18	2.2 uF	20%	Needed for circuit protection
L2 (Xmtr-)	S20	220 nF	10%	
L2 (Xmtr+)	S21	220 nF	10%	
L3 (Rcvr+)	S23	2.2 uF	20%	Needed for circuit protection
L3 (Rcvr-)	S24	2.2 uF	20%	Needed for circuit protection
L3 (Xmtr-)	S26	220 nF	10%	
L3 (Xmtr+)	S27	220 nF	10%	

TABLE 4-12 DEVICE (QUAD PCIE MODE) AC COUPLING CAPACITOR LOCATIONS AND VALUES

Signal Name	Pin	Nominal	Tolerance	Notes
L0 (Rcvr+)	E10	-	-	Not required
L0 (Rcvr-)	E11	-	-	Not required
L0 (Xmtr-)	E13	220 nF	10%	
L0 (Xmtr+)	E14	220 nF	10%	
L1 (Rcvr+)	S17	2.2 uF	20%	Needed for circuit protection
L1 (Rcvr-)	S18	2.2 uF	20%	Needed for circuit protection
L1 (Xmtr-)	S20	220 nF	10%	
L1 (Xmtr+)	S21	220 nF	10%	
L2 (Rcvr+)	S23	2.2 uF	20%	Needed for circuit protection
L2 (Rcvr-)	S24	2.2 uF	20%	Needed for circuit protection
L2 (Xmtr-)	S26	220 nF	10%	
L2 (Xmtr+)	S27	220 nF	10%	
L3 (Rcvr+)	E17	-	-	Not required
L3 (Rcvr-)	E18	-	-	Not required
L3 (Xmtr-)	E20	220 nF	10%	
L3 (Xmtr+)	E21	220 nF	10%	

A. Appendix (Informative): Tri-mode Applications

Defining a physical link that covers different communication protocols creates certain system design implications that are not considered in a governing protocol specification and therefore needs to be accounted for by the system designer. For example, defining a physical link between a host and device where either may be SAS/SATA or PCIe (tri-mode) calls into question the selection of characteristics of the transmission medium (host connector selection, cable impedance, cable-to-backplane connector, backplane impedance, and additional AC coupling capacitance). This specification mandates the additional AC coupling capacitance exists in the physical link. The SFF-8639 connector specification mandates the impedance of the device connector. The various protocol specifications and the SFF-9402 interoperability tables guide the selection of connectors on the cabled end of the backplane. All other aspects of the system design are for the discretion of the system designer to rectify.

B. Appendix (Informative): SAS Backplane Construction

This standard does not mandate that a PCIe connection be the full x4 lane width. A standard SAS backplane construction may take advantage of the HPT0 (S15) signal pin to indicate the device slot is SFF-TA-1001. When an SFF-TA-1001 PCIe device is installed in such a backplane, the device responds to the SFF-TA-1001 slot indication and communicates on the SAS0/SAS1 lanes. If the host is capable of PCIe as well as the designed SAS interface, a PCIe link is established. Such a system needs to accommodate either of two additional design necessities:

1. The PCIe device needs to be an SRIS capable drive without the need for the PERST# pin to be activated. This is due to the non-SAS signals not being routed to the device slot.
2. The backplane includes the additional REFCLK and PERST# signal routing from the cable to the device slot. These signals are ignored for any SAS/SATA device installation in the slot.