This document was developed by the SFF Committee prior to it becoming the SFF TA (Technology Affiliate) TWG (Technical Working Group) of the SNIA (Storage Networking Industry Association) in 2016.

The information below should be used instead of the equivalent herein.

SFF Committee

SFF-8045 Specification for

40-pin SCA-2 Connector w/Parallel Selection

Rev 4.7   January 12 2005

Secretariat: SFF Committee

Abstract: This document defines a 40-pin SCA (Single Connector Attach) connector
for use in applications for Fibre Channel disk drives racked in a cabinet.

This document provides a common specification for systems manufacturers, system
integrators, and suppliers of drives. This is an internal working document of the
SFF Committee, an industry ad hoc group.

This document is made available for public review, and written comments are
solicited from readers. Comments received by the members will be considered for
inclusion in future revisions of this document.

Support: This document is supported by the identified member companies of the SFF
Committee.

Documentation: This document has been prepared in a similar style to that of the ISO
(International Organization of Standards).

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EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of
this industry specification.

                AMP
                Circuit Assembly
                Compaq
                DDK Electronics
                DDK Fujikura
                EMC
                ENDL
                FCI/Berg
                Foxconn Int'l
                Fujitsu CPA
                Hitachi Cable
                Honda Connector
                I/O Interconnect
                IBM
                Intel
                Madison Cable
                Molex
                Ricoh
                Seagate
                Sun Microsystems
                TI Japan
                Tyco AMP
                Unisys
                Volex

The following member companies of the SFF Committee voted to abstain on
this industry specification.

                Adaptec
                Amphenol
                Matsushita
                Maxtor
                Montrose/CDT
                Pioneer NewMedia
                Quantum
                Toshiba America
                Tyco AMP
                Yamagata Fujitsu
                YC Cable

If you are not a member of the SFF Committee, but you are interested in participating, the following principles have been reprinted here for your information.

PRINCIPLES OF THE SFF COMMITTEE

The SFF Committee is an ad hoc group formed to address storage industry needs in a prompt manner. When formed in 1990, the original goals were limited to defining de facto mechanical envelopes within which disk drives can be developed to fit compact computer and other small products.

Adopting a common industry size simplifies the integration of small drives (2 1/2" or less) into such systems. Board-board connectors carrying power and signals, and their position relative to the envelope are critical parameters in a product that has no cables to provide packaging leeway for the integrator.

In November 1992, the SFF Committee objectives were broadened to encompass other areas which needed similar attention, such as pinouts for interface applications, and form factor issues on larger disk drives. SFF is a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Specifications created by the SFF Committee are expected to be submitted to bodies such as EIA (Electronic Industries Association) or an ASC (Accredited Standards Committee). They may be accepted for separate standards, or incorporated into other standards activities.

The principles of operation for the SFF Committee are not unlike those of an accredited standards committee. There are 3 levels of participation:

 - Attending the meetings is open to all, but taking part in discussions is
   limited to member companies, or those invited by member companies
 - The minutes and copies of material which are discussed during meetings
   are distributed only to those who sign up to receive documentation.
 - The individuals who represent member companies of the SFF Committee
   receive documentation and vote on issues that arise. Votes are not taken
   during meetings, only guidance on directions. All voting is by letter
   ballot, which ensures all members an equal opportunity to be heard.

Material presented at SFF Committee meetings becomes public domain. There are no restrictions on the open mailing of material presented at committee meetings. In order to reduce disagreements and misunderstandings, copies must be provided for all agenda items that are discussed. Copies of the material presented, or revisions if completed in time, are included in the documentation mailings.

The sites for SFF Committee meetings rotate based on which member companies volunteer to host the meetings. Meetings have typically been held during the ASC T10 weeks.

The funds received from the annual membership fees are placed in escrow, and are used to reimburse ENDL for the services to manage the SFF Committee.

If you are not receiving the documentation of SFF Committee activities or are interested in becoming a member, the following signup information is reprinted here for your information.

Membership includes voting privileges on SFF Specs under development.

    CD_Access Electronic documentation contains:
      - Minutes for the year-to-date plus all of last year
      - Email traffic for the year-to-date plus all of last year
      - The current revision of all the SFF Specifications, as well as any
        previous revisions distributed during the current year.

    Meeting documentation contains:
      - Minutes for the current meeting cycle.
      - Copies of Specifications revised during the current meeting cycle.

Each electronic mailing obsoletes the previous mailing of that year e.g. July replaces May. To build a complete set of archives of all SFF documentation, retain the last SFF CD_Access mailing of each year.

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        SFF Committee   408-867-6630
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        Saratoga CA 95070   endlcom@acm.org

Foreword

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers in which space was at a premium and time to market with the latest machine was an important factor. System integrators worked individually with vendors to develop the packaging. The result was wide diversity, and with space being such a major consideration in packaging, it was not possible to replace one vendor's drive with a competitive product.

The desire to reduce disk drive sizes to even smaller dimensions such as 1.8" and 1.3" made it likely that devices would become even more constrained in dimensions because of a possibility that such small devices could be inserted into a socket, not unlike the method of retaining semiconductor devices.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology in disk drives. After two informal gatherings on the subject in the summer of 1990, the SFF Committee held its first meeting in August.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced problems other than the physical form factors of disk drives. In November 1992, the members approved an expansion in charter to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

At the same time, the principle was adopted of restricting the scope of an SFF project to a narrow area, so that the majority of specifications would be small and the projects could be completed in a rapid timeframe. If proposals are made by a number of contributors, the participating members select the best concepts and uses them to develop specifications which address specific issues in emerging storage markets.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in 1990 has included a mix of companies which are leaders across the industry.

SFF Committee --

40-pin SCA-2 Connector w/Parallel Selection

1. Scope

In an effort to broaden the applications for small form factor disk drives, an ad hoc industry group of companies representing system integrators, peripheral suppliers, and component suppliers decided to address the issues involved.

The purpose of this SFF Specification is to define a single connector suitable for the direct attachment of Fibre Channel drives to backplanes and motherboards.

The FC-SCA has been designed for serial transfer Fibre Channel devices, and carries all signals as required by the Fibre Channel Physical Interface and the FIbre Channel Arbitrated Loop standards. In addition, all required power and auxiliary signals are carried by the same single connector. The SCA mechanical definition allows the device to be plugged into a board socket. The dimensions are provided for both 1" and 1.6" high 3 1/2" disk devices. The same connector structure is appropriate for 2 1/2" devices as well.

The SFF Committee was formed in August, 1990 and the first working document was introduced in January, 1991.

1.1 Description of Clauses

Clause 1 contains the Scope and Purpose.

Clause 2 contains Referenced and Related Standards and SFF Specifications.

Clause 3 contains the General Description.

Clause 4 contains the Glossary.

Clause 5 contains the physical positioning requirements.

Clause 6 contains the signal assignments.

Clause 7 defines the connector requirements.

Clause 8 specifies the connector.

2. References

The SFF Committee activities support the requirements of the storage industry, and it is involved with several standards.

2.1 Industry Documents

The following interface standards are relevant to this Specification.

```
 - Project T11/1619-D      FC-FS-2  Fibre Channel - Framing and Signaling
 - Project T11/1506-D      FC-PI-2  Fibre Channel - PHYSICAL INTERFACES
 - ANSI  INCITS 332-1999   FC-AL-2  Arbitrated Loop 2
 - ANSI  INCITS 332-1999/AM1-2003    FC-AL-2  Arbitrated Loop 2 Amendment
 - ANSI  INCITS 350-2003   FCP-2    Fibre Channel Protocol 2
```

2.2 SFF Specifications

There are several projects active within the SFF Committee. At the date of printing document numbers had been assigned to the following projects. The status of Specifications is dependent on committee activities.

```
F = Forwarded    The document has been approved by the members for
                 forwarding to a formal standards body.
P = Published    The document has been balloted by members and is
                 available as a published SFF Specification.
A = Approved     The document has been approved by ballot of the members
                 and is in preparation as an SFF Specification.
C = Canceled     The project was canceled, and no Specification was
                 Published.
D = Development  The document is under development at SFF.
E = Expired      The document has been published as an SFF
                 Specification, and the members voted against re-
                 publishing it when it came up for review.
a = archive      Used as a suffix to indicate an SFF Specification which
                 has been Archived. This specification will always be
                 available at the ftp site and new development effort
                 in the subject area shall be done under a new number.
e = electronic   Used as a suffix to indicate an SFF Specification which
                 has Expired but is still available in electronic form
                 from SFF e.g. a specification has been incorporated
                 into a draft or published standard which is only
                 available in hard copy.
i = Information  The document has no SFF project activity in progress,
                 but it defines features in developing industry
                 standards. The document was provided by a company,
                 editor of an accredited standard in development, or an
                 individual. It is provided for broad review (comments
                 to the author are encouraged). As the copyright on such
                 documents is retained by the author, the INF or 'i'
                 specifications cannot be freely copied for distribution.
s = submitted    The document is a proposal to the members for
                 consideration to become an SFF Specification.
```

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 Spec #    Rev  List of Specifications as of January 14, 2005
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 SFF-8000       SFF Committee Information
 INF-8001i  E   44-pin ATA (AT Attachment) Pinouts for SFF Drives
 INF-8002i  E   68-pin ATA (AT Attachment) for SFF Drives
 SFF-8003   E   SCSI Pinouts for SFF Drives
 SFF-8004   E   Small Form Factor 2.5" Drives
 SFF-8005   E   Small Form Factor 1.8" Drives
 SFF-8006   E   Small Form Factor 1.3" Drives
 SFF-8007   E   2mm Connector Alternatives
 SFF-8008   E   68-pin Embedded Interface for SFF Drives
 SFF-8009  4.1  Unitized Connector for Cabled Drives

 SFF-8010   E   Small Form Factor 15mm 1.8" Drives
 INF-8011i  E   ATA Timing Extensions for Local Bus
 SFF-8012  3.0  4-Pin Power Connector Dimensions
 SFF-8013   E   ATA Download Microcode Command
 SFF-8014   C   Unitized Connector for Rack Mounted Drives
 SFF-8015   E   SCA Connector for Rack Mounted SFF SCSI Drives
 SFF-8016   C   Small Form Factor 10mm 2.5" Drives
 SFF-8017   E   SCSI Wiring Rules for Mixed Cable Plants
 SFF-8018   E   ATA Low Power Modes
 SFF-8019   E   Identify Drive Data for ATA Disks up to 8 GB

 INF-8020i  E   ATA Packet Interface for CD-ROMs
 SFF-8025  0.7  SFF Committee Specification Categories
```

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INF-8028i  E   - Errata to SFF-8020 Rev 2.5
SFF-8029   E   - Errata to SFF-8020 Rev 1.2


SFF-8030  2.0  SFF Committee Charter
SFF-8031       Named Representatives of SFF Committee Members
SFF-8032  1.6  SFF Committee Principles of Operation
INF-8033i  E   Improved ATA Timing Extensions to 16.6 MBs
INF-8034i  E   High Speed Local Bus ATA Line Termination Issues
INF-8035i  E   Self-Monitoring, Analysis & Reporting Technology
INF-8036i  E   ATA Signal Integrity Issues
INF-8037i  E   Intel Small PCI SIG
INF-8038i  E   Intel Bus Master IDE ATA Specification
INF-8039i  E   Phoenix EDD (Enhanced Disk Drive) Specification


SFF-8040  1.2  25-pin Asynchronous SCSI Pinout
SFF-8041   C   SCA-2 Connector Backend Configurations
SFF-8042   C   VHDCI Connector Backend Configurations
SFF-8043   E   40-pin MicroSCSI Pinout
SFF-8045  4.7  40-pin SCA-2 Connector w/Parallel Selection
SFF-8046   E   80-pin SCA-2 Connector for SCSI Disk Drives
SFF-8047   C   40-pin SCA-2 Connector w/Serial Selection
SFF-8048   C   80-pin SCA-2 Connector w/Parallel ESI
SFF-8049   E   80-conductor ATA Cable Assembly


INF-8050i 1.0  Bootable CD-ROM
INF-8051i  E   Small Form Factor 3" Drives
INF-8052i  E   ATA Interface for 3" Removable Devices
SFF-8053  5.5  GBIC (Gigabit Interface Converter)
SFF-8054  0.2  Automation Drive Interface Connector
INF-8055i  E   SMART Application Guide for ATA Interface
SFF-8056   C   50-pin 2mm Connector
SFF-8057   E   Unitized ATA 2-plus Connector
SFF-8058   E   Unitized ATA 3-in-1 Connector
SFF-8059   E   40-pin ATA Connector


SFF-8060  1.1  SFF Committee Patent Policy
SFF-8061   E   Emailing drawings over the SFF Reflector
SFF-8062       Rolling Calendar of SSWGs and Plenaries
SFF-8064       Unshielded HD Cable/Board Connector System
SFF-8065   C   40-pin SCA-2 Connector w/High Voltage
SFF-8066   C   80-pin SCA-2 Connector w/High Voltage
SFF-8067  3.3  40-pin SCA-2 Connector w/Bidirectional ESI
INF-8068i  E   Guidelines to Import Drawings into SFF Specs
SFF-8069   E   Fax-Access Instructions


INF-8070i 1.3  ATAPI for Rewritable Removable Media
SFF-8072  1.2  80-pin SCA-2 for Fibre Channel Tape Applications
SFF-8073   C   20-pin SCA-2 for GBIC Applications
INF-8074i 1.0  SFP (Small Formfactor Pluggable) Transceiver
SFF-8075  1.0  PCI Card Version of SFP Cage
SFF-8076   -   SFP Additional IDs
INF-8077i 3.1  XFP (10 Gbs Small Form Factor Pluggable Module)
SFF-8078   C   XFP-E
SFF-8079  1.6  SFP Rate and Application Selection
SFF-8080   E   ATAPI for CD-Recordable Media
SFF-8082  4.0  Labeling of Ports and Cable Assemblies
SFF-8084  0.2  0.8mm SFP Card Edge Connector Dimensioning
SFF-8085  0.9  100 Mbs Small Formfactor Transceivers
SFF-8086       0.8mm Card Edge Connector Dimensioning
SFF-8087       0.8mm Unshielded Connector Interface
SFF-8088       0.8mm Shielded Connector Interface
SFF-8089  1.2  SFP Rate and Application Selection Values
INF-8090i 1.6  ATAPI for Multimedia Devices (Mt Fuji5)
```

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SFF-8101   C   3 Gbs and 4 Gbs Signal Characteristics
SFF-8110   C   5V Parallel 1.8" drive form factor
SFF-8111  1.3  1.8" drive form factor (60x70mm)
SFF-8122       1.8" (60x70mm) w/SCA-2 Connector
SFF-8120  2.6  1.8" drive form factor (78x54mm)
SFF-8123  2.1  1.8" (60x70mm) w/Serial Attachment Connector
SFF-8124  0.2  Memory Form Factor Disk Drive Connections


SFF-8200e 1.1  2 1/2" drive form factors (all of 82xx family)
SFF-8201  2.3  2 1/2" drive form factor dimensions
SFF-8212e 1.2  2 1/2" drive w/SFF-8001 44-pin ATA Connector
SFF-8221  3.5  Pre-Aligned 2.5" Drive >10mm Form Factor
SFF-8222  2.1  2.5" Drive w/SCA-2 Connector
SFF-8223  2.4  2.5" Drive w/Serial Attachment Connector
SFF-8225   C   2.5" Single Voltage Drive


SFF-8300  1.2  3 1/2" drive form factors (all of 83xx family)
SFF-8301  1.4  3 1/2" drive form factor dimensions
SFF-8302e 1.1  3 1/2" Cabled Connector locations
SFF-8323  1.4  3 1/2" drive w/Serial Attachment Connector
SFF-8332e  E   3 1/2" drive w/80-pin SFF-8015 SCA Connector
SFF-8337e  E   3 1/2" drive w/SCA-2 Connector
SFF-8342e 1.3  3 1/2" drive w/Serial Unitized Connector
INF-8350i  E   3 1/2" Packaged Drives


SFF-8400   C   VHDCI (Very High Density Cable Interconnect)
SFF-8410 16.1  High Speed Serial Testing for Copper Links
INF-8411  1.0  High Speed Serial Testing for Backplanes
SFF-8412 12.2  HSOI (High Speed Optical Interconnect) Testing
SFF-8415  4.1  HPEI (High Performance Electrical Interconnect)
SFF-8416 10.0  HPEI Bulk Cable Measurement/Performance Reqmnts


SFF-8420 11.1  HSSDC-1 Shielded Connections
SFF-8421  2.4  HSSDC-2 Shielded Connections
SFF-8422   C   FCI Shielded Connections
SFF-8423   C   Molex Shielded Connections
SFF-8424  0.5  Dual Row HSSDC-2 Shielded Connections
SFF-8425  1.4  Single Voltage 12V Drives
SFF-8426       HSSDC Double Width
SFF-8429  0.0  Signal Specification Architecture for HSS Links


SFF-8430  4.1  MT-RJ Duplex Optical Connections
SFF-8431       SFP+
SFF-8441 14.1  VHDCI Shielded Configurations
SFF-8451 10.1  SCA-2 Unshielded Connections
SFF-8452  3.1  Glitch Free Mating Connections for Multidrop Aps
SFF-8453       Shielded High Speed Serial connectors


SFF-8460  1.2  HSS Backplane Design Guidelines
SFF-8464       Improved MM HSS Optical Link Performance
SFF-8470  2.9  Multi Lane Copper Connector
SFF-8471   C   ZFP Multi Lane Copper Connector
SFF-8472  9.5  Diagnostic Monitoring Interface for Optical Xcvrs
INF-8475i 2.2  XPAK Small Formfactor Pluggable Receiver
SFF-8480  2.1  HSS (High Speed Serial) DB9 Connections
SFF-8482  1.5  Unshielded Dual Port Serial Attachment Connector
SFF-8483   C   External Serial Attachment Connector
SFF-8484  0.6  MultiLane Unshielded Serial Attachment Connector
SFF-8485  0.4  Serial GPIO (General Purpose Input/Output) Bus


SFF-8500e 1.1  5 1/4" drive form factors (all of 85xx family)
SFF-8501e 1.1  5 1/4" drive form factor dimensions
SFF-8508e 1.1  5 1/4" ATAPI CD-ROM w/audio connectors
SFF-8523  1.3  5 1/4" drive w/Serial Attachment Connector
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SFF-8551 3.2 5 1/4" CD Drives form factor
SFF-8552 1.0 5 1/4" 9.5mm/12.7mm Optical Drive Form Factor
SFF-8572 C   5 1/4" Tape form factor
SFF-8610 C   SDX (Storage Device Architecture)

2.3 Sources

Copies of ANSI standards or proposed ANSI standards may be purchased from Global
Engineering.

        15 Inverness Way East   800-854-7179 or 303-792-2181
        Englewood   303-792-2192Fx
        CO 80112-5704

Copies of SFF Specifications are available by joining the SFF Committee as an
Observer or Member.

        14426 Black Walnut Ct   408-867-6630x303
        Saratoga   408-867-2115Fx
        CA 95070   FaxAccess: 408-741-1600

The increasing size of SFF Specifications has made FaxAccess impractical to obtain
large documents. Document subscribers and members are automatically updated every
two months with the latest specifications. Specifications are available by FTP at
ftp://ftp.seagate.com/sff

Electronic copies of documents are also made available via CD_Access, a service
which provides copies of all the specifications plus SFF reflector traffic. CDs are
mailed every 2 months as part of the document service, and provide the letter ballot
and paper copies of what was distributed at the meeting as well as the meeting
minutes.

TABLE OF CONTENTS

3. General Description

The environment for this Specification is a Fibre Channel drive which uses a common connector structure for racking drives in a cabinet.

The FC-SCA system includes:

 - Dual ported Fibre Channel In/Out control signals
 - +5V and +12V power
 - ID select
 - Motor start control
 - LED drive signals
 - PBC Interlock control
 - Fibre Channel link rate selection
 - Power control

SCA is designed and placed to allow plugging a drive directly into a backplane by providing the necessary electrical connection. Mechanical stability and device retention must be provided by other mechanisms, including mounting brackets, guide rails, clips, or screw attachments.

The connector is a 40-position ribbon (aka leaf or single beam) design. There are various options available to meet the different mounting requirements of the connector to the device and for different drive plugging requirements.

The connector shall conform to the requirements of EIA-700A0AE (SFF-8451). It shall be positioned on the drive per the SCA-2 positional requirements of EIA-PN3876 (SFF-8337).

Since power and address information are provided to the drives through the connector, special cables must be provided if daisy-chaining of drives is required.

SCA is designed principally for the direct plugging of drives into a backplane and provisions have been made in this specification for the hot insertion of drives. Where hot plugging is a requirement, appropriate electrostatic discharge management shall be provided by the guide rails and guide slots.

4. Definitions and Conventions

4.1 Definitions

For the purpose of SFF Specifications, the following definitions apply:

4.1.1 Optional: This term describes features which are not required by the SFF Specification. However, if any feature defined by the SFF Specification is implemented, it shall be done in the same way as defined by the Specification.

4.1.2 Reserved: Where this term is used for bits, bytes, fields and code values; the bits, bytes, fields and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

4.1.3 VU (Vendor Unique): This term is used to describe bits, bytes, fields, pins, signals, code values and features which are not described in this SFF Specification, and may be used in a way that varies between vendors.

4.1.4 VU Mode: A mode of execution by the drive in which its use is not defined by this SFF Specification. The means by which a vendor invokes vendor unique operations within a drive is defined by this SFF Specification.

4.2 Conventions

Certain terms used herein are the proper names of signals. These are printed in

uppercase to avoid possible confusion with other uses of the same words; e.g., ATTENTION. Any lower-case uses of these words have the normal American-English meaning.

A number of conditions, commands, sequence parameters, events, English text, states or similar terms are printed with the first letter of each word in uppercase and the rest lower-case; e.g., In, Out, Request Status. Any lower- case uses of these words have the normal American-English meaning.

The American convention of numbering is used i.e., the thousands and higher multiples are separated by a comma and a period is used as the decimal point. This is equivalent to the ISO convention of a space and comma.

```
   American:         0.6                 ISO:         0,6
                    1,000                             1 000
                1,323,462.9                       1 323 462,9
```

4.3 Glossary

4.3.1 Backplane: The components of the enclosure that mechanically support the SCA connector and create or route the required signals and power to the SCA connector from the enclosure. The backplane may be a true multi-drive backplane, a paddle card inserted in a host computer, a paddle card attached to an appropriately designed cable, or any component with similar capabilities.

4.3.2 Drive: The FC-AL peripheral that plugs into the backplane using the SCA connector. The device may be removable from the enclosure through an external port or may be permanently installed in the enclosure. The FC-AL peripheral may be any FC-AL device of any type that meets one of the standard form factors and establishes its connection to the backplane through an SCA- 2 connector.

5. Physical Positioning Requirements

The SCA-2 connector is fixed with respect to the drive form factor as specified by EIA-PN3876 (SFF-8337) and SFF-8222.

 - The connector is located in the Y dimension with respect to the drive mounting holes with the specified tolerances.
 - The connector is centered side to side in the end of the drive in the X dimension with the specified tolerances.
 - The connector is centered at a fixed location above the base of the drive with the specified tolerances.

When the SCA-equipped drive is mated to a vertical board mount receptacle, there is 3.45+/-0.7mm clearance (reference value for the standard height receptacle using a 3.5" form factor drive) between the drive and the mated backplane. To insure a minimum contact wipe of 1.32mm, the drive must be fully seated with the mating socket connector.

Fully seated is defined by the distance from the backplane printed circuit board surface to the drive connector face as being 3.55+/-0.20mm for the standard height vertical receptacle, or 9.55+/- 0.20mm for the extended height vertical receptacle. For right angle and cable receptacle applications, the connectors are considered fully seated when the two connector housings limit further engagement.

6. Signals

6.1 Signal Conventions

Signal names are shown in all upper case letters. Signals can be asserted (active, true) in either a high (more positive voltage) or low (less positive voltage) state. A dash character (-) at the beginning or end of a signal name indicates it is asserted at the low level (active low). No dash or a plus character (+) at the

beginning or end of a signal name indicates it is asserted high (active high). An asserted signal may be driven high or low by an active circuit, or it may be allowed to be pulled to the correct state by the bias circuitry. Details of the requirements are included in the signal definitions.

Unless noted otherwise, tables specify the voltage and/or current requirements at the device connector. Current flow into the device is positive and current flow out of the device is negative.

6.2 Signal Assignments

The signals that are not defined in this clause are defined in FC-PI-2 and FC-AL-2.

The signal pinout is shown in Table 6-1.

TABLE 6-1 FIBRE CHANNEL SCA SIGNAL ASSIGNMENTS

40-pin SFF-8045 Connector Contact and Signal Name		Driven by Backplane/Drive		40-pin SFF-8045 Connector Contact and Signal Name	
1 -ENBL BYP CH1	(S)	D	B	(L) 12V CHARGE	21
2 12 VOLTS	(S)	B	B	(L) GROUND (12V)	22
3 12 VOLTS	(S)	B	B	(L) GROUND (12V)	23
4 12 VOLTS	(S)	B	B	(S) +PORT 1_IN	24
5 -PARALLEL ESI	(S)	D	B	(S) -PORT 1_IN	25
6 -DRIVE PRESENT	(S)	D	B	(L) GROUND (12V)	26
7 READY LED OUT	(S)	B/D	B	(S) +PORT 2_IN	27
8 POWER_CONTROL	(S)	B	B	(S) -PORT 2_IN	28
9 START_1/MATED	(S)	B	B	(L) GROUND (12V)	29
10 START_2/MATED	(S)	B	D	(S) +PORT 1_OUT	30
11 -ENBL BYP CH2	(S)	D	D	(S) -PORT 1_OUT	31
12 SEL_6 / -EFW	(S)	B	B	(L) GROUND (5V)	32
13 SEL_5 / -P_ESI_5	(S)	B	D	(S) +PORT 2_OUT	33
14 SEL_4 / -P_ESI_4	(S)	B	D	(S) -PORT 2_OUT	34
15 SEL_3 / -P_ESI_3	(S)	B	B	(L) GROUND (5V)	35
16 FAULT LED OUT	(S)	B/D	B	(L) SEL_2 / -P_ESI_2	36
17 DEV_CTRL_CODE_2	(S)	B	B	(L) SEL_1 / -P_ESI_1	37
18 DEV_CTRL_CODE_1	(S)	B	B	(L) SEL_0 / -P_ESI_0	38
19 5 VOLTS	(S)	B	B	(L) DEV_CTRL_CODE_0	39
20 5 VOLTS	(S)	B	B	(L) 5V CHARGE	40
Guide pins: Connected to GROUND (5V) on backplane and device.					

6.3 Design Considerations

No equalizer is present on the drive. The equalizer for termination of long data lines is either on the backplane, at the bulkhead, or built into the connecting cables.

Backplane applications shall use power planes for power distribution.

These are requirements to assist in protecting the signal and power pins from possible ESD damage and from power sequencing damage.

- All drives shall connect the guide pins to GROUND (5V).

- All backplanes shall connect the guide pins to the GROUND (5V).

If the drive does not use a particular voltage, all the power signals associated with that voltage shall be not connected.

Regardless of whether or not a particular voltage is provided by the backplane or used by the drive, all ground signals shall always be connected by the backplane and by the drive.

6.4 Signal Definitions

6.4.1 VOLTAGE and GROUND signals

Two voltage supplies and corresponding ground return signals are provided by the backplane connector to the drive. Table 6-2 provides the specifications for each of the voltage supplies. NOTE: The details of the actual drive supply requirements need to be studied for each drive and enclosure combination.

TABLE 6-2   VOLTAGE SPECIFICATION LIMITS

Voltage	# of pins	# of GNDs	Requirements on Supply at SCA Connector	Current Capability Average/Peak
12 VOLTS	3	4	12V +5% -7%	0/0 to 2.5/5 Amps
5 VOLTS	2	2	5V +/- 5%	0/0 to 2/2.5 Amps

The peak current capability is measured during operation or initialization after voltages have stabilized at the operating level. Inrush currents are managed by the power supply during normal power up and by the CHARGE signals during hot plugging.

For each voltage, the current supplied to the drive should be distributed as evenly as possible among the connecting pins.

The backplane power supplies shall operate correctly and maintain regulation from zero current to the peak current. Drive sequencing provisions may be required to avoid overloading power supplies during drive spin-up sequencing. Voltage dips to -10% are allowed on the 12 VOLTS supply during spin up.

For each voltage, an appropriate number of current return GROUND signal pins have been assigned.

- The GROUND signal pins for all voltages shall be tied together in the drive.
- The GROUND signals in the backplane may be tied together or connected separately to the power supplies as required by the particular subsystem.

6.4.2 CHARGE signals

Two charge signals, one for each of the power supply voltages, provide controlled precharging of the drive's internal circuits to avoid excessive surge currents during hot plugging.

The precharge pin mates early to allow the precharge to take place before the voltage pins make contact. The precharge control circuits are located on the backplane side of the connector if required. The backplane should assume that the VOLTS signals for each voltage are shorted together with the corresponding CHARGE signal on the drive. Systems without a hot-plug capability or with an alternative hot plugging mechanism are not required to implement the precharge control circuit and are not required to use long and short pins on the backplane connector.

After the drive capacitance is charged, but before the MATED signal indicates that the power signals are seated, the drive shall not use more than 1 Amp on the precharge voltage pin. This is required to protect the precharge pin from over-current damage and to provide additional flexibility in the design of the precharge circuit. The voltage provided by the precharge circuitry shall be as specified by Table 6-3. Note that any circuitry on the drive that uses the CHARGE voltage for executing initialization operations shall operate within the current and

voltage constraints specified for the CHARGE signals.

```
               TABLE 6-3   CHARGE SUPPLY TO DRIVE
   +---------------+-----------------------+----------+------------------+
   |       CHARGE  | Requirements on Supply |   Max   |       Max        |
   |       signal  |   at SCA Connector    |  Surge  |   Continuous     |
   |               |   from backplane      | to drive | required by drive |
   |               |   after CHARGE complete |         |                  |
   +---------------+-----------------------+----------+------------------+
   |     12 VOLTS  |     12V +5%, -12%     | 6 Amps  |      1 Amp       |
   |      5 VOLTS  |      5V +5%, -17%     | 6 Amps  |      1 Amp       |
   +---------------+-----------------------+----------+------------------+
```

After precharge is complete and the drive is mated, there is no guarantee that the precharge signal can provide any current to the drive and the drive should not depend on such current for operation.

The system designer should assume that the VOLTS signal(s) and the corresponding CHARGE signal are shorted together on the drive.

6.4.3 POWER_CONTROL

The implementation of the POWER_CONTROL signal is optional for both the backplane and the drive. This signal is driven by the backplane to control 5V and 12V power switches located on the drive. When this signal is asserted, high, 5V and 12V supplies are applied to the drive circuitry. When this signal is negated, low, 5V and 12V supplies are not connected to the drive circuitry.

When implemented in the drive, the drive provides a 10 KOhm pull up resistor from this signal to the 5V input to the drive. The electrical characteristics of the POWER_CONTROL signal are in Table 6-4.

```
      TABLE 6-4   ELECTRONIC REQUIREMENTS FOR POWER_CONTROL INPUT
     +--------+---------------------+---------------------------+
     | State  |       Current       |          Voltage          |
     +--------+---------------------+---------------------------+
     |  HIGH  |-250 uA < IIH < 250 uA|   2.2V < VIH  < 5.25V    |
     |  LOW   |   0 < IIL < -1 mA   |  -0.5V < VIL  < 0.7V     |
     +--------+---------------------+---------------------------+
```

6.4.4 FAULT LED OUT

The FAULT LED OUT signal is driven by the drive when the drive has established or detected any of the following conditions.

 - The drive is asserting both of the Enable Bypass signals.
 - The drive has detected an internal failure.
 - The drive has been instructed by the host to turn on the Fault LED.

Support of the FAULT LED OUT signal is mandatory for the drive. The host system is not required to generate any visual output when the FAULT LED OUT signal is asserted, but if such a visual output is provided, it shall be yellow to indicate that it is a warning signal. The requirement to replace a failing unit when the link is inaccessible is indicated by the Fault LED.

The FAULT LED OUT signal is designed to pull down the cathode of an LED using an open collector or open drain driver circuit. The anode is attached to an appropriate supply through a current limiting resistor. The LED and the current limiting resistor are external to the drive. See Table 6-5 for the driver characteristics.

The FAULT LED OUT signal may optionally be driven by the backplane to turn on the external LED. This usage is host system unique.

```
         TABLE 6-5   OUTPUT CHARACTERISTICS OF LED OUT SIGNALS
```

```
+---------------+-----------------------+----------------+
|  State        | Current Drive Available | Output Voltage |
+---------------+-----------------------+----------------+
| DRIVE LED OFF | -100 uA < IOH < 100 uA |                |
| DRIVE LED ON  |        IOL >  30 mA   | 0 < VOL < 0.5V |
+---------------+-----------------------+----------------+
```

6.4.5 READY LED OUT

The READY LED OUT signal is driven by the drive to turn on an externally visible LED that indicates the state of readiness and activity of the drive. Two alternative indication patterns are defined. The hot plug implementation should be used for drives installed in hot plugged environments and is recommended for all drives. The legacy implementation is allowed where compatibility with previous indication systems is required.

Support of the READY LED OUT signal is mandatory for the drive. The host system is not required to generate any visual output when the READY LED OUT signal is raised, but if such a visual output is provided, it shall be white or green to indicate that normal activity is being performed. Additional optional flashing patterns can be used to signal vendor unique conditions, but these patterns are not part of the standard failure analysis procedures. Failure analysis is performed through the FC-AL and FCP SCSI commands if the link is accessible. The requirement to replace a failing unit when the link is inaccessible is indicated by the Fault LED signal.

The READY LED OUT signal is designed to pull down the cathode of an LED using an open collector or open drain driver circuit. The anode is attached to an appropriate supply through a current limiting resistor. The LED and the current limiting resistor are external to the drive. The characteristics are described in Table 6-5.

The READY LED OUT signal may optionally be driven by the backplane to turn on the external LED. This usage is host system unique.

6.4.5.1 Hot Plug Implementation

The READY LED OUT signal is driven by the drive in the following patterns in hot plugged environments:

(a) If the drive is not mated, the signal shall not be asserted. The LED shall be off.
(b) If the drive is mated, but is not spinning, the signal shall be asserted when a SCSI command or task management function is received by the drive. The intent is that the light appears to be mostly off when the drive is not spinning but that an indication is presented each time SCSI activity is requested. The drive may be removed with no danger of mechanical damage in this state.
(c) If the drive is mated and is in the process of performing a spin-up or spin-down, the signal shall be asserted in such a manner that the light shall flash on and off. The light shall be on for approximately 0.5 sec and off for approximately 0.5 sec.
(d) If the drive is mated and ready, the signal shall be asserted continuously, except that the signal shall be negated for a period long enough to be detected by an observer when a SCSI command is received by the drive. The intent is that the light appear to be mostly on, but to flash off when commands are occurring.

During the spin-down process, the drive transitions immediately from state (d) to state (c). When the drive has reached a state stable enough for it to be removed without mechanical damage, the READY LED OUT changes from state (c) to state (b).

6.4.5.2 Legacy Implementation

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The READY LED OUT signal may be driven by the drive in the following patterns in
legacy environments.

 (a) If the drive is not mated, the signal shall not be asserted. The LED
     shall be off.
 (b) If the drive is mated, whether the drive is not spinning or is ready,
     the signal shall be asserted when a SCSI command or task management
     function is received by the drive. The intent is that the light flashes
     on more often as drive activity increases.
 (c) If the drive is performing a spin-up or spin-down, the assertion
     pattern for the signal is vendor specific.
 (d) If the drive is mated and ready, same as (b).

Note that only state (d) is necessarily different from the states defined for hot
plug implementation.

6.4.6 START_x/MATED Controls

The method of starting the drive's motor is established by the signals START_1 and
START_2, as described in Table 6-6. The state of these signals can either be wired
into the backplane socket or driven by logic on the backplane. In addition, the
signals indicate to the drive that the drive has been mated to a backplane. The
signals can also be optionally used by the backplane to indicate to the drive that
the drive should prepare itself to be removed from the backplane.

Each drive location should have these signals supplied independently to ensure
proper operation. If the signals were bussed, a drive with a power failure might
clamp the signals in a condition that caused operational drives to behave
incorrectly.

 - If the GROUND state is implemented for START_1, bussing between drives is
   permissible.
 - If the GROUND state is implemented for START_2, bussing between drives is
   permissible.
 - If the OPEN state is implemented for START_1, this signal shall not be
   bussed between drives.
 - If the OPEN state is implemented for START_2, this signal shall not be
   bussed between drives.
 - If the enclosure contains logic that requests the drive to power down,
   the START_1 and START_2 signals shall not be bussed between drives.

TABLE 6-6 DEFINITION OF MOTOR START / MATED CONTROLS

Case	START_2 / MATED	START_1 / MATED	Motor Spin Function
1	OPEN	OPEN	Drive is not mated. No spin-up will occur and precharge average current demands shall not be exceeded. Optional prepare-for-removal indication to drive from enclosure.
2	OPEN	GROUND	Drive is mated. After a mating deskew time has passed, the motor will spin up when the SCSI start command is received.
3	GROUND	OPEN	Drive is mated. After a mating deskew time has passed, the motor will spin up after a delay in seconds of 12 times* the modulo 8 value of the numeric SEL_ID of the drive.
4	GROUND	GROUND	Drive is mated. After a mating deskew time has passed, the Motor spins up immediately after the completion of its reset and POST functions.

  * This value may be reduced by drive suppliers to reflect the worst case
     time duration of peak current drains at the 12V or 5V source (or both)
     during motor spin up. In no case should the delay exceed 12 seconds.

The mating deskew time is 250 msecs. The drive shall wait a minimum of 250 msecs
after detecting one of the mated controls before setting its final values for the
Motor Start/Mated controls, the selection ID values, and the FC link rate, since
minor mechanical misalignments may cause the final mating to occur in any time
order.

The backplane may optionally establish an open indication to both the START_1 and
START_2 signals to indicate to the drive that it should prepare itself to have power
removed. The drive may optionally detect the case 1 condition and elect to perform
those behaviors necessary to prepare for the drive to spin down and be removed. SFF
8067 defines a method to enable and disable this behavior.

If the drive supports detection of Case 1 to prepare itself for power removal or for
physical removal from the enclosure, the detection shall occur within 1 second from
the time that the Case 1 condition is presented to the drive.

The following drive behaviors are defined.

 a) The drive shall gracefully establish the bypass condition on both ports.
    The graceful bypass mechanism is still being defined, but basically
    requires that the drive win arbitration, then assert the -ENBL BYP CH1
    and -ENBL BYP CH2 signals. This eliminates the possibility that data may
    be corrupted while flowing on the loop.
 b) The drive may optionally perform a spin-down operation. This option is
    controlled by a MODE SELECT operation.
 c) The drive may optionally transfer any cached information to the media.
    This option is controlled by a MODE SELECT operation.

A 10 KOhm (typical) pull up resistor is provided on the drive for each of the
START_x/MATED signals to be sure that the control value is maintained in its "OPEN"
state unless a ground is provided from the backplane.

The OPEN and GROUND states are established as described in Table 6-7.

```
        TABLE 6-7  ELECTRONIC REQUIREMENTS FOR INPUT CONTROLS
   +--------+---------------------+---------------------------+
   | State  |       Current       |          Voltage          |
   +--------+---------------------+---------------------------+
   |  OPEN  |-250 uA < IIH < 250 uA|   2.2V < VIH  < 5.25V     |
   | GROUND |   0    < IIL < -1 mA |  -0.5V < VIL  < 0.7V      |
   +--------+---------------------+---------------------------+
```

6.4.7 SEL_n/-P_ESI_n/-EFW and -PARALLEL ESI

6.4.7.1 -PARALLEL ESI

The optional -PARALLEL ESI signal allows the drive to selectively examine the SEL_ID values that provide physical addressing information or a set of information about the enclosure that can be transmitted across the drive's Fibre Channel interface.

 - If -PARALLEL ESI is not implemented on an SFF-8045 drive, there shall be
   no connection to the signal from the drive.
 - If -PARALLEL ESI is not implemented by the backplane, there shall be no
   connection to the signal from the backplane.
 - The -P_ESI_n and -EFW bits can be examined by the drive 4 usec (includes
   1 usec for enclosure response and 3 usecs for the SEL_n signals rise time)
   after -PARALLEL ESI is asserted and shall remain valid until -PARALLEL ESI
   is negated.
 - The SEL_n bits can be examined by the drive 7 usec (includes 3 usecs
   for rise time of the -PARALLEL_ESI signal, 1 usec for enclosure response
   and 3 usecs for the SEL_n signals rise time) after -PARALLEL ESI is negated
   and shall remain valid until -PARALLEL ESI is asserted.

When the -PARALLEL ESI signal is negated (high) by the drive, the backplane shall present SEL_n information to the connector. If the -PARALLEL ESI signal is not implemented by the backplane, only SEL_n information shall be presented. Each drive must have a separate -PARALLEL ESI signal, since drives perform their initialization procedures independently of each other and at different times.

When the -PARALLEL ESI signal is asserted (low) by the drive, the backplane presents up to 6 Enclosure Status Information bits and the -EFW bit to the drive on the -P_ESI bits. The -PARALLEL ESI signal may be asserted by the drive at any time that the drive does not need to examine the SEL_n signals.

```
        TABLE 6-8  OUTPUT CHARACTERISTICS OF -PARALLEL ESI
   +--------------+-----------------------+-------------------+
   |    State     | Current Drive Available | Output Voltage  |
   +--------------+-----------------------+-------------------+
   |    HIGH      | -100 uA < IOH  < 100 uA | 2.4V < VOH < 5.25V |
   +--------------+-----------------------+-------------------+
   |    LOW       |       IOL > 2 mA      | 0 < VOL < 0.5V    |
   +--------------+-----------------------+-------------------+
```

6.4.7.2 SEL_n Function

The backplane uses SEL_6 through SEL_0 ID lines to provide the binary value of the Loop Identifier to the drive in that location. A SEL decode of 126 creates an AL_PA of 0 and is reserved for the fabric port, if any. A SEL decode of 127 is a flag for the drive to use a soft address for the AL_PA. The SEL lines are used in a system to assign a physical location for each connection to a backplane, allowing the management of configuration and the simple identification of devices that need to be changed for maintenance reasons. The SEL lines specify the hard address for each drive unless the system is required to override the values to manage duplicate SEL decodes.

If a drive were removed from the backplane and plugged into a different location in the backplane, the system normally uses the label information recorded on the drive to recognize where this drive should be mapped into its file management tables. This

flexibility can be very desirable in data security applications or for configuration expansion. In some RAID configurations, the physical location in a string of drives can be extremely important and should remain consistent. It is recommended that physical location dependent systems use the capability to read the SEL ID value and the logical address to ensure proper configuration in the event of a maintenance or other error.

The ID Selection signals are tested by the drive at power on to determine the proper Loop Identifier for a drive. The signals may be tested at other times as required by the drive. The ID Selection signal is expected to remain constant for a given drive location, although some bits may be settable externally to differentiate the Loop Identifiers for different drive enclosures.

The high state is the asserted state and the low state is the negated state for the SEL_n signals, as described in Table 6-9. The driver, if any, shall be an open collector driver or other circuit without an active drive to the high state. The pull up resistor shall be on the backplane.

SEL_n signals having the high state shall not be bussed together.

Note: Violating the requirement to not buss SEL_n signals to drives with supply voltages less than the input voltage (may be due to insertion, removal, or separate power control to individual drives) may draw current on the inputs (ESD diodes become forward biased) and pull a buss low.

The minimum backplane pull up resistor value for each of the SEL_n signals shall be 3.3 Kohm. This protects drives implementing SFF-8067 ESI functions from short circuit conditions during the identification protocol. A 10 KOhm resistor is suggested.

```
      TABLE 6-9  ELECTRONIC REQUIREMENTS FOR SEL_n/P_ESI_n INPUTS
      +--------+---------------------+----------------------------+
      | State  |       Current       |           Voltage          |
      +--------+---------------------+----------------------------+
      |  HIGH  |-250uA < Iih < 250 uA|    2.2V  < Vih  < 5.25V    |
      |  LOW   |    0 < Iil < -1 mA   |   -0.5V  < Vil  < 0.7V     |
      +--------+---------------------+----------------------------+
```

If a P_ESI_n bit is not provided, the corresponding SEL_n bit can be implemented using the pullup for the asserted state and ground for the negated state. The asserted (high) state establishes the binary 1 value.

 - SEL_6 is the most significant binary bit, having the value of $2**6$.
 - SEL_0 is the least significant binary bit, having the value of $2**0$.

The Loop Identifier is mapped according to tables in FC-AL to the proper AL_PA (AL Physical Address) for the drive.

6.4.7.3 -P_ESI_n Function

When the -PARALLEL ESI signal is asserted (low) by the drive, the backplane optionally presents up to 6 Enclosure Status Information bits on the - P_ESI_n signals and an Enclosure Failure Warning (-EFW) signal to the drive. If the backplane does not implement the -P_ESI function, the SEL_n values are provided to the signals regardless of the state of the -PARALLEL ESI signal. This document does not define a mechanism for determining that the backplane does not implement parallel ESI.

The drive senses the state of the bits after the assertion of -PARALLEL ESI. Other than the -EFW bit, the meaning of the bits is unique to the enclosure. The -PARALLEL ESI signal may be asserted by the drive at any time that the drive does not need to examine the SEL_n signals. During this period, the drive monitors the -EFW signal as described below. - PARALLEL ESI is asserted in response to a SCSI command requesting the presentation of enclosure information. The SCSI command indicates a 1 value for

each -P_ESI bit that is asserted to the low state.

The high and low states are established as specified in Table 6-9.

6.4.7.4 -EFW Function

The Enclosure Failure Warning signal (-EFW) is optional. The enclosure failure warning is driven by the backplane and has the same driver properties as the -P_ESI_n signals. The -EFW signal is available to the drive only when -PARALLEL ESI is asserted and is available continuously while the signal is asserted.

6.4.8 DEV_CTRL_CODE Function

The backplane uses the Device Control function, DEV_CTRL_CODE_2 through DEV_CTRL_CODE_0 signals, to provide a binary code to the drive to control functions such as FC link rate, Power Failure Warning and Hard Reset. The control function is either identified by a code or a sequence of codes on the DEV_CTRL_CODE signals. Table 6-11 defines the functions and assigned codes that use a decode of the value on the DEV_CTRL_CODE signals.

A 10 KOhm (typical) pull up resistor is provided on the drive for each of the DEV_CTRL_CODE signals to be sure that each signal is maintained in its high state unless a low is provided from the backplane. An open collector or open drain driver circuit is the recommended implementation on the backplane. The electrical input characteristics the DEV_CTRL_CODE_2 through DEV_CTRL_CODE_0 signals are defined in Table 6-10.

TABLE 6-10 ELECTRONIC REQUIREMENTS FOR DEV_CTRL_CODE INPUTS

State	Current	Voltage
HIGH	-250uA < Iih < 250 uA	2.2V < Vih < 5.25V
LOW	0 < Iil < -1 mA	-0.5V < Vil < 0.7V

TABLE 6-11 - DEFINITION OF DEVICE CONTROL CODES

Value	Function
7	1.0625 GHZ - The FC interfaces for both ports of the drive are set to run at a link rate of 1.0625 GHZ.
6	2.1250 GHZ - The FC interfaces for both ports of the drive are set to run at a link rate of 2.1250 GHZ.
5	4.250 GHZ - The FC interfaces for both ports of the drive are set to run at a link rate of 4.250 GHZ.
4	8.500 GHZ - The FC interfaces for both ports of the drive are set to run at a link rate of 8.500 GHZ.
3 to 1	Reserved for future functions and initiation of Hard Reset.
0	Power Failure Warning (see below)

6.4.8.1 Link Rate

Following power-on-reset, the drive shall wait a minimum of 250 msec after detecting one of the mated controls (see 6.4.6) and verify the DEV CTRL CODE signals have not changed for 5 msec before accepting the link rate. If the value on DEV_CTRL_CODE_2-0 is not a supported link rate, the drive remains in the bypassed state on the FC ports. The drive continues to read the DEV_CTRL_CODE signals waiting for a supported value.

After the drive reads a supported link rate value on the DEV_CTRL_CODE signals, it shall read the DEV_CTRL_CODE signals at least once a second to determine if a change of link rate is requested. When the drive reads a different link rate, it shall wait at least 30 msecs to deskew the new value before accepting the value as valid. If

the new value is still present at the end of the deskew period, the drive shall
perform the equivalent of a power-on-reset and attempt to operate at the new link
rate.

6.4.8.2 Power Failure Warning (PFW)

The PFW function is optional for the drive and backplane. If supported the drive
shall detect a transition to the PFW code from any other code within 2 msecs of
being asserted by the backpanel. Upon detecting the PFW value, the drive waits at
least 1 usec to deskew the value before accepting it as a valid PFW. The enclosure
shall provide full power to the drive for a minimum of 4 msecs from assertion of the
PFW code value.

When the drive detects the assertion of the PFW code it shall take the following
actions:

a) The drive shall disable both ports gracefully at a frame boundary.
b) If Write Caching is enabled:
   - the drive shall write as much of the data to nonvolatile storage
     as possible, and
   - the drive shall stop writing data to nonvolatile storage on a
     block boundary.
c) If Write Caching is disabled, the drive shall stop writing data to
   nonvolatile storage on a block boundary.

If the value on the DEV_CTRL_CODE signals changes to another value after PFW is
detected, the drive shall complete the required actions above and wait 1 sec before
accepting the new value as valid. After the validation period, the drive shall
perform the equivalent of a power-on-reset.

6.4.8.3 Hard Reset

The Hard Reset function is optional for the drive and the backplane. The recommended
implementation is in hardware independent of the drive's microprocessor.

The Hard Reset function uses a sequence of values on the DEV_CTRL_CODE signals. The
sequence is 5,1,3,2,3,1,5. Each value shall be valid for 1 msec +/- 200 usec. When
a transition between values occurs on the DEV_CTRL_CODE signals, the new value shall
be valid within 20 nsec.

The enclosure shall ensure a transition of values occurs at the start of the reset
sequence. If the value on the DEV_CTRL_CODE signals is a 5 prior to the reset
sequence, the enclosure shall transition to a 4 before starting the reset sequence.
The enclosure shall follow the same timing requirements for transition to a 4 as for
the other values of the reset sequence. The drive ignores the transient value of 4.

Note: DEV_CTRL_CODE values of 7, 6, and 0 are avoided in the reset sequence. Legacy
drives may take transient occurrences of these values for the link rate or PFW.

A drive supporting the Hard Reset function shall evaluate the DEV_CTRL_CODE signals
at least once every 500 uS. The drive validates each value of the sequence by
verifying it is the expected value and does not change for a minimum of 400 usec.
When the drive detects the final value of the reset sequence (5), it shall start the
reset function without waiting for the DEV_CTRL_CODE signals to transition to
another value.

Note: With the Hard Reset timing, transient values on the DEV_CTRL_CODE signals will
not be mistaken for other functions due to the deskew requirements for those
functions.

A drive detecting a valid Hard Reset sequence shall perform the equivalent of a
power-on-reset. The drive shall complete the reset and be ready to communicate on
the FC ports in less than 1 sec. The drive does not spin-down. The drive shall wait
a minimum of 250 msecs after a valid Hard Reset sequence is detected before reading

the selection ID values and the DEV_CTRL_CODE signals.

While performing the reset function, the drive continues to monitor the DEV_CTRL_CODE signals for the reset sequence. The detection of a new reset sequence restarts the function.

When a drive that supports Hard Reset detects any sequence of values other than a valid reset sequence, it shall follow the requirements for other functions defined for the DEV_CTRL_CODE signals.

6.4.9 Fibre Channel Signals

The Fibre Channel signals define an interface in which the voltage and current levels supplied to and expected from the drives are as defined in the FC-PI-2 and FC-AL standards. FC-0 voltage and current levels are supplied to the drives and expected from the drives. The signals are transmitted on Twinax transmission lines and are capable of long distance (up to 30 meters) and high transfer rates. Systems using hot plugging shall provide short pins on these signals to avoid the introduction of excessive AC transients during the plugging process.

Jitter, eye, and amplitude requirements are those expected of a standard Fibre Channel device. Redriving of the FC signals leaving the drive enclosure may be required to assure compliance with Fibre Channel specifications at the external interface of the enclosure.

If only a single Fibre Channel port is implemented on an SFF-8045 drive, it shall be PORT 1 (Pins 24, 25, 30, and 31).

Bypass circuits are provided as indicated in section 6.4.9

6.4.9.1 PORT OUT

The PORT OUT signals are driven by the drive. These signals are differential copper with a source termination of 100 Ohms. The outputs are DC coupled. The AC coupling is at the receiver whether a Port Bypass Circuit or the next device. For compliance with the Fibre Channel standards, the output from the drive enclosure to external devices should be AC coupled as described in the standard.

Note: FC-PI-2 requires 100 ohm transmission lines for 4 Gbps high speed signals. 1 Gbps and 2 Gbps FC specified 150 ohm transmission lines. The two requirements are compatible. In actual implementation, most backpanel designs for 1 Gbps and 2 Gbps used 100 ohm transmission lines. All new designs should use 100 ohm transmission line and termination.
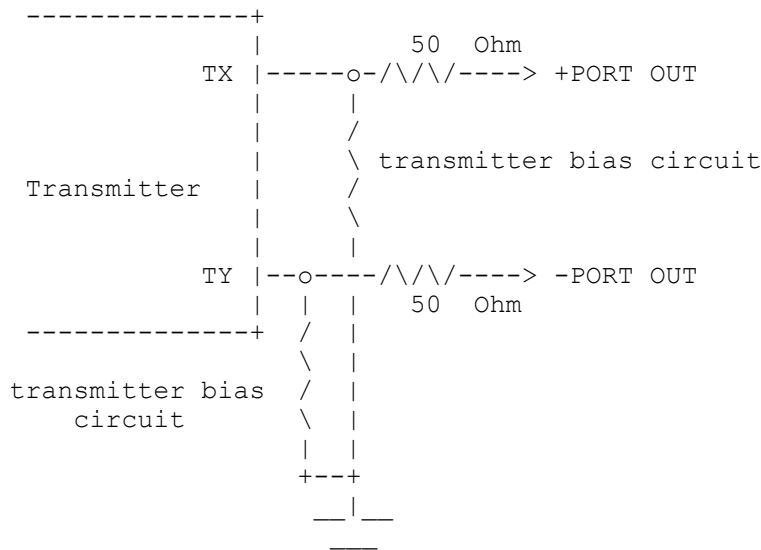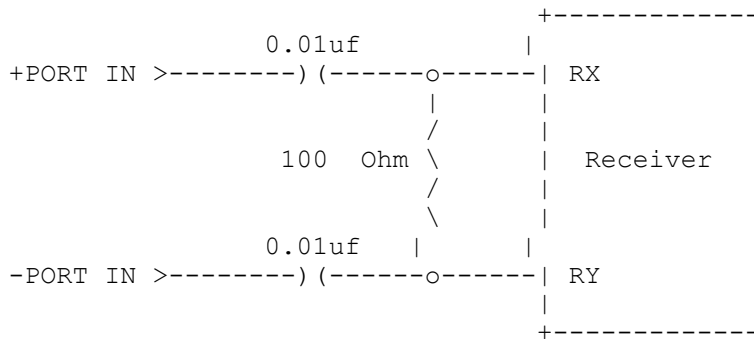
```
-------------+
            |              50  Ohm
        TX  |-----o-/\/\/----> +PORT OUT
            |     |
            |     /
            |     \ transmitter bias circuit
   Transmitter   /
            |     \
            |     |
        TY  |--o----/\/\/----> -PORT OUT
            | |  |     50  Ohm
-------------+  /  |
              \  |
transmitter bias  /  |
     circuit     \  |
                 |  |
                 +--+
                 __|__
                  ___
```

                    FIGURE 6-1 FIBRE CHANNEL OUTPUT CIRCUIT

6.4.9.2 PORT IN

The PORT IN signals to the drive are differential copper with 100 Ohm termination.
These signals are AC coupled with capacitors.

```
                                   +-------------
              0.01uf               |
  +PORT IN >--------)(------o------| RX
                          |     |
                          /     |
          100  Ohm \      |  Receiver
                          /     |
                          \     |
              0.01uf    |     |
  -PORT IN >--------)(------o------| RY
                                |
                                +-------------
```

   NOTE: Exact values of capacitors are to be chosen to present a nominal
          termination impedance of 100 Ohms. Values of 0.01 uf are shown
          for reference only.

              FIGURE 6-2 FIBRE CHANNEL INPUT CIRCUIT

6.4.10 -ENBL BYP CH1 and -ENBL BYP CH2

These Enable Bypass signals control Port Bypass Circuits (PBC) located external to
the drive. The PBC allows a loop to remain functional in the event of a drive
failure or removal. -ENBL BYP CH1 controls the PBC for Channel 1, while -ENBL BYP
CH2 controls the PBC for Channel 2. The electrical characteristics are shown in
Table 6-12.

          TABLE 6-12 -ENABLE BYP ELECTRICAL CHARACTERISTICS

Circuit/State	Voltage	Current
Driver/Asserted	0 < Vol < 0.5V	
Driver/Negated	2.4 < Voh < 5.25	+3 mA at 2.4V

When these signals are asserted (low), the PBC bypasses the drive on the associated

channel. A pull down resistor of 1 KOhm located on the PBC should be used to insure
the bypass is enabled if the drive is not installed (see Figure 6-3).

The -ENBL BYP CHn signals will remain passively enabled during the hot plugging
process and will remain enabled until the drive has performed appropriate internal
initialization and has met the requirements of any states established by MODE SELECT
or other commands.

The Enable Bypass signal is activated under failing conditions within the drive, on
detection of the Loop Port Bypass primitive sequence, or on removal of the. In the
bypass state the drive continues to receive on the inbound fibre. Enable Bypass may
be deactivated by detection of a Loop Port Enable primitive sequence if the drive
has completed self-test and a hardware failure is not present.

Failure modes detected by the drive that enable bypass include:

 - Transmitter/ receiver wrap test failure
 - Loss of receive clock
 - Loss of transmission clock
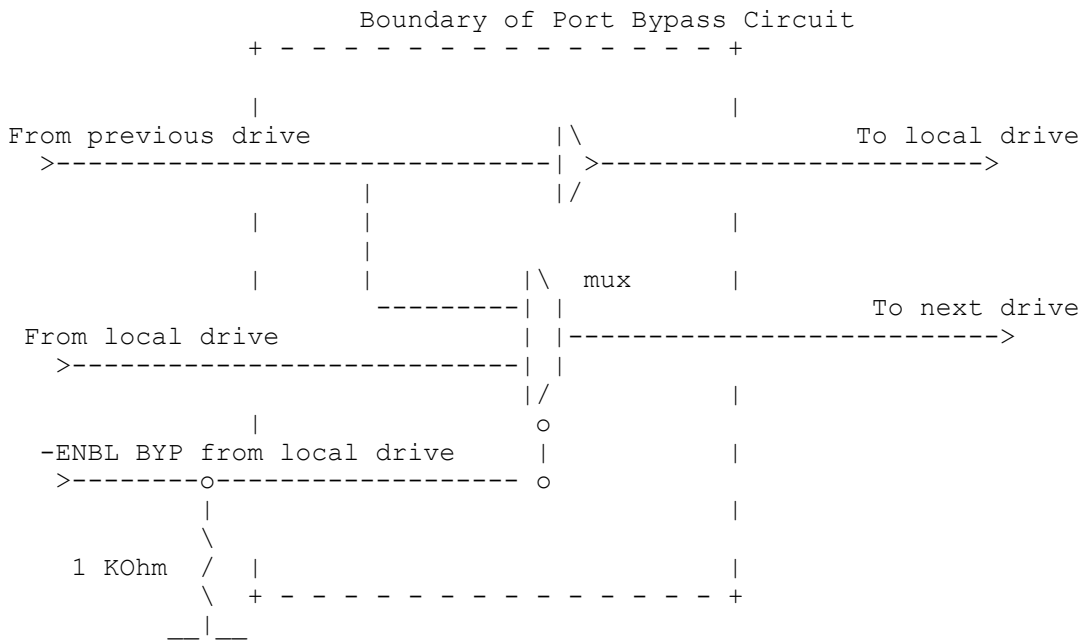 - Drive interface hardware error

```
                       Boundary of Port Bypass Circuit
                  + - - - - - - - - - - - - - - - +

                  |                           |
 From previous drive                  |\                  To local drive
   >-----------------------------| >------------------------>
                  |             |/
                  |      |               |
                  |
                  |      |      |\  mux      |
                   --------| |                   To next drive
  From local drive        | |--------------------------->
   >---------------------------| |
                  |/          |
                  |            o
  -ENBL BYP from local drive   |          |
   >--------o------------------ o
              |                   |
              \
    1 KOhm  /  |                   |
            \  + - - - - - - - - - - - - - - +
        __|__
        ___          FIGURE 6-3  SAMPLE CIRCUIT FOR PORT BYPASS
```

6.4.11 -DRIVE PRESENT

This signal is connected to the drive's ground plane.

The backplane can optionally use the signal to passively detect the presence of a drive by using a detection circuit connected to a tie up resistor.

- When the drive is not installed, the detection circuit can see the signal provided through the tie up resistor.
- When the drive is installed, the signal shall be grounded through the drive's ground signal and the grounded state can be detected by the detection circuit.
- The detection circuit and tie up resistor should be designed so that no more than 3 mA of current can be grounded through the -DRIVE PRESENT signal.

If the backplane does not passively detect the presence of a drive, this signal may be used as a GROUND (5V) and grounded to the appropriate plane in the backplane or it may be left with no connection.