SFF specifications are available at http://www.snia.org/sff/specifications
or ftp://ftp.seagate.com/sff

This specification was developed by the SFF Committee prior to it becoming the SFF TA (Technology Affiliate) TWG (Technical Working Group) of SNIA (Storage Networking Industry Association).

The information below should be used instead of the equivalent herein.

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If you are interested in participating in the activities of the SFF TWG, the membership application can be found at:
http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on can be found at:
http://www.snia.org/sff/specifications/SFF-8000.TXT

The operations which complement the SNIA's TWG Policies & Procedures to guide the SFF TWG can be found at:
http://www.snia.org/sff/specifications/SFF-8032.PDF

Suggestions for improvement of this specification will be welcome, they should be submitted to:
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SFF Committee documentation may be purchased in hard copy or electronic form.
SFF Specifications are available at fission.dt.wdc.com/pub/standards/SFF/spec

SFF Committee

SFF-8053 Specification for

GBIC (Gigabit Interface Converter)

Rev 5.5 September 27, 2000

Secretariat: SFF Committee

Abstract: This specification describes the GBIC (Gigabit Interface Converter) for Fibre Channel applications.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of pluggable Gigabit Interface Converters. This is an internal working document of the SFF Committee, an industry ad hoc group.

This document is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this document.

Support: This document is supported by the identified member companies of the SFF Committee.

Documentation: This document has been prepared in a similar style to that of the ISO (International Organization of Standards).

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EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

Adaptec
AMP
Amphenol
ENDL
FCI/Berg
Hitachi Cable
Madison Cable
Sun Microsystems
TI Japan
Unisys

The following SFF member companies voted no on the technical content of this industry specification.

Compaq
Methode

The following member companies of the SFF Committee voted to abstain on this industry specification.

DDK Electronics
Foxconn Int'l
Fujitsu CPA
Honda Connector
IBM
Matsushita
Maxtor
Molex
Montrose/CDT
Pioneer NewMedia
Quantum
Ricoh
Seagate
Toshiba America
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Yamagata Fujitsu
YC Cable

If you are not a member of the SFF Committee, but you are interested in participating, the following principles have been reprinted here for your information.

PRINCIPLES OF THE SFF COMMITTEE

The SFF Committee is an ad hoc group formed to address storage industry needs in a prompt manner. When formed in 1990, the original goals were limited to defining de facto mechanical envelopes within which disk drives can be developed to fit compact computer and other small products.

Adopting a common industry size simplifies the integration of small drives (2 1/2" or less) into such systems. Board-board connectors carrying power and signals, and their position relative to the envelope are critical parameters in a product that has no cables to provide packaging leeway for the integrator.

In November 1992, the SFF Committee objectives were broadened to encompass other areas which needed similar attention, such as pinouts for interface applications, and form factor issues on larger disk drives. SFF is a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Documents created by the SFF Committee are expected to be submitted to bodies such as EIA (Electronic Industries Association) or an ASC (Accredited Standards Committee). They may be accepted for separate standards, or incorporated into other standards activities.

The principles of operation for the SFF Committee are not unlike those of an accredited standards committee. There are 3 levels of participation:

- Attending the meetings is open to all, but taking part in discussions is limited to member companies, or those invited by member companies
- The minutes and copies of material which are discussed during meetings are distributed only to those who sign up to receive documentation.
- The individuals who represent member companies of the SFF Committee receive documentation and vote on issues that arise. Votes are not taken during meetings, only guidance on directions. All voting is by letter ballot, which ensures all members an equal opportunity to be heard.

Material presented at SFF Committee meetings becomes public domain. There are no restrictions on the open mailing of material presented at committee meetings. In order to reduce disagreements and misunderstandings, copies must be provided for all agenda items that are discussed. Copies of the material presented, or revisions if completed in time, are included in the documentation mailings.

The sites for SFF Committee meetings rotate based on which member companies volunteer to host the meetings. Meetings have typically been held during the ASC T10 weeks.

The funds received from the annual membership fees are placed in escrow, and are used to reimburse ENDL for the services to manage the SFF Committee.

Annual SFF Committee Membership Fee	$ 1,800.00
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SFF Specifications

There are several projects active within the SFF Committee. At the date of printing document numbers had been assigned to the following projects. The status of Specifications is dependent on committee activities.

F = Forwarded	The document has been approved by the members for forwarding to a formal standards body.
P = Published	The document has been balloted by members and is available as a published SFF Specification.
A = Approved	The document has been approved by ballot of the members and is in preparation as an SFF Specification.
C = Canceled	The project was canceled, and no Specification was Published.
D = Development	The document is under development at SFF.
E = Expired	The document has been published as an SFF Specification, and the members voted against re-publishing it when it came up for annual review.
e = electronic	Used as a suffix to indicate an SFF Specification which has Expired but is still available in electronic form from SFF e.g. a specification has been incorporated into a draft or published standard which is only available in hard copy.
i = Information	The document has no SFF project activity in progress, but it defines features in developing industry standards. The document was provided by a company, editor of an accredited standard in development, or an individual. It is provided for broad review (comments to the author are encouraged).
s = submitted	The document is a proposal to the members for consideration to become an SFF Specification.

Spec #	Rev	List of Specifications as of September 30, 2000
SFF-8000		SFF Committee Information
SFF-8001i	E	44-pin ATA (AT Attachment) Pinouts for SFF Drives
SFF-8002i	E	68-pin ATA (AT Attachment) for SFF Drives
SFF-8003	E	SCSI Pinouts for SFF Drives
SFF-8004	E	Small Form Factor 2.5" Drives
SFF-8005	E	Small Form Factor 1.8" Drives
SFF-8006	E	Small Form Factor 1.3" Drives
SFF-8007	E	2mm Connector Alternatives
SFF-8008	E	68-pin Embedded Interface for SFF Drives
SFF-8009	4.1	Unitized Connector for Cabled Drives
SFF-8010	E	Small Form Factor 15mm 1.8" Drives
SFF-8011i	E	ATA Timing Extensions for Local Bus
SFF-8012	3.0	4-Pin Power Connector Dimensions
SFF-8013	E	ATA Download Microcode Command
SFF-8014	C	Unitized Connector for Rack Mounted Drives
SFF-8015	E	SCA Connector for Rack Mounted SFF SCSI Drives
SFF-8016	C	Small Form Factor 10mm 2.5" Drives
SFF-8017	E	SCSI Wiring Rules for Mixed Cable Plants

SFF-8018	E	ATA Low Power Modes
SFF-8019	E	Identify Drive Data for ATA Disks up to 8 GB
INF-8020i	E	ATA Packet Interface for CD-ROMs
SFF-8028i	E	- Errata to SFF-8020 Rev 2.5
SFF-8029	E	- Errata to SFF-8020 Rev 1.2
SFF-8030	1.8	SFF Committee Charter
SFF-8031		Named Representatives of SFF Committee Members
SFF-8032	1.4	SFF Committee Principles of Operation
SFF-8033i	E	Improved ATA Timing Extensions to 16.6 MBs
SFF-8034i	E	High Speed Local Bus ATA Line Termination Issues
SFF-8035i	E	Self-Monitoring, Analysis and Reporting Technology
SFF-8036i	E	ATA Signal Integrity Issues
INF-8037i	E	Intel Small PCI SIG
INF-8038i	E	Intel Bus Master IDE ATA Specification
SFF-8039i	E	Phoenix EDD (Enhanced Disk Drive) Specification
SFF-8040	1.2	25-pin Asynchronous SCSI Pinout
SFF-8041	C	SCA-2 Connector Backend Configurations
SFF-8042	C	VHDCI Connector Backend Configurations
SFF-8043	E	40-pin MicroSCSI Pinout
SFF-8045	4.2	40-pin SCA-2 Connector w/Parallel Selection
SFF-8046	E	80-pin SCA-2 Connector for SCSI Disk Drives
SFF-8047	C	40-pin SCA-2 Connector w/Serial Selection
SFF-8048	C	80-pin SCA-2 Connector w/Parallel ESI
SFF-8049	E	80-conductor ATA Cable Assembly
INF-8050i	1.0	Bootable CD-ROM
INF-8051i	E	Small Form Factor 3" Drives
INF-8052i	E	ATA Interface for 3" Removable Devices
SFF-8053	5.5	GBIC (Gigabit Interface Converter)
INF-8055i	E	SMART Application Guide for ATA Interface
SFF-8056	C	50-pin 2mm Connector
SFF-8057	E	Unitized ATA 2-plus Connector
SFF-8058	E	Unitized ATA 3-in-1 Connector
SFF-8059	E	40-pin ATA Connector
SFF-8060	1.1	SFF Committee Patent Policy
SFF-8061	1.1	Emailing drawings over the SFF Reflector
SFF-8062		Rolling Calendar of SSWGs and Plenaries
SFF-8065	C	40-pin SCA-2 Connector w/High Voltage
SFF-8066	C	80-pin SCA-2 Connector w/High Voltage
SFF-8067	2.6	40-pin SCA-2 Connector w/Bidirectional ESI
INF-8068i	1.0	Guidelines to Import Drawings into SFF Specs
SFF-8069	E	Fax-Access Instructions
INF-8070i	1.2	ATAPI for Rewritable Removable Media
SFF-8072	1.2	80-pin SCA-2 for Fibre Channel Tape Applications
SFF-8073	-	20-pin SCA-2 for GBIC Applications
SFF-8080	E	ATAPI for CD-Recordable Media
INF-8090i	5.0	ATAPI for DVD (Digital Video Data)
SFF-8101		3 Gbs and 4 Gbs Signal Characteristics

SFF-8200e	1.1	2 1/2" drive form factors (all of 82xx family)
SFF-8201e	1.3	2 1/2" drive form factor dimensions
SFF-8212e	1.2	2 1/2" drive w/SFF-8001 44-pin ATA Connector
SFF-8300e	1.1	3 1/2" drive form factors (all of 83xx family)
SFF-8301e	1.2	3 1/2" drive form factor dimensions
SFF-8302e	1.1	3 1/2" Cabled Connector locations
SFF-8332e	1.2	3 1/2" drive w/80-pin SFF-8015 SCA Connector
SFF-8337e	1.2	3 1/2" drive w/SCA-2 Connector
SFF-8342e	1.3	3 1/2" drive w/Serial Unitized Connector
INF-8350i	6.1	3 1/2" Packaged Drives
SFF-8400	C	VHDCI (Very High Density Cable Interconnect)
SFF-8410	16.1	High Speed Serial Testing for Copper Links
SFF-8411		High Speed Serial Testing for Backplanes
SFF-8412		HSS Requirements for Duplex Optical Links D
SFF-8415		HPEI (High Performance Electrical Interconnect)
SFF-8420	11.1	HSSDC-1 Shielded Connections
SFF-8421	tbd	HSSDC-2 Shielded Connections
SFF-8422	tbd	**FCI** Shielded Connections
SFF-8423	tbd	*Molex* Shielded Connections
SFF-8430	4.1	MT-RJ Duplex Optical Connections
SFF-8441	14.1	VHDCI Shielded Configurations
SFF-8451	10.1	HSS (High Speed Serial) SCA-2 Connections
SFF-8452		SCA-3 for Low Disturbance Insertion
SFF-8460		HSS Backplane Design Guidelines
SFF-8480	2.1	HSS (High Speed Serial) DB9 Connections
SFF-8500e	1.1	5 1/4" drive form factors (all of 85xx family)
SFF-8501e	1.1	5 1/4" drive form factor dimensions
SFF-8508e	1.1	5 1/4" ATAPI CD-ROM w/audio connectors
SFF-8551	3.2	5 1/4" CD Drives form factor
SFF-8572	-	5 1/4" Tape form factor
SFF-8610	C	SDX (Storage Device Architecture)

SFF document number: SFF-8053, revision 5.5

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Gigabit Interface Converter (GBIC)

Revision 5.5

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Publication History

Revision Number	Description	Date
1.0	Initial Publication of Document, Preliminary	11/29/95
1.1	Correct length dimension of module	12/01/95
2.0, 2.1	Corrections of mechanical and electrical definitions	03/25/96
3.0, 3.1	Reformatting document, adding new dimensions	07/14/96
3.2	Not published	11/20/96
3.3	Major revision.	12/13/96
3.4	Minor updates and clarifications	02/11/97
4.0	Minor revision	02/25/97
4.1	Clarifications and revisions	04/28/97
4.2	Minor editorial improvements	06/03/97
4.3	Refinements	08/22/97
4.4	Add GBIC MM/SM color coding Update jitter values and define them by reference to appropriate standards. Clarify MOD_DEF support for 6 and 7. Modified definition of MOD_DEF 1 and 2 to separate intracabinet and intercabinet connections. Included long-wave power trade-off charts. Add SONET parameters for MOD_DEF 4. Correct receptacle dimensions and drawing.	12/01/97
4.5	Final revision for GBIC document.	1/28/98

Revision Number	Description	Date
5.0	Clarifications of revision 4.5 Resolution of active copper GBIC RX_LOS Review of slider tolerancing and drawings	6/4/98
5.1	Clarifications of revision 4.5, 5.0 Improve wording of copper RX_LOS Improve wording of all RX_LOS chattering (change bars for both 5.0 and 5.1) Typos	7/4/98
5.1a	Minor corrections to receive power budgets Preparation for SFF proposal	1/12/99
5.2	Minor adjustment of description of DB-9 GBIC dimensions Update of long-wave single-mode Ethernet compatible GBIC transmitted power curves. Update Ethernet requirements for Ethernet compatible shortwave GBIC. Correct connector reference part number.	3/18/99
5.3	Update of long-wave single-mode Ethernet compatible GBIC transmitted power curves to have a k factor of 0.5 Define new parameter in serial identification string to specify compliance with one or more pre-defined MOD_DEF requirements. Change jitter specification to obtain values from MJS and similar standard documents. Includes minor changes in section 2, section 4.2, tables 5 and 6, and each annex.	6/28/99
5.4	Correct reserved bit definition, Table D.3	8/16/99
5.5	Annex B - indicates that GBIC external interface is not the same as the intra-cabinet FC standard. 5.3.8 - clarify that RX_LOS is not consistent enough to be used for binary signaling on the link. Annex D - include serial ID parameters required to support SFP. 1 - Scope is modified to include non-GBIC devices with GBIC compatible controls such as SFP.	9/27/00

Table of Contents

Foreword

AMP Incorporated, Compaq Computers, Sun Microsystems, and Vixel Corporation have created a design for a serial transceiver module. The module provides a single very small form factor for a wide variety of standard Fibre Channel connectors and transmission media. The module can be inserted in or removed from a host or switch chassis without powering off the receiving socket. Any copper and optical transmission technologies consistent with the form factor may be used.

AMP Incorporated, Compaq Computers, Sun Microsystems, and Vixel Corporation expect that this design will prove useful to the disk drive, computer system, networking, and communications industries and will make the design available to interested companies.

The document is considered stable and suitable as a design specification. The status of each section of the document is shown in table 1.

Table 1: Status of document sections

Chapter/ Annex	Title	Status
1	Scope	Stable, suitable for design specification
2	Applicable Documents	Stable, suitable for design specification
3	Introduction and Overview	Stable, suitable for design specification
4	Electronic Specification for All GBICs	Stable, suitable for design specification
5	Operational Description	Stable, suitable for design specification
6	Mechanical interface for all GBICs	Stable, suitable for design specification
7	Environmental Requirements for all GBICs	Stable, suitable for design specification
Annex	Module definition 1 (copper DB-9)	Stable, suitable for design specification
Annex B	Module definition 2 (copper HSSDC)	Stable, suitable for design specification
Annex C	Module definition 3 (single mode laser)	Stable, suitable for design specification
Annex	Module definition 4 (Serial Identification)	Stable, suitable for design specification
Annex E	Module definition 5 (short wave laser, FC)	Stable, suitable for design specification
Annex F	Module definition 6 (single mode laser, FC and Ethernet)	Stable, suitable for design specification
Annex G	Module definition 7 (short wave laser, FC and Ethernet)	Stable, suitable for design specification

Gigabit Interface Converter (GBIC)

1 Scope

This document defines the electronic, electrical, and physical interfaces of a removable serial transceiver module designed to provide gigabaud capability for Fibre Channel (FC) and other protocols that use the same physical layer. The contents of this document represent a cooperative design effort among AMP, Inc., Compaq Computer Corporation, Sun Microsystems Computer Company, and Vixel Corporation.

Revision 5.5 is expanded to define the control and management interfaces for new devices designed to provide the same control and managment capability as a standard GBIC. Such devices may have form factors and data signaling rates that are not the same as a standard GBIC.

2 Applicable Documents

Fibre Channel Physical and Signaling Interface (FC-PH), X3.230:1995
Fibre Channel Physical and Signaling Interface - 2 (FC-PH-2), X3.297:1997
Fibre Channel Physical and Signaling Interface - 3 (FC-PH-3), X3.303:1998
Fibre Channel Low Cost 10 km Optical 1063 MBaud Interface (100-SM-LC-L),
NCITS T11.2 Project 1300D, Revision 3, (June, 1998)
Fibre Channel - Methodologies for Jitter Specification, (FC-MJS)
draft proposed Technical Report, Project 1230-DT, Revision 10
Safety of laser products - Part 1: Equipment classification requirements and user's guide,
IEC 825-1
Supplement to Carrier Sense Multiple Access with Collision Detection (CMSA/CD)
"Access Method & Physical Layer Specifications:
Media Access Control (MAC) Parameters, Physical Layer, repeater and Management
Parameters for 1000 Mb/s Operation", IEEE *DRAFT* P802.3z/D1, Clause 38.
Title 21, Code of Federal Regulations, Chapter I, Subchapter J (CDRH)

3 Introduction and overview

This document describes the Gigabit Interface Converter (GBIC). Although originally designed for Fibre Channel implementations using the Fibre Channel Arbitrated Loop (FC-AL), the design is practical for point-to-point Fibre Channel implementations and for other high performance serial technologies, including 1000 Mbit Ethernet. The body of the d ocument describes the mechanical and electrical properties of the GBIC and its interface with the host board. Annexes provide technical details of individual implementations of the GBIC supporting a variety of high performance serial technologies, including:

100-M5-SN-I	100 Mbyte multi-mode short wave laser without OFC
100-SM-LC-L	100 Mbyte single-mode long-wave laser with 10 km range.
100-TW-EL-S	Style 1 intraenclosure differential ECL
100-TW-EL-S	Style 2 intraenclosure differential ECL

Since the GBIC is hot pluggable, a suitably designed enclosure could be changed from one type of external interface to another simply by plugging in a GBIC having the alternative external interface.

The form factor, connectorization, and functionality of the GBIC have been selected to allow the device to be produced for a very low cost. The connector structure has been selected to allow reliable operation at 1Gbit/second. Testing at 2 Gbit/second and above has been performed and indicates that a data rate of 2.5 Gbit/second can be achieved with normal design care.

A block diagram of a typical 100-M5-SN-I GBIC is shown in figure 1.

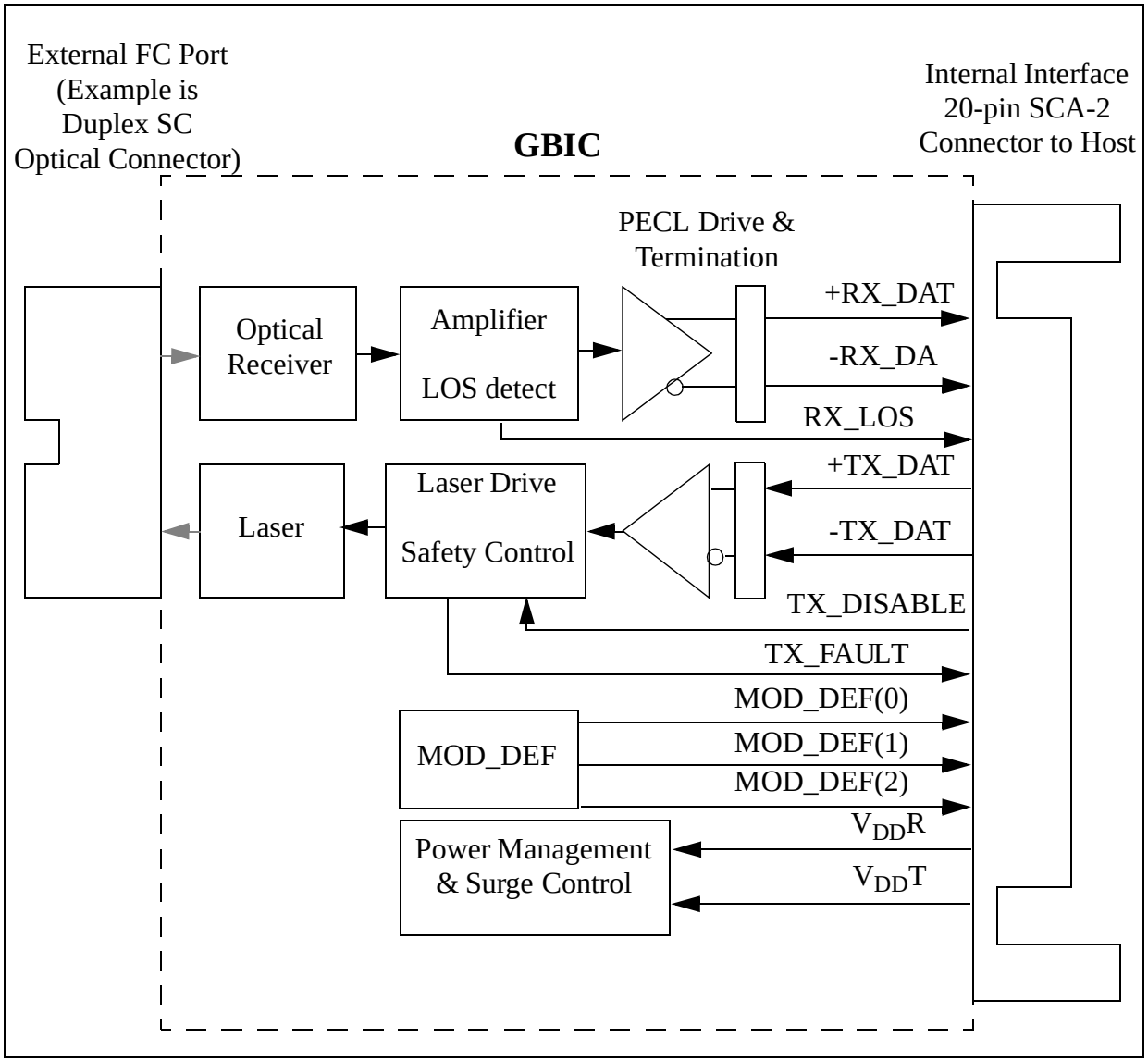


Figure 1: Functional diagram of typical shortwave laser GBIC

3.1 Connection to external Fibre Channel

The external Fibre Channel connection is selected to be appropriate for the cable plant technology selected. The dimensions provided in this document describe a standard GBIC suitable for SC fiber optic connectors and for style-2 copper connectors. The style-1 copper connectors may require the GBIC to have a larger area reserved for the connector and latches, as described in clause 6.3.

Recommendations for GBIC spacing and suggestions for reserved clearance areas around the GBIC slot are provided in clause 6.4.

3.2 Connection of GBIC to host enclosure

The connection of the GBIC to the circuit board in the host enclosure (the host board) is identical for all implementations, regardless of external media type. The mechanical form factor of the GBIC with reference to the host board is always the same. While not requiring a fixed form factor guide-rail or slot, common components are available that will suffice for most applications. Special socketing components can be built as required. Every GBIC will fit in a socket designed for any other GBIC.

The power interface includes 2 guide tabs integrated into the connector structure. The guide tabs shall be connected to circuit ground on both the host and GBIC. If the TGND and RGND pins are separated on the GBIC, one guide tab shall be connected to TGND and the other to RGND. The guide tabs shall engage before any of the connector pins. This harmlessly discharges any stray static charges and establishes a reference voltage for the voltage supplies that are sequenced later. The connector itself has two stages of contact sequencing, sequence stage 1 making contact before sequence 2 during insertion. Grounds and certain signals make contact in sequence stage 1. Power makes contact in stage 2.

Chassis grounds and external electromagnetic interference shields should not be attached to circuit ground.

The control interface provides controls for the transmitter, monitors for the transmitter and receiver, and identification information indicating the GBIC module definition. These signals are level compatible with TTL as shown in table 7.

The serial transfer interface uses 150 Ohm differential PECL signaling that is AC coupled.

The GBIC uses a 20-pin connector to the host circuit board. The pin assignments are shown in table 2.

Table 2: GBIC to host connector pin assignment

Pin Name	Pin #	Sequence	Sequence	Pin #	Pin Name
RX_LOS	1	2	1	11	RGND
RGND	2	2	1	12	-RX_DAT
RGND	3	2	1	13	+RX_DAT
MOD_DEF(0)	4	2	1	14	RGND
MOD_DEF(1)	5	2	2	15	$V_{DD}R$
MOD_DEF(2)	6	2	2	16	$V_{DD}T$
TX_DISABLE	7	2	1	17	TGND
TGND	8	2	1	18	+TX_DAT
TGND	9	2	1	19	-TX_DAT
TX_FAULT	10	2	1	20	TGND

3.3 Overview of internal interface signal functions

The electrical signals at the internal interface are defined in table 3.

Table 3: Signal Definitions

Pin Name	Pin #	Name/Function	Signal Specification
RECEIVER SIGNALS			
RGND	2, 3, 11, 14	Receiver Ground (may be connected with TGND in GBIC)	Ground, to GBIC
$V_{DD}R$	15	Receiver +5 volt (may be connected with $V_{DD}T$ in GBIC)	Power, to GBIC
-RX_DAT	12	Receive Data, Differential PECL	High speed serial, from GBIC
+RX_DAT	13	Receive Data, Differential PECL	High speed serial, from GBIC
RX_LOS	1	Receiver Loss of Signal, logic high, open collector compatible, 4.7 K to 10 K Ohm pullup to $V_{DD}T$ on host	Low speed, from GBIC
TRANSMITTER SIGNALS			
TGND	8, 9, 17, 20	Transmitter Ground (may be connected with RGND internally)	Ground, to GBIC
$V_{DD}T$	16	Transmitter +5 volt (may be connected with $V_{DD}R$ in GBIC)	Power, to GBIC
+TX_DAT	18	Transmit Data, Differential PECL	High speed serial, to GBIC
-TX_DAT	19	Transmit Data, Differential PECL	High speed serial, to GBIC
TX_DISABLE	7	Transmitter Disable, logic high, open collector compatible, 4.7 K to 10 K Ohm pullup to $V_{DD}T$ on GBIC	Low speed, to GBIC
TX_FAULT	10	Transmitter Fault, logic high, open collector compatible, 4.7 K to 10 K Oh pullup to $V_{DD}T$ on host	Low speed, from GBIC
CONTROL SIGNALS			
MOD_DEF(0)	4	GBIC module definition and presence, bit 0, 4.7 K to 10 K Ohm pullup to $V_{DD}T$ on host	Low speed, from GBIC
MOD_DEF(1)	5	GBIC module definition and presence, bit 1, 4.7 K to 10 K Ohm pullup to $V_{DD}T$ on host	Low speed, from GBIC
MOD_DEF(2)	6	GBIC module definition and presence, bit 2, 4.7 K to 10 K Ohm pullup to $V_{DD}T$ on host	Low speed, from GBIC

4 Electronic Specification for all GBICs

The electronic interface between GBICs of all module definitions and the host enclosure socket is specified in this section.

4.1 Power

Table 4: +5V Electrical Power Interface

Parameter	Symbol	Min.	Nom.	Max.	Unit	Conditions (measured at host side of connector)
Maximum voltage	$V_{DD}T$ $V_{DD}R$			6	V	Laser safety circuit shall operate from 0 to this voltage.
Operating voltage	$V_{DD}T$, $V_{DD}R$	4.75	5	5.25	V	Inclusive of ripple from 0 to 500 KHz.
Current	I			300	mA	Steady state, after t_init
Surge Current	I_{surge}			+30	mA	Hot plug, above actual steady state current

The electronic interface shall be designed to allow hot plugging into the host board without damage to the GBIC or the host board circuitry. Surge currents shall be limited using a built-in slow-start circuit and pin sequencing.

4.2 High speed serial interface electronic characteristics

The PECL transmitter and receiver characteristics have been selected so that passive circuitry can be used to meet the requirements of the intraenclosure balanced differential interface specified in FC-PH-3. For the transmitter specifications a small margin is provided for the transfers of ECL signals between the internal point b (corresponding to the SCA-2 connector between the host and the GBIC) and the external point S (corresponding to the external connector between the GBIC and the transmission cables). For the receiver specifications, sufficient margin is provided to allow the GBIC to receive signals from a driver meeting the intraenclosure specifications.

The specifications for the electrical signals transmitted to the GBIC from the host board for the high speed serial transmission circuit are shown in table 5.

Table 5: Electrical signal interface from host board, high speed serial transmitter

Parameter	Symbol	Min.	Max.	Unit	Conditions (measured at GBIC side of connector)
PECL amplitude	V_i	650	2000	mV	differential, pk-pk
PECL rise/fall		100	350	ps	20 - 80%, differential
differential skew			20	ps	

For other details of eye pattern requirements for the transmitter, see FC-PH-3.

For a Fibre Channel host transmitter, jitter output values are specified by the value δ_T,as specified in FC-MJS. For a 1000BASE host transmitter, jitter output values are specified by the value TP1 in IEEE802.3z, clause 38, table 38-10.

The specifications for the electrical signals received from the GBIC by the host board for the high speed serial receiver circuit are shown in table 6.

Table 6: Electrical signal interface to host board, high speed serial receiver

Parameter	Symbol	Min.	Max.	Unit	Conditions (measured at host side of connector)
PECL amplitude	V_o	370	2000	mV	differential, pk-pk
PECL skew			205	psec	

For other details of eye pattern requirements for the receiver, see FC-PH-3.

For a Fibre Channel host receiver, jitter tolerance values are specified by the value δ_R, as specified in FC-MJS. For a 1000BASE host receiver, jitter tolerance values are specified by the value TP4 in IEEE802.3z, clause 38, table 38-10.

The specifications for the differential line characteristic impedance of a passive copper GBIC shall meet the requirements of FC-PH-3. The exception window of 800 psec should include both the GBIC to host connector and the GBIC external connector. FC-PH-3 specifies the maximum range of characteristic impedance in the exception window to be 100 to 200 ohms.

The specifications for the differential line characteristic impedance of a GBIC with active PECL circuitry shall meet the requirements of FC-PH-3. The exception window is restricted in length to the impedance discontinuities, if any, related to the GBIC internal connector.

Impedance measurements shall be made with a 100 psec (20-80%) time domain reflectometer (TDR) as specified in FC-PH-3.

4.3 Low Speed signals, electronic characteristics

Table 7: Low speed control and sense signals, electronic characteristics

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output from GBIC	V_{OL}	0.0	0.50	V	4.7K to 10K Ohms pullup to host_Vcc, measured at host side of connector
	V_{OH}	host_Vcc - 0.5	host_Vcc + 0.3	V	
Input to GBIC	V_{IL}	0	0.8	V	4.7K to 10K Ohms to $V_{DD}T$, measured at GBIC side of connector
	V_{IH}	2.0	$V_{DD}T + 0.3$	V	

Note that host_Vcc may be either +5 volts or +3.3 volts. Hosts that support the serial module definition protocol shall use a pullup resistor connected to a host_Vcc of +5 volts (4.75 to 5.25 volts)

on the MOD_DEF_1 (SCL) and MOD_DEF_2 (SDA) signals to assure proper operation of the serial EEPROMs.

The GBIC or host may provide a TTL LOW level for a signal that has a fixed value by grounding the signal.

Total load capacitance should not exceed 100 pF.

4.4 Termination

The following figure provides examples of termination circuits for the PECL drivers and receivers in the host and the GBIC.

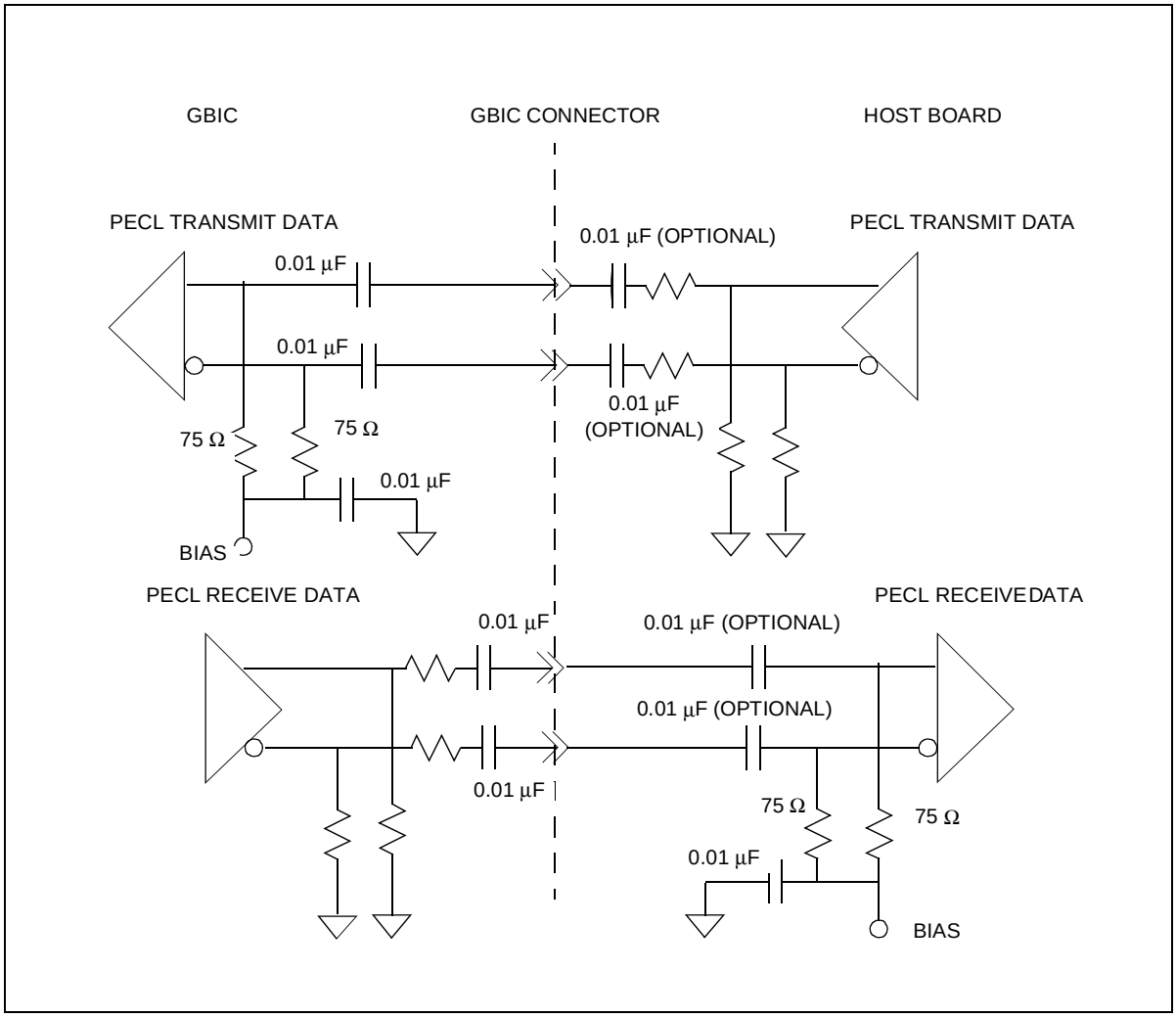


Figure 2: Termination Circuit Examples

The impedance of the terminations shall comply with FC-PH-3. Source termination is recommended for PECL drivers.

Blocking capacitors shall be provided as shown in the circuit diagrams above. Blocking capacitors are desirable, but optional, in the host board PECL circuits.

4.5 Safety requirements

For GBICs providing external optical interfaces, the manufacturer shall ensure that the optical power emitted from an open connector or fiber is compliant with IEC825-1 and CDRH during initialization procedures, during error reset procedures, during normal operation, and in the event of any reasonable single fault condition.

Any electrical power provided to the external interface shall meet applicable safety regulations, including fusing requirements.

5 Operational Description

The following descriptions of GBIC operation apply to all module definitions of GBIC.

5.1 Overview of data transfer

The GBIC is driven from the host board with serial differential PECL signals applied to +TX_DAT and -TX_DAT. The signals may drive either a transmission conversion circuit providing a standard serial output or may directly drive an intraenclosure connection compatible with FC-PH-3. The output from the transmission conversion circuit may optionally be disabled via the TX_DISABLE pin. The TX_FAULT pin indicates a failure has been detected in the transmission conversion circuit. If a safety fault occurs in the transmitter, the fault condition shall be latched and the output shall be controlled to a safe condition. The latch may be reset according to the protocol defined in clause 5.3.7. TX_FAULT shall also indicate loss of +5V power at the transmit circuit or that some pins of the GBIC to host enclosure socket are not making contact or meeting their contact resistance specifications. Those two fault conditions are not latched.

The serial receiver detects the incoming signals and amplifies and converts them as required. Output from the GBIC to the host board consists of serial differential PECL data signals on +RX_DAT and -RX_DAT, compatible with the received signal from a copper intraenclosure connection. A receiver loss of signal function on the RX_LOS pin may optionally indicate that the incoming data signal amplitude is not acceptable to achieve the specified Bit Error Rate (BER). In addition, the RX_LOS signal shall indicate loss of +5 volt power at the receiver circuit or that some pins of the GBIC to host enclosure socket are either not making contact or not meeting their contact resistance specifications. The PECL output signals may optionally be disabled when RX_LOS is active. The circuitry receiving the RX_DAT signals should not make use of the signals when the RX_LOS signal is asserted, since the data value is not guaranteed to be stable in magnitude or frequency.

The annex for each module definition indicates which of the control and status signals, TX_DISABLE, TX_FAULT, and RX_LOS, are mandatory.

5.2 GBIC module definition determination

The module definition of GBIC that is installed is indicated by the 3 module definition pins. The information about the external serial interface for each GBIC module definition is included in the appropriate annex.

The assigned values for the MOD_DEF(0:2) bits are provided below.

Table 8: MOD_DEF(0:2)

Module Definition	MOD_DEF(0) pin 4	MOD_DEF(1) pin 5	MOD_DEF(2) pin 6	Interpretation by host	Reference
0	NC	NC	NC	GBIC not present	clause 5.2
1	NC	NC	TTL LOW	Copper Style 1 or Style 2 connector, 1.0625 Gbd, 100-TW-EL- or 100-TP-EL-S, active inter-enclosure connection. and IEEE802.3 1000BASE-CX	Annex A
2	NC	TTL LO	NC	Copper Style 1 or Style 2 connector, 1.0625 Gbd, 100-TW-EL-S, or 100-TP-EL-S, active or passive intraenclosure connection	Annex B
3	NC	TTL LO	TTL LOW	Optical LW, 1.0625 Gbd 100-SM-LC-L	Annex C
4	TTL LOW	SCL	SDA	Serial module definition protocol	clause 5.2.1 Annex D
5	TTL LOW	NC	TTL LOW	Optical SW, 1.0625 Gbd 100-M5-SN-I or 100-M6-SN-I	Annex E
6	TTL LOW	TTL LO	NC	Optical LW, 1.0625 Gbd 100-SM-LC-L and similar to 1.25 Gbd IEEE802.3z 1000BASE-LX, single mode	Annex
7	TTL LOW	TTL LO	TTL LOW	Optical SW, 1.0625 Gbd 100-M5-SN-I or 100-M6-SN-I and 1.25 Gbd, IEEE 802.3z, 1000BASE-SX	Annex G

The value NC indicates that the GBIC makes no connection to the pin.

5.2.1 Serial module definition protocol

Definition 4 specifies a serial definition protocol. For this definition, upon power up, the MOD_DEF(1:2) shall appear as NC. If the host system detects definition number 4, the serial protocol may then be activated using MOD_DEF(1:2). The protocol uses the 2-wire serial CMOS E^2PROM protocol typical of theATMEL AT24C01A/02/04/08/16 family of parts.

When the serial protocol is activated, the serial clock signal (SCL) is generated by the host. The positive edge clocks data into the GBIC into those segments of the E^2PROM that are not write protected. The negative edge clocks data from the GBIC.

The serial data signal (SDA) is bidirectional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation.

The data transfer protocol and the details of the mandatory and vendor specific data structures are defined in Annex D.

5.3 GBIC management algorithms

All GBICs, regardless of module definition, shall successfully operate if the management and error recovery protocols defined in the following clauses are used. Since some GBIC functions are not implemented for some module definitions, GBICs of some module definitions may not invoke certain recovery procedures or may appear to provide instantaneous responses to host actions.

5.3.1 GBIC timing parameters

The following timing parameters (see table 9) are used in procedures defined in this section. Details that depend on the module definition are provided in the appropriate annexes.

Table 9: Timing parameters for GBIC management

Parameter	Symbol	Min.	Max.	Unit	Conditions
TX_DISABLE assert time	t_off		10	µsec	rising edge of TX_DISABLE to fall of output signal below 10% of nominal
TX_DISABLE negate time	t_on		1	msec	Falling edge of TX_DISABLE to rise of output signal above 90% of nominal
Time to initialize, includes reset of TX_FAULT	t_init		300	msec	From power on or hot plug after $V_{DD}T > 4.75$ volts or From negation of TX_DISABLE during reset of TX_FAULT.
TX_FAULT from fault to assertion	t_fault		100	µsec	From occurrence of fault (output safety violation or $_{DD}T <$ 4.5 volts)
TX_DISABLE time to start reset	t_reset	10		µsec	TX_DISABLE HIGH before TX_DISABLE set LOW
RX_LOS assert delay	t_loss_on		100	µsec	From detection of loss of signal to assertion of RX_LOS
RX_LOS negate delay	t_loss_off		100	µsec	From detection of presence of signal to negation of RX_LOS

5.3.2 GBIC power on initialization procedure, TX_DISABLE negated.

During power on of the GBIC, TX_FAULT, if implemented, may be asserted (High) as soon as power supply voltages are within specification. For GBIC initialization with TX_DISABLE negated, TX_FAULT shall be negated when the transmitter safety circuitry, if implemented, has detected that the transmitter is operating in its normal state. If a transmitter fault has not occurred, TX_FAULT shall be negated within a period t_init from the time that $V_{DD}T$ exceeds the specified minimum operating voltage (see table 4). If TX_FAULT remains asserted beyond the period t_init, the host may assume that a transmission fault has been detected by the GBIC.

If no transmitter safety circuitry is implemented, the TX_FAULT signal may be tied to its negated state.

The power on initialization timing for a GBIC with TX_DISABLE negated is shown in figure 3.

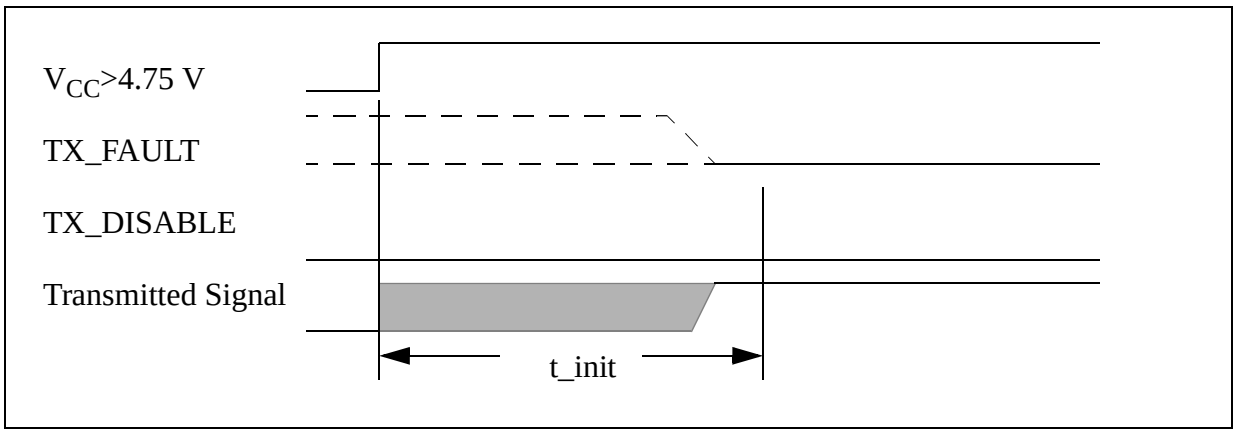


Figure 3: Power on initialization of GBIC, TX_DISABLE negated

5.3.3 GBIC power on initialization procedure, TX_DISABLE asserted.

For GBIC power on initialization with TX_DISABLE asserted, the state of TX_FAULT is not defined while TX_DISABLE is asserted. After TX_DISABLE is negated, TX_FAULT may be asserted while safety circuit initialization is performed. TX_FAULT shall be negated when the transmitter safety circuitry, if implemented, has detected that the transmitter is operating in its normal state. If a transmitter fault has not occurred, TX_FAULT shall be negated within a period t_init from the time that TX_DISABLE is negated. If TX_FAULT remains asserted beyond the period t_init, the host may assume that a transmission fault has been detected by the GBIC.

If no transmitter safety circuitry is implemented, the TX_FAULT signal may be tied to its negated state.

The power on initialization timing for a GBIC with TX_DISABLE asserted is shown in figure 4.

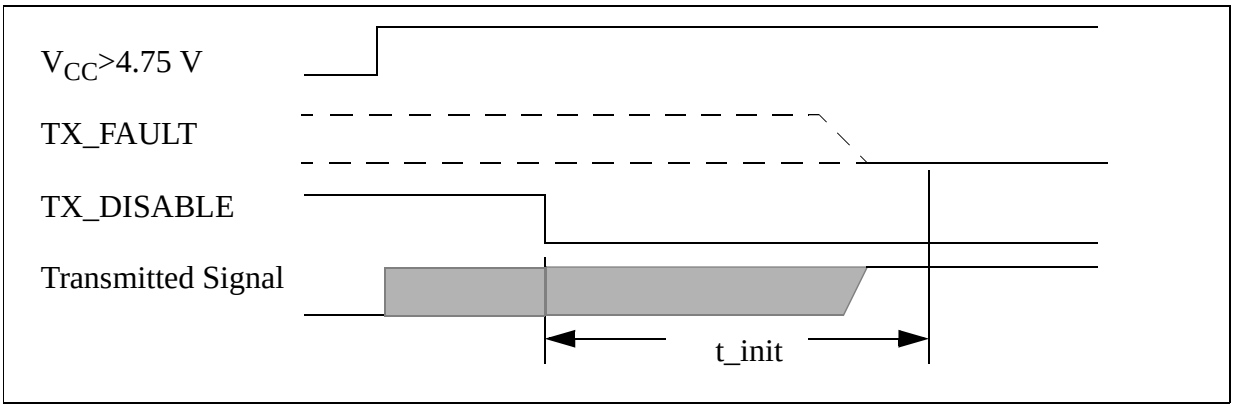


Figure 4: Power on initialization of GBIC, TX_DISABLE asserted

Note that the management of the transmit signal by TX_DISABLE is not required for GBICs of some module definitions, so that the transmitted signal may appear while TX_DISABLE is asserted.

5.3.4 Initialization during hot plugging of GBIC.

When a GBIC is not installed, TX_FAULTis held to the asserted state by the pull up circuits on the host (see table 3). As the GBIC is installed, contact is made with the ground, voltage, and signal contacts in the specified order. After the GBIC has determined that V_{DD}T has reached the specified value, the power on initialization takes place as described in clause 5.3.2 and clause 5.3.3.

An example of initialization during hot plugging is provided in figure 5.

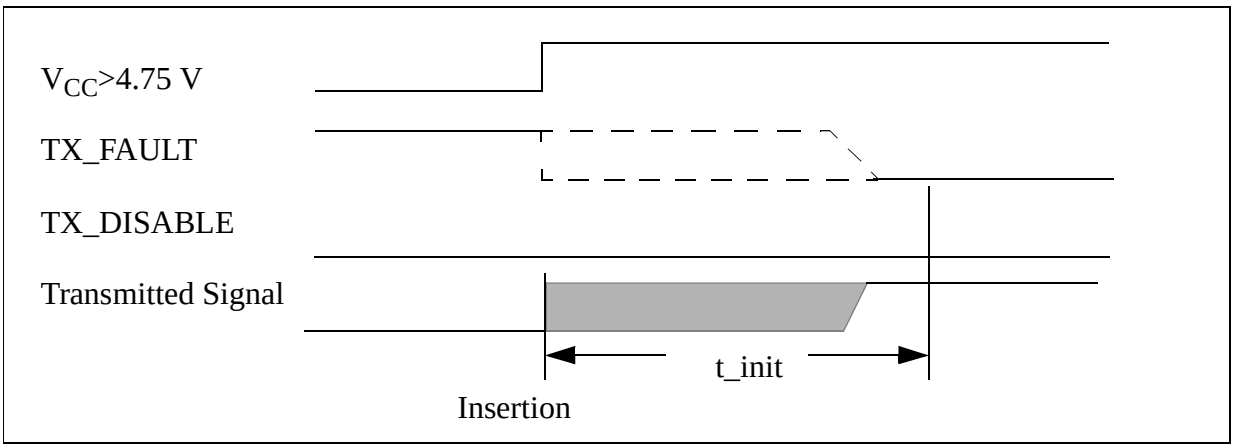


Figure 5: Example of initialization during hot plugging, TX_DISABLE negated.

5.3.5 GBIC transmitter management

If implemented, the TX_DISABLE may be asserted to disable the transmitter for diagnostic, configuration, or security purposes. Since control of the transmit signal by TX_DISABLE is not

required for all module definitions, the software managing the GBIC transmitter must consider the MOD_DEF value to determine how the interface will respond when TX_DISABLE is asserted.

The timing requirements for the management of optical outputs from the GBIC using the TX_DISABLE signal are shown in figure 6. Implementation of the TX_DISABLE signal is required for module definitions that use TX_DISABLE to clear a latched TX_FAULT condition and is optional for other module definitions unless specifically required by the appropriate annex.

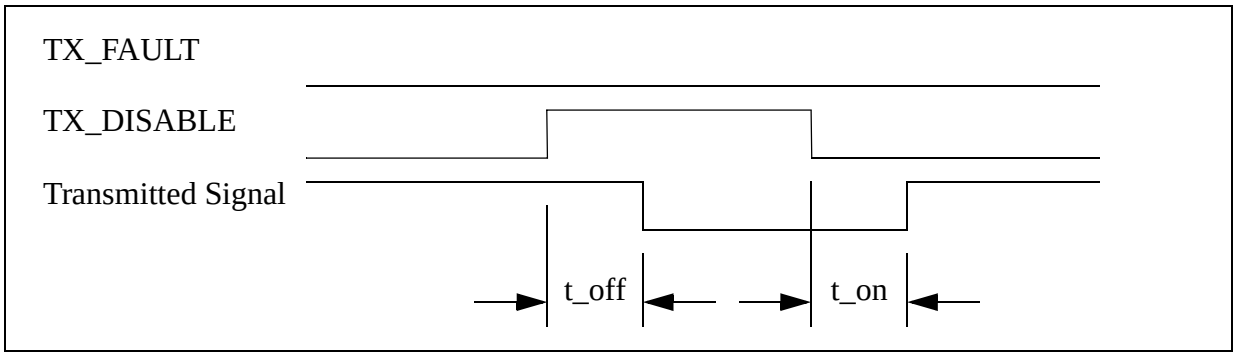


Figure 6: Management of GBIC during normal operation, TX_DISABLE implemented

5.3.6 GBIC fault detection and presentation

TX_FAULT shall be implemented by those module definitions of GBIC supporting safety circuitry. If TX_FAULT is not implemented, the signal shall be held to the low state by the GBIC.

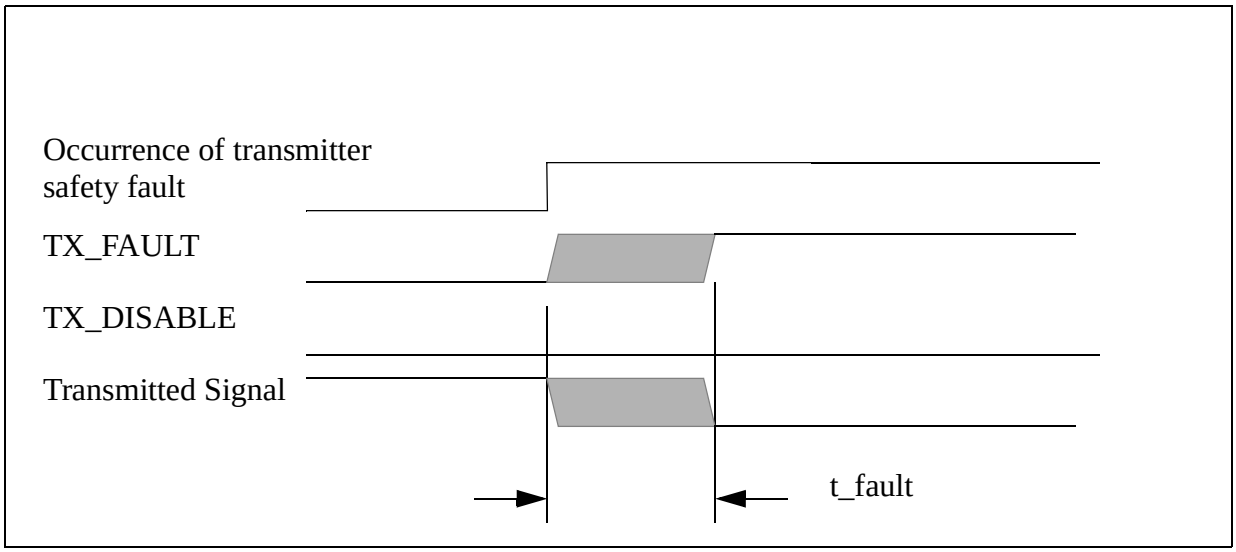


Figure 7: Detection of transmitter safety fault condition

5.3.7 GBIC fault recovery

The detection of a safety-related transmitter fault condition presented by TX_FAULT shall be latched. The following protocol may be used to reset thelatch in case the transmitter fault condition is transient.

To reset the fault condition and associated detection circuitry, TX_DISABLE shall be asserted for a minimum of t_reset. TX_DISABLE shall then be negated. In less than the maximum value of t_init the optical transmitter will correctly reinitialize the laser circuits, negate TX_FAULT, and begin normal operation if the fault condition is no longer present. If a fault condition is detected during the reinitialization, TX_FAULT shall again be asserted, the fault condition again latched, and the optical transmitter circuitry will again be disabled until the next time a reset protocol is attempted. The manufacturer of the GBIC shall ensure that the optical power emitted from an open connector or fiber is compliant with IEC825-1 and CDRH during all reset attempts, during normal operation or upon the occurrence of reasonable single fault conditions. The GBIC may require internal protective circuitry to prevent the frequent assertion of the TX_DISABLE signal from generating frequent pulses of energy that violate the safety requirements. The timing forsuccessful recovery from a transient safety fault condition is shown in figure 8.

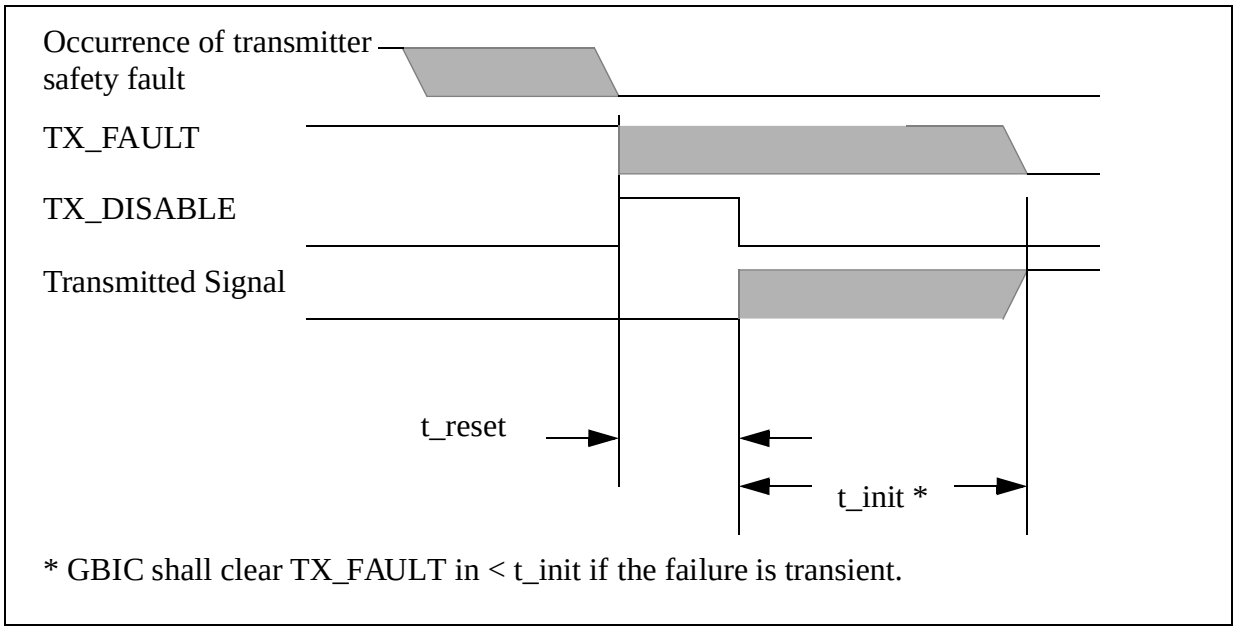


Figure 8: Successful recovery from transient safety fault condition

An example of an unsuccessful recovery, where the fault condition was not transient, is shown in figure 9.

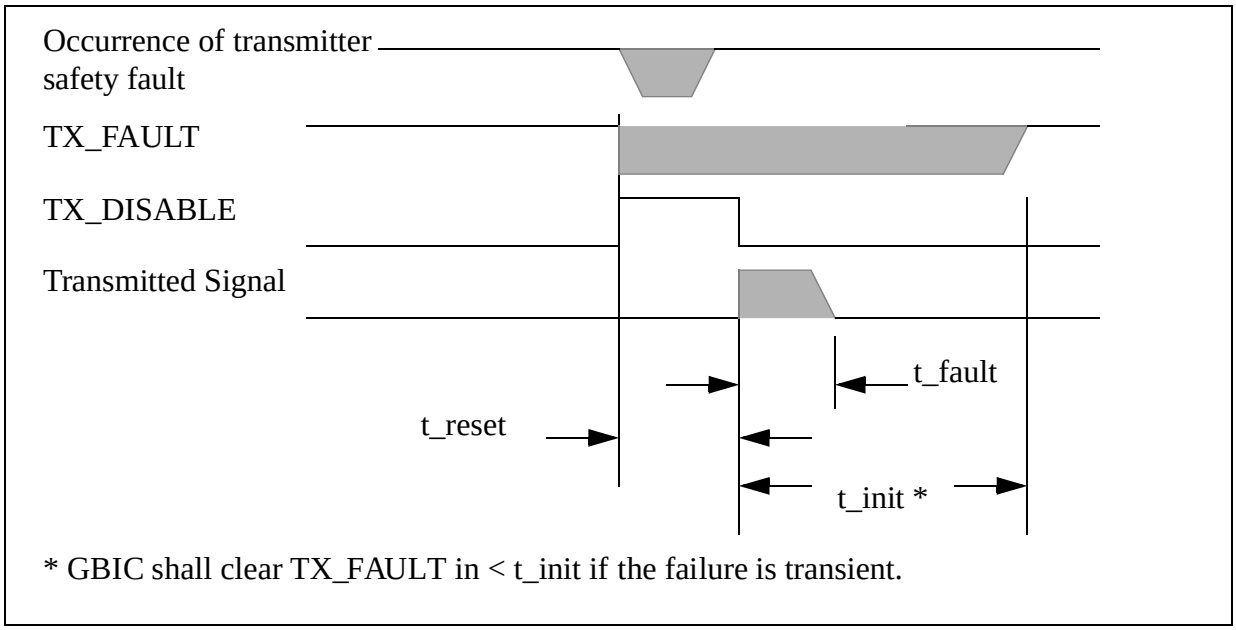


Figure 9: Unsuccessful recovery from safety fault condition

5.3.8 GBIC loss of signal indication

The RX_LOS signal is intended as a preliminary indication to the system in which the GBIC is installed that the link signals are likely to be outside the required values for proper operation. Such indications typically point to non-installed cables, broken cables, or a disabled, failing or powered off transmitter at the far end of the cable. Additional indications are provided by the system in which the GBIC is installed to verify that the information being transmitted is valid, correctly encoded, and in the correct format. Such additional indications are outside the scope of the GBIC specification.

The signal levels that create RX_LOS and the timing of RX_LOS assertion and negation are not precise enough to be used for low-frequency binary signaling on the link.

If RX_LOS is not implemented on a GBIC, it shall be held to the low state by the GBIC. If the module definition of the GBIC is specified as implementing RX_LOS, the timing is specified in figure 10.

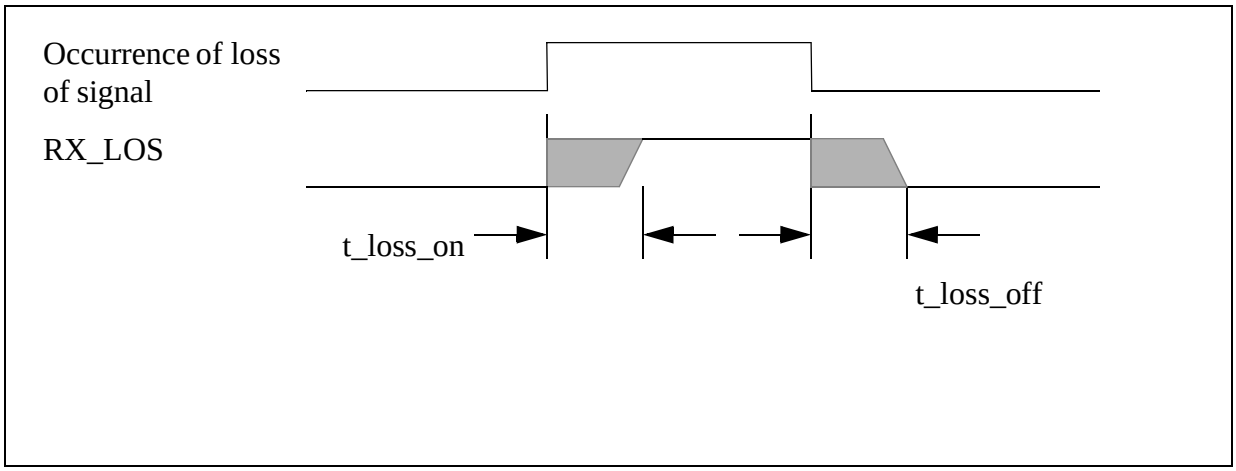


Figure 10: Timing of RX_LOS detection

6 Mechanical interface for all GBICs

A common mechanical outline is used for all GBICs. The outline of the GBIC is described in figure 11 and table 10.

Table 10: Dimension table for drawing of GBIC

Designator	Dimension (mm)	Tolerance (mm)	Comments
A	57.15	+0.25 -0.25	GBIC length from stop to end of connector
B	10.00	+0.10 -0.15	GBIC height- main body
C	12.01	+0.00 -0.15	GBIC height- overall
D	8.18	Reference	SC connector beyond stop
E	3.05	+0.00 -0.15	Latch arm height
F	30.48	+0.00 -0.15	GBIC width- main body
G	0.91	Basic	Center line of latch
H	33.91	Maximum	Latch release tabs, installed position
J	31.50	+0.00 -0.15	Latch arm and retention recess width, installed position
K	33.27	+0.10 -0.10	Latch retention detail width, installed position
	31.45	Maximum	Latch retention detail width, during compression while being inserted/removed
	35	Maximum	Latch retention detail width, uninstalled position
L	14.5	Maximum	Latch arm length
M	4.34	Maximum	Latch retention detail length
N	1.17	+0.10 -0.00	Retention detail to stop
P	0.40	Maximum	Retention recess to stop
Q	1.52	+0.10 -0.00	Guide slot height
R	3.05	Basic	Guide slot centerline
S	13.56	Maximum	Guide slot length - to stop
T	27.69	+0.15 -0.15	Guide slot width (depth)
U	5.08	Minimum	Chassis ground contact zone
V		Reference	

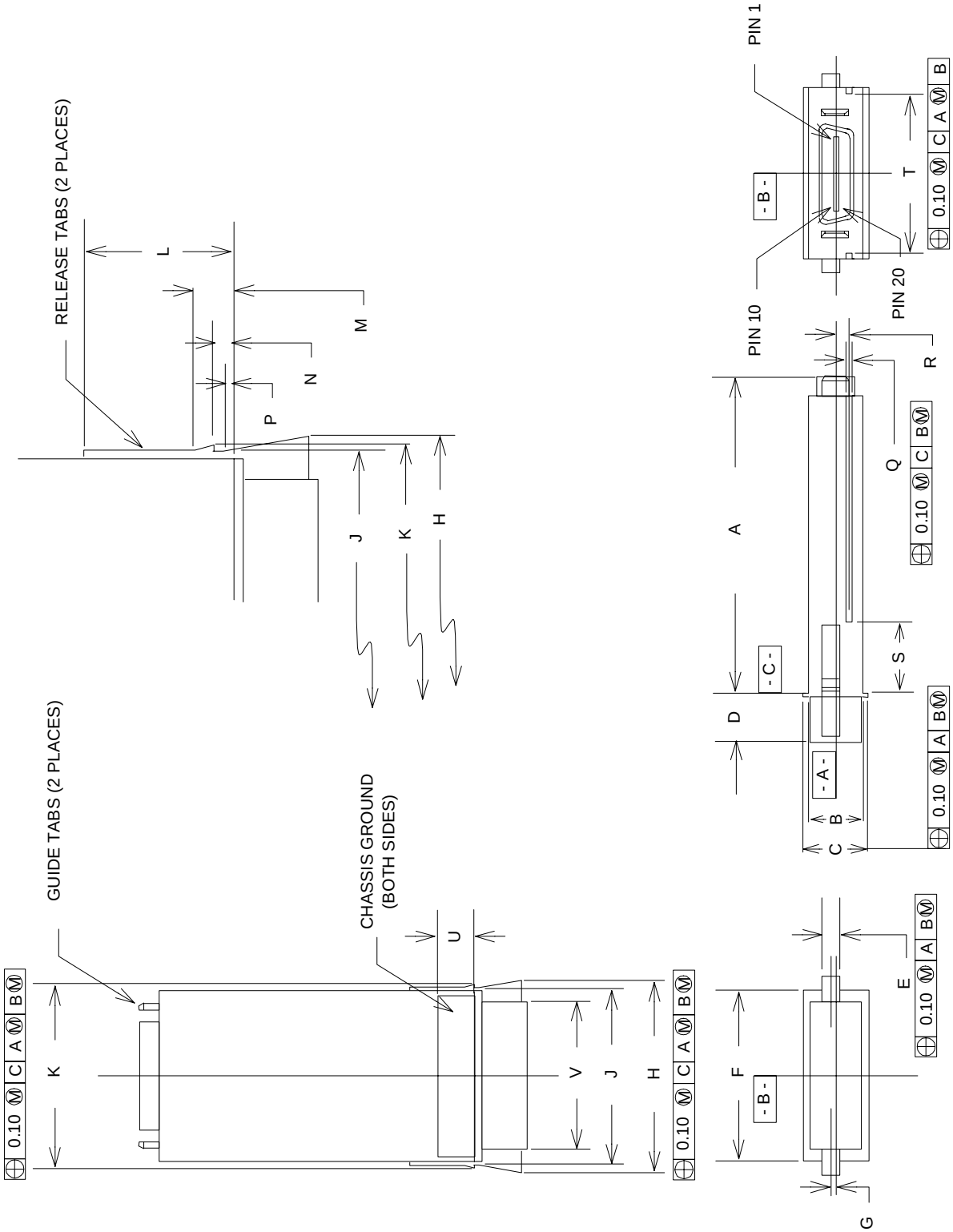
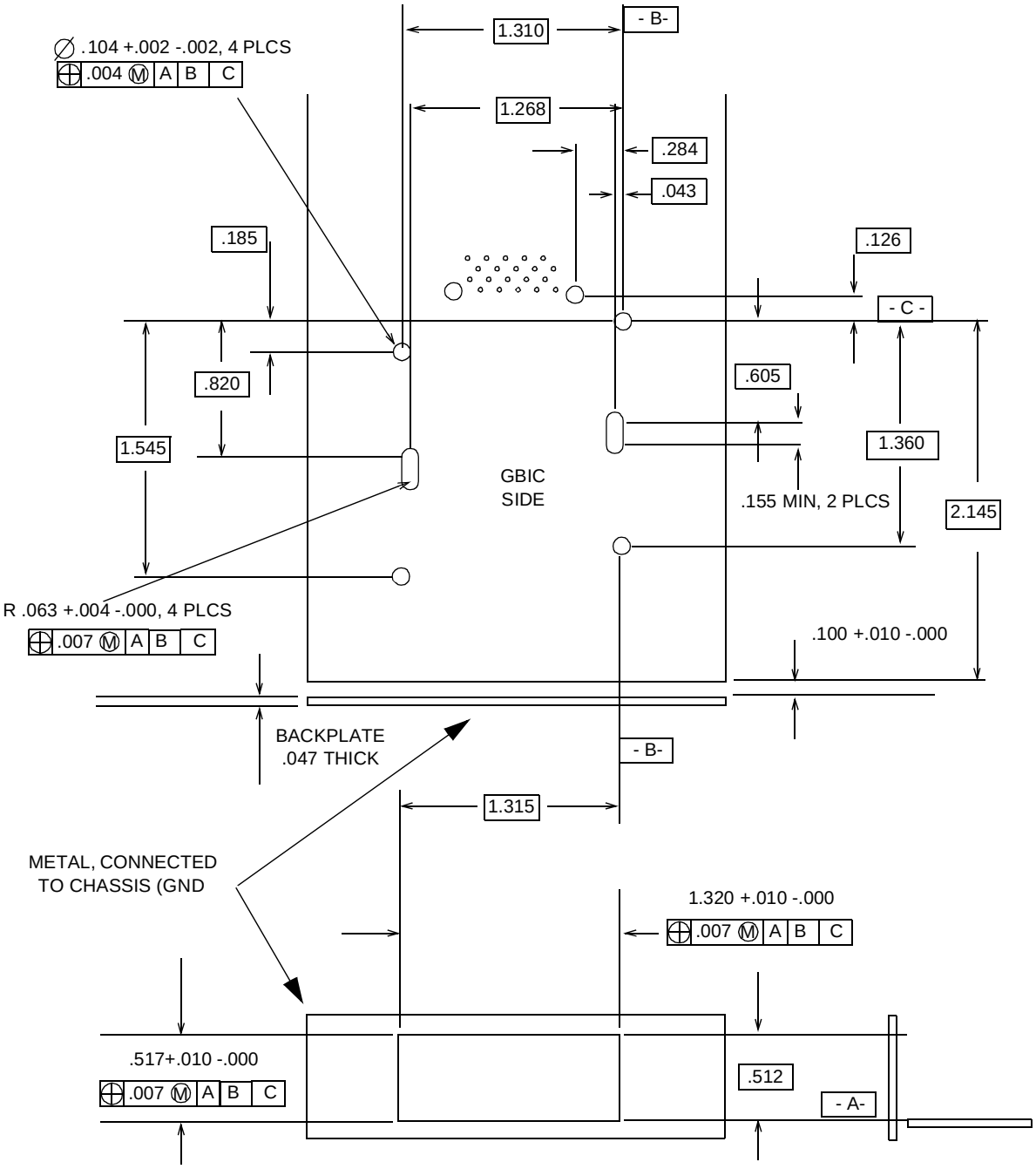


Figure 11: Drawing of GBIC

A typical host board mechanical layout for attaching a typical guide-rail and connector to receive a GBIC is shown in figure 12. Dimensions in this figure are in inches.



NOTE: REFERENCE ONLY: SEE RECOMMENDED LAYOUT FROM GUIDE-RAIL AND CONNECTOR MANUFACTURERS.

Figure 12: Typical Host Card Footprint

6.1 Insertion and removal

The requirements for insertion forces, extraction forces, and retention forces are specified in table 11.

Table 11: Insertion, extraction, and retention forces

Measurement	Minimum	Maximum	Units	Comments
GBIC insertion	0	20	newtons	(~4.5 lbs)
GBIC extraction	0	15	newtons	(~3.3 lbs)
GBIC retention	130	N/A	newtons	straight out (~29.3 lbs)
Insertion/removal cycles	100		cycles	

6.2 Labeling requirements

Color coding requirements for optical GBICs are specified in the appropriate annex.

Each GBIC should be clearly labeled. The complete labeling need not be visible when the GBIC is installed. Labeling should include appropriate manufacturing and part number identification, appropriate regulatory compliance labeling, and a clear specification of the external port characteristics. The external port characteristic label may include such information as optical wavelength, required fiber characteristics, operating data rate, interface standards supported, and link length supported.

6.3 Special mechanical information for GBICs with MOD_DEF 1 or 2

GBICs with style 1 copper connectors are slightly larger than the standard GBIC size. The maximum size envelope for MOD_DEF 1 and MOD_DEF 2 GBICs using the style 1 copper connector is shown in figure 13. Some style 1 GBICs may not be usable in systems that do not make provision for the larger GBIC envelope.

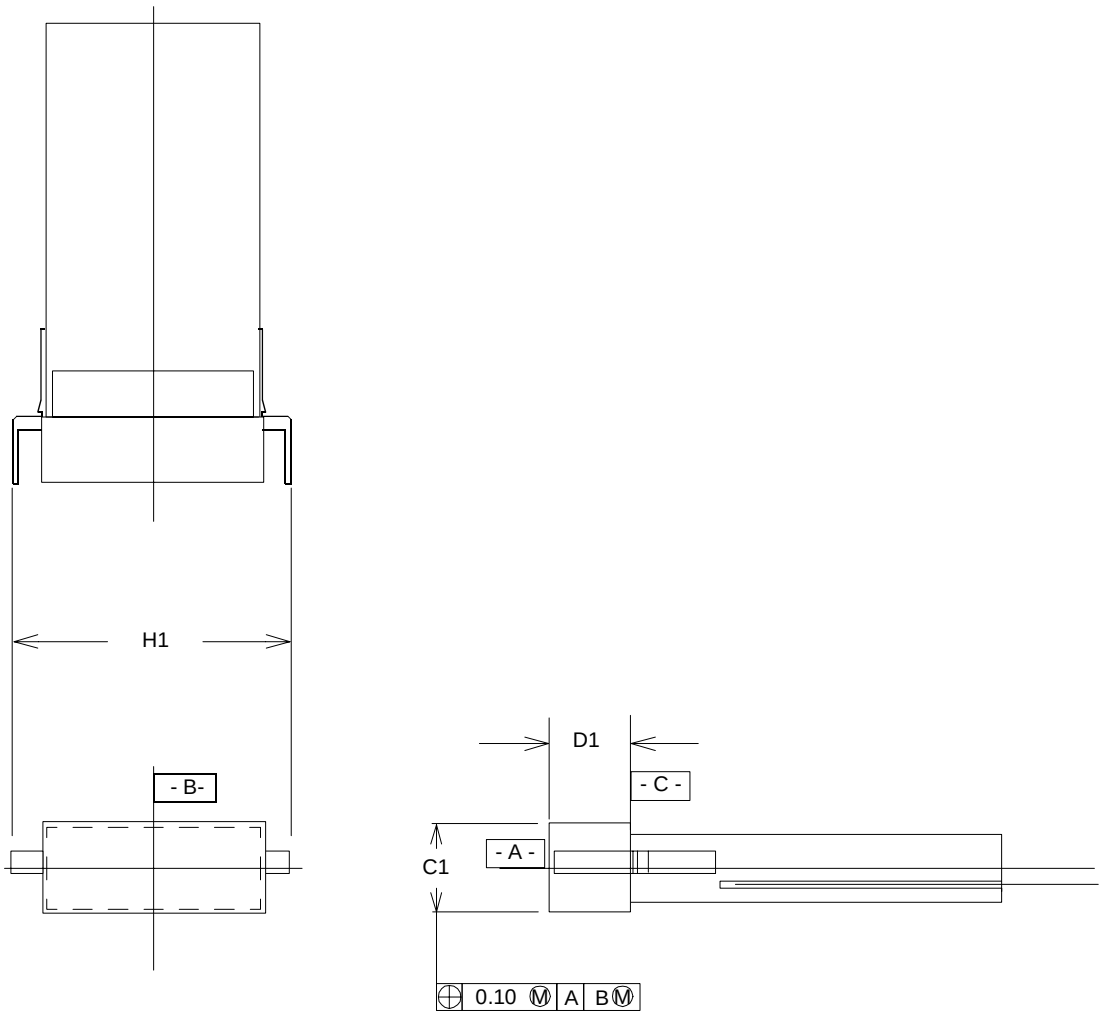


Figure 13: Drawing of Style-1 copper connector GBIC envelope

Table 12: Dimension table for drawing of Style-1 copper connector GBIC envelope

Designator	Dimension (mm)	Tolerance (mm)	Comments
C_1	14.00	maximum	GBIC height- overall
D_1	24.80	Reference	SC connector beyond stop
H_1	37.60	Maximum	Latch release tabs, installed position

6.4 Mechanical considerations for systems using GBICs

Host enclosures that use GBICs should provide appropriate clearances between GBICs to allow insertion and extraction without special tools. Formost systems, a center-line to center-line distance greater than 1.5” (38.1 mm) usually provides sufficient separation for access.

The GBIC insertion slot should be clear of nearby moldings and covers which might block convenient access to the latching mechanisms, the GBIC, or the cables connected to the GBIC.

6.5 Connector definition

The connector used by the GBIC is a 20-pin model of the AMP SCA-2 connector. The following AMP part numbers are given for reference purposes, but any licensed manufacturer of the connector may produce similar components.

Straddle mount male plug, placed on GBIC:

AMP 84598-1

Vertical receptacle, placed on backplane for connection of a GBIC perpendicular to surface of backplane.

AMP 787646-1

Right angle receptacle, placed on motherboard for connection of a GBIC parallel to surface of backplane as a daughter board.

AMP 787653-1

GBIC guide systems are presently being used by many applications. It is expected that those guide systems will be offered by a number of vendors. The following AMP part numbers are given for reference purposes.

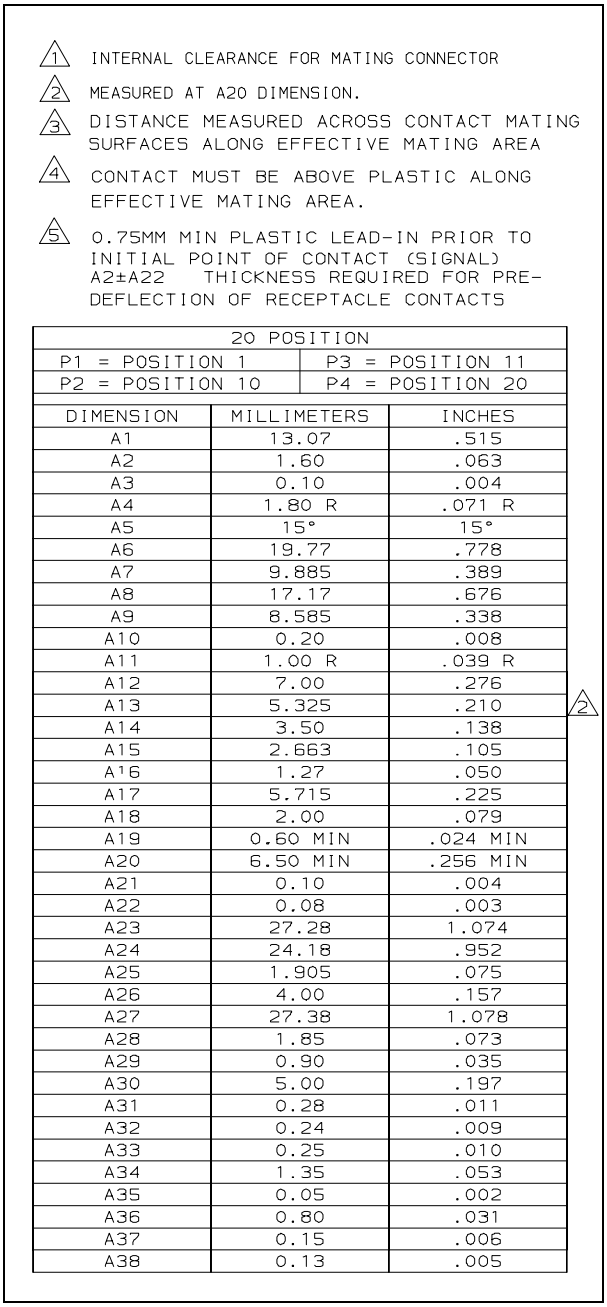
GBIC guide system for PCB with thickness 0.062 +/- 0.008 inches

AMP 787663-3

GBIC guide system for PCB with thickness 0.100 +/- 0.008 inches

AMP 787663-4

A reference drawing describing the GBIC plug is provided in table 13 and figure 14.



1. INTERNAL CLEARANCE FOR MATING CONNECTOR
2. MEASURED AT A20 DIMENSION.
3. DISTANCE MEASURED ACROSS CONTACT MATING SURFACES ALONG EFFECTIVE MATING AREA
4. CONTACT MUST BE ABOVE PLASTIC ALONG EFFECTIVE MATING AREA.
5. 0.75MM MIN PLASTIC LEAD-IN PRIOR TO INITIAL POINT OF CONTACT (SIGNAL) A2±A22 THICKNESS REQUIRED FOR PRE-DEFLECTION OF RECEPTACLE CONTACTS

20 POSITION	
P1 = POSITION 1	P3 = POSITION 11
P2 = POSITION 10	P4 = POSITION 20

DIMENSION	MILLIMETERS	INCHES	
A1	13.07	.515	
A2	1.60	.063	
A3	0.10	.004	
A4	1.80 R	.071 R	
A5	15°	15°	
A6	19.77	.778	
A7	9.885	.389	
A8	17.17	.676	
A9	8.585	.338	
A10	0.20	.008	
A11	1.00 R	.039 R	
A12	7.00	.276	
A13	5.325	.210	2
A14	3.50	.138	
A15	2.663	.105	
A16	1.27	.050	
A17	5.715	.225	
A18	2.00	.079	
A19	0.60 MIN	.024 MIN	
A20	6.50 MIN	.256 MIN	
A21	0.10	.004	
A22	0.08	.003	
A23	27.28	1.074	
A24	24.18	.952	
A25	1.905	.075	
A26	4.00	.157	
A27	27.38	1.078	
A28	1.85	.073	
A29	0.90	.035	
A30	5.00	.197	
A31	0.28	.011	
A32	0.24	.009	
A33	0.25	.010	
A34	1.35	.053	
A35	0.05	.002	
A36	0.80	.031	
A37	0.15	.006	
A38	0.13	.005	

Table 13: Value of dimensions for GBIC plug reference drawing

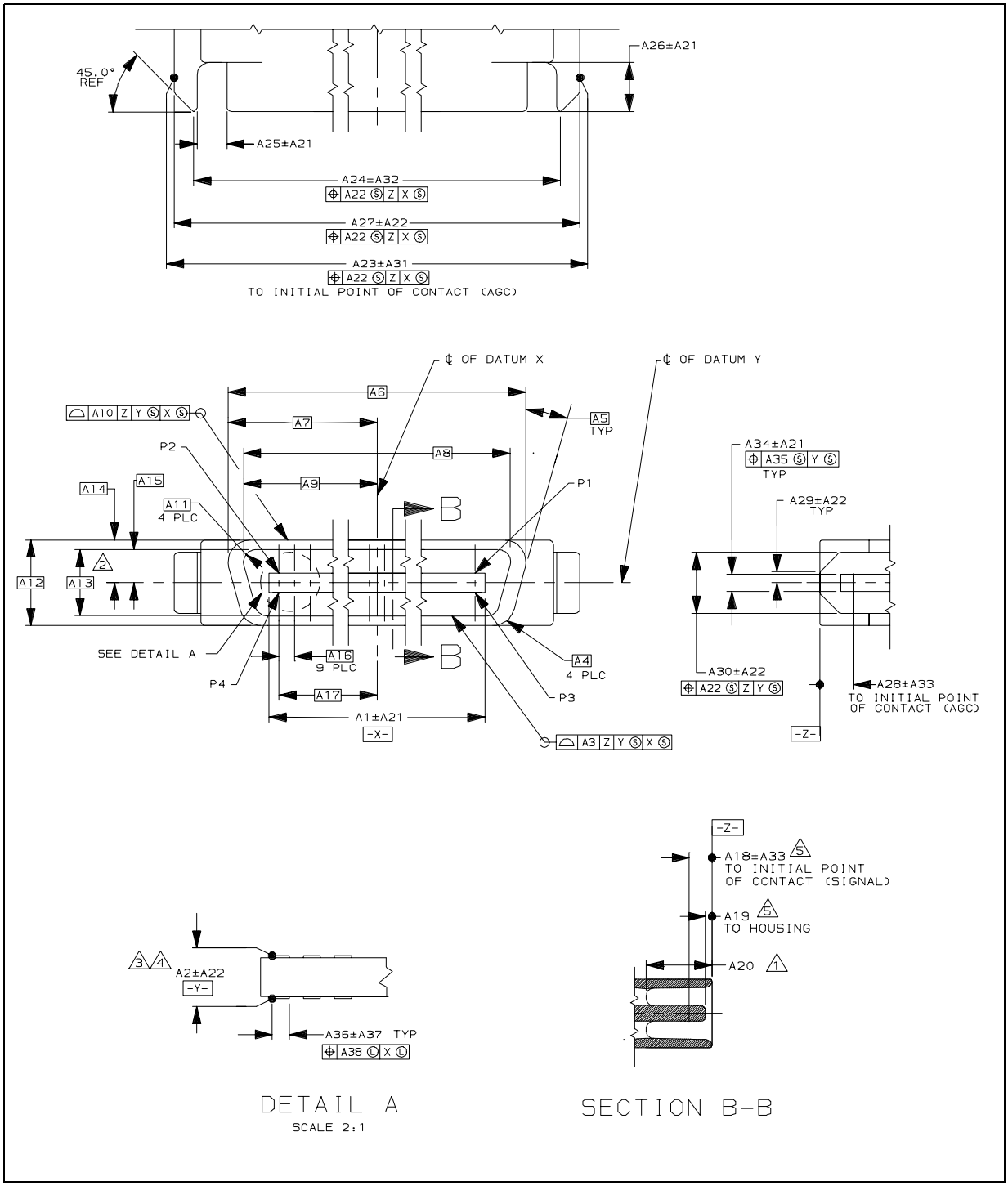
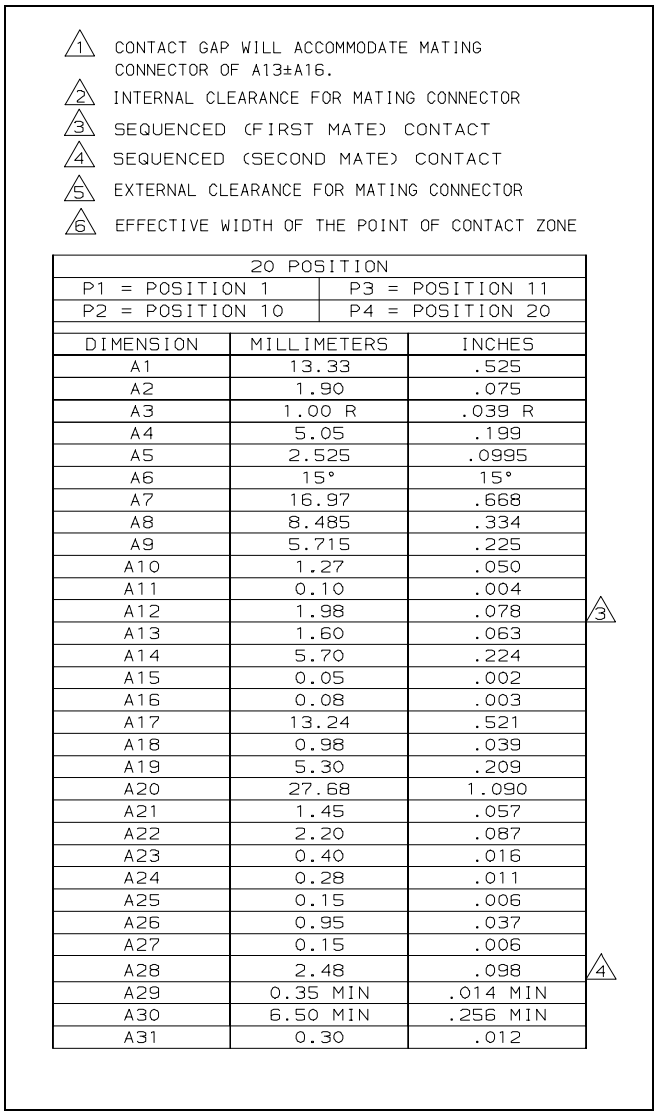


Figure 14: Reference drawing for GBIC plug

A reference drawing describing the GBIC receptacle is provided in table 14 and figure 15.



1. CONTACT GAP WILL ACCOMMODATE MATING CONNECTOR OF A13±A16.
2. INTERNAL CLEARANCE FOR MATING CONNECTOR
3. SEQUENCED (FIRST MATE) CONTACT
4. SEQUENCED (SECOND MATE) CONTACT
5. EXTERNAL CLEARANCE FOR MATING CONNECTOR
6. EFFECTIVE WIDTH OF THE POINT OF CONTACT ZONE

20 POSITION	
P1 = POSITION 1	P3 = POSITION 11
P2 = POSITION 10	P4 = POSITION 20

DIMENSION	MILLIMETERS	INCHES	
A1	13.33	.525	
A2	1.90	.075	
A3	1.00 R	.039 R	
A4	5.05	.199	
A5	2.525	.0995	
A6	15°	15°	
A7	16.97	.668	
A8	8.485	.334	
A9	5.715	.225	
A10	1.27	.050	
A11	0.10	.004	
A12	1.98	.078	3
A13	1.60	.063	
A14	5.70	.224	
A15	0.05	.002	
A16	0.08	.003	
A17	13.24	.521	
A18	0.98	.039	
A19	5.30	.209	
A20	27.68	1.090	
A21	1.45	.057	
A22	2.20	.087	
A23	0.40	.016	
A24	0.28	.011	
A25	0.15	.006	
A26	0.95	.037	
A27	0.15	.006	
A28	2.48	.098	4
A29	0.35 MIN	.014 MIN	
A30	6.50 MIN	.256 MIN	
A31	0.30	.012	

Table 14: Value of dimensions for GBIC receptacle reference drawing

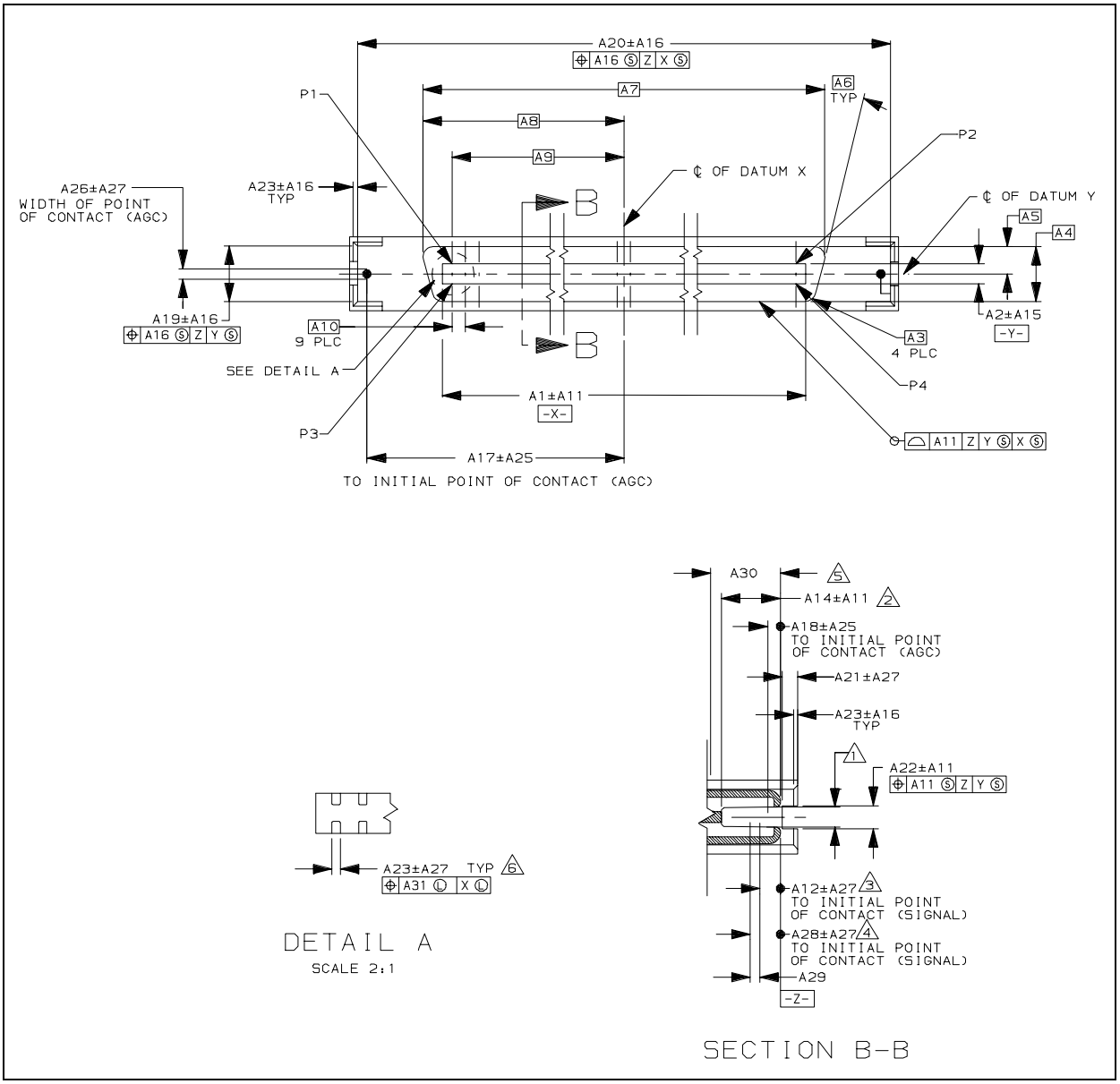


Figure 15: Reference drawing for GBIC receptacle

7 Environmental Requirements for all GBICs

The environmental requirements for all GBICs are specified in this section. All GBICs should meet their mechanical, electronic, optical, and timing specifications for all specified environments.

7.1 Temperatur

The specifications shall apply for operating temperatures from 0 to 50°C in moving air. More or less restrictive temperature ranges may be specified as required. Cooling shall be provided as appropriate.

Annex A: Module definition “1” GBIC (copper inter-enclosure)

(normative annex)

A.1 Overview of module definition 1 GBIC

A GBIC having module definition 1 presents a standard copper interface having the same characteristics as the Fibre Channel 100-TP-EL-S and 100-TW-EL-Sinter-enclosure interface using the style 1 or style 2 balanced cable connector. This GBIC is also compatible with the Gigabit Ethernet definition IEEE802.3, 1000BASE-CX. The transmitter and receiver specifications for the inter-enclosure interface will usually require additional electronic buffering to adapt the PECL signals available on the host side of the GBIC to the inter- enclosure requirements. The copper transmitter and receiver specification is defined by FC-PH-3. An overview of the copper Fibre Channel characteristics is provided in table A.1.

Table A.1: Overview, module definition 1 GBIC

Parameter	Value
Application	Fibre Channel, 100-TW-EL-S or 100-TP-EL-S, style 1 or 2 balanced connector, inter-enclosure and 1.25 Gbit IEEE802.3z, 1000BASE-CX
Distance, 100-XX-EL-S	TP cable, 0 - 28 meters TW cable, 0 - 33 meters
Data Rate	1062.5 Mbit +/- 100 ppm (100-TW-EL-S 1062.5 Mbit +/- 100 ppm (100-TP-EL-S) 1.25 Gbit IEEE802.3z, 1000BASE-CX
Data Format	8B/10B
Link Characteristic Impedance	150 +/- 10 Ohms
Transmitted signal	1100 - 2000 mv, differential PECL (inter-enclosure)
Received signal	400 - 2000 mv, differential PECL

The GBIC to host connection is modified for use with the inter-enclosure balanced cable GBIC.

The GBIC shall meet both the jitter requirements specified for the δ and γ points specified in FC-MJS and the appropriate TP points specified by table 39-5 of IEEE 802.3z.

The signals provided to the host by the GBIC are defined in table A.2.

Table A.2: GBIC pin usage, style 1 or style 2 balanced cable connectors,

Pin Name	Pin #	Description	Pin Name	Pin #	Description
RX_LOS	1	Receiver Loss of Signal	RGND	11	GND
RGND	2	GND	-RX_DAT	12	- RX, ext. connector***
RGND	3	GND	+RX_DAT	13	+ RX, ext. connector***
MOD_DEF(0)	4	NC	RGND	14	GND
MOD_DEF(1)	5	NC	$V_{DD}R$	15	V_{DDR} or NC
MOD_DEF(2)	6	TTL LOW from GBIC	$V_{DD}T$	16	$V_{DD}T$
TX_DISABLE	7	Transmitter Disable	TGN	17	GND
TGND	8	GND	+TX_DAT	18	+ TX, ext. connector**
TGND	9	GND	-TX_DAT	19	- TX, ext. connector**
TX_FAULT	10	TTL LOW from GBIC*	TGN	20	GND

* Signal may optionally be implemented as specified in 3.3.
** Signal is buffered by copper transmitter circuit from GBIC pins.
*** Signal is buffered by copper receiver circuit from GBIC pins.

A.2 Operation

The protocols and timing specified in clause 5 shall be used by module definition 1 GBICs.

A GBIC having a MOD_DEF of 1 shall implement the RX_LOS and TX_DISABLE signals. The GBIC may fix the TX_FAULT signal at a TTL LOW level. As a result of tying the TX_FAULT to the negated level, the GBIC behaves as if the t_init period is very short and as if no transmitter faults ever occur.

The signal levels and signal quality shall meet the requirements of FC-PH-3.

The signal emitted by the transmitter when TX_DISABLE is asserted shall be less than 70 mv, peak to peak. This measurement shall be made with the specified maximum signal input being provided to the transmitter interface input as defined by section 4.2.

Near end cross talk (NEXT) associated with cables and connectors shall be less than 3%.

The GBIC shall implement RX_LOS detection which asserts RX_LOS to the high state when the received signal is less than a vendor specific RX_LOS threshold. The vendor specific RX_LOS threshold shall be selected to be at a level higher than the sum of:

1) the background signal occurring when TX_DISABLE is asserted by the transmitter on the opposite end of the receiving cable, and;
2) the NEXT associated with the enabled transmitter on the near end of the receiving cable, and;

3) whatever other ambient noise sources may exist in the GBIC and its environment.

Typical values for the vendor specific RX_LOS threshold are between 150 and 200 millivolts.

The value of the RX_LOS signal shall be generated according to the conditions defined in Table A.3.

Table A.3: RX_LOS detection

receive conditions	RX_LOS value
Vinput (receiver) < vendor specific RX_LOS threshold	high
Minimum differential sensitivity[a] < Vinput (receiver)	low
All other conditions	unspecified

a. Minimum differential sensitivity is 400 mV as defined by FC-PH-3.

Clause 5.3.1 and 5.3.8 define the timing requirements and protocol for the generation of the RX_LOS parameter.

The RX_LOS detection circuitry shall be designed such that the RX_LOS signal does not rapidly change state with small variations in received power. This may be accomplished by a vendor specific detection circuit that may use one or more of the following mechanisms:

- signal level measurement hysteresis
- signal level measurement averaging over a sufficient period to remove pattern dependent amplitude variations
- analysis of the preferred state of the detection circuitry
- other appropriate mechanisms

A.3 External Connector Definition

The external connector shall be the style 1 or style 2 balanced cable connector defined by FC-PH-3.

Table A.4 defines the pin assignments for style 1 balanced cable connectors.

Table A.4: Pin assignment for style 1 balanced cable connector

Pin Name	Pin #
+ TX	1
No connection	2
No connection	3
No connection	4
+ RX	5
- TX	6
No connection	7
No connection	8
- RX	9

Table A.5 defines the pin assignments for style 2 balanced cable connectors.

Table A.5: Pin assignment for style 2 balanced cable connector

Pin Name	Pin #
+ TX	1
No connection	2
- TX	3
No connection	4
No connection	5
- RX	6
No connection	7
+ RX	8

Annex B: Module definition '2' GBIC (copper intra-enclosure)

(normative annex)

B.1 Overview of module definition 2 GBIC

A GBIC having module definition 2 presents a standard copper interface having characteristics similar to the Fibre Channel 100-TP-EL-S or 100-TW-EL-S intra-enclosure interface using the style 1 or style 2 balanced cable connector. The GBIC is not compliant with the Gigabit Ethernet definition IEEE802.3, 1000BASE-CX, but should operate on short cables that do not require the higher signals of the inter-enclosure transmitters. The PECL transmitter and receiver specifications (see 4.2) have been selected so that a MOD_DEF 2 GBIC may use passive circuitry to pass the signals to the GBIC's interface with the host. Additional functionality can be provided by using active circuitry. The copper transmitter and receiver specification is defined by FC-PH-3. An overview of the copper Fibre Channel characteristics is provided in table B.1.

Table B.1: Overview, module definition 2 GBIC

Parameter	Value
Application	Fibre Channel, 100-TW-EL-S or 100-TP-EL-S, Style 1 or style 2 balanced connector, intra-enclosure
Distance, 100-TW-EL-S	0 - 13 meters
Data Rate	1062.5 Mbit +/- 100 ppm (100-TW-EL-S) 1062.5 Mbit +/- 100 ppm (100-TP-EL-S) 1.25 Gbit IEEE802.3z, 1000BASE-CX
Data Format	8B/10B
Link Characteristic Impedance	150 +/- 10 Ohms
Transmitted signal	600 - 2000 mv, differential PECL (note maximum is higher than standard intra-enclosure connections)
Received signal	400 - 2000 mv, differential PECL (note maximum is higher than standard intra-enclosure connection)

The GBIC to host connection is modified for use with the intra-enclosure balanced cable GBIC. The signals provided to the host by GBIC are defined in table B.2.

The GBIC shall meet both the jitter requirements specified for the δ and γ points specified in FC-MJS and the appropriate TP points specified by table 39-5 of IEEE 802.3z.

Table B.2: GBIC pin usage for style 1 and style 2 balanced cable connectors

Pin Name	Pin #	Description	Pin Name	Pin #	Description
RX_LOS	1	TTL LOW from GBIC*	RGN	11	GND
RGND	2	GND	-RX_DAT	12	- RX, ext. connector***
RGND	3	GND	+RX_DAT	13	+ RX, ext. connector***
MOD_DEF(0)	4	NC	RGN	14	GND
MOD_DEF(1)	5	TTL LOW from GBIC	$V_{DD}R$	15	$V_{DD}R$ or NC
MOD_DEF(2)	6	NC	$V_{DD}T$	16	$V_{DD}T$
TX_DISABLE	7	Pull-up on GBIC*	TGND	17	GND
TGND	8	GND	+TX_DAT	18	+ TX, ext. connector**
TGND	9	GND	-TX_DAT	19	- TX, ext. connector**
TX_FAULT	10	TTL LOW from GBIC*	TGND	20	GND

* Signals may optionally be implemented as specified in 3.3.
** Signal may optionally be buffered by copper transmitter circuit from GBIC pins.
*** Signal may optionally be buffered by copper receiver circuit from GBIC pins.

B.2 Initialization and error management

The protocols and timing specified in clause 5 shall be used by module definition 2 GBICs.

A passive GBIC having a MOD_DEF of 2 shall fix the TX_FAULT and the RX_LOS signals at a TTL LOW level. As a result of tying the TX_FAULT to the negated level, the GBIC behaves as if the t_init period is very short and as if no transmitter faults ever occur. As a result of tying the RX_LOS signal to the negated level, the GBIC behaves as if no receiver faults or loss of signal occu . The host shall be responsible for determining that a signal is not being received. The GBIC shall ignore the state of the TX_DISABLE signal.

A GBIC having a MOD_DEF of 2 may use active circuits to implement TX_FAULT, TX_DISABLE, and/or RX_LOS. The signal levels and signal quality shall meet the requirements of FC-PH and shall be interoperable with a passive GBIC. The protocols and timing specified in clause 5 shall be used by active GBICs. If implemented, RX_LOS shall meet the requirements specified in A.2.

B.3 External Connector Definition

The external connector shall be the style 1 or style 2 balanced cable connector defined by FC-PH-3.

Table B.3 defines the pin assignments for style 1 balanced cable connectors.

Table B.3: Pin assignment for style 1 balanced cable connector

Pin Name	Pin #
+ TX	1
No connection	2
No connection	3
No connection	4
+ RX	5
- TX	6
No connection	7
No connection	8
- RX	9

Table B.4 defines the pin assignments for style 2 balanced cable connectors.

Table B.4: Pin assignment for style 2 balanced cable connector

Pin Name	Pin #
+ TX	1
No connection	2
- TX	3
No connection	4
No connection	5
- RX	6
No connection	7
+ RX	8

Annex C: Module definition “3” GBIC

Long-wave laser for single-mode fiber

(normative annex)

C.1 Overview of module definition 3 GBIC

A GBIC having module definition 3 presents the 100-SM-LC-L interface as defined in revision 1.0 of the Fibre Channel Low Cost 10 km Optical 1063 Mbit Interface document. The characteristics are summarized in table C.1.

Table C.1: Overview, module definition 3 GBIC

Parameter	Value
Application	Fibre Channel single-mode transceiver, 100-SM-LC-L
Distance	2 meters to 10 kilo eters
Data Rate	1062.5 Mbit +/- 100 ppm
Data Format	8B/10B
Fiber Type	9 μm core, single mode, 1310 nm, < 0.45 db/km loss
Nominal link budget	7.8 dB, including all connectors, splices, cable
Transmitter	Laser
Laser center wavelength	see 100-SM-LC-L standard
Laser spectral width, RMS	see 100-SM-LC-L standard
Transmitter, launched power	non-OFC, see 100-SM-LC-L standard
Extinction ratio	9 dB minimum
RIN_12	-116 dB/Hz
Received power	-20 dBm to -3 dBm average power. as specified by 100-SM-LC-L standard.
Power penalties	see 100-SM-LC-L standard
Receiver return los	12 dB minimum
Laser safety features	Transmit power level management with laser overdrive protection circuit.

The standard GBIC pinout and pin definitions shall be used.

The GBIC shall meet the jitter requirements specified for the δ and γ points specified in FC-MJS.

C.2 Optical transmitter power

The optical power launched by the transmitter is a function of the wavelength deviation from the zero dispersion value of the fiber and the spectral width of the source laser as specified by the 100-SM-LC-L standard.

C.3 Optical signal definitions

The relationship between the states of the transmitter, receiver, and the received optical power is shown in table C.2.

Table C.2: Relationship between electrical signal polarity and optical power

Signal state	+TX_DAT	-TX_DAT	Optical Power	+RX_DAT	-RX_DAT
“1”	HIGH	LOW	HIGH	HIGH	LOW
“0”	LOW	HIGH	LOW	LOW	HIGH

For electrical signals “LOW” is a less positive (more negative) signal than the “HIGH” signal in the same differential pair. For the optical power signal, “LOW” is the minimum optical power state, corresponding to minimum drive to the laser, while “HIGH” is the maximum optical power state, corresponding to maximum laser drive.

C.4 Optical transceiver timing

The optical transceiver interface is defined by the 100-SM-LC-L standards document. Additional information is shown in tab leC.3

Table C.3: Optical Transceiver Interface

Parameter	Symbol	Min	Max Unit	Unit	Conditions
Optical Output TX_DISABLE asserted	Poff	dBm	- 35	dBm	Into fiber, average, steady state.

The value of the RX_LOS signal shall be generated according to the conditions defined in table C.4.

Table C.4: RX_LOS detection

receive conditions	RX_LOS value
Received optical power < -31 dBm[a]	high
Received optical power > -20 dBm	low
All other condition	unspecified

a. This value is selected to be above typical system noise environments.

The RX_LOS detection circuitry shall be designed such that the RX_LOS signal does not rapidly change state with small variations in received power. This may be accomplished by a vendor specific detection circuit that may use one or more of the following mechanisms:

- signal level measurement hysteresis
- signal level measurement averaging over a sufficient period to remove pattern dependent amplitude variations
- analysis of the preferred state of the detection circuitry
- other appropriate mechanisms

C.5 Initialization and error management

The protocols and timing specified in clause 5 shall be used by module definition 3 GBICs. The TX_DISABLE, TX_FAULT, and RX_LOS signals shall be implemented and operate with the specified protocols.

C.6 External connector definition and color coding

The external optical connector shall be the duplex SC connector defined by FC-PH. Exposed surfaces of the external SC connector and/or retention mechanism shall be blue to indicate that only single-mode fiber should be connected to this GBIC.

C.7 Recommended external plug color coding

For compliance with international standards and to simplify error free configuration of systems, fibre optic plugs that are used with this GBIC should have blue exposed connector surfaces to indicate that the fibre optic cable is a single-mode cable. Overmolding of the connector is not required to be color coded, but the plug should be clearly identified as single mode by appropriate additional labeling or color coding.

Annex D: Module definition “4” GBIC (Serial Identification) (normative annex)

D.1 Overview of module definition 4 GBIC

A GBIC having module definition 4 provides access to sophisticated identification information that describes the GBIC’s capabilities, standard interfaces, manufacturer, and other information. The serial interface uses the 2-wire serial CMOS E ^{2}PROM protocol defined for the ATMEL AT24C01A/02/04 family of components (see 5.2.1). The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

This annex defines the information structures that are obtained from the GBIC.

A GBIC shall meet the electrical and optical requirements, including amplitude, eye diagram, jitter, and other parameters, specified for the standards with which the GBIC claims compliance.

D.2 Serial information definition

The 2-wire serial CMOS E^{2}PROM provides sequential or random access to 8 bit parameters, addressed from 0000h to the maximum address of the memory. The address select pins for the serial CMOS E^{2}PROM shall be set to zero (fixed at the V_{IL} low level). The fields specified by this annex shall not be written by the host in which it is installed. The GBIC may enforce this by using the write protect features of the CMOS E^{2}PROM.

The word address is transmitted with the high order bit transmitted first. The protocol for the 2-wire serial interface sequentially transmits one or more 8-bit bytes, with the data byte addressed by the lowest word address transmitted first. In each data byte, the high order bit (bit 7 in the accompanying tables) is transmitted first.

Numeric fields are expressed in binary, with the high order byte being transferred first and the high order bit of each byte being transferred first. Numeric fields are padded on the left with binary zero values.

Character strings are ordered with the first character to be displayed located in the lowest word address of the string. Each character shall be coded as a US-ASCII character as defined by ISO 8859-1, with the high order bit transmitted first. All character strings will be padded on the right with ASCII spaces (20h) to fill empty bytes.

All bits of reserved fields shall be set to zero until future definitions require their use.

A minimum of 96 bytes shall be readable by the serial identification process.

The maximum clock rate of the serial interface shall be 100 KHz.

The following tables define the contents of the serial CMOS E^{2}PROM. The first table is a summary of all the data fields in the serial ID chip. The remaining tables contain detailed descriptions of the individual data fields.

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Table D.1: Serial ID: Data Fields

Data Address	Field Size (Bytes)	Name of field	Description of field
BASE ID FIELDS			
0	1	Identifier	Type of serial transceiver (see table D.2)
1	1	Ext. Identifier	Extended identifier of type of serial transceiver (See table D.3)
2	1	Connector	Code for connector type (see table D.4)
3-10	8	Transceiver	Code for electronic compatibility or optical compatibility (see table D.5)
11	1	Encoding	Code for serial encoding algorithm (see table D.6)
12	1	BR, Nominal	Nominal bit rate, units of 100 MBits/sec.
13	1	Reserved	
14	1	Length (9µ)	Link length supported for 9/125 mm fiber, units of k
15	1	Length (9µ)	Link length supported for 9/125 µm fiber, units of 100 m
16	1	Length (50µ)	Link length supported for 50/125 µm fiber, units of 10 m
17	1	Length (62.5µ)	Link length supported for 62.5/125 µm fiber, units of 10 m
18	1	Length (Copper)	Link length supported for copper, units of meters
19	1	Reserved	
20-35	16	Vendor name	GBIC vendor name (ASCII)
36	1	Reserved	
37-39	3	Vendor OUI	GBIC vendor IEEE company ID
40-55	16	Vendor PN	Part number provided by GBIC vendor (ASCII)
56-59	4	Vendor rev	Revision level for part number provided by vendor (ASCII)
60-62	3	Reserved	
63	1	CC_BASE	Check code for Base ID Fields (addresses 0 to 62)
EXTENDED ID FIELDS			
64-65	2	Options	Indicates which optional GBIC signals are implemented (see table D.7)
66	1	BR, max	Upper bit rate margin, units of %
67	1	BR, min	Lower bit rate margin, units of %
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)
84-91	8	Date code	Vendor’s manufacturing date code (see table D.8)
92-94	3	Reserved	
95	1	CC_EXT	Check code for the Extended ID Fields (addresses 64 to 94)
VENDOR SPECIFIC ID FIELDS			
96-127	32	Read-only	Vendor specific data, read only
128-51	384	Reserved	
512-n			Vendor specific

Identifier

The identifier value specifies the physical device described by the serial information. This value shall be included in the serial data. The defined identifier values are shown in table D.2.

Table D.2: Identifier values

Value	Description of physical device
00h	Unknown or unspecified
01h	GBIC
02h	Module/connector soldered to motherboard
03h	SFP transceiver
04-7Fh	Reserved
80-FFh	Vendor specific

Extended Identifier

The extended identifier value provides additional information about the transceiver. At present, extended identifier values are specified only for the identifier value of 01h (GBIC). The Extended Identifier value is reserved for all other identifier values.

In many cases, the GBIC elects to use MOD_DEF 4 to make additional information about the GBIC available, even though the GBIC is actually compliant with one of the 6 other MOD_DEF values. The extended identifier allows the GBIC to explicitly specify such compliance without requiring the MOD_DEF value to be inferred from the other information provided. The defined extended identifier values for the GBIC are shown in table D.3.

Table D.3: Extended Identifier values for Identifier 01h (GBIC)

Value	Description of connector
00h	GBIC definition is not specified or the GBIC definition is not compliant with a defined MOD_DEF. See product specification for details.
01h	GBIC is compliant with MOD_DEF 1
02h	GBIC is compliant with MOD_DEF 2
03h	GBIC is compliant with MOD_DEF 3
04h	GBIC function is defined by serial ID only
05h	GBIC is compliant with MOD_DEF 5
06h	GBIC is compliant with MOD_DEF 6
07h	GBIC is compliant with MOD_DEF 7
08-FFh	Reserved

Connector

The Connector value indicates the external connector provided on the interface. This value shall be included in the serial data. The defined connector values are shown in table D.4.

Table D.4: Connector values

Value	Description of connector
00h	Unknown or unspecified
01h	Fibre Channel definition of SC connector
02h	Fibre Channel definition of style 1 copper connector
03h	Fibre Channel definition of style 2 copper connector
04h	Fibre Channel definition of BNC/TNC
05h	Fibre Channel definition of coaxial headers
06h	FiberJack
07h	LC
08h	MT-RJ
09h	MU
0Ah	SG
0Bh	Optical pigtail
0C - 1Fh	Reserved
20h	HSSDC II
21h	Copper Pigtail
22-7Fh	Reserved
80-FFh	Vendor specific

Transceiver

The following bit significant indicators define the electronic or optical interfaces that are supported by the GBIC. At least one bit shall be set in this field. For Fibre Channel GBICs, the Fibre Channel speed, transmission media, transmitter technology, and distance capability shall all be indicated.

Table D.5: Transceiver codes

Data Addr	Bit[a]	Description of transceiver	Data Addr	Bit[a]	Description of transceiver
Reserved Standard Compliance Codes			Fibre Channel link length		
3	7-0	Reserved	7	7	Reserved
4	7-4	Reserved	7	6	short distance (S)
SONET Compliance Codes			7	5	intermediate distance (I)
4	3	Reserved	7	4	long distance (L)
4	2	OC 48, long reach	Fibre Channel transmitter technology		
4	1	OC 48, intermediate reach	7	3-2	Reserved
4	0	OC 48, short reach	7	1	Longwave laser (LC)
5	7	Reserved	7	0	Electrical inter-enclosure (EL)
5	6	OC 12, single mode long reach	8	7	Electrical intra-enclosure (EL)
5	5	OC 12, single mode intermediate reach	8	6	Shortwave laser w/o OFC (SN)
5	4	OC 12 multi-mode short reach	8	5	Shortwave laser w/ OFC (SL)
5	3	Reserved	8	4	Longwave laser (LL)
5	2	OC 3, single mode long reach	Fibre Channel transmission media		
5	1	OC 3, single mode intermediate reach	8	0-3	Reserved
5	0	OC 3, multi-mode short reach	9	7	Twin Axial Pair (TW)
Gigabit Ethernet Compliance Code			9	6	Shielded Twisted Pair (TP)
6	7-4	Reserved	9	5	Miniature Coax (MI)
6	3	1000BASE-T	9	4	Video Coax (TV)
6	2	1000BASE-CX	9	3	Multi-mode, 62.5µ (M6)
6	1	1000BASE-LX	9	2	Multi-mode, 50 µ (M5)
6	0	1000BASE-SX	9	1	Reserved
			9	0	Single Mode (SM)
			Fibre Channel speed		
			10	7-5	Reserved
			10	4	400 MBytes/Sec
			10	3	Reserved
			10	2	200 MBytes./Sec
			10	1	Reserved
			10	0	100 MBytes/Sec

a. Bit 7 is the high order bit and is transmitted first in each byte.

Encoding

The encoding value indicates the serial encoding mechanism that is the nominal design target of the particular GBIC. The value shall be contained in the serial data. The defined encoding values are shown in table D.6.

Table D.6: Encoding codes

code	Description of encoding mechanism
00h	Unspecified
01h	8B10B
02h	4B5B
03h	NRZ
04h	Manchester
05h -FFh	Reserved

BR, nominal

The nominal bit rate (BR, nominal) is specified in units of 100 Megabits per second, rounded off to the nearest 100 Megabits per second. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of 0 indicates that the bit rate is not specified and must be determined from the transceiver technology.The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value.

Length (9μ)-km

This value specifies the link length that is supported by a GBIC or other transceiver while operating in compliance with the applicable standards using single mode fiber. The value is in units of kilometers. A value of 255 means that the transceiver supports a link length greater than 254 km. A value of zero means that the transceiver does not support single mode fiber or that the length information must be determined from the transceiver technology.

Length (9μ)

This value specifies the link length that is supported by the GBIC while operating in compliance with the applicable standards using single mode fiber. The value is in units of 100 meters. A value of 255 means that the GBIC supports a link length greater than 25.4 km. A value of zero means that the GBIC does not support single mode fiber or that the length information must be determined from the transceiver technology.

Length (50μ)

This value specifies the link length that is supported by the GBIC while operating in compliance with the applicable standards using 50 micron multi-mode fiber. The value is in units of 10 meters. A value of 255 means that the GBIC supports a link length greater than 2.54 km. A value of zero

means that the GBIC does not support 50 micron multi-mode fiber or that the length information must be determined from the transceiver technology.

Length (62.5μ)

This value specifies the link length that is supported by the GBIC while operating in compliance with the applicable standards using 62.5 micron multi-mode fiber. The value is in units of 10 meters. A value of 255 means that the GBIC supports a link length greater than 2.54 km. A value of zero means that the GBIC does not 62.5 micron multi-mode fiber or that the length information must determined from the transceiver technology. It is common for GBICs to support both 50 micron and 62.5 micron fiber.

Length (Copper)

This value specifies the minimum link length that is supported by the GBIC while operating in compliance with the applicable standards using copper cable. The value is in units of 1 meter. A value of 255 means that the GBIC supports a link length greater than 254 meters. A value of zero means that the GBIC does not support copper cables or that the length information must be determined from the transceiver technology. Further information about the cable design, equalization, and connectors is usually required to guarantee meeting a particular length requirement.

Vendor name

The vendor name is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

Vendor OUI

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

Vendor PN

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

Vendor Rev

The vendor revision number (vendor rev) is a 4-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the 4-byte field indicates that the vendor PN is unspecified.

CC_BASE

The check code is a one byte code that can be used to verify that the first 64 bytes of serial information in the GBIC is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 0 to byte 62, inclusive.

Options

The bits in the option field shall specify the options implemented in the GBIC as described in table D.7.

Table D.7: Option values

data address	bit	Description of option
64	7-0	Reserved
65	7-6	Reserved
65	5	RATE_SELECT is implemented If bit is set then active control of the rate select pin is required to change rates. If bit is not set, no control of pin is required. In all cases, compliance with multiple rate standards should be determined by Transceiver Codes in Bytes 4, 5, 6 and 10. (See table D.5)
65	4	TX_DISABLE is implemented and disables the serial output.
65	3	TX_FAULT signal implemented. (Reset as defined in 5.3)
65	2	Loss of Signal implemented, signal inverted from definition in 3.3 NOTE: This is not standard GBIC behavior and should be avoided, since non-interoperable behavior results.
65	1	Loss of Signal implemented, signal as defined in 3.3
65	0	Reserved

BR, max

The upper bit rate limit at which the GBIC will still meet its specifications (BR, max) is specified in units of 1% above the nominal bit rate. A value of zero indicates that this field is not specified.

BR, min

The lower bit rate limit at which the GBIC will still meet its specifications (BR, min) is specified in units of 1% below the nominal bit rate. A value of zero indicates that this field is not specified.

Vendor SN

The vendor serial number (vendor SN) is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the GBIC. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

Date Code

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the format specified by table D.8.

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Table D.8: Date Code

Data Address	Description of field
84-85	ASCII code, two low order digits of year. (00 = 2000).
86-87	ASCII code, digits of month (01 = Jan through 12 = Dec)
88-89	ASCII code, day of month (01 - 31)
90-91	ASCII code, vendor specific lot code, may be blank

CC_EXT

The check code is a one byte code that can be used to verify that the first 32 bytes of extended serial information in the GBIC is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 64 to byte 94, inclusive.

Read-only

This area may contain vendor specific information which can be read from the GBIC. The data is read only.

D.3 Color coding of optical connectors

If the transceiver code specifies a single mode medium, exposed surfaces of the external connector and/or retention mechanism shall be blue to indicate that single-mode fiber should be connected to this GBIC.

If the transceiver code specifies a multi-mode medium, exposed surfaces of the external connector and/or retention mechanism shall be beige or black to indicate that multi-mode fiber should be connected to this GBIC.

If conflicting values are specified, the transceiver shall have the color for the most appropriate transceiver code.

D.4 Recommended external plug color coding

For compliance with international standards and to simplify error free configuration of systems, fibre optic plugs that are used with this GBIC's receptacle should have exposed connector surfaces of the proper color to indicate that the fibre is single-mode or multi-mode. Overmolding of the connector is not required to be color coded, but the plug should be clearly identified as the proper mode by appropriate additional labeling or color coding.

Annex E: Module definition “5” GBIC (shortwave laser) (normative annex)

E.1 Overview of module definition 5 GBIC

A GBIC having module definition 5 presents a standard optical interface compatible with the Fibre Channel 100-M5-SN-I and 100-M6-SN-I interfaces. Those characteristics are summarized in table E.1.

Table E.1: Overview, module definition 5 GBIC

Parameter	Value
Application	Fibre Channel, 100-M5-SN- I or 100-M6-SN-I, no OFC or compatible physical interface
Distance	500 meters maximum using 50 micron fiber. 300 meters maximum using 62.5 micron fiber.
Data Rate	1062.5 Mbit +/- 100 ppm
Data Format	8B/10B
Fiber Type	50 μm or 62.5 μm, multimode
Wavelength	770-860 nm
Minimum Power into Fiber	-10 dBm average
Received power	-16 dBm to 0 dBm average power per 100-SN-M5-I and 100-SN-M6-I. BER shall be <1E-12 when the data is sampled across a +/- 10% UI window centered in the receiver output eye.
Laser safety features	Transmit power level management with laser overdrive protection circuit.

The standard GBIC pinout and pin definitions shall be used.

The GBIC shall meet the jitter requirements specified for the δ and γ points specified in FC-MJS.

E.2 Optical signal definitions

The relationship between the states of the transmitter, receiver, and the received optical power is shown in table E.2.

Table E.2: Relationship between electrical signal polarity and optical power

Signal state	+TX_DAT	-TX_DAT	Optical Power	+RX_DAT	-RX_DAT
“1”	HIGH	LOW	HIGH	HIGH	LOW
“0”	LOW	HIGH	LOW	LOW	HIGH

For electrical signals “LOW” is a less positive (more negative) signal than the “HIGH” signal in the same differential pair. For the optical power signal, “LOW” is the minimum optical power state, corresponding to minimum drive to the laser, while “HIGH” is the maximum optical power state, corresponding to maximum laser drive.

E.3 Optical transceiver timing

The optical transceiver interface is defined by the FC-PH-2 standards document. Additional information is shown in table E.3

Table E.3: Optical Transceiver Interface

Parameter	Symbol	Min	Max Unit	Unit	Conditions
Optical Output TX_DISABLE asserted	Poff	dBm	-35	dBm	Into fiber, average, steady state.

The value of the RX_LOS signal shall be generated according to the conditions defined in table E.4.

Table E.4: RX_LOS detection

receive conditions	RX_LOS value
Received optical power < -31 dBm[a]	high
Received optical power > -16 dBm	low
All other condition	unspecified

a. This value is selected to be above typical system noise environments.

The RX_LOS detection circuitry shall be designed such that the RX_LOS signal does not rapidly change state with small variations in received power. This may be accomplished by a vendor specific detection circuit that may use one or more of the following mechanisms:

- signal level measurement hysteresis
- signal level measurement averaging over a sufficient period to remove pattern dependent amplitude variations
- analysis of the preferred state of the detection circuitry
- other appropriate mechanisms

E.4 Initialization and error management

The protocols and timing specified in clause 5 shall be used by module definition 5 GBICs. The TX_DISABLE, TX_FAULT, and RX_LOS signals shall be implemented and operate with the specified protocols.

E.5 External connector definition and color coding

The external optical connector shall be the duplex SC connector defined by FC-PH. Exposed surfaces of the external SC connector and/or retention mechanism shall be beige or black to indicate that only multi-mode fiber should be connected to this GBIC.

E.6 Recommended external plug color coding

For compliance with international standards and to simplify error free configuration of systems, fibre optic plugs that are used with this GBIC should have beige or black exposed connector surfaces to indicate that the fibre optic cable is a multi-mode cable. Overmolding of the connector is not required to be color coded, but the plug should be clearly identified as multi-mode by appropriate additional labeling or color coding.

Annex F: Module definition “6” GBIC

Long-wave laser for single-mode fiber

(normative annex)

F.1 Overview of module definition 6 GBIC

A GBIC having module definition 6 presents a standard optical interface that is fully compliant with the Fibre Channel 100-SM-L C-L interface. When used as a Fibre Channel interface, a compliant GBIC shall interoperate with GBICs having a module definition of 3 or 6.

The GBIC will also operate on single mode fibers transmitting the IEEE 802.3 Gigabit Ethernet signals over a 10 kilometer distance. While this GBIC operates at 1.25 GBd and is compatible with the electrical and jitter specifications for operation with IEEE 802.3z compliant hardware, it is not compliant with the 1000BASE-LX specification. Interoperability between this specification and 1000BASE-LX may be possible under carefully restricted circumstances

The present characteristics are summarized in table F.1.

Table F.1: Overview, module definition 6 GBIC

Parameter	Value
Application	Fibre Channel single-mode transceiver, 100-SM-LC-L and 10 km IEEE802.3 Gigabit Ethernet similar to 1000BASE-LX, but modified for longer distance.
Distance	2 meters to 10 kilometers
Data Rate	1062.5 Mbit +/- 100 ppm and 1250 Mbit
Data Format	8B/10B
Fiber Type	9 µm core, single mode, 1310 nm, < 0.45 db/km loss
Nominal link budget	7.8 dB, including all connectors, splices, cable
Transmitter	Laser
Laser center wavelength	from Figure F.1
Laser spectral width, RMS	from Figure F.1
Transmitter, launched power	non-OFC, from Figure F.1
Extinction ratio	9 dB minimum
RIN_12	-116 dB/Hz
Received power	-20 dBm to -3 dBm average power. as specified by 100-SM-LC-L standard.
Power penalties	from Figure F.1
Receiver return loss	12 dB minimum
Laser safety features	Transmit power level management with laser overdrive protection circuit.

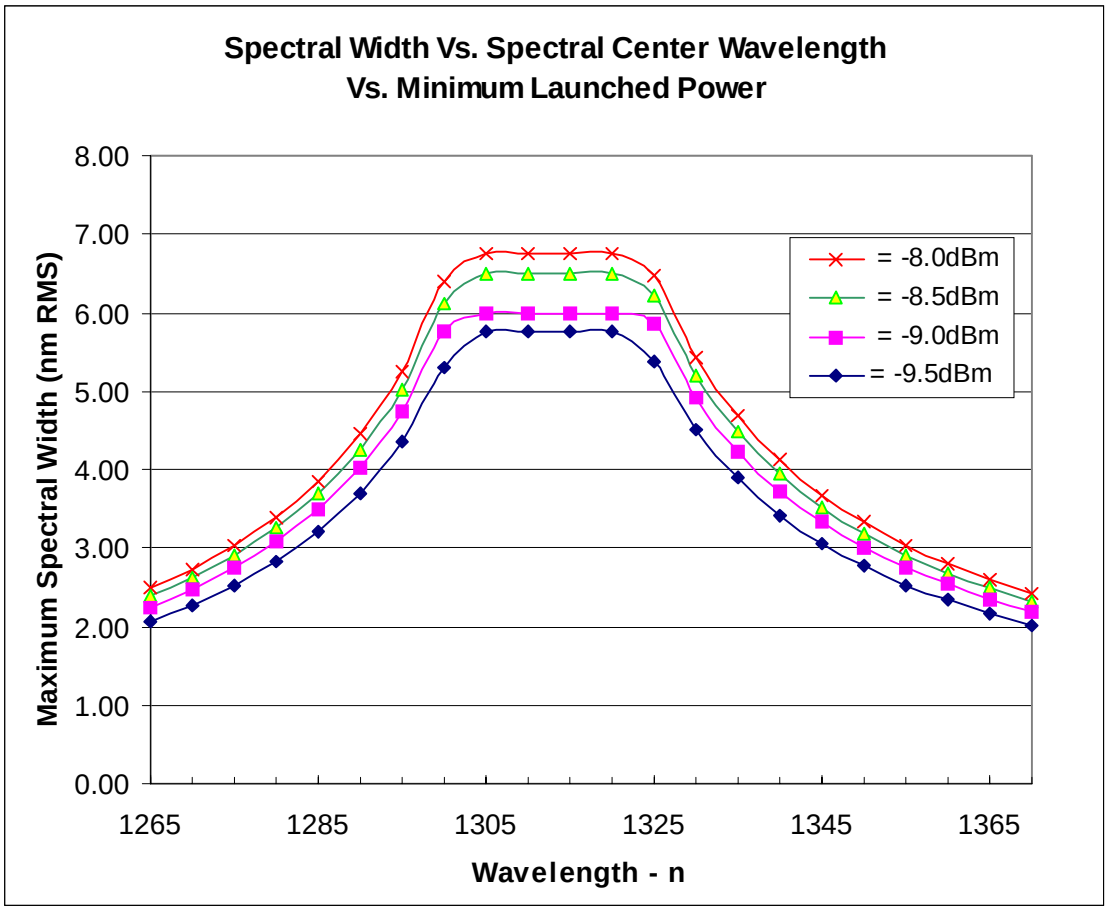
The standard GBIC pinout and pin definitions shall be used.

The GBIC shall meet both the jitter requirements specified for the δ and γ points specified in FC-MJS and the appropriate TP points specified by table 38-10 of IEEE 802.3z.

F.2 Optical transmitter power

The optical power required to be launched by the transmitter is a function of the wavelength deviation from the zero dispersion value of the fiber and the spectral width of the source laser. The required optical power can be calculated based on Figure F.1.

Figure F.1: Spectral Width vs. Spectral Center Wavelength vs. Launched Power



The information contained in Figure F.1 is presented in tabular form in table F.2 and table F.3

Table F.2: Spectral Width vs Spectral Center Wavelength vs. Launched Power, 1 of 2

Minimum Launched Power (dB)	Center Wavelength (µm)										
	1.265	1.270	1.275	1.280	1.285	1.290	1.295	1.300	1.305	1.310	1.315
-8.0	2.49	2.74	3.03	3.40	3.86	4.45	5.25	6.38	6.75	6.75	6.75
-8.5	2.39	2.62	2.91	3.26	3.70	4.27	5.03	6.12	6.50	6.50	6.50
-9.0	2.25	2.47	2.74	3.07	3.49	4.02	4.75	5.77	6.00	6.00	6.00
-9.5	2.07	2.28	2.52	2.83	3.21	3.70	4.37	5.31	5.75	5.75	5.75
	Spectral Width (nm)										

Table F.3: Spectral Width vs Spectral Center Wavelength vs. Launched Power, 2 of 2

Minimum Launched Power (dB)	Center Wavelength (μm)										
	1.320	1.325	1.330	1.335	1.340	1.345	1.350	1.355	1.360	1.365	1.370
-8.0	6.75	6.48	5.43	4.68	4.12	3.68	3.33	3.04	2.80	2.60	2.43
-8.5	6.50	6.21	5.20	4.48	3.95	3.53	3.19	2.92	2.69	2.49	2.33
-9.0	6.00	5.86	4.91	4.23	3.72	3.33	3.01	2.75	2.54	2.35	2.20
-9.5	5.75	5.39	4.52	3.89	3.42	3.06	2.77	2.53	2.33	2.16	2.02
	Spectral Width (nm)										

F.3 Optical signal definitions

The relationship between the states of the transmitter, receiver, and the received optical power is shown in table F.4.

Table F.4: Relationship between electrical signal polarity and optical power

Signal state	+TX_DAT	-TX_DAT	Optical Power	+RX_DAT	-RX_DAT
“1”	HIGH	LOW	HIGH	HIGH	LOW
“0”	LOW	HIGH	LOW	LOW	HIGH

For electrical signals “LOW” is a less positive (more negative) signal than the “HIGH” signal in the same differential pair. For the optical power signal, “LOW” is the minimum optical power state, corresponding to minimum drive to the laser, while “HIGH” is the maximum optical power state, corresponding to maximum laser drive.

F.4 Optical transceiver timing

The optical transceiver interface is defined by the 100-SM-LC-L standards document. Additional information is shown in table F.5

Table F.5: Optical Transceiver Interface

Parameter	Symbol	Min	Max Unit	Unit	Conditions
Optical Output TX_DISABLE asserted	Poff	dBm	- 35	dBm	Into fiber, average, steady state.

The value of the RX_LOS signal shall be generated according to the conditions defined in table

F.6.

Table F.6: RX_LOS detection

receive conditions	RX_LOS value
Received optical power < -31 dBm[a]	high
Received optical power > -20 dBm	low
All other condition	unspecified

a. This value is selected to be above typical system noise environments.

The RX_LOS detection circuitry shall be designed such that the RX_LOS signal does not rapidly change state with small variations in received power. This may be accomplished by a vendor specific detection circuit that may use one or more of the following mechanisms:

- signal level measurement hysteresis
- signal level measurement averaging over a sufficient period to remove pattern dependent amplitude variations
- analysis of the preferred state of the detection circuitry
- other appropriate mechanisms

F.5 Initialization and error management

The protocols and timing specified in clause 5 shall be used by module definition 6 GBICs. The TX_DISABLE, TX_FAULT, and RX_LOS signals shall be implemented and operate with the specified protocols.

F.6 External connector definition and color coding

The external optical connector shall be the duplex SC connector defined by FC-PH. Exposed surfaces of the external SC connector and/or retention mechanism shall be blue to indicate that only single-mode fiber should be connected to this GBIC.

F.7 Recommended external plug color coding

For compliance with international standards and to simplify error free configuration of systems, fibre optic plugs that are used with this GBIC should have blue exposed connector surfaces to indicate that the fibre optic cable is a single-mode cable. Overmolding of the connector is not required to be color coded, but the plug should be clearly identified as single mode by appropriate additional labeling or color coding.

Annex G: Module definition “7” GBIC (shortwave laser) (normative annex)

G.1 Overview of module definition 7 GBIC

A GBIC having module definition 7 presents a standard optical interface that is fully compliant with the Fibre Channel 100-M5-SN-I interface, the 100-M6-SN-I interface, and with the IEEE802.3 Gigabit Ethernet 1000BASE-SX interface. When used as a Fibre Channel interface, a compliant GBIC shall interoperate with GBICs having a module definition of 5 or 7. The characteristics are summarized in table G.1

A GBIC having module definition 7 presents a standard optical interface compatible with the Gigabit Ethernet 1000BASE-SX interface. Those characteristics are summarized in table G.1.

Table G.1: Overview, module definition 7 GBIC

Parameter	Value
Application	Gigabit Ethernet, 1000BASE-SX interface and Fibre Channel 100-M5-SN-I and 100-M6-SN-I interface
Distance	In 1000BASE-SX environment, 550 meters maximum using 50 micron fiber and 260 meters maximum using 62.5 micron fiber. In Fibre Channel environment, see Annex E.
Data Rate	1250 Mbit +/- 100 ppm and 1062.5 Mbit +/- 100 ppm
Data Format	8B/10B
Fiber Type	50 μm or 62.5 μm, multimode
Wavelength	770-860 nm
Minimum Power into Fiber	For Fibre Channel: -10 dBm average For 1000BASE-SX: -9.5 dBm average
Received power	FC: -16 dBm to 0 dBm average power per 100-SN-M5-I and 100-SN-M6-I. BER shall be <1E-12 when the data is sampled across a +/- 10% UI window centered in the receiver output eye. GBE: -17 dBm to 0 dBm @ center of the receiver output eye, per IEEE 802.3 1000BASE-SX.
Laser safety features	Transmit power level management with laser overdrive protection circuit.

The standard GBIC pinout and pin definitions shall be used.

The GBIC shall meet both the jitter requirements specified for the δ and γ points specified in FC-MJS and the appropriate TP points specified by table 38-10 of IEEE 802.3z.

G.2 Optical signal definitions

The relationship between the states of the transmitter, receiver, and the received optical power is shown in table G.2.

Table G.2: Relationship between electrical signal polarity and optical power

Signal state	+TX_DAT	-TX_DAT	Optical Power	+RX_DAT	-RX_DAT
“1”	HIGH	LOW	HIGH	HIGH	LOW
“0”	LOW	HIGH	LOW	LOW	HIGH

For electrical signals “LOW” is a less positive (more negative) signal than the “HIGH” signal in the same differential pair. For the optical power signal, “LOW” is the minimum optical power state, corresponding to minimum drive to the laser, while “HIGH” is the maximum optical power state, corresponding to maximum laser drive.

G.3 Optical transceiver timing

The optical transceiver interface is defined by IEEE 802.3z, clause 38. Additional information is shown in table G.3

Table G.3: Optical Transceiver Interface

Parameter	Symbol	Min	Max Unit	Unit	Conditions
Optical Output TX_DISABLE asserted	Poff	dBm	-35	dBm	Into fiber, average, steady state.

The value of the RX_LOS signal shall be generated according to the conditions defined in table G.4.

Table G.4: RX_LOS detection

receive conditions	RX_LOS value
Received optical power < -31 dBm[a]	high
Received optical power > -17 dBm	low
All other condition	unspecified

a. This value is selected to be above typical system noise environments.

The RX_LOS detection circuitry shall be designed such that the RX_LOS signal does not rapidly

change state with small variations in received power. This may be accomplished by a vendor specific detection circuit that may use one or more of the following mechanisms:

- signal level measurement hysteresis
- signal level measurement averaging over a sufficient period to remove pattern dependent amplitude variations
- analysis of the preferred state of the detection circuitry
- other appropriate mechanisms

G.4 Initialization and error management

The protocols and timing specified in clause 5 shall be used by module definition 7 GBICs. The TX_DISABLE, TX_FAULT, and RX_LOS signals shall be implemented and operate with the specified protocols.

G.5 External connector definition and color coding

The external optical connector shall be the duplex SC connector defined by 802.3z. Exposed surfaces of the external SC connector and/or retention mechanism shall be beige or black to indicate that only multi-mode fiber should be connected to this GBIC.

G.6 Recommended external plug color coding

For compliance with international standards and to simplify error free configuration of systems, fibre optic plugs that are used with this GBIC should have beige or black exposed connector surfaces to indicate that the fibre optic cable is a multi-mode cable. Overmolding of the connector is not required to be color coded, but the plug should be clearly identified as multi-mode by appropriate additional labeling or color coding.