SFF-9639

Reference Guide for

Multifunction 6X Unshielded Connector Pinouts

Rev 2.2 May 2, 2025

Secretariat: SFF TWG

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This document has been released by SNIA. The SFF TWG believes that the ideas, methodologies, and technologies described in this document are technically accurate and are appropriate for widespread distribution.

The description of a connector in this document does not assure that the specific component is actually available from connector suppliers. If such a connector is supplied it must comply with this document to achieve interoperability between suppliers.

Abstract: This document is a guide to the pinout usage of the SFF-8639 six-lane, high speed multifunction plug and receptacle connector that is designed for use as a common connector system supporting both SAS and PCIe based devices.

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Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, as well as since SFF's transition to SNIA in 2016, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/join.

Revision History

Rev 0.1 - Extracted Informative Annex A from SFF-8639
Rev 0.2 - Tables revised with the signal names of the using interfaces
Rev 0.3 - Specified how PET and PER pins are to be connected.
Rev 0.4 - Updated USB pinouts to tables
- Added note on how PCIe names signals on devices
Rev 0.5 - Identified interface documents for usage models
Rev 0.6 - Updated the interface document references and moved them to Section 2.1
- Added clarification that signal grounds are electrical reference grounds
Rev 0.7 - Added OCP and SNIA network pinouts to tables
- Removed speed references
Rev 0.8 – SNIA pinouts finalized
- SATA P3 DEVSLP updated to DVSLP/Power Disable
Rev 0.9 - Moved reference for Notes 1 and 2 in Table 4-2 and Table 4-3
Rev 1.0 - Removed *1 and *2 from SATA Express column in Table 4-3
Rev 1.1 – Updated SFF links to SNIA links
- Added SFF-TA-1001 references & pinout, removed USB
- Adjusted Quad PCIe pin names to align with changes in reference spec
- Added PCI-SIG source to section 2.3
- Added Note 3 to tables 4-2 & 4-3, replaced SFF-8639 with PCIe
- Added Section 5

– Updated chairman contact in POINTS OF CONTACT
- Updated boilerplate items to SFF TA TWG terms
- Fixed spacing in listings in Section 2.1
- Removed dimensioning conventions in Section 2.4

Rev 2.0 *July 18, 2018*
- Upgraded to SNIA template
- Replaced "Development Reference Guide" with "Published" in header
- Added "Reference" watermark
- Reformatted Change History

Rev 2.0a *July 24, 2018*
- Updated some boiler plate material
- Corrected "Reference" watermark
- Added missing pages (pages 8 & 9)

Rev 2.1 *December 13, 2019*
- Removed SNIA Ethernet Drive and SATA Express columns
- Added SNIA Native NVMe-oF pinout column from SNIA specification
- Added SNIA Native NVMe-oF Dual Port Usage section
- Replaced Table 5.1

Rev 2.2 *May 2, 2025*
- Added new boilerplate
- Table 5-1 incorrectly calls out E16=0 in the headers, polarity should be E16=1
- All signal references to '1' changed to correct term of 'Open'
- All signal references to '0' changed to correct term of 'GND'

CONTENTS

TABLES

1. Scope

This specification defines pinouts used with the SFF-8639 Multifunction 6X Unshielded Connector.

1.1 Application Specific Criteria

This is an informational document. See Industry Documents for official information.

2. References

2.1 Industry Documents

The following interface standards and specifications are relevant to this specification as of the date of publication.

SATA	SATA-IO Serial ATA Revision 3.2
SATA Express	SATA-IO Serial ATA Revision 3.2
Dual Port SAS	SFF-8482 & INCITS/ T10 Serial Attached SCSI-3
Multi-Link SAS	SFF-8629 & INCITS/ T10 Serial Attached SCSI-3
Quad PCIe	PCI-SIG PCI Express SFF-8639 Module Specification
SFF-TA-1001	Universal x4 Link Definition for SFF-8639
OCP (Kinetic)	Storage Device with Ethernet Interface
NXP	I2C-Bus Specification and User Manual
Native NVMe-oF	SNIA Native NVMe-oF Drive Specification

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://www.techstreet.com/incitsgate.tmpl).

2.3 Conventions

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	**French**	**ISO**
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

Reserved: Defines the signal on a connector contact. Its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

There are no unique Acronyms or Abbreviations used in this document.

3.3 Definitions

Connector: Each half of an interface that, when joined together, establish electrical contact and mechanical retention between two components. In this specification, the term connector does not apply to any specific gender; it is used to describe the receptacle, the plug or the card edge, or the union of receptacle to plug or card edge. Other common terms include: connector interface, mating interface, and separable interface.

Contacts: A term used to describe connector terminals that make electrical connections across a separable interface.

Module: In this specification, module may refer to a plug assembly at the end of a copper (electrical) cable (passive or active), an active optical cable assembly, an optical transceiver, or a loopback.

Plug: A term used to describe the connector that contains the penetrating contacts of the connector interface as shown in Figure 3-1. Plugs typically contain stationary contacts. Other common terms include male, pin connector, and card edge.

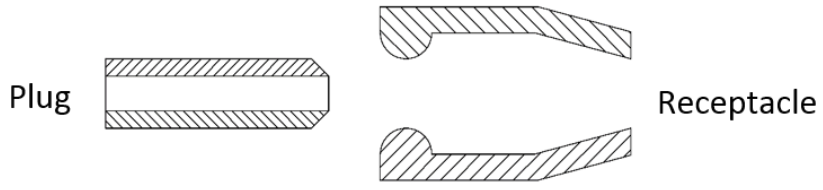

FIGURE 3-1 PLUG AND RECEPTACLE DEFINITION

Receptacle: A term used to describe the connector that contains the contacts that accept the plug contacts as shown in Figure 3-1. Receptacles typically contain spring contacts. Other common terms include female and socket connector.

4. General Description

When a new SFF connector specification is developed there may be more than one industry interface planning to make use of it. Groups working on interfaces being developed under non-disclosure are unable to compare and discuss anticipated usage.

Pinouts are discussed during connector development and initial definitions assigned to ensure that the connector meets the needs of the interested interfaces.

This specification is a guide to the anticipated pinout usage of the interfaces under development.

5. Connector Usage Models

The connector system defined in SFF-8639 is considered to be an extension of the connector systems defined in SFF-8482 and SFF-8629. The SFF-8639 specification defines a multi-function connector system that may be used to implement specific storage device use cases.

The connector system defines a total of 68 contacts. The receptacle may implement all of the defined contacts while the plug may implement only the contacts required by the use case supported on a particular device. This allows for multiple device types supporting different use cases to be inserted into a common receptacle.

The connector system may be used for use cases not defined in this specification. The following three tables define the signal utilization based on use case. The signal name is given with respect to the receptacle. The signal ground is the electrical reference ground, the mechanical shell is a separate ground.

WARNING: The definitive reference for signals are the using interfaces identified in Sections 2.1. Readers should be aware that the tables below may not be accurate after these interfaces have been completed and distributed for public use.

TABLE 5-1: P SERIES SIGNALS (PLUG)

		SATA	SAS	MultiLink SAS	Quad PCIe	SFF-TA-1001	OCP Kinetic	SNIA Native NVMe-oF
P1		Retired	P1->P2	P1->P2	WAKE#	WAKE#	Presence Detect	
P2		Retired	P2->P1	P2->P1		Reserved	I2C Clock	
P3		DVSLP/ Power Disable	POWER DISABLE	POWER DISABLE	PWRDIS	PWRDIS	I2C Data	PWRDIS
P4		GND	GROUND	GROUND	IfDet#	IfDet#	Ground	IfDet#= Ground
P5	Ground	GND	GROUND	GROUND	Ground	Ground	Ground	Ground
P6	Ground	GND	GROUND	GROUND	Ground	Ground	Ground	Ground
P7	+5V	V5	V5, precharge	V5, precharge			+5V Precharge	
P8	+5V	V5	V5	V5			+5V	
P9	+5V	V5	V5	V5			+5V	
P10		GND	GROUND	GROUND	PRSNT#	PRSNT#	Ground	PRSNT# = Ground
P11		DAS/DSS/ DHU	READY LED	READY LED	ACTIVITY#	ACTIVITY#	Vendor Specific	ACTIVITY#
P12	Ground	GND	GROUND	GROUND	Ground	Ground	Ground	Ground
P13	+12V	V12	V12, precharge	V12, precharge	+12 V Precharge	+12 V Precharge	+12V Precharge	+12V Precharge
P14	+12V	V12	V12	V12	+12 V	+12 V	+12V	+12V
P15	+12V	V12	V12	V12	+12 V	+12 V	+12V	+12V

TABLE 5-2 S SERIES SIGNALS (PLUG)

		SATA	SAS	MultiLink SAS	Quad PCIe	SFF-TA-1001	OCP Kinetic	SNIA Native NVMe-oF
S1	Ground	GND	GROUND	GROUND	Ground	Ground	Ground	Ground
S2	Rcvr+	A+	PR+	RX0+		PETp0	RX0+	
S3	Rcvr-	A-	PR-	RX0-		PETn0	RX0-	
S4	Ground	GND	GROUND	GROUND	Ground	Ground	Ground	Ground
S5	Xmtr-	B-	TP-	TX0-		PERn0	TX0-	
S6	Xmtr+	B+	TP+	TX0+		PERp0	TX0+	
S7	Ground	GND	GROUND	GROUND	Ground	Ground	Ground	Ground
S8	Ground		GROUND	GROUND	Ground	Ground	Ground	Ground
S9	Rcvr+		SR+	RX1+		PETp1	RX1+	
S10	Rcvr-		SR-	RX1-		PETn1	RX1-	
S11	Ground		GROUND	GROUND	Ground	Ground	Ground	Ground
S12	Xmtr-		ST+	TX1-		PERn1	TX1-	
S13	Xmtr+		ST-	TX1+		PERp1	TX1+	
S14	Ground		GROUND	GROUND	Ground	Ground	Ground	Ground
S15				Reserved	Reserved	HPT0		HPT0 = Open
S16	Ground			GROUND	Ground	Ground		Ground
S17	Rcvr+			RX2+	PETp1	PETp2		TX0+
S18	Rcvr-			RX2-	PETn1	PETn2		TX0-
S19	Ground			GROUND	Ground	Ground		Ground
S20	Xmtr-			TX2-	PERn1	PERn2		
S21	Xmtr+			TX2+	PERp1	PERp2		
S22	Ground			GROUND	Ground	Ground		Ground
S23	Rcvr+			RX3+	PETp2	PETp3		TX1+
S24	Rcvr-			RX3-	PETn2	PETn3		TX1-
S25	Ground			GROUND	Ground	Ground		Ground
S26	Xmtr-			TX3-	PERn2	PERn3		
S27	Xmtr+			TX3+	PERp2	PERp3		
S28	Ground			GROUND	Ground	Ground		Ground

Note: PCIe names the signals on the device from the host perspective i.e. for PCIe products, a receiver on the device has a transmitter signal name.

TABLE 5-3 E SERIES SIGNALS (PLUG)

		SATA	SAS	MultiLink SAS	Quad PCIe *1 *2 *3	SFF-TA-1001 *1 *2 *3	OCP Kinetic	SNIA Native NVMe-oF
E1					REFCLKB+	REFCLKB+		
E2					REFCLKB-	REFCLKB-		
E3	+3.3V				+3.3 Vaux	+3.3V aux		+3.3V aux
E4					CLKREQ#/ PERSTB#	PERSTB#		ENRST1#
E5					PERST#	PERST#		ENRST#
E6					Reserved	IFDET2#		IFDET2# = Ground
E7					REFCLK+	REFCLK+		
E8					REFCLK-	REFCLK-		
E9					Ground	Ground		Ground
E10	Rcvr+				PETp0			
E11	Rcvr-				PETn0			
E12	Ground				Ground	Ground		Ground
E13	Xmtr-				PERn0			RX0-
E14	Xmtr+				PERp0			RX0+
E15	Ground				Ground	Ground		Ground
E16					Reserved	HPT1		HPT1 = Open
E17	Rcvr+				PETp3			
E18	Rcvr-				PETn3			
E19	Ground				Ground	Ground		Ground
E20	Xmtr-				PERn3			RX1-
E21	Xmtr+				PERp3			RX1+
E22	Ground				Ground	Ground		Ground
E23					SMBCLK	SMBCLK		SMBCLK
E24					SMBDAT	SMBDAT		SMBDAT
E25					DualPort En#	DualPort En#		DualPort En#

6. PCIe Dual Port Lane Usage

For PCIe Dual Port mode, both Quad PCIe and SFF-TA-1001 redefine some of the PCIe lanes to explicitly be a second port with the secondary port starting the lane numbering at 0. The below table describes the Port and Lane numbering change when in dual port mode.

TABLE 6-1 PCIE DUAL PORT LANE USAGE

SFF-TA-1001 Dual Port S15=GND, E16=Open	Quad PCIe Dual Port S15=Open, E16=Open	PCIe Lane	
		E25 = Open	E25 = GND
S[2-6]	E[10-14]	PortA Lane0	
S[17-21]	S[17-21]	PortA Lane1	
S[9-13]	S[23-27]	PortA Lane2	PortB Lane0
S[23-27]	E[17-21]	PortA Lane3	PortB Lane1

Note: Single lane (x1) port usage shall use Lane0.

7. SNIA Native NVMe-oF Dual Port Lane Usage

For SNIA Native NVMe-oF Dual Port mode, DualPortEn# redefines how the two Ethernet lanes are configured. Table 7-1 describes the Port and Lane numbering change when in dual port mode.

TABLE 7-1 SNIA NATIVE NVME-OF DUAL PORT LANE USAGE

SNIA Native NVMe-oF Lane	E25 = GND	E25 = Open
S[17-18]	TX0	TX0.1
S[23-24]	TX1	TX0.2
E[13-14]	RX0	RX0.1
E[20-21]	RX1	RX0.2