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SFF-TA-1009

Specification for

Enterprise and Datacenter SSD Pin and Signal Specification

Rev 2.0 May 22, 2018

Secretariat: SFF TA TWG

Abstract: This specification defines the pin list and pin placement, function of the pins, SSD specific electrical requirements, and specific features of enterprise and datacenter based SSDs. This specification relies on SFF-TA-1002 for the connector mechanicals and SFF-TA-1006, SFF-TA-1007, and SFF-TA-1008 form factor specifications for the form factor mechanicals.

This specification provides a common reference for host systems manufacturers, host system integrators, and device suppliers. This specification originates from Enterprise and Datacenter SSD Form Factor Working Group (EDSFF).

The description of the details in this specification does not assure that the specific component is actually available from device suppliers. If such a device is supplied it shall comply with this specification to achieve interoperability between device suppliers.

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Change History

1.0 March 23, 2018
- Initial release

2.0 May 22, 2018
- Change to TX/RX ordering and changed table orientation for tables 4-4, 4-5, and 4-6.
- Clarification to power sequencing requirements (section 5.2).
- Update to unused reference clock guidance (section 4.2.2).
- Minor editorial and formatting changes throughout document.

Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors. The SFF Committee provided a forum for system integrators and vendors to define the form factor of disk drives.

During their definition, other activities were suggested because participants in SFF faced more challenges than the form factors. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

In July 2016, the SFF Committee transitioned to SNIA (Storage Networking Industry Association), as a TA (Technology Affiliate) TWG (Technical Work Group).

Industry consensus is not a requirement to publish a specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF meets during the T10 (see www.t10.org) and T11 (see www.t11.org) weeks, and SSWGs (Specific Subject Working Groups) are held at the convenience of the participants.

Many of the specifications developed by SFF have either been incorporated into standards or adopted as standards by ANSI, EIA, JEDEC and SAE.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at:

http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee is contained in the document SFF-8000 which can be found at:

http://www.snia.org/sff/specifications

Suggestions for improvement of this specification will be welcome, they should be submitted to:

http://www.snia.org/feedback

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1. Scope

The following specification defines the requirements for a Solid State Storage Device (SSD) that is optimized for Enterprise and Datacenter applications.

1.1 Application Specific Criteria

This specification defines the pin list and pin placement, function of the pins, SSD specific electrical requirements, and specific features of enterprise and datacenter based SSDs. This specification relies on SFF-TA-1002 for the connector mechanicals and SFF-TA-1006, SFF-TA-1007, and SFF-TA-1008 form factor specifications for the form factor mechanicals.

1.2 Copyright

1.3 Disclaimer

The information contained in this publication is subject to change without notice. The SNIA makes no warranty of any kind with regard to this specification, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The SNIA shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this specification.

Suggestions for revisions should be directed to http://www.snia.org/feedback.

2. References

2.1 Industry Documents

- PCI Express® (PCIe) Base Specification, Revision 4.0
- PCI Express® (PCIe) Card Electromechanical Specification, Revision 3.0
- PCI Express® (PCIe) Mini Card Electromechanical Specification, Revision 1.1
- System Management Bus (SMBus) Specification, Version 2.0, August 3, 2000
- SNIA SFF-TA-1002 Card Edge multilane protocol agnostic connector specification
- SNIA SFF-TA-1006 Enterprise and Datacenter 1U Short SSD Form Factor
- SNIA SFF-TA-1007 Enterprise and Datacenter 1U Long SSD Form Factor
- SNIA SFF-TA-1008 Enterprise and Datacenter Form Factor for a 3” Media Device
- SNIA SFF-8489 Serial GPIO IBPI

2.2 Sources

There are several projects active within the SFF TWG. The complete list of specifications which have been completed or are still being worked on is contained in the document SFF-8000 which can be found at http://www.snia.org/sff/specifications.

Copies of PCIe standards may be purchased from the PCI-SIG (http://www.pcisig.com).

Copies of SMBus standards may be purchased from the System Management Interface Forum, Inc (http://smbus.org).

2.3 Conventions

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

2.4 Definitions

For the purpose of this SFF Specification, the following definitions apply:

Card: Refers to the device plugged into a connector

Contact Sequence: The order of events that a device card edge pin makes physical contact to the host connector pin.

Device: Refers to the interface slave

EDSFF: Enterprise and Datacenter Form Factor. This refers to the mechanical connectors and devices that this document references.

Host: Refers to the interface source or master

NVM: Acronym for Non-Volatile Memory

SRIS: Acronym for Separate Reference clock Independent Spread spectrum clocking. This is a PCI Express feature that allows independent reference clocks for host and device. In this implementation, the host does not need to provide the reference clock. Each independent source supports Spread Spectrum Clocking (SSC).

SRNS: Acronym for Separate Reference clock with No Spread spectrum clocking. This is a PCI Express feature that allows independent reference clocks for host and device. In this implementation, the host does not need to provide the reference clock. Spread Spectrum Clocking (SSC) is not supported by either source.

SSD: Acronym for Solid State Drive

3. General Description

The Enterprise and Datacenter SSD Pin and Signal specification is meant for serviceable SSDs that connect electrically to the system through a card edge connector as defined in SFF-TA-1002. The following features are supported:

- Support for multiple form factors:
  - SFF-TA-1006 Enterprise and Datacenter 1U Short SSD Form Factor
  - SFF-TA-1007 Enterprise and Datacenter 1U Long SSD Form Factor
  - SFF-TA-1008 Enterprise and Datacenter Form Factor for a 3” Media Device
- PCIe support for existing and future specifications
  - Supports 4.0 specification (up to 16GTs signaling) and intended for future signaling to 32 GTs.
  - Single port operation: One (1), x4 or x8 or x16 PCIe port supported
  - Dual port: Two (2) x2 or two (2) x4 or two (2) x8 PCIe ports supported
- 3 connector types using SFF-TA-1002
  - A 56 pin receptacle supporting Four (4) Tx and Rx PCIe lanes.
  - A 84 pin receptacle supporting Eight (8) Tx and Rx PCIe lanes.
  - A 140 pin receptacle supporting Sixteen (16) Tx and Rx PCIe lanes.
- Hot-plug Support
- Common clock, SRIS, or SRNS support is supported by both host and device
- Support for out of band management over SMBus
- Connector supports up to 70W sustained operation (actual power is specified per form factor).

4. Signal List

This chapter covers the signal summary, definitions, and signal placement for the EDSFF connectors. Signal directions (I/O) are with respect to the host and are mandatory unless otherwise specified.

TABLE 4-1. EDSFF CONNECTOR PIN LIST

Interface	Signal Name	Host I/O	Function
Power and Grounds	12 V	O	+12 V source
	3.3 Vaux	O	+3.3 V Source
	GND	O	Return current path
PCIe	PETp0, PETn0	O	PCIe TX Differential signals defined by the *PCI Express Card Electromechanical Specification*. PETp/n[0..3] are supported in the x4, x8, and x16 connectors. PETp/n[4..7] are supported with the x8 and x16 connectors. PETp/n[8..15] are supported only with the x16 connector.
	PETp1, PETn1		
	PETp2, PETn2		
	PETp3, PETn3		
	PETp4, PETn4		
	PETp5, PETn5		
	PETp6, PETn6		
	PETp7, PETn7		
	PETp8, PETn8		
	PETp9, PETn9		
	PETp10, PETn10		
	PETp11, PETn11		
	PETp12, PETn12		
	PETp13, PETn13		
	PETp14, PETn14		
	PETp15, PETn15		
	PERp0, PERn0	I	PCIe RX Differential signals defined by the *PCI Express Card Electromechanical Specification*. PERp/n[0..3] are supported in the x4, x8, and x16 connectors. PERp/n[4..7] are supported with the x8 and x16 connectors. PERp/n[8..15] are supported only with the x16 connector.
	PERp1, PERn1		
	PERp2, PERn2		
	PERp3, PERn3		
	PERp4, PERn4		
	PERp5, PERn5		
	PERp6, PERn6		
	PERp7, PERn7		
	PERp8, PERn8		
	PERp9, PERn9		
	PERp10, PERn10		
	PERp11, PERn11		
	PERp12, PERn12		
	PERp13, PERn13		
	PERp14, PERn14		
	PERp15, PERn15		
	REFCLKp0, REFCLKn0	O	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Base Specification*. Note: This reference clock is the common ref clock that shall be used with PCIe.
	PERST0#	O	PE-Reset is a functional reset to the device as defined as PERST# by the *PCI Express Base Specification*. The host shall provide PERST0# to the device.

Interface	Signal Name	Host I/O	Function
	REFCLKp1, REFCLKn1	O	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Base Specification*. This clock is for dual port mode only and is only used if DUALPORTEN# is low. Note: This reference clock is the common ref clock that shall be used with PCIe.
	PERST1#/CLKREQ#	I/O	PERST1#: PE-Reset is a functional reset to the device as defined as PERST# by the *PCI Express Base Specification*. If dual port mode is supported by the device, PERST1# is only used when DUALPORTEN# is low. CLKREQ#: Clock Request is an optional reference clock request signal as defined as CLKREQ# by the *PCI Express Base Specification.* It may be supported by a device in single port mode only. If CLKREQ# is supported by the host and the device, the signal is Open Drain with a pull up on host. CLKREQ# is active low and used by L1 PM Substates.
Sideband Signals	PRSNT0#	I	Active low signal. This signal indicates to the host that the device is electrically attached.
	PRSNT1#	I	PRSNT1#: Active low signal. This signal is in the x8 connector as a 2nd presence signal to indicate to the host that the device is electrically attached.
	PRSNT2#	I	PRSNT2#: Active low signal. This signal is in the x16 connector as a 3rd presence signal to indicate to the host that the device is electrically attached.
	SMBCLK	O	SMBus Clock, Open Drain with pull-up on host.
	SMBDATA	I/O	SMBus Data, Open Drain with pull-up on host.
	SMBRST#	O	Active low signal: SMBRST# is a reset for the management interface. It shall operate independently of PERST[0..1]#.
	DUALPORTEN#	O	Active low signal. This signal indicates if dual port mode is supported by the host.
	LED/ACTIVITY	O or I	LED: Active high output signal. This signal is used to drive the amber LED state from the host to the device. ACTIVITY: Active high input signal. This signal allows the device to provide status of data transfer to the host. The ACTIVITY function is reserved for future use.
	PWRDIS	O	Power Disable. Active high. This signal notifies the device to turn off all systems connected to 12 V power.
	MFG	O	Manufacturing Mode for device. Host should not use/connect.
	RFU		Reserved for Future Use

4.1 Power and Grounds

The EDSFF connector supports a 12 V power source to power the majority of the device with a smaller 3.3 Vaux power source to provide power to manage sideband communication. Both voltages are expected to be powered while the device is in the system.

4.2 PCIe Signals

4.2.1 High Speed Signals (PERp/n, PETp/n)

The PCIe interface supports a minimum of one (1) lane. A lane consists of an input and output differential pair. Refer to the PCI Express Base Specification for more details on the functional requirements of the interface signals.

The PET signals (PETp[0..15], PETn[0..15]) on the host shall connect to the PET signals on the connector and the PER signals on the Device Logic. The PER signals (PERp[0..15], PERn[0..15]) on the host shall connect to the PER signals on the connector and the PET signals on the Device Logic. For a high level wiring diagram, see Figure 4-1.

Lane Polarity Inversion shall be supported on both the host and the device to simplify host and device PCB trace routing constraints.

Lane reversal may be supported on both the host and device. If it is supported, then the transmitting and receiving lanes shall be connected using the same ordering.

Table 4-2 shows the connectivity in both single and dual port systems. Dual Port usage is enabled with DUALPORTEN# assertion.

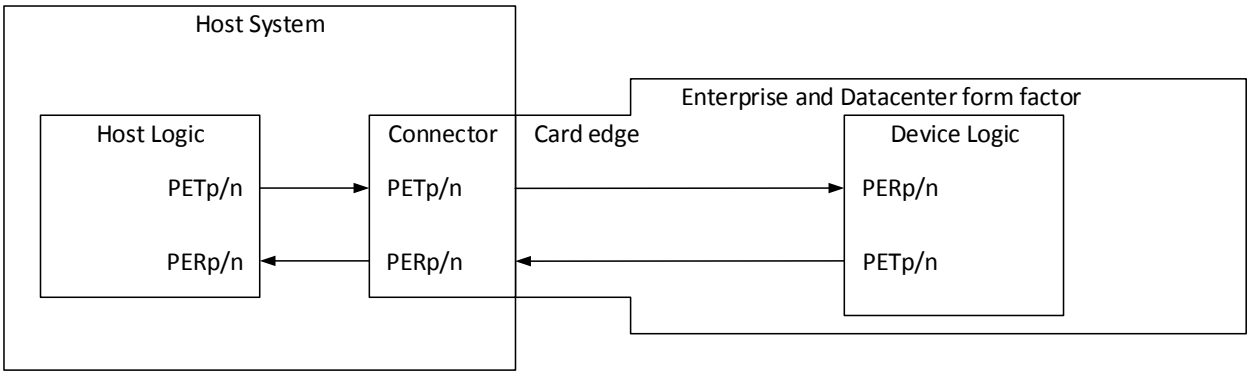

FIGURE 4-1. PET AND PER SIGNAL CONNECTIVITY BETWEEN HOST AND DEVICE

TABLE 4-2. PCIE LANES CONNECTIVITY IN SINGLE AND DUAL PORT IMPLEMENTATIONS (WITHOUT LANE REVERSAL)

PCIe lanes	x4 Single Port (1 port x4)	x4 Dual Port (2 ports x2)	X8 Single Port (1 port x8)	x8 Dual Port (2 ports x4)	x16 Single Port (1 port x16)	x16 Dual Port (2 ports x8)
PERp0, PERn0, PETp0, PETn0	Port A, lane 0	Port A, lane 0	Port A, lane 0	Port A, lane 0	Port A, lane 0	Port A, lane 0
PERp1, PERn1, PETp1, PETn1	Port A, lane 1	Port A, lane 1	Port A, lane 1	Port A, lane 1	Port A, lane 1	Port A, lane 1
PERp2, PERn2, PETp2, PETn2	Port A, lane 2	Port B, lane 0	Port A, lane 2	Port B, lane 0	Port A, lane 2	Port B, lane 0
PERp3, PERn3, PETp3, PETn3	Port A, lane 3	Port B, lane 1	Port A, lane 3	Port B, lane 1	Port A, lane 3	Port B, lane 1
PERp4, PERn4, PETp4, PETn4	No connect	No connect	Port A, lane 4	Port A, lane 2	Port A, lane 4	Port A, lane 2
PERp5, PERn5, PETp5, PETn5	No connect	No connect	Port A, lane 5	Port A, lane 3	Port A, lane 5	Port A, lane 3
PERp6, PERn6, PETp6, PETn6	No connect	No connect	Port A, lane 6	Port B, lane 2	Port A, lane 6	Port B, lane 2
PERp7, PERn7, PETp7, PETn7	No connect	No connect	Port A, lane 7	Port B, lane 3	Port A, lane 7	Port B, lane 3
PERp8, PERn8, PETp8, PETn8	No connect	No connect	No connect	No connect	Port A, lane 8	Port A, lane 4
PERp9, PERn9, PETp9, PETn9	No connect	No connect	No connect	No connect	Port A, lane 9	Port A, lane 5
PERp10, PERn10, PETp10, PETn10	No connect	No connect	No connect	No connect	Port A, lane 10	Port B, lane 4
PERp11, PERn11, PETp11, PETn11	No connect	No connect	No connect	No connect	Port A, lane 11	Port B, lane 5
PERp12, PERn12, PETp12, PETn12	No connect	No connect	No connect	No connect	Port A, lane12	Port A, lane 6
PERp13, PERn13, PETp13, PETn13	No connect	No connect	No connect	No connect	Port A, lane 13	Port A, lane 7
PERp14, PERn14, PETp14, PETn14	No connect	No connect	No connect	No connect	Port A, lane 14	Port B, lane 6
PERp15, PERn15, PETp15, PETn15	No connect	No connect	No connect	No connect	Port A, lane 15	Port B, lane 7

4.2.2 Reference Clock

The REFCLKp/REFCLKn signals are used to assist the synchronization of the device's PCI Express interface timing circuits. Refer to the *PCI Express Card Base Specification* for more details on the functional and tolerance requirements for the reference clock signals.

There are two sets of clock pairs. In a single port implementation (indicated by DUALPORTEN# de-asserted), only REFCLKp0 and REFCLKn0 are used. In a dual port implementation (indicated by DUALPORTEN# asserted), REFCLKp0 and REFCLKn0 connects to Port A while REFCLKp1 and REFCLKn1 connects to port B.

If SRIS or SRNS is supported by both the system and the device then the reference clock may not be connected on the host. The reference clock shall be the default configuration on the device. If the reference clock is not detected upon detecting PERST# de-assertion, then the SRIS/SRNS supported device shall switch into SRIS/SRNS mode. The device shall only enter SRNS if the device is configured for this usage through a method outside the scope of this version of the specification.

It is recommended that the host terminates the reference clock signals at the connector with a pull-down resistor if the clocks are not provided by the host.

4.2.3 PERST#

The PERST# signal shall operate as a fundamental reset for PCI Express driven by the host. Refer to the *PCI Express Base Specification* for more details on the functional requirements. PERST0# shall be implemented by the host.

In single port mode (indicated by DUALPORTEN# de-asserted), PERST0# is used. In this single port mode, PERST1# is not used; however, the CLKREQ# function may be used. If neither function (i.e. PERST1# or CLKREQ#) is supported by the host, then the signal should be tied to ground.
In dual port mode (indicated by DUALPORTEN# asserted), PERST0# connects to Port A and PERST1# connects to Port B.

4.2.4 CLKREQ#

The CLKREQ# signal is used by the L1 PM Substates mechanism. In this case, CLKREQ# may be asserted by either the system or the device to initiate an L1 exit. See the PCI Express Base Specification for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.

If DUALPORTEN# is asserted, CLKREQ# shall not be used.

4.3 Side Band Signals

4.3.1 PRSNT[0..2]#

The PRSNT# signals are used to indicate physical presence of a device plugged into the connector. The x4 connector utilizes only one signal (PRSNT0#). The x8 connector utilizes a second signal (PRSNT1#). The x16 connector utilizes a third signal (PRSNT2#). These shall be connected to ground on the device.

4.3.2 SMBus Interface

The SMBus interface is intended as a side band management interface. SMBus is a two-wire interface through which various system component chips are able to communicate with each other and with rest of the system. It is based on I2C principles of operation. Refer to the SMBus Specification for details of the operation.

SMBus is an Open Drain interface. The pull-ups for SMBDAT and SMBCLK shall be on the host.
The SMBCLK signal provides the clock signaling from the SMBus master to the SMBus slave device to be able to decode the data on the SMBDATA line.

The SMBDATA signal is used to transfer the data packets between the host and the device according to the SMBus protocol.

4.3.3 SMBRST#

The SMBRST# signal shall place the SMBus management interface of the SSD in an initial state without interrupting the PCIe link or losing NVMe controller data. Details of what is reset and the implementation on the device is not defined in this specification.

There are usages where the host may have SMBus connected to multiple devices. If the host asserts SMBRST#, then the device shall keep the SMBCLK and SMBDATA in a high impedance state and ignore any communication on SMBCLK and SMBDATA.

Cycling 3.3 Vaux shall not be used by the host to reset the SMBus.

4.3.4 DUALPORTEN#

The SSD shall be configured by the host as a single port or dual port device using the DUALPORTEN# signal. DUALPORTEN# shall be asserted or de-asserted by the host prior to 12 V power being applied. Any change to DUALPORTEN# state requires a Power cycle. See Table 4-3 for expected functionality.

TABLE 4-3. SSD CONFIGURATION FOR SINGLE PORT VS. DUAL PORT

System	DUALPORTEN# state	x4 SSD	x8 SSD	X16 SSD
x4	De-asserted	Single Port x4	Single Port x4	Single Port x4
	Asserted	Dual Port x2	Dual Port x2	Dual Port x2
x8	De-asserted	Single Port x4	Single Port x8	Single Port x8
	Asserted	Dual Port x2	Dual Port x4	Dual Port x4
X16	De-asserted	Single Port x4	Single Port x8	Single Port x16
	Asserted	Dual Port x2	Dual Port x4	Dual Port x8

4.3.5 LED/ACTIVITY

The LED signal is asserted by the host to drive an amber LED on the device. The host use of the LED signal is optional. Details of the usage of LED are beyond the scope of this specification.

The ACTIVITY signal is asserted by the device to indicate SSD activity. The host use of the ACTIVITY signal is not defined in this revision of the specification.

The default mode of the LED/ACTIVITY signal for the device in the absence of any configuration shall be LED mode, which is an input to the device. To prevent contention, if the host supports the LED/ACTIVITY signal, then it shall support the same mode as set in the device.

4.3.6 PWRDIS

The PWRDIS signal is asserted to tell the device to shut off power to all circuitry connected to the 12 V power supply. When PWRDIS is asserted, the host shall allow the device time to shut down. When PWRDIS is de-asserted, the host shall allow the device to settle before de-asserting PERST0#. See Sections 5.2 and 5.3 for more details.

4.3.7 MFG

The MFG signal is used for device manufacturing only and details are beyond the scope of this specification. This signal shall be electrically no-connect on non-manufacturing hosts.

Post device manufacturing, the device manufacturer should ensure the pin is disabled.

4.3.8 RFU

Signals documented as RFU are reserved for future use. These pins shall be electrically no-connect on the host and the device. These pins are reserved for future assignment as functional signals.

4.4 Connector pinout definitions

The following tables show the signal pinouts for the connector. These pinouts are shown from the host point of view. Hot plug shall be supported by the device. The contact sequence for each pinout is shown to indicate the ordering of pins making contact to the host. For more details, please refer to *SFF-TA-1002 Card Edge multilane protocol agnostic connector specification*.

- Table 4-4 lists the pinout for the x4 connector
- Table 4-5 lists the pinout for the x8 connector
- Table 4-6 lists the pinout for the x16 connector

TABLE 4-4. EDSFF X4 DEVICE EDGE PINOUT

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6
B7	2nd mate	MFG	SMBCLK	2nd mate	A7
B8	2nd mate	RFU	SMBDAT	2nd mate	A8
B9	2nd mate	DUALPORTEN#	SMBRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED#/ACTIVITY	2nd mate	A10
B11	2nd mate	3.3 VAux	PERST1#/CLKREQ#	2nd mate	A11
B12	2nd mate	PWRDIS	PRSNT0#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28

TABLE 4-5. EDSFF X8 DEVICE EDGE PINOUT

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6
B7	2nd mate	MFG	SMBCLK	2nd mate	A7
B8	2nd mate	RFU	SMBDAT	2nd mate	A8
B9	2nd mate	DUALPORTEN#	SMBRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED#/ACTIVITY	2nd mate	A10
B11	2nd mate	3.3 VAux	PERST1#/CLKREQ#	2nd mate	A11
B12	2nd mate	PWRDIS	PRSNT0#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28
		Key	Key		
B29	1st mate	GND	GND	1st mate	A29
B30	2nd mate	PETn4	PERn4	2nd mate	A30
B31	2nd mate	PETp4	PERp4	2nd mate	A31
B32	1st mate	GND	GND	1st mate	A32
B33	2nd mate	PETn5	PERn5	2nd mate	A33
B34	2nd mate	PETp5	PERp5	2nd mate	A34
B35	1st mate	GND	GND	1st mate	A35
B36	2nd mate	PETn6	PERn6	2nd mate	A36
B37	2nd mate	PETp6	PERp6	2nd mate	A37

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B38	1st mate	GND	GND	1st mate	A38
B39	2nd mate	PETn7	PERn7	2nd mate	A39
B40	2nd mate	PETp7	PERp7	2nd mate	A40
B41	1st mate	GND	GND	1st mate	A41
B42	2nd mate	PRSNT1#	RFU	2nd mate	A42

TABLE 4-6. EDSFF X16 DEVICE EDGE PINOUT

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6
B7	2nd mate	MFG	SMBCLK	2nd mate	A7
B8	2nd mate	RFU	SMBDAT	2nd mate	A8
B9	2nd mate	DUALPORTEN#	SMBRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED#/ACTIVITY	2nd mate	A10
B11	2nd mate	3.3 VAux	PERST1#/CLKREQ#	2nd mate	A11
B12	2nd mate	PWRDIS	PRSNT0#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28
		Key	Key		
B29	1st mate	GND	GND	1st mate	A29
B30	2nd mate	PETn4	PERn4	2nd mate	A30
B31	2nd mate	PETp4	PERp4	2nd mate	A31
B32	1st mate	GND	GND	1st mate	A32
B33	2nd mate	PETn5	PERn5	2nd mate	A33
B34	2nd mate	PETp5	PERp5	2nd mate	A34
B35	1st mate	GND	GND	1st mate	A35
B36	2nd mate	PETn6	PERn6	2nd mate	A36
B37	2nd mate	PETp6	PERp6	2nd mate	A37

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B38	1st mate	GND	GND	1st mate	A38
B39	2nd mate	PETn7	PERn7	2nd mate	A39
B40	2nd mate	PETp7	PERp7	2nd mate	A40
B41	1st mate	GND	GND	1st mate	A41
B42	2nd mate	PRSNT1#	RFU	2nd mate	A42
		Key	Key		
B43	1st mate	GND	GND	1st mate	A43
B44	2nd mate	PETn8	PERn8	2nd mate	A44
B45	2nd mate	PETp8	PERp8	2nd mate	A45
B46	1st mate	GND	GND	1st mate	A46
B47	2nd mate	PETn9	PERn9	2nd mate	A47
B48	2nd mate	PETp9	PERp9	2nd mate	A48
B49	1st mate	GND	GND	1st mate	A49
B50	2nd mate	PETn10	PERn10	2nd mate	A50
B51	2nd mate	PETp10	PERp10	2nd mate	A51
B52	1st mate	GND	GND	1st mate	A52
B53	2nd mate	PETn11	PERn11	2nd mate	A53
B54	2nd mate	PETp11	PERp11	2nd mate	A54
B55	1st mate	GND	GND	1st mate	A55
B56	2nd mate	PETn12	PERn12	2nd mate	A56
B57	2nd mate	PETp12	PERp12	2nd mate	A57
B58	1st mate	GND	GND	1st mate	A58
B59	2nd mate	PETn13	PERn13	2nd mate	A59
B60	2nd mate	PETp13	PERp13	2nd mate	A60
B61	1st mate	GND	GND	1st mate	A61
B62	2nd mate	PETn14	PERn14	2nd mate	A62
B63	2nd mate	PETp14	PERp14	2nd mate	A63
B64	1st mate	GND	GND	1st mate	A64
B65	2nd mate	PETn15	PERn15	2nd mate	A65
B66	2nd mate	PETp15	PERp15	2nd mate	A66
B67	1st mate	GND	GND	1st mate	A67
B68	2nd mate	RFU	RFU	2nd mate	A68
B69	2nd mate	RFU	RFU	2nd mate	A69
B70	2nd mate	PRSNT2#	RFU	2nd mate	A70

5. Electrical Requirements

This chapter covers the electrical requirements of the EDSFF devices. Unless otherwise specified, follow the PCI Express Card Electromechanical Specification.

5.1 Power Supply Requirements

EDSFF devices shall get the majority of its power from the 12 V pins. Table 5-1 provides the 12 V power supply requirements and Table 5-2 provides the 3.3V aux power supply requirements.

TABLE 5-1. 12 V POWER SUPPLY REQUIREMENTS

Symbol	Parameter	Value	Unit	Comment
12Vtol	12 V supply Tolerance	10.8 to 13.2	V	Includes Ripple.
12Vpmax	Maximum Power	70	W	Continuous (Average) power over any 1 s period. Refer to the form factor specifications for maximum form factor capabilities.
12Vinrush	Max inrush current	2	A	Maximum current load presented by the device 12V supply to the host receptacle over any 5us period during the initial power-up ramp to 90% of the device operating voltage.
12Vcap	Max capacitance for inrush	5	uF	Capacitance system sees during the initial power-up ramp to 90% of the device operating voltage.

TABLE 5-2. 3.3 VAUX POWER SUPPLY REQUIREMENTS

Symbol	Parameter	Value	Unit	Comment
33Vauxtol	3.3 Vaux supply Tolerance	2.970 to 3.465	V	Includes Ripple.
33VauxIpin	3.3 Vaux pin current	25	mA	Average current.
33Vauxcap	Max capacitance for inrush	5	uF	For inrush current limit.

5.2 Timings

There are no power sequencing requirements for 12 V and 3.3 Vaux. These two voltages are independent from each other. If 3.3 Vaux is not present but 12 V is present and SMBRST# and PWRDIS are de-asserted, then the PCIe link shall be fully functional and the SMBus interface may be fully functional. For other timing requirements, see Table 5-3.

TABLE 5-3. EDSFF DEVICE TIMING REQUIREMENTS

Parameter	Description	Min	Max	Units
Tsmbrst	SMBRST# assertion time	1		ms
Tpwrdis	PWRDIS assertion time	5		s
Tdisrst	PWRDIS de-assertion time to PERST# de-assertion	100		ms

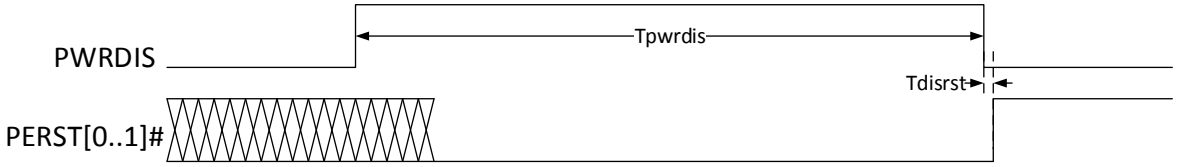

FIGURE 5-1. EDSFF DEVICE TIMING DIAGRAM FOR PWRDIS

5.3 3.3 Vaux Logic Signal Requirements

The 3.3 V device logic levels for single-ended digital signals (PERST[0..1]#, CLKREQ#, PRSNT[0..2]#, SMBRST#, DUALPORTEN#, LED/ACTIVITY, PWRDIS) are defined in Table 5-4. For SMBus signals (SMBCLK, SMBDAT) logic levels, refer to the *System Management Bus (SMBus) Specification, Version 2.0*.

TABLE 5-4. DC SPECIFICATION FOR 3.3 V LOGIC SIGNALING

Symbol	Parameter	Condition	Min	Max	Unit	Notes
Vih1	Input High Voltage		2.0	3.465	V	
Vil1	Input Low Voltage		-0.3	0.8	V	
Vih2	Input High Voltage for LED/ACTIVITY		3.0	3.465	V	1,2
Voh	Output High Voltage	4.0 mA		3.465	V	
Vol	Output Low Voltage	4.0 mA		0.2	V	
Iled	LED/ACTIVITY input current			20	mA	1
Iin	Input Leakage Current	0 V to 3.3 V	-10	10	µA	
Iout	Output Leakage Current	0 V to 3.3 V	-50	50	µA	
Cin	Input Pin Capacitance			30	pF	
Cout	Output Pin Capacitance			30	pF	

Notes:

1. LED/ACTIVITY signal when it is in the LED signal mode.
2. Voltage is based on Iled current.

6. LEDs

The following section covers the usage and details of the LEDs on EDSFF devices. For EDSFF devices, there shall be two LEDs supported; a green LED and an amber LED. Table 6-1 defines the LED requirements.

TABLE 6-1. LED REQUIREMENTS

LED high level description	Green	Amber
Driven by	Device	Host (LED/ACTIVITY signal in LED mode)
Function	Power, Activity	Host defined
Wavelength (nm)	520 to 530	590 to 600
Point Intensity[1] (mcd)	Minimum: 45 Typical: 60	Minimum: 120 Typical: 150

Notes:

1. The point intensity is measured at the location defined by the form factor specification.

6.1 Green LED

The green LED is driven and completely controlled by the device. The two functions for this LED are defined as follows in Table 6-2:

- Power: This function indicates if device has power and has no issues with its power regulation.
- Activity: This function indicates if the device is being used. Note that the activity function defined for this LED is not related to the mode of the LED/Activity signal pin.

TABLE 6-2. LED AND SSD STATE PER FUNCTION FOR GREEN LED

Function	LED state	Device State
Power On	“On”	Device is powered, no activity occurring
Activity	Follow SFF-8489 for activity (4 Hz)	Device is powered, activity occurring
Power Off	“Off”	Device is not powered

6.2 Amber LED

The amber LED is driven by the host signal through the LED/ACTIVITY pin. A current limiting resistor shall be in the device to protect it against overcurrent. The functionality and blink rates of this LED are beyond the scope of this specification. Host manufacturers are recommended to reference SFF-8489 for blink and status definitions.