SFF-TA-1009

Specification for

Enterprise and Datacenter Standard Form Factor Pin and Signal Specification

Rev 4.0.1 January 6, 2025May 3, 2024

SECRETARIAT: SFF TA TWG

This specification is made available for public review at https://www.snia.org/sff/specifications. Comments may be submitted at https://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

This specification provides a common reference for host systems manufacturers, host system integrators, and device suppliers. This specification originates from Enterprise and Datacenter SSD Form Factor Working Group (EDSFF). With non-SSD devices also using EDSFF and agreement from the EDSFF Working Group, the SFF TA TWG changed EDSFF to Enterprise and Datacenter Standard Form Factor.

This document has been released by SNIA. The SFF TWG believes that the ideas, methodologies, and technologies described in this document are technically accurate and are appropriate for widespread distribution.

The description of the details in this specification does not assure that the specific component is available from device suppliers. If such a device is supplied, then it shall comply with this specification to achieve interoperability between device suppliers.

ABSTRACT: This specification defines the pin list and pin placement, function of the pins, device specific electrical requirements, and specific features of enterprise and datacenter-based devices. This specification relies on SFF-TA-1002 for the connector mechanicals and SFF-TA-1006, SFF-TA-1007, and SFF-TA-1008 form factor specifications for the form factor mechanicals.

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Additional information can be found at the following locations:

- Results of IP Disclosures: https://www.snia.org/sffdisclosures
- SNIA IP Policy: https://www.snia.org/ippolicy

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Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, as well as since SFF's transition to SNIA in 2016, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/sff/join.

Revision History

Rev 1.0 *March 23, 2018:*
- Initial release

Rev 2.0 *May 22, 2018*:
- Change to TX/RX ordering and changed table orientation for tables 4-4, 4-5, and 4-6.
- Clarification to power sequencing requirements (section 5.2).
- Update to unused reference clock guidance (section 4.2.2).
- Minor editorial and formatting changes throughout document.

Rev 3.0 *March 19, 2021*:
- Name change to Enterprise and Datacenter Standard Form Factor
- Revised to new format used in SFF
- Updated Revision of reference documents
- Editorial cleanup throughout document
- Minor clarifications made throughout document
- Power and Grounds: Additional requirements and expectations added to power sequencing
- PCIe signals: Clarifications made to PCIe single port mode below x4
- CLKREQ: Clarifications made to CLKREQ# and PERST1# behavior in relation to DUALPORTEN#
- Addition of Pull-up/Pull-down locations and values to signals requiring Pull-up/Pull-down
- SMBus: Clarification on device and host pull-ups
- SMRST#: Clarifications made to SMRST behavior
- DUALPORTEN#: Replaced table on dual port vs. single port usage with simpler definition
- LED/ACTIVITY: ACTIVITY portion removed. Spec will no longer support the use of ACTIVITY
- Errata fix in tables 4-4, 4-5, and 4-6 to rename LED#/Activity to LED to match functional definition along with title of these tables. Changed 3.3 VAux to 3.3 Vaux
- 12V supply requirements: Added new requirements for Max sustained power, Initial power, max power, and slew rate
- 3.3 Vaux supply requirements: Clarified measurement time for current.
- Timing requirements: Added specs for SMRST#, PWRDIS de-assertion time and PERST to 12V power
- 3.3V Logic signaling: Added SMBus to signals covered and its operating voltage, a new Vil for LEDs, updated leakage currents, and added notes.
- Added Amber/Blue LED for SFF-TA-1008 along with description, values, and example schematics
- LED Requirements: relaxed wavelength and point intensity ranges
- Clarified Amber LED usage for SFF-TA-1006 and SFF-TA-1007
- Section 8 added for Electrical Requirements including S-parameters and eye masks

Rev 3.1 *January 6, 2023*:
- Added I3C Basic signal requirements, voltage details, and transition timings.
- Added I3CCLK/I3CDATA to pin list, pin description and shared places with SMBCLK/SMBDATA
- Changed name of SMBRST# to SMRST#
- Added NIC signals to pin list for support of a 4C+ pin out.
- Added NIC_DETECT signal, modified RSVD and MFG definitions for 4C+ usage.
- Added 4C+ pin out.
- Added clarification on LED behavior for activity behavior and PWRDIS for the amber/blue LED
- Added informative section on I3C basic implementation including transition flow

- Added informative NIC implementation section including signal definitions and other notes. Clarified usage where pins are muxed with non 4C+ signals.

Rev 4.0 *May 3, 2024*:

- Added USB 2.0 signals into pin list and NIC signals description
- Clarification on SMBus/I3C Basic state during power cycle
- Comments added for 12Vtol and 12Vpinit in Table 6-1
- Clarification to notes in Table 6-3
- Addition of ILED minimum current in Table 6-4
- Addition of White LED to Section 7
- Added PCIe 6.0 electrical requirements into Section 8 and updated reference to 6.0.
- Added pointers to PCI-SIG ECN for I3C Basic and comment for Tsmb2i3c relation to pull-up
- Editorial cleanup throughout document

Rev 4.0.1 January 6, 2025:

- Boiler plate language changes.
- Corrected SMBus initiator to controller and host/device to controller/target in section 5.3.2
- Errata changes and clarifications to I3C timings in Section 6.4.
- Fixed reference in Section 7.2.1
- Clarified wording around I3C Basic in Section 10

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1. Scope

The following specification defines the requirements for a device that is optimized for Enterprise and Datacenter applications.

1.1 Application Specific Criteria

This specification defines the pin list and pin placement, function of the pins, device specific electrical requirements, and specific features of enterprise and datacenter-based devices. This specification relies on SFF-TA-1002 for the connector mechanicals and SFF-TA-1006, SFF-TA-1007, and SFF-TA-1008 form factor specifications for the form factor mechanicals.

2. References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:
- PCI Express® (PCIe®) Base Specification, revision 6.2 available from https://www.pcisig.com.
- PCI Express® (PCIe®) Card Electromechanical Specification, revision 5.1, Version 1.0 available from https://www.pcisig.com.
- System Management Bus (SMBus) Specification, Version 3.2, available from http://smbus.org.
- SNIA SFF-TA-1002 Card Edge multilane protocol agnostic connector specification available at https://www.snia.org/sff/specifications.
- SNIA SFF-TA-1006 Enterprise and Datacenter 1U Short device Form Factor available at https://www.snia.org/sff/specifications.
- SNIA SFF-TA-1007 Enterprise and Datacenter 1U Long device Form Factor available at https://www.snia.org/sff/specifications.
- SNIA SFF-TA-1008 Enterprise and Datacenter Form Factor for a 3” Media Device available at https://www.snia.org/sff/specifications.
- Compute Express Link™ (CXL™) Specification available from https://www.computeexpresslink.org/
- CIE 127-2007 Measurement of LEDs available at https://www.techstreet.com/cie/searches/29093398
- NVM Express® Base Specification available at https://nvmexpress.org/.
- MIPI™ Alliance Specification for I3C Basic, Version 1.0 available at https://www.mipi.org.
- MIPI™ Alliance Specification I3C Basic Slave Reset Addendum available at https://resources.mipi.org/mipi-i3c-basic-slave-reset-download.
- Open Compute Project OCP NIC 3.0 Design Specification, revision 1.2.0 available at https://www.opencompute.org/wiki/Server/Mezz.
- Distributed Management Task Force (DMTF) DSP0222 Network Controller Sideband Interface (NC-SI) Specification, Rev 1.1.0 available at https://www.dmtf.org/sites/default/files/standards/documents/DSP0222_1.1.0.pdf
- United Serial Bus (USB) Specification, Version 2.0, available from https://usb.org.

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS: Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a. red (i.e., one of the following colors):
    A. crimson; or
    B. pink;
b. blue; or
c. green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1. top;
2. middle; and
3. bottom.

Lists are associated with an introductory paragraph or phrase and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

DIMENSIONING CONVENTIONS: The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Defines the signal on a connector contact when its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes (e.g., entities). If the context of the specification applies the restricted designation, then the restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word, or field (e.g., a restricted byte uses the same value as defined for a reserved byte).

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

EDSFF: Enterprise and Datacenter Standard Form Factor
NVM: Non-Volatile Memory
SSD: Solid State Drive

3.3 Definitions

Card: Refers to the device plugged into a connector

Chiclet: A building block for use in naming convention defined as 8 differential pairs of data signals.

Contact Sequence: The order that a device card edge pin makes physical contact to the host connector.

Device: Refers to the interface target.

Dual Port: When enabled, the device is configured with a PCIe port A and a PCIe port B. This is known as Dual Port mode. When disabled, all lanes form a single PCIe port A. In dual port mode, the two ports must operate independently. Any interaction between the two ports is outside the scope of the specification.

Endpoint: The PCIe interface target logic located on the Device.

Host: Refers to the interface source or initiator.

nC: Connector naming (1C, 2C, 4C) convention that indicates the number of Chiclets. This convention is used because common naming such as "x4, x8" etc. implies symmetrical data transfer in each direction.

Root Complex: The initiator source logic located on the Host.

SRIS: Acronym for Separate Reference clock Independent Spread spectrum clocking. This is a PCI Express feature that allows independent reference clocks for host and device. In this implementation, the host does not need to provide the reference clock and each independent source supports Spread Spectrum Clocking (SSC).

SRNS: Acronym for Separate Reference clock with No Spread spectrum clocking. This is a PCI Express feature that allows independent reference clocks for host and device. In this implementation, the host does not need to provide the reference clock and Spread Spectrum Clocking (SSC) is not enabled by either source.

Switch: A logic component located on the Host used to connect between a Root Complex and 1 or more Endpoints.

4. General Description

The Enterprise and Datacenter Standard Form Factor Specification is meant for serviceable devices that connect electrically to the system through a card edge connector as defined in SFF-TA-1002. This specification defines the following features:

- Support for multiple form factors:
    - SFF-TA-1006 Enterprise and Datacenter 1U Short Device Form Factor
    - SFF-TA-1007 Enterprise and Datacenter 1U Long Device Form Factor
    - SFF-TA-1008 Enterprise and Datacenter Form Factor for a 3" Media Device
- PCIe support for existing and future specifications
    - Supports PCIe 6.2 specification (up to 64.0 GT/s signaling).
    - Single port operation: One (1) x1, x2, x4, x8, or x16 PCIe port supported
    - Dual port: Two (2) x2, two (2) x4, or two (2) x8 PCIe ports supported
- 4 connector types using SFF-TA-1002
    - A 56-pin receptacle supporting Four (4) Tx and Rx PCIe lanes (1C).
    - An 84-pin receptacle supporting Eight (8) Tx and Rx PCIe lanes (2C).
    - A 140-pin receptacle supporting Sixteen (16) Tx and Rx PCIe lanes (4C).
    - A 168-pin receptacle supporting Sixteen (16) Tx and Rx PCIe lanes with additional sideband (4C+).
- Hot-plug (add and remove) capable connector and pin out
- Common clock with options for SRIS and SRNS support by both host and device
- Support for sideband management over SMBus or I3C Basic.
- Connector supports up to 80W sustained operation (actual power is specified per form factor).

5. Signal List

This chapter covers the signal summary, definitions, and signal placement for the EDSFF connectors. Signal directions (I/O) are with respect to the host and the signals are mandatory for the device unless otherwise specified.

Table 5-1. EDSFF Connector Pin List

Interface	Signal Name	Host I/O	Function
Power and Grounds	12 V	O	+12 V power
	3.3 Vaux	O	+3.3 V power
	GND	O	Return current path
PCIe	PETp0, PETn0 PETp1, PETn1 PETp2, PETn2 PETp3, PETn3 PETp4, PETn4 PETp5, PETn5 PETp6, PETn6 PETp7, PETn7 PETp8, PETn8 PETp9, PETn9 PETp10, PETn10 PETp11, PETn11 PETp12, PETn12 PETp13, PETn13 PETp14, PETn14 PETp15, PETn15	O	PCIe TX Differential signals defined by the *PCI Express Card Electromechanical Specification*. PETp/n[0..3] are supported in the x4, x8, and x16 connectors. PETp/n[4..7] are supported with the x8 and x16 connectors. PETp/n[8..15] are supported only with the x16 connector.
	PERp0, PERn0 PERp1, PERn1 PERp2, PERn2 PERp3, PERn3 PERp4, PERn4 PERp5, PERn5 PERp6, PERn6 PERp7, PERn7 PERp8, PERn8 PERp9, PERn9 PERp10, PERn10 PERp11, PERn11 PERp12, PERn12 PERp13, PERn13 PERp14, PERn14 PERp15, PERn15	I	PCIe RX Differential signals defined by the *PCI Express Card Electromechanical Specification*. PERp/n[0..3] are supported in the x4, x8, and x16 connectors. PERp/n[4..7] are supported with the x8 and x16 connectors. PERp/n[8..15] are supported only with the x16 connector.
	REFCLKp0, REFCLKn0	O	PCIe Reference Clock signals defined by the *PCI Express Base Specification*.
	PERST0#	O	PE-Reset is a fundamental reset to the device defined as PERST# by the *PCI Express Base Specification*.
	REFCLKp1, REFCLKn1	O	PCIe Reference Clock signals defined by the *PCI Express Base Specification*. This clock is for dual port mode only and is only used if DUALPORTEN# is low.

Interface	Signal Name	Host I/O	Function
	PERST1#/CLKREQ#	I/O	PERST1#: PE-Reset is a fundamental reset to the device defined as PERST# by the *PCI Express Base Specification*. If dual port mode is supported by the device, PERST1# is only used when DUALPORTEN# is low. CLKREQ#: Clock Request is a reference clock request signal defined by the *PCI Express Base Specification.* It may be supported by a device in single port mode only. If CLKREQ# is supported by the host and the device, then the signal is Open Drain with a pull up on host.
Sideband Signals	PRSNT0#	I	Active low signal. This signal indicates to the host that the device is electrically attached.
	PRSNT1#	I	Active low signal. This signal is available in the x8 and x16 versions of the connector as a 2nd presence signal to indicate to the host that the device is electrically attached. This signal is not available in the x4 version of the connector.
	PRSNT2#	I	Active low signal. This signal is available in the x16 connector as a 3rd presence signal to indicate to the host that the device is electrically attached. This signal is not available in the x4 and x8 versions of the connector.
	SMBCLK/I3CCLK	O	SMBCLK: Open Drain with pull-up on host. SMBus Clock. I3CCLK: Active high push-pull and open drain signal. I3C Basic Clock.
	SMBDATA/I3CDATA	I/O	SMBDATA: Open Drain with pull-up on host. SMBus Data. I3CDATA: Active high push-pull and open drain signal. I3C Basic Data.
	SMRST#	O	Active low signal. SMRST# is a reset for the management interface.
	DUALPORTEN#	O	Open drain. Pull-up on device. This signal indicates if dual port mode is supported by the host.
	LED	O	Active high signal. This signal is used to drive the amber or amber/blue LED state from the host to the device.
	PWRDIS	O	Active high signal. Power Disable notifies the device to turn off all systems connected to 12 V power.
	MFG		Manufacturing mode, signal used only for the manufacturing of the device.
	RFU		Reserved for Future Use
NIC signals	GND/NIC_DETECT#	I	Active low signal. This signal indicates to the host that a NIC is attached.
	REFCLKp2, REFCLKn2 REFCLKp3, REFCLKn3	O	PCIe Reference Clock signals defined by the *PCI Express Base Specification*. These clocks are only used if bifurcation supports 4 links.
	PERST2#, PERST3#	O	PE-Reset is a fundamental reset to the device defined as PERST# by the *PCI Express Base Specification*. PERST2# and PERST3# are only used if bifurcation supports 4 links.
	WAKE#	I	Open drain active low signal with pull-up on host. WAKE# restores the PCIe link as specified in the *PCI Express Base Specification.*
	PWRBRK#	O	Open drain active low signal with pull-up on device. PWRBRK# communicates that an emergency power reduction is needed as defined in the *PCI Express Card Electromechanical Specification*.

Interface	Signal Name	Host I/O	Function
	BIF0#, BIF1#, BIF2#	O	Active low signals. The bifurcation signals allow the host to configure the bifurcation support of the device as defined in the *OCP NIC 3.0 Design Specification*.
	PRSNTA#	O	Active low signal. This signal is used to detect device presence as defined in the *OCP NIC 3.0 Design Specification*.
	PRSNTB[0..3]#	I	Active low signals. These signals are used to detect card presence and capabilities as defined in the *OCP NIC 3.0 Design Specification*.
	AUX_PWR_EN	O	Active high signal. Auxiliary power enable is used to indicate the host is in aux power mode as defined in the *OCP NIC 3.0 Design Specification*.
	MAIN_PWR_EN	O	Active high signal. Main power enable is used to indicate the host is in main power mode as defined in the *OCP NIC 3.0 Design Specification*.
	NIC_PWR_GOOD	I	Active high signal. NIC power good is used to indicate that the device has good internal power in aux power mode and main power mode.
	RBT_CLK_IN	O	Active high signal. Reference clock as defined by *DSP0222 NC-SI Specification*.
	RBT_CRS_DV	I	Active high signal. Carrier sense/receive data valid signal as defined by *DSP0222 NC-SI Specification*.
	RBT_RXD0, RBT_RXD1	I	Active high signal. Receive data signals as defined by *DSP0222 NC-SI Specification*.
	RBT_TX_EN	O	Active high signal. Transmit receive signal as defined by *DSP0222 NC-SI Specification*.
	RBT_TXD0, RBT_TXD1	O	Active high signal. Transmit data signals as defined by *DSP0222 NC-SI Specification*.
	RBT_ARB_OUT	O	Active high signal. Hardware arbitration output signal as defined by *DSP0222 NC-SI Specification*.
	RBT_ARB_IN	I	Active high signal. Hardware arbitration input signal as defined by *DSP0222 NC-SI Specification*.
	SLOT_ID0, SLOT ID1	O	Active high signal. Package ID addressing and FRU address signals as defined by *DSP0222 NC-SI Specification*.
	USB_DATp, USB_DATn	I/O	USB interface as defined in the *USB 2.0 Specification*.
	CLK	O	Active high signal. Scan Chain clock.
	DATA_OUT	O	Active high signal. Scan Chain data output signal.
	DATA_IN	I	Active high signal. Scan Chain data input signal.
	LD#	O	Active low signal. Scan Chain shift register load signal.

5.1 Power and Grounds

The EDSFF connector supports a 12 V power source to power the device. It also supports a 3.3 Vaux power source to provide power to manage sideband communication. All power and grounds shall be supported by the implemented connector on the host and the implemented card edge on the device.

There are no power sequencing requirements for 12 V and 3.3 Vaux. These two voltages are independent from each other. If 12 V is present and PWRDIS is de-asserted, regardless of the presence of 3.3 Vaux, then the PCIe interface shall be functional. If 3.3 Vaux is not present, 12 V is present, and SMRST# is de-asserted, then the SMBus or I3C Basic interface may be functional. If 3.3 Vaux is present but 12 V is not present, then the SMBus or I3C Basic interface should be functional. The functionality of the SMBus or I3C Basic interface with 3.3 Vaux only is out of scope for this specification. See Section 5.3.2 for additional details.

NOTE: If the device has host accessible volatile memory (e.g., CXL.mem supported device), then 12V is expected to remain powered if volatile data is expected to remain valid in a low power mode. Details of the volatile requirements of the device is beyond the scope of this specification.

5.2 PCIe Signals

5.2.1 High Speed Signals (PERp/n, PETp/n)

A device compliant to SFF-TA-1009 shall implement a minimum of one (1) PCIe lane. A lane consists of an input and output differential pair. Additional lanes are optional. Refer to the *PCI Express Base Specification* for more details on the functional requirements of the interface signals.

The PET signals (PETp[0..15], PETn[0..15]) on the host shall connect to the PET signals on the connector and the PER signals on the Device Logic. The PER signals (PERp[0..15], PERn[0..15]) on the host shall connect to the PER signals on the connector and the PET signals on the Device Logic. For a high-level wiring diagram, see Figure 5-1.

Lane Polarity Inversion shall be supported on both the host and the device to simplify host and device PCB trace routing constraints.

Lane reversal may be supported on both the host and device. If it is supported, then the transmitting and receiving lanes shall be connected using the same ordering.

Table 5-2 shows the connectivity in both single and dual port systems. Note that x1 and x2 Single Port is a subset of x4 Single Port. Dual Port usage is enabled with DUALPORTEN# assertion. See 5.3.5 for more details.

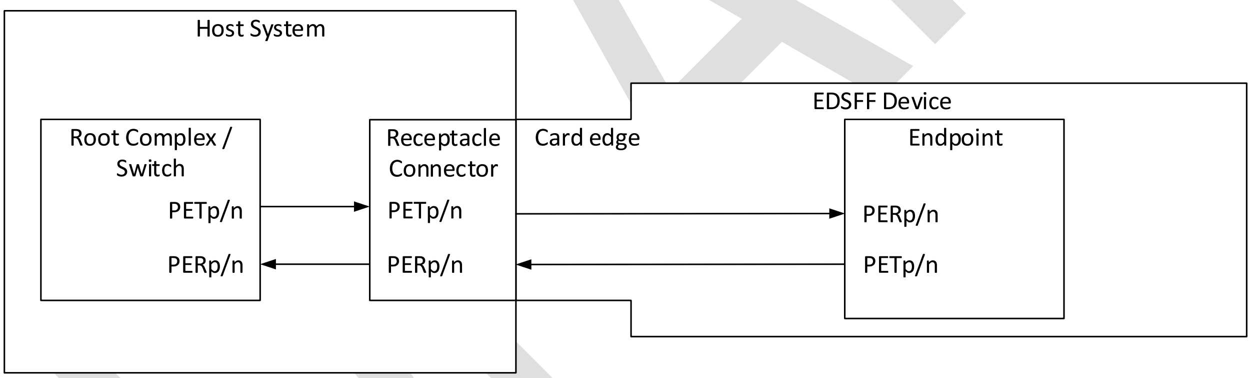


Figure 5-1. PET and PER Signal Connectivity Between Host and Device

Table 5-2. PCIe lanes connectivity in single and dual port implementations (without lane reversal)

PCIe lanes	x4 Single Port (1 port x4)	x4 Dual Port (2 ports x2)	X8 Single Port (1 port x8)	x8 Dual Port (2 ports x4)	x16 Single Port (1 port x16)	x16 Dual Port (2 ports x8)
PERp0, PERn0, PETp0, PETn0	Port A, lane 0	Port A, lane 0	Port A, lane 0	Port A, lane 0	Port A, lane 0	Port A, lane 0
PERp1, PERn1, PETp1, PETn1	Port A, lane 1	Port A, lane 1	Port A, lane 1	Port A, lane 1	Port A, lane 1	Port A, lane 1
PERp2, PERn2, PETp2, PETn2	Port A, lane 2	Port B, lane 0	Port A, lane 2	Port B, lane 0	Port A, lane 2	Port B, lane 0
PERp3, PERn3, PETp3, PETn3	Port A, lane 3	Port B, lane 1	Port A, lane 3	Port B, lane 1	Port A, lane 3	Port B, lane 1
PERp4, PERn4, PETp4, PETn4	No connect	No connect	Port A, lane 4	Port A, lane 2	Port A, lane 4	Port A, lane 2
PERp5, PERn5, PETp5, PETn5	No connect	No connect	Port A, lane 5	Port A, lane 3	Port A, lane 5	Port A, lane 3
PERp6, PERn6, PETp6, PETn6	No connect	No connect	Port A, lane 6	Port B, lane 2	Port A, lane 6	Port B, lane 2
PERp7, PERn7, PETp7, PETn7	No connect	No connect	Port A, lane 7	Port B, lane 3	Port A, lane 7	Port B, lane 3
PERp8, PERn8, PETp8, PETn8	No connect	No connect	No connect	No connect	Port A, lane 8	Port A, lane 4
PERp9, PERn9, PETp9, PETn9	No connect	No connect	No connect	No connect	Port A, lane 9	Port A, lane 5
PERp10, PERn10, PETp10, PETn10	No connect	No connect	No connect	No connect	Port A, lane 10	Port B, lane 4
PERp11, PERn11, PETp11, PETn11	No connect	No connect	No connect	No connect	Port A, lane 11	Port B, lane 5
PERp12, PERn12, PETp12, PETn12	No connect	No connect	No connect	No connect	Port A, lane12	Port A, lane 6
PERp13, PERn13, PETp13, PETn13	No connect	No connect	No connect	No connect	Port A, lane 13	Port A, lane 7
PERp14, PERn14, PETp14, PETn14	No connect	No connect	No connect	No connect	Port A, lane 14	Port B, lane 6
PERp15, PERn15, PETp15, PETn15	No connect	No connect	No connect	No connect	Port A, lane 15	Port B, lane 7

5.2.2 Reference Clock

The REFCLKp/REFCLKn signals are used to assist the synchronization of the device's PCI Express interface timing circuits. Refer to the *PCI Express Base Specification* for more details on the functional and tolerance requirements for the reference clock signals.

There are two sets of clock pairs. All devices shall implement REFCLKp0 and REFCLKn0. All devices that support dual port mode shall also implement REFCLKp1 and REFCLKn1. In a single port implementation (indicated by DUALPORTEN# de-asserted), only REFCLKp0 and REFCLKn0 are used. In a dual port implementation (indicated by DUALPORTEN# asserted), REFCLKp0 and REFCLKn0 connects to Port A while REFCLKp1 and REFCLKn1 connects to port B.

If SRIS or SRNS is supported by both the system and the device then the reference clock is optional on the host. The common reference clock driven by the host shall be the default configuration on the device. If the common reference clock is not detected upon detecting PERST# de-assertion, then the SRIS/SRNS supported device shall switch into SRIS/SRNS mode. The device shall only enter SRNS if the device is configured for this usage through a method outside the scope of this version of the specification.

It is recommended that the host terminate the reference clock signals with a pull-down resistor if the clocks are not provided by the host.

5.2.3 PERST#

All devices and hosts shall implement PERST0#. All devices and hosts that support dual port mode shall also implement PERST1#. Refer to the *PCI Express Base Specification* for more details on the functional requirements.

In single port mode (indicated by DUALPORTEN# de-asserted), PERST0# is used. In this single port mode, PERST1# is not used; however, the CLKREQ# function may be used.

In dual port mode (indicated by DUALPORTEN# asserted), PERST0# connects to Port A and PERST1# connects to Port B.

5.2.4 CLKREQ#

CLKREQ# is an optional signal. See the *PCI Express Base Specification* for details on the functional requirements for the CLKREQ# signal.

If DUALPORTEN# is asserted by the host, then CLKREQ# is not available.

If DUALPORTEN# is de-asserted by the host and CLKREQ# is supported by the host, then the PERST1#/CLKREQ# pin shall be pulled up on the host with a 9 kΩ to 60 kΩ resistor.

If DUALPORTEN# is de-asserted by the host and CLKREQ# is not supported by the host, then the PERST1#/CLKREQ# pin shall be left floating.

If the device does not support Dual Port and CLKREQ#, then the PERST1#/CLKREQ# pin should be left unconnected on the device.

5.3 Sideband Signals

5.3.1 PRSNT[0..2]#

PRSNT[0..2]# signals indicate physical presence of a device plugged into the host connector and the type of connector on the device. All devices supporting the x4 device connector shall implement PRSNT0#. All devices supporting the x8 device connector shall implement PRSNT0# and PRSNT1#. All devices supporting the x16 device connector shall implement PRSNT0#, PRSNT1#, PRSNT2#. The device shall connect each implemented PRSNT[0..2]# signal to ground.

5.3.2 SMBus Interface

The SMBus interface is a sideband management interface. SMBus is a two-wire interface through which various system component chips communicate with each other and with rest of the system. Refer to the *System Management Bus (SMBus) Specification*.

SMBus is an Open Drain interface. The pull-ups for SMBDATA and SMBCLK shall be on the host and powered within the voltage limits defined for Vddsmb in Table 6-4. The device is allowed to have weak pull-up resistors to protect from floating inputs. If present, then the pull-up resistors on the device are recommended to be greater than or equal to 45 kΩ.

The SMBCLK signal provides the clock signaling from the SMBus ~~initiator~~ controller to the SMBus target to be able to decode the data on the SMBDATA line.

The SMBDATA signal is used to transfer the data packets between the SMBus controller and target ~~host and the~~

device according to the SMBus protocol.

If all host power rails are removed from the device, SMBus should be quiesced and SMRST# should be asserted during this time to prevent undefined behavior.

5.3.3 I3C Basic Interface

The I3C Basic interface is an optional sideband management interface. It is a two-wire interface through which various system component chips communicate with each other and with rest of the system. Refer to the *I3C Basic Specification* and Section 10 of this specification for more details.

Devices that support I3C Basic shall support SMBus and tolerate SMBus voltage signaling for backwards compatibility.

If all host power rails are removed from the device, I3C Basic should be quiesced and SMRST# should be asserted during this time to prevent undefined behavior.

5.3.4 SMRST#

The SMRST# signal is an external reset signal for the SMBus interface as defined by the System Management Bus (SMBus) Specification and an external reset for the I3C Basic interface if I3C Basic is supported. SMRST# shall be implemented by the device and is optional for the host. It shall not affect the PCIe interface or other non SMBus/I3C Basic circuit related functions. The device shall have a pull-up resistor greater than or equal to 9 kΩ on SMRST#.

If the host asserts SMRST#, then the device shall keep the SMBCLK/I3CCLK and SMBDATA/I3CDATA in a high impedance state and ignore any transitions on SMBCLK/I3CCLK and SMBDATA/I3CDATA. When the host de-asserts SMRST#, the device shall place the SMBus or I3C Basic in the SMBus power-on reset state at 3.3 V.

Cycling 3.3 Vaux shall not be used by the host to reset the SMBus or I3C Basic. Cycling 3.3 Vaux may or may not have an effect on the device's SMBus or I3C Basic interface.

SMRST# timings are defined in Table 6-3Table 6-3.

5.3.5 DUALPORTEN#

If the device supports dual port, then it shall be configured by the host as a single port or dual port device using the DUALPORTEN# signal. To enable dual port mode, the host shall assert DUALPORTEN# prior to or simultaneous with 12 V power being applied to the device. Any change to DUALPORTEN# requires a power cycle or a PWRDIS event. The device shall have a pull-up resistor greater than or equal to 4.7 kΩ on DUALPORTEN#.

If DUALPORTEN# is not asserted, then the device shall operate all available lanes in single port mode. If DUALPORTEN# is asserted, then the device shall assign half of the available lanes to each port. A single lane host or device shall not support dual port mode. See Table 5-2 for more details.

5.3.6 LED

The LED signal is asserted by the host to drive an amber or an amber/blue LED on the device. LED shall be supported by the device and is optional for the host. See Sections 6.3 and 7 for more details.

5.3.7 PWRDIS

The PWRDIS signal is asserted by the host to command the device to shut off power to all circuitry connected to the 12 V power supply. It shall be supported by the device and is optional for the host. When PWRDIS is asserted, the host shall allow the device time to shut down. When PWRDIS is de-asserted, the host shall allow the device to settle before de-asserting PERST0#. See Sections 6.2 and 6.3 for more details. If PWRDIS is asserted before a hot plug insertion then the drive shall not power on.

PWRDIS may or may not have an impact on the state of SMBus/I3C Basic.

The device shall have a pull-down resistor greater than or equal to 9kΩ on PWRDIS.

5.3.8 MFG

The MFG signal is optional for the device. The MFG signal is used for device manufacturing only and details are beyond the scope of this specification. This signal shall be electrically not connected on 1C, 2C, and 4C non-manufacturing hosts. In a 4C+ non-manufacturing host, the signal shall float unless the host detects a 4C+ supported device through NIC_DETECT# or host specific means (e.g., out of band).

Post device manufacturing, the device manufacturer should ensure the pin is disabled.

5.3.9 RFU

Signals documented as RFU are reserved for future use. These pins shall be electrically not connected on the 1C, 2C, and 4C host and the device.

NOTE: There are pins on the 4C+ pinout that utilize RFU pins within the 1C, 2C, 4C pinout. Proper care should be taken if these RFU pins are allocated to other functions in the future.

5.4 NIC Signals

See Section 9 NIC Implementation (Informative) for NIC signals not listed below.

5.4.1 GND/NIC_DETECT#

The GND/NIC_DETECT# signal indicates a network (NIC) device is plugged into the host connector. This signal is only used with the 4C+ connector and is optional for the host. If GND/NIC_DETECT# is asserted then it indicates a NIC is plugged into the host. If the device supports the 4C+ connector then this signal is directly connected to ground. If the host supports the 4C+ connector then this signal on the host shall have a pull-up resistor greater than 9 kΩ.

5.5 Connector pinout definitions

The following tables show the signal pinouts for the connector. These pinouts are shown from the host point of view. If the host supports 4C+ but detects the device supports 1C, 2C, or 4C, the host shall configure the connector pins based on the 1C, 2C, or 4C pinouts. Hot plug shall be supported by the device. The contact sequence for each pinout is shown to indicate the order in which the pins make contact to the host. For more details, please refer to *SFF-TA-1002 Card Edge multilane protocol agnostic connector specification*.

- Table 5-3 lists the pinout for the x4 connector (1C)
- Table 5-4 lists the pinout for the x8 connector (2C)
- Table 5-5 lists the pinout for the x16 connector (4C)
- Table 5-6 lists the pinout for the x16 connector with additional sideband (4C+)

Table 5-3. EDSFF x4 (1C) Connector Pinout

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6
B7	2nd mate	MFG	SMBCLK/I3CCLK	2nd mate	A7
B8	2nd mate	RFU	SMBDATA/I3CDATA	2nd mate	A8
B9	2nd mate	DUALPORTEN#	SMRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED	2nd mate	A10
B11	2nd mate	3.3 Vaux	PERST1#/CLKREQ#	2nd mate	A11
B12	2nd mate	PWRDIS	PRSNT0#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28

Table 5-4. EDSFF x8 (2C) Connector Pinout

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6
B7	2nd mate	MFG	SMBCLK/I3CCLK	2nd mate	A7
B8	2nd mate	RFU	SMBDATA/I3CDATA	2nd mate	A8
B9	2nd mate	DUALPORTEN#	SMRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED	2nd mate	A10
B11	2nd mate	3.3 Vaux	PERST1#/CLKREQ#	2nd mate	A11
B12	2nd mate	PWRDIS	PRSNT0#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28
		Key	Key		
B29	1st mate	GND	GND	1st mate	A29
B30	2nd mate	PETn4	PERn4	2nd mate	A30
B31	2nd mate	PETp4	PERp4	2nd mate	A31
B32	1st mate	GND	GND	1st mate	A32
B33	2nd mate	PETn5	PERn5	2nd mate	A33
B34	2nd mate	PETp5	PERp5	2nd mate	A34
B35	1st mate	GND	GND	1st mate	A35

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B36	2nd mate	PETn6	PERn6	2nd mate	A36
B37	2nd mate	PETp6	PERp6	2nd mate	A37
B38	1st mate	GND	GND	1st mate	A38
B39	2nd mate	PETn7	PERn7	2nd mate	A39
B40	2nd mate	PETp7	PERp7	2nd mate	A40
B41	1st mate	GND	GND	1st mate	A41
B42	2nd mate	PRSNT1#	RFU	2nd mate	A42

Table 5-5. EDSFF x16 (4C) Connector Pinout

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6
B7	2nd mate	MFG	SMBCLK/I3CCLK	2nd mate	A7
B8	2nd mate	RFU	SMBDATA/I3CDATA	2nd mate	A8
B9	2nd mate	DUALPORTEN#	SMRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED	2nd mate	A10
B11	2nd mate	3.3 Vaux	PERST1#/CLKREQ#	2nd mate	A11
B12	2nd mate	PWRDIS	PRSNT0#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28
		Key	Key		
B29	1st mate	GND	GND	1st mate	A29
B30	2nd mate	PETn4	PERn4	2nd mate	A30
B31	2nd mate	PETp4	PERp4	2nd mate	A31
B32	1st mate	GND	GND	1st mate	A32
B33	2nd mate	PETn5	PERn5	2nd mate	A33
B34	2nd mate	PETp5	PERp5	2nd mate	A34
B35	1st mate	GND	GND	1st mate	A35

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B36	2nd mate	PETn6	PERn6	2nd mate	A36
B37	2nd mate	PETp6	PERp6	2nd mate	A37
B38	1st mate	GND	GND	1st mate	A38
B39	2nd mate	PETn7	PERn7	2nd mate	A39
B40	2nd mate	PETp7	PERp7	2nd mate	A40
B41	1st mate	GND	GND	1st mate	A41
B42	2nd mate	PRSNT1#	RFU	2nd mate	A42
		Key	Key		
B43	1st mate	GND	GND	1st mate	A43
B44	2nd mate	PETn8	PERn8	2nd mate	A44
B45	2nd mate	PETp8	PERp8	2nd mate	A45
B46	1st mate	GND	GND	1st mate	A46
B47	2nd mate	PETn9	PERn9	2nd mate	A47
B48	2nd mate	PETp9	PERp9	2nd mate	A48
B49	1st mate	GND	GND	1st mate	A49
B50	2nd mate	PETn10	PERn10	2nd mate	A50
B51	2nd mate	PETp10	PERp10	2nd mate	A51
B52	1st mate	GND	GND	1st mate	A52
B53	2nd mate	PETn11	PERn11	2nd mate	A53
B54	2nd mate	PETp11	PERp11	2nd mate	A54
B55	1st mate	GND	GND	1st mate	A55
B56	2nd mate	PETn12	PERn12	2nd mate	A56
B57	2nd mate	PETp12	PERp12	2nd mate	A57
B58	1st mate	GND	GND	1st mate	A58
B59	2nd mate	PETn13	PERn13	2nd mate	A59
B60	2nd mate	PETp13	PERp13	2nd mate	A60
B61	1st mate	GND	GND	1st mate	A61
B62	2nd mate	PETn14	PERn14	2nd mate	A62
B63	2nd mate	PETp14	PERp14	2nd mate	A63
B64	1st mate	GND	GND	1st mate	A64
B65	2nd mate	PETn15	PERn15	2nd mate	A65
B66	2nd mate	PETp15	PERp15	2nd mate	A66
B67	1st mate	GND	GND	1st mate	A67
B68	2nd mate	RFU	RFU	2nd mate	A68
B69	2nd mate	RFU	RFU	2nd mate	A69
B70	2nd mate	PRSNT2#	RFU	2nd mate	A70

Table 5-6. EDSFF x16 With Additional Sideband (4C+) Connector Pinout

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
BO1	2nd mate	NIC_PWR_GOOD	PERST2#	2nd mate	AO1
BO2	2nd mate	MAIN_PWR_EN	PERST3#	2nd mate	AO2
BO3	2nd mate	LD#	WAKE#	2nd mate	AO3
BO4	2nd mate	DATA_IN	RBT_ARB_IN	2nd mate	AO4
BO5	2nd mate	DATA_OUT	RBT_ARB_OUT	2nd mate	AO5
BO6	2nd mate	CLK	SLOT_ID1	2nd mate	AO6
BO7	2nd mate	SLOT_ID0	RBT_TX_EN	2nd mate	AO7
BO8	2nd mate	RBT_RXD1	RBT_TXD1	2nd mate	AO8
BO9	2nd mate	RBT_RXD0	RBT_TXD0	2nd mate	AO9
BO10	1st mate	GND	GND	1st mate	AO10
BO11	2nd mate	REFCLKn2	REFCLKn3	2nd mate	AO11
BO12	2nd mate	REFCLKp2	REFCLKp3	2nd mate	AO12
BO13	1st mate	GND/NIC_DETECT#	GND	1st mate	AO13
BO14	2nd mate	RBT_CRS_DV	RBT_CLK_IN	2nd mate	AO14
		Key	Key		
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6
B7	2nd mate	MFG/BIF0#	SMBCLK/I3CCLK	2nd mate	A7
B8	2nd mate	RFU/BIF1#	SMBDATA/I3CDATA	2nd mate	A8
B9	2nd mate	DUALPORTEN#/BIF2#	SMRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED/PRSNTA#	2nd mate	A10
B11	2nd mate	3.3 Vaux	PERST1#/CLKREQ#	2nd mate	A11
B12	2nd mate	PWRDIS/AUX_PWR_EN	PRSNT0#/PRSNTB2#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28
		Key	Key		
B29	1st mate	GND	GND	1st mate	A29
B30	2nd mate	PETn4	PERn4	2nd mate	A30
B31	2nd mate	PETp4	PERp4	2nd mate	A31
B32	1st mate	GND	GND	1st mate	A32
B33	2nd mate	PETn5	PERn5	2nd mate	A33
B34	2nd mate	PETp5	PERp5	2nd mate	A34
B35	1st mate	GND	GND	1st mate	A35
B36	2nd mate	PETn6	PERn6	2nd mate	A36
B37	2nd mate	PETp6	PERp6	2nd mate	A37
B38	1st mate	GND	GND	1st mate	A38
B39	2nd mate	PETn7	PERn7	2nd mate	A39
B40	2nd mate	PETp7	PERp7	2nd mate	A40
B41	1st mate	GND	GND	1st mate	A41
B42	2nd mate	PRSNT1#/PRSNTB0#	RFU/PRSNTB1#	2nd mate	A42
		Key	Key		
B43	1st mate	GND	GND	1st mate	A43
B44	2nd mate	PETn8	PERn8	2nd mate	A44
B45	2nd mate	PETp8	PERp8	2nd mate	A45
B46	1st mate	GND	GND	1st mate	A46
B47	2nd mate	PETn9	PERn9	2nd mate	A47
B48	2nd mate	PETp9	PERp9	2nd mate	A48
B49	1st mate	GND	GND	1st mate	A49
B50	2nd mate	PETn10	PERn10	2nd mate	A50
B51	2nd mate	PETp10	PERp10	2nd mate	A51
B52	1st mate	GND	GND	1st mate	A52
B53	2nd mate	PETn11	PERn11	2nd mate	A53
B54	2nd mate	PETp11	PERp11	2nd mate	A54
B55	1st mate	GND	GND	1st mate	A55
B56	2nd mate	PETn12	PERn12	2nd mate	A56

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B57	2nd mate	PETp12	PERp12	2nd mate	A57
B58	1st mate	GND	GND	1st mate	A58
B59	2nd mate	PETn13	PERn13	2nd mate	A59
B60	2nd mate	PETp13	PERp13	2nd mate	A60
B61	1st mate	GND	GND	1st mate	A61
B62	2nd mate	PETn14	PERn14	2nd mate	A62
B63	2nd mate	PETp14	PERp14	2nd mate	A63
B64	1st mate	GND	GND	1st mate	A64
B65	2nd mate	PETn15	PERn15	2nd mate	A65
B66	2nd mate	PETp15	PERp15	2nd mate	A66
B67	1st mate	GND	GND	1st mate	A67
B68	2nd mate	RFU	USB_DATn	2nd mate	A68
B69	2nd mate	RFU	USB_DATp	2nd mate	A69
B70	2nd mate	PRSNT2#/PRSNTB3#	PWRBRK0#	2nd mate	A70

6. Electrical Requirements

This chapter covers the electrical requirements of the EDSFF devices. Unless otherwise specified, follow the PCI Express Card Electromechanical Specification.

6.1 Power Supply Requirements

Table 6-1 provides the 12 V power supply requirements and Table 6-2 provides the 3.3 Vaux power supply requirements.

Table 6-1. 12 V Power Supply Requirements

Symbol	Parameter	Value	Unit	Comment
12Vtol	12 V supply Tolerance	10.8 to 13.2	V	Includes DC+AC noise up to 20 MHz.
12Vpsus	Maximum sustained device power	The lesser of the Slot Power Limit Value in the *PCI Express Base Specification* and, if configured, the Power State Descriptor value in the *NVM Express Base Specification*.	W	Maximum average power over any 1s period. A device shall not consume more power than the slot power limit regardless of other settings (e.g. PSD in NVMe).
12Vpinit	Initial slot power limit	See form factor specification	W	This is the initial max power the device can draw over any 1s period prior to reading the Slot Power Limit Value in the *PCI Express Base Specification*
12Vppmax	Maximum device power	For: 12Vpsus ≤ 25 W: 1.5 X 12Vpsus 25 W ≤ 12Vpsus ≤ 29 W: 37.5 W 12Vpsus > 29 W: 1.3 X 12Vpsus	W	Maximum average power measured over any 100 µs period.
12Vslewrate	Maximum slew rate	0.3	A/us	Maximum slew rate for any step current as measured at the connector. This does not include hot plug
12Vinrush	Max inrush current	2	A	Maximum current load presented by the device 12V supply to the host receptacle averaged over any 5us period during the initial power-up ramp to 90% of the device operating voltage.
12Vcap	Max capacitance for inrush	5	uF	Capacitance system sees during the initial power-up ramp to 90% of the device operating voltage.

Table 6-2. 3.3 Vaux Power Supply Requirements

Symbol	Parameter	Value	Unit	Comment
3.3Vauxtol	3.3 Vaux supply Tolerance	2.970 to 3.465	V	Includes Ripple.
3.3VauxIpin	3.3 Vaux pin current	25	mA	Maximum averaged current value over any 100 us period after the voltage reaches its operating range.
3.3Vauxcap	Max capacitance for inrush	5	uF	For inrush current limit.

6.2 Timings

There are no power sequencing requirements for 12 V and 3.3 Vaux. These two voltages are independent from each other.

For SMBus, refer to the *System Management Bus (SMBus) Specification* and Table 6-3~~Table 6-3~~.

For other timing requirements, see Table 6-3~~Table 6-3~~ and Figure 6-1.

Table 6-3. EDSFF Device Timing requirements

Parameter	Description	Min	Max	Units	Notes
Tsmrst	SMRST# assertion hold time	1		ms	3
Tsmrston	SMRST# de-assertion to SMBus operational		500	ms	4
Tpwrdis	PWRDIS assertion hold time	5		s	1, 2
Tpwrdis#	PWRDIS de-assertion hold time	5		s	1, 2
Tdisrst	PWRDIS de-assertion hold time to PERST# de-assertion	100		ms	
Tpvper	12 V power within 12Vtol range to PERST# de-assertion	100		ms	

Notes:

1. Devices are responsible for filtering noise of <1 us on PWRDIS.
2. The length of time from PWRDIS assertion/de-assertion to the disabling or allowing of power application to the device circuitry is device specific. Meeting Tpwrdis and Tpwrdis# are the responsibility of the host. Not meeting these timings while the device is connected to the host may result in undefined behavior with the device.
3. Meeting Tsmrst is the responsibility of the host. Not meeting this timing while the device is connected to the host may result in undefined behavior with the device.
4. Meeting Tsmrston is the responsibility of the device's SMBus interface to ensure the device is operational

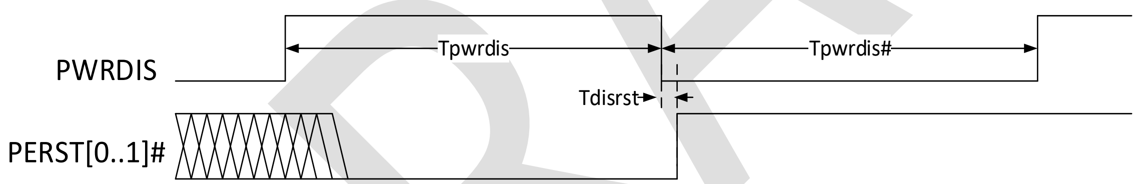


Figure 6-1. EDSFF Device Timing Diagram for PWRDIS

6.3 3.3 V Logic Signal Requirements

The 3.3 V device logic levels for single-ended digital signals (PERST[0..1]#, CLKREQ#, PRSNT[0..2]#, SMBCLK, SMBDATA, SMRST#, DUALPORTEN#, LED, PWRDIS) are defined in Table 6-4. Inputs and outputs are referenced from the device standpoint.

Table 6-4. DC Specification for 3.3 V Logic Signaling

Symbol	Parameter	Condition	Min	Max	Unit	Notes
Vddsmb	SMBus Operating Voltage		2.97	3.465	V	
Vih1	Input High Voltage		2.0	3.465	V	
Vil1	Input Low Voltage		-0.3	0.8	V	2
Vih2	Input High Voltage for LED		3.0	3.465	V	
Vil2	Input Low Voltage for amber/blue LED		-0.3	0.4	V	2
Voh	Output High Voltage			3.465	V	
Vol	Output Low Voltage	4.0 mA		0.2	V	
Iledamber	LED sink current (amber)		20		mA	4
Iledblue	LED source current (blue)		15		mA	4
Iin	Input Leakage Current	0 V to 3.3 V	-100	100	µA	3
Iout	Output Leakage Current	0 V to 3.3 V	-100	100	µA	3
Cin	Input Pin Capacitance			30	pF	1
Cout	Output Pin Capacitance			30	pF	1

Notes:

1. Measured at the card edge-finger. Does not apply to LED.
2. For the LED pin, Vil1 is used for devices supporting the amber LED. Vil2 is used for devices supporting the amber/blue LED.
3. The leakage current requirement excludes current related to mandatory termination (e.g., a pull up) on the side-band signals (e.g., DUALPORTEN# and SMRST#).
4. This is the minimum current required by the device to meet specified brightness. See Section 7 for the brightness specification.

6.4 I3C Basic Signal Requirements

The I3C Basic operating voltage and capacitance for I3CCLK and I3CDATA is defined in Table 6-5.

Table 6-6 defines the device maximum transition times between SMBus and I3C Basic. During Tsmb2i3c, the host will transition the pull-ups from Vddsmb to Vddi3c and the device will transition to Vddi3c based signaling. During Ti3c2smb, the host will transition the pull-ups from Vddi3c to Vddsmb and the device will transition to Vddsmb based signaling.

For more information on logic levels or bus timings, refer to the *I3C Basic Specification*.

Table 6-5. DC Specification for I3C Basic Logic Signaling

Symbol	Parameter	Min	Nominal	Max	Unit	Notes
Vddi3c	I3C Basic Operating Voltage	1.65	1.80	1.95	V	
Ci3c	Device capacitance for I3C Basic support			20	pF	1

Notes:

1. Total capacitance host will see from the device including the PCB routing, package routing, and on die parasitics if device is in I3C Basic mode.

Table 6-6. I3C Basic Timing Requirements

Symbol	Parameter	Min	Max	Unit	Notes
Tsmb2i3c	Device transition time from SMBus to I3C Basic		20	ms	1,2
Tdcl	Device Clock low reset time	25	35	ms	2,3
Ti3c2smb	Device transition time from I3C Basic to SMBus		20	ms	2,3
T2wrst	Host clock held low reset time	55~~0~~		ms	

Tsmbsettle	Host pull-up settling time until first command	1		ms	3

Notes:

1. The host shall wait a minimum of Tsmb2i3c before sending I3C Basic commands. The host is recommended to complete the pull-up change during Tsmb2i3c to prevent undefined behavior by the device.
2. No SMBus or I3C Basic transmissions shall occur during Tsmb2i3c, Tdcl, and Ti3c2smb.
3. The host shall wait a minimum of ~~Tdcl+Ti3c2smb~~Tsmbsettle before sending SMBus commands.

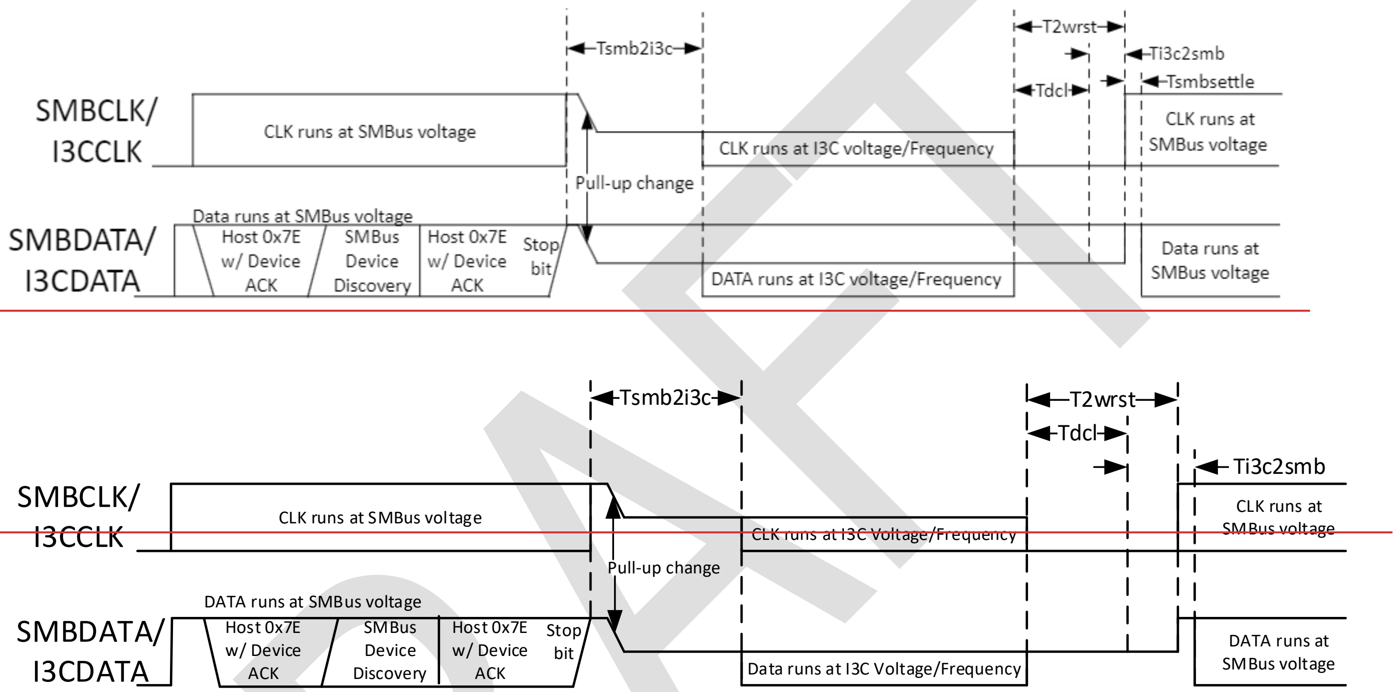


Figure 6-2. EDSFF Device Timing Diagram for Transition to I3C Basic Signaling Voltage

7. LEDs

The following section covers the usage and details of the LEDs on EDSFF devices. For EDSFF devices, there shall be two LED locations supported within the form factor:

1. Location 1 color(s):
    a. green
    b. white
2. Location 2 color(s):
    a. amber
    b. blue

The LED location colors are dependent on form factor and usage. Table 7-1 defines the LED requirements.

Table 7-1. LED Requirements

LED description	Green	White	Amber	Blue
Driven by	Device	Device	Host (LED signal)	Host (LED signal)
Function	Power, Activity	Power, Orderly Removal indication	Host defined	Host Defined
Wavelength[1] (dominant, nm)	515 to 535	NA	585 to 600	460 to 475
Point Intensity[1] (mcd)	Minimum: 45	Minimum: 60	Minimum[2]: 40	Minimum: 20

Notes:

1. The wavelength and point intensity are measured at the center-point location defined by the form factor specification where the light exits the volumetric of the form factor as viewed from the front of the device, also called the LED facing side (i.e., end opposite the connector) 100 mm away. The measurements should follow the methods defined in the technical report CIE 127-2007.
2. Minimum point intensity assumes a voltage of 3.30 V.

7.1 Location 1 LED(s)

There shall be either a Green or White LED or Green/White LED that is driven by the device. Table 7-2 below defines the LED colors depending on the implementation.

Table 7-2. Device-driven LED Implementation

Device Type	LED Support	Implementation
Class A	Green	Power, activity indication
Class B	White	Power, activity, removal state indication
Class C	Green and White	Power, activity, removal state indication

7.1.1 Green LED (Class A Device)

The green LED is driven and completely controlled by the device. The two functions for the green LED are defined in Table 7-3:

- Power: This function indicates the device has power and has no issues with its power regulation. Once the green LED is "on", it shall either remain on or blink at the Activity frequency unless the device determines power is no longer within its operating range.
- Activity: This function indicates if the device is being used.

Table 7-3. LED and Device State Per Function for Green LED (Class A Device)

Green LED State	Device State
"On"	Device is powered, no activity occurring
4 Hz nominal "blink" rate	Device is powered, host initiated I/O activity occurring
"Off"	Device is not powered

7.1.2 White LED (Class B Device)

The white LED is driven by the device. The host initiates the change of white LED state. The method that the host changes the state of the white LED is beyond the scope of this specification. The functions for the white LED are defined in Table 7-4:

- Power: This function indicates the device has power and has no issues with its power regulation. Once the white LED is "on", it shall either remain on or blink depending on the host programmed state.
- Activity: This function indicates if the device is being used.
- Removal State: This function indicates if it is safe to remove the device from the host. If device is not safe to remove and is removed from the host then this may result in undefined behavior of the host.

Table 7-4. LED and Device State Per Function for White LED (Class B Device)

White LED State	Device State
"On"	Device is powered. No activity occurring. Removal not permitted.
4 Hz nominal "blink" rate	Device is powered. Host initiated activity occurring. Removal not permitted.
"Off"	Device is not powered. Removal permitted.

7.1.3 Green and White LED(s) (Class C Device)

The green and white LED(s) support is driven by the device and implementation is up to the device. The device controls the state of the green LED. The host initiates the change the state of the white LED. The method that the host changes the state of the white LED is beyond the scope of this specification. The functions for the green and white LED(s) are defined in Table 7-5:

Table 7-5. LED and Device State Per Function for Green and White LED (Class C Device)

Green LED State	White LED State	Device State
"On"	"Off"	Device is powered. No activity occurring. Removal permitted.
4 Hz nominal "blink" rate	"Off"	Device is powered. Host initiated activity occurring. Removal permitted.
"Off"	"On"	Device is powered. No activity occurring. Removal not permitted.
"Off"	4 Hz nominal "blink" rate	Device is powered. Host initiated activity occurring. Removal not permitted.
"Off"	"Off"	Device is not powered. Removal permitted.

7.2 Location 2 LED(s)

There shall be either an amber or amber/blue LED that is driven by the host signal through the LED pin. A current limiting resistor shall be in the device to protect the LED against overcurrent.

7.2.1 Amber LED (SFF-TA-1006 and SFF-TA-1007)

The amber LED function shall be independent of 12V, 3.3Vaux, and PWRDIS state. The LED states are defined in ~~Table 7-7~~Table 7-6.

Table 7-6. LED and Device State per Function for Amber LED

LED signal state	Amber LED state
Asserted (driven high)	"On"
De-asserted (driven low)	"Off"
High impedance (not driven)	"Off"

7.2.2 Amber/Blue LED (SFF-TA-1008)

The amber/blue is a bi-color LED driven by the host signal through the LED pin. The amber LED function shall be independent of 12V, 3.3Vaux, and PWRDIS state. The blue LED function shall be independent of the PWRDIS state. The functionality and blink rates of this LED are beyond the scope of this specification. The LED states are defined in Table 7-7. Example schematics to meet these states are provided in Figure 7-1~~Figure 7-1~~ and Figure 7-2~~Figure 7-2~~:

Table 7-7. LED and Device State per Function for Amber/Blue LED

LED signal state	Amber LED state	Blue LED state
Asserted (driven high)	"On"	"Off"
De-asserted (driven low)	"Off"	"On"
High impedance (not driven)	"Off"	"Off"

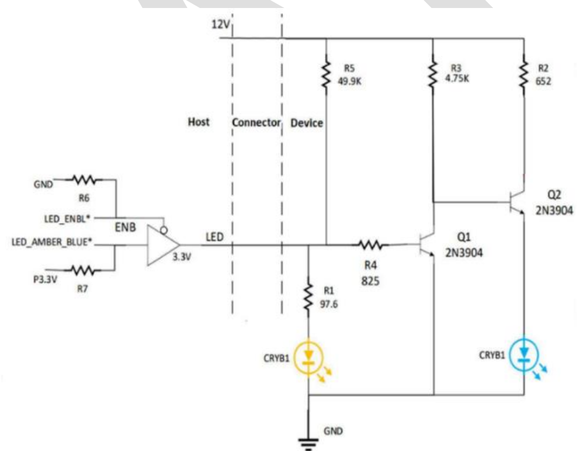


Figure 7-1. Example Schematic for Controlling the Blue/Amber LED (Common Cathode)

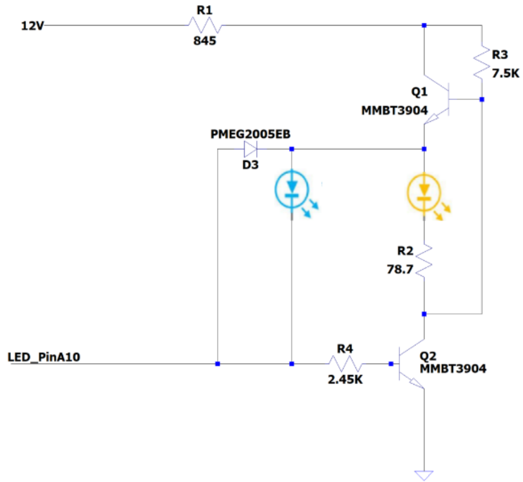


Figure 7-2. Example Schematic for Controlling the Blue/Amber LED (Common Anode)

8. PCIe Electrical Requirements

In general, EDSFF devices are expected to follow requirements as specified in both the *PCI Express Base Specification* and the *PCI Express Card Electromechanical Specification*. This chapter provides device requirements that deviate from the *PCI Express Card Electromechanical Specification*. For details on the connector electricals, please refer to *SFF-TA-1002 Card Edge multilane protocol agnostic connector specification*.

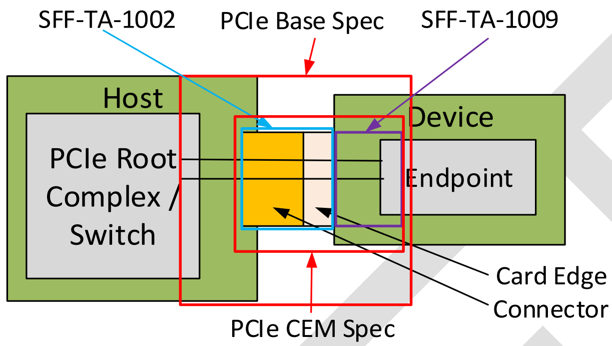


Figure 8-1. EDSFF Electrical Requirements Coverage

8.1 Signal Integrity Requirements

Table 8-1 summarizes the signal integrity requirements for the device. Additional explanation is provided in the subsequent sections. All measurements are referenced to an 85 Ω differential impedance.

Table 8-1. Summary of Signal Integrity Requirements

Line Rate	Insertion Loss (IL)	Return Loss (RL)	Power Sum Near End Crosstalk (PSNEXT)[1]	Power Sum Far End Crosstalk (PSFEXT)[1]
16.0 GT/s	-5.5 dB (f = 0 to 8 GHz)	≤ -10 dB (< 4 GHz) ≤ -7 dB (4 to 24 GHz)	≤ -40 dB (0 to 12 GHz)	≤ -40 dB (0 to 8 GHz) ≤ -48 + 1.0 * f dB (f = 8 to 12 GHz)
32.0 GT/s	≥ -0.2 - 0.425 * f dB (f = 0 to 16 GHz) ≥ 5 - 0.75 * f dB (f = 16 to 24 GHz)		≤ -45 dB (0 to 16 GHz) ≤ -55 + 0.625 * f dB (f = 16 to 24 GHz)	≤ -36 dB (0 to 16 GHz) ≤ -44 + 0.5 * f dB (f = 16 to 24 GHz)
64.0 GT/s	≥ -1.5 - 0.28125 * f dB (f = 0 to 16 GHz) ≥ 6 - 0.75 * f dB (f = 16 to 24 GHz)	≤-15dB (< 1.25 GHz) ≤-10dB (1.25 to 24 GHz)	≤ -60 dB (0 to 16 GHz) ≤ -70 + 0.625 * f dB (f = 16 to 24 GHz)	≤ -50 dB (0 to 16 GHz) ≤ -60 + 0.625 * f dB (f = 16 to 24 GHz)

Notes:

1. PSNEXT and PSFEXT are validated through simulation only.
2. In all equations, f is the frequency expressed in GHz.

For Insertion Loss and Return Loss, these measurements are defined as the measurement from where the conductive route exits the gold finger on the card edge to the die TX or RX of the endpoint package. Examples of this include the on die parasitics and ESD structures (but not the driver's output impedance), PCB route for TX or RX loss including vias and coupling capacitors (for TX), package TX and RX insertion loss, and reference plane location. The gold fingers are not included in the loss budget. An example is shown in Figure 8-2.

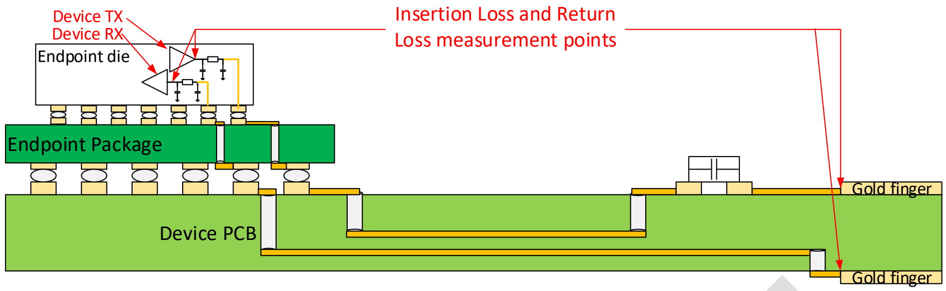


Figure 8-2. Example of Circuit Contributions to Insertion Loss and Return Loss

8.1.1 Insertion Loss (IL)

The Insertion Loss formulas for 16 GT/s, 32GT/s, and 64 GT/s are defined in Table 8-1.

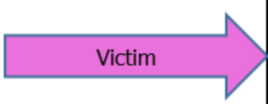
8.1.2 Return Loss (RL)

The Return Loss formulas for 16 GT/s, 32GT/s, and 64 GT/s are defined in Table 8-1.

8.1.3 Power Sum Near End Crosstalk (PSNEXT)

NEXT is defined between TX differential pair and RX differential pair. The power summation of NEXT on one pair TX/RX includes all the contribution of RX/TX pairs from the other side of the card edge. Figure 8-3 shows an example of the 3 worst lanes contributing to PSNEXT however devices should consider the connector pinout, the ASIC pinout, and routing when choosing the lanes for PSNEXT measurements. PSNEXT is measured at where the signal route exits the gold finger. NEXT and PSNEXT shall be referenced to 85 Ω differential impedance.

The Power Sum Near End Crosstalk formulas for 16 GT/s, 32GT/s, and 64 GT/s are defined in Table 8-1.



Pin	Signal	Signal	Pin
B16	GND	GND	A16
B17	PETn0	PERn0	A17
B18	PETp0	PERp0	A18
B19	GND	GND	A19
B20	PETn1	PERn1	A20
B21	PETp1	PERp1	A21
B22	GND	GND	A22
B23	PETn2	PERn2	A23
B24	PETp2	PERp2	A24
B25	GND	GND	A25
B26	PETn3	PERn3	A26
B27	PETp3	PERp3	A27
B28	GND	GND	A28

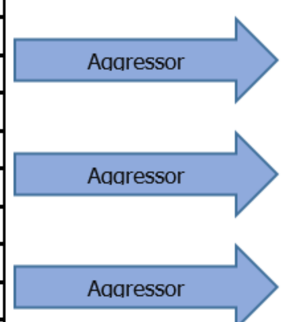
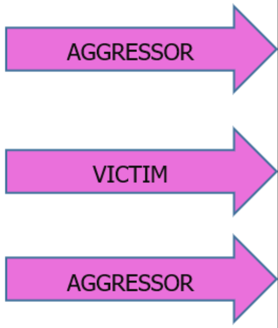


Figure 8-3. Example of PSNEXT Test Configuration for Device

8.1.4 Power Sum Far End Crosstalk (PSFEXT)

FEXT is defined between TX (or RX) differential pair at the card edge side and adjacent TX (or RX) differential pair to the die of the end point package. The power summation of FEXT on one pair includes all the contribution of TX (or RX) pairs starting from the same side of the card edge. Figure 8-4 shows an example of the worst lanes contributing to PSFEXT however devices should consider the connector pinout, the ASIC pinout, and routing when choosing the lanes for PSFEXT measurements. PSFEXT is measured at where the signal route exits the gold finger.

The Power Sum Far End Crosstalk formulas for 16 GT/s, 32GT/s, and 64 GT/s are defined in Table 8-1.



Pin	Signal	Signal	Pin
B16	GND	GND	A16
B17	PETn0	PERn0	A17
B18	PETp0	PERp0	A18
B19	GND	GND	A19
B20	PETn1	PERn1	A20
B21	PETp1	PERp1	A21
B22	GND	GND	A22
B23	PETn2	PERn2	A23
B24	PETp2	PERp2	A24
B25	GND	GND	A25
B26	PETn3	PERn3	A26
B27	PETp3	PERp3	A27
B28	GND	GND	A28

Figure 8-4. Example of PSFEXT Victim and Aggressors

8.2 Transmitter and Receiver Sensitivity Eye Limits

The following goes through the specific parameter deviations from the *PCI Express Card Electromechanical Specification* for the transmitter and receiver sensitivity (minimum Eye opening) for an EDSFF host and device to meet the PCIe electrical specifications. All methodologies and patterns shall follow what is documented in the *PCI Express Card Electromechanical Specification.* All measurements are based on simulations assuming test fixtures like what is used in the *PCI Express Card Electromechanical Specification.* The requirements in the following tables may change once test fixtures for EDSFF are produced.

8.2.1 EDSFF Device Transmitter Eye Mask

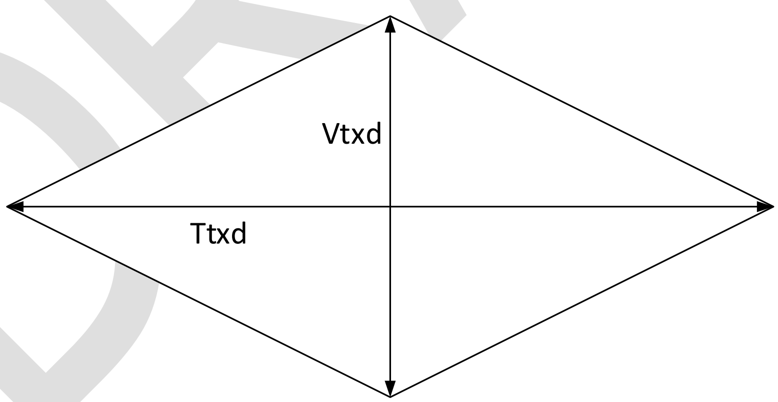


Figure 8-5. Eye Diagram for EDSFF Device Transmitter

Table 8-2. EDSFF Device Transmitter Eye Mask for PCIe at 16.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxd	24.25	1300	mV	
Ttxd	25.69		ps	

Table 8-3. EDSFF Device Transmitter Eye Mask for PCIe at 32.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxd	24.70	1300	mV	
Ttxd	13.40		ps	

Table 8-4. EDSFF Device Transmitter Eye Mask for PCIe at 64.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxd	6.7		mV	WC eye among all levels
Ttxd	3.28		ps	WC eye among all levels

8.2.2 EDSFF Host Transmitter Eye Mask

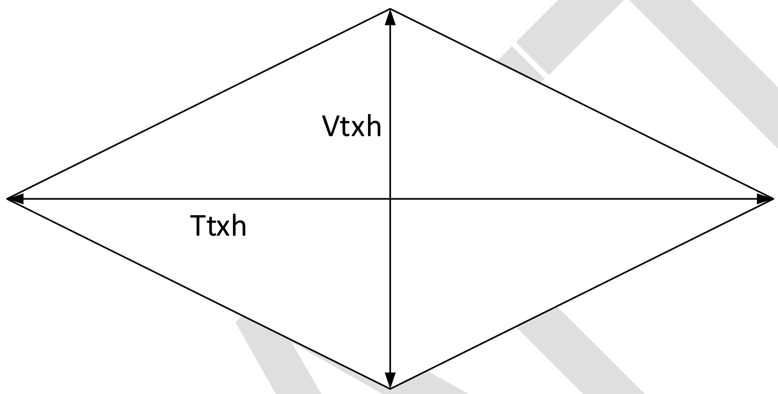


Figure 8-6. Eye Diagram for EDSFF Host Transmitter

Table 8-5. EDSFF Host Transmitter Eye Mask for PCIe at 16.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxh	17.75	1300	mV	
Ttxh	21.06		ps	

Table 8-6. EDSFF Host Transmitter Eye Mask for PCIe at 32.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxh	16.60	1300	mV	
Ttxh	10.10		ps	

Table 8-7. EDSFF Host Transmitter Eye Mask for PCIe at 64.0 GT/s

Parameter	Min	Max	Unit	Notes
Vtxh	5.30		mV	WC eye among all levels
Ttxh	2.97		ps	WC eye among all levels

8.2.3 EDSFF Device Receiver Minimum Sensitivity

No deviations from the *PCI Express Card Electromechanical Specification* for 64.0 GT/s and below except for the following:

For 32.0 GT/s and 64.0 GT/s, receiver sensitivity testing shall be tested with all device TX lines terminated and programmed to the same swing as what was used for device transmitter eye testing. The TX lines shall be sending data during this testing.

8.2.4 EDSFF Host Receiver Minimum Sensitivity

No deviations from the *PCI Express Card Electromechanical Specification* for 64.0 GT/s and below.

8.3 Test Fixtures

EDSFF uses SFF-TA-1002 which requires its own test fixtures.

9. NIC Implementation (Informative)

This section is provided to aid in the implementation of an OCP NIC 3.0 device in an EDSFF form factor. Unless otherwise specified, refer to the *OCP NIC 3.0 Design Specification* for more details on signaling and electricals.

The BIF[0..2], PRSNTA#, PRSNTB[0..3]#, PWRBRK0#, and AUX_PWR_EN signals used by the 4C+ connector are overlaid with different functions defined for the EDSFF 1C, 2C, and 4C connectors. It is the host's responsibility to detect what device is plugged into the host and configure for the correct usage to ensure proper device functionality. The GND/NIC_DETECT# signal is provided to help the host with this detection. This discovery process is beyond the scope of this specification.

The *OCP NIC 3.0 Design Specification* has different requirements on the 3.3 Vaux pin (called +3.3V_EDGE in the spec). See Section 9.2 for more details.

9.1 NIC Signals

NIC signals are only applicable if the 4C+ is implemented on the host and device. These signals are not applicable for the 1C, 2C, and 4C connectors. All pull-ups are referenced to 3.3 V.

This section is provided as a courtesy only. refer to the *OCP NIC 3.0 Design Specification* for more details on the signal functions.

9.1.1 REFCLKp2, REFCLKn2, REFCLKp3, REFCLKn3

Devices and hosts that support 4 link bifurcation of the PCIe lanes shall also implement REFCLKp2, REFCLKn2, REFCLKp3,REFCLKn3. Refer to the *PCI Express Base Specification* for more details on the functional and tolerance requirements for the reference clock signals.

9.1.2 PERST2#, PERST3#

Devices and hosts that support 4 link bifurcation of the PCIe lanes shall also implement PERST2# and PERST3#. Refer to the *PCI Express Base Specification* for more details on the functional requirements.

9.1.3 WAKE#

WAKE# is an optional signal. See the *PCI Express Base Specification* for details on the functional requirements for the WAKE# signal. If WAKE# is supported by the host, then the WAKE# pin shall be pulled up on the host with a 9 kΩ to 60 kΩ resistor.

9.1.4 PWRBRK0#

PWRBRK# is an optional signal. See the *PCI Express Card Electromechanical Specification and the PCI Express Base Specification* for details on the functional requirements for PWRBRK# and transitioning into the Emergency Power Reduction State. If PWRBRK# is supported by the host, then the PWRBRK# pin shall be pulled up on the device with a 9 kΩ to 60 kΩ resistor.

This signal is shared with a RFU pin. Correct detection and configuration of this signal is the responsibility of the host. Not configuring the signal for the correct usage may result in undefined behavior with the device.

9.1.5 BIF[0..2]#

BIF[0..2]# are used by the host to configure the bifurcation support of a device. The signal is actively driven by the host. For functionality, sequencing, and timing details, refer to the *OCP NIC 3.0 Design Specification*.

These signals are shared with RFU, MFG, and DUALPORTEN# signals. Correct detection and configuration of these signals are the responsibility of the host. Not configuring these signals for the correct usage may result in undefined behavior with the device.

9.1.6 PRSNTA#

The PRSNTA# signal is used to indicate device presence. It is connected directly to ground on the host and connected to the PRSNTB[0..3]# pins on the device that are used. Refer to the *OCP NIC 3.0 Design Specification* for more details.

This signal is shared with the LED signal. Correct detection and configuration of this signal is the responsibility of the host. Not configuring the signal for the correct usage may result in undefined behavior with the device.

9.1.7 PRSNTB[0..3]#

The PRSNTB[0..3]# are used to detect device presence and provide the host PCIe capability information. The signals shall each be pulled up on the host by a 1 kΩ resistor. If used on the device, the signals shall have a 200 Ω series resistor between the card edge and the PRSNTA# signal and shall float if not used. Refer to the *OCP NIC 3.0 Design Specification* for more details on how to configure these resistors.

These signals are shared with PRSNT[0..2]# and RFU signals. Correct detection and configuration of these signals are the responsibility of the host. Not configuring these signals for the correct usage may result in undefined behavior with the device.

9.1.8 AUX_PWR_EN

AUX_PWR_EN is asserted by the host to indicate that the host and device are to be in aux power mode and tells the device aux power mode power rails are allowed to be powered. The signal shall be pulled down on the host using a 10 kΩ resistor. For sequencing and timing details, refer to the *OCP NIC 3.0 Design Specification*.

This signal is shared with the PWRDIS signal. Correct detection and configuration of this signal is the responsibility of the host. Not configuring the signal for the correct usage may result in undefined behavior with the device.

9.1.9 MAIN_PWR_EN

MAIN_PWR_EN is asserted by the host to indicate that the host and device are to be in main power mode and tells the device main power mode power rails are allowed to be powered. The signal shall be pulled down on the host using a 10 kΩ resistor. For sequencing and timing details, refer to the *OCP NIC 3.0 Design Specification*.

9.1.10 NIC_PWR_GOOD

NIC_PWR_GOOD is asserted by the device to indicate to the host that power is good when the host initiates the aux power mode or main power mode. The signal shall be pulled down on the host using a 100 kΩ resistor. For sequencing and timing details, refer to the *OCP NIC 3.0 Design Specification*.

9.1.11 RBT Interface

The RMII-Based Transport (RBT) interface is an optional sideband management interface. It's a nine-wire interface through which the NIC device can communicate with the rest of the system. Refer to the *DSP0222 NC-SI Specification* for more details.

9.1.12 SLOT_ID[0..1]

SLOT_ID[0..1] are used to assign the address for the Field Replaceable Unit (FRU) or the RBT interface address. The host shall either have a 100 Ω pull down or a 4.7 kΩ pull up depending on the physical slot mapping.

9.1.13 USB Interface (USB_DATp, USB_DATn)

The USB interface provides an optional sideband interface between host and device. It's a 2-pin differential interface with the device being the endpoint. Refer to the *United Serial Bus (USB) Specification* for more details on enumeration, protocol, electricals, and other features.

9.1.14 Scan Chain Interface

The Scan Chain Interface provides status indication between host and device. Refer to the *OCP NIC 3.0 Design Specification* for more details on functional and timing requirements.

The CLK pin shall be pulled up on the device through a 1 kΩ resistor. The DATA_OUT pin shall be pulled down on the device through a 10 kΩ resistor. The LD# pin shall be pulled up on the device through a 10 kΩ resistor

If the host supports the Scan Chain Interface, the DATA_IN pin shall be pulled up using a 10 kΩ resistor.

If the host supports a 4C+ connector but does not support Scan Chain Interface, the CLK pin shall be connected to ground and the DATA_OUT pin shall be pulled down using a 1 kΩ resistor, and the LD# pin shall be pulled up with a 1 kΩ resistor.

9.2 3.3 Vaux consideration

EDSFF supports a much lower current on the 3.3 Vaux pin than what is supported on the same pin in the *OCP NIC 3.0 Design Specification* (pin is called +3.3V_EDGE). Hosts that support the 4C+ connector will need to support up to 1.1 A on the 3.3 Vaux pin.

10. I3C Basic Implementation (Informative)

This section is provided to aid in the implementation of I3C Basic on EDSFF devices. This section is provided as informative only. For normative details, please refer to the *PCI Express® (PCIe) Base Specification.*

10.1 I3C Basic features and discovery

For context, an I3C Basic capable host and an I3C Basic capable device are physical entities. An I3C Basic controller and I3C Basic target are logical entities.

The following I3C Basic features from *I3C Basic Specification revision 1.1.1* should be supported if I3C Basic is supported:

a) The Target Reset pattern (RSTACT) with Common Command Code 2Ah (Broadcast) and 9Ah (Direct). This allows the ~~host~~ I3C Basic controller to perform a I3C Basic peripheral reset without having to go back to SMBus mode.
b) Asynchronous Timing Control (Mode 0) (support determined if GETXTIME CCC is acknowledged). This aids in scenarios needing real time communication by providing a timestamp.
c) Grouped addressing (support determined through GETCAPS CCC). This allows broadcast request to multiple I3C Basic ~~endpoints~~ targets using a single message.
d) SETBUSCON CCC. MIPI recommends using SETBUSCON to inform I3C Basic targets of the specific use of the ~~Bus~~interface, and that vendor specific CCCs will be used. ~~Can~~ SETBUSCON also informs I3C Basic targets of the version of the specification that the I3C Basic ~~C~~controller supports.

The goal of the I3C Basic device discovery flow as shown in Figure 10-1 is to enable an I3C Basic capable host and I3C Basic capable ~~endpoints~~ devices to establish I3C Basic communication while allowing backward compatibility with legacy SMBus capable devices. If one side of communication supports both SMBus and I3C Basic and the other side is SMBus only, SMBus protocol and voltage is used. If there is a mix of I3C Basic and SMBus devices that are active on the same bus, then only SMBus protocol and voltage is used. ~~This flow should be initiated after any power rail state change.~~

Any time a device transitions from no power applied to power applied, whether powered via auxiliary or main power, the device starts in SMBus mode. Executing the SMBus to I3C transition flow is allowed any time the I3C Basic capable host and I3C Basic capable device are both powered and accessible.

A device transitions from I3C to SMBus mode when the I3C Basic target observes SMBCLK low for at least Tdcl or the device is reset through other supported hardware means (e.g., SMRST#).

The discovery flow uses reserved address (7Eh) to determine if there are ~~devices that support~~ I3C Basic targets on the bus. Address 7Eh is reserved in the *System Management Bus (SMBus) Specification* and cannot be assigned to any SMBus ~~device~~target. Address 7Eh is defined for I3C Basic and every I3C Basic ~~device~~ target responds as per the *I3C Basic Specification*. Any time a device that supports both SMBus and I3C Basic sees address 7Eh, it should disable SMBus (not drive or stretch the clock, nor ACK SMBus addresses) until reset to help the I3C Basic capable host determine if there are SMBus only ~~devices~~ targets on the bus. If only I3C Basic ~~devices~~ targets are detected and the I3C Basic capable host chooses to use I3C Basic then the I3C Basic capable device requires a transition time from 3.3 V to the I3C Basic voltage within the time Tsmb2i3c. A reset by driving a system management hardware mechanism (e.g., SMRST# or power removal) if supported by a given form factor or driving the clock low for T2wrst~~a specified period~~ reverts the interface to SMBus at 3.3 V signaling within the time Ti3c2smb. An I3C Basic Target Reset issued by the ~~host~~ I3C Basic controller resets the I3C Basic interface but not impact the signaling voltage. See Figure 10-1 for more details into this flow.

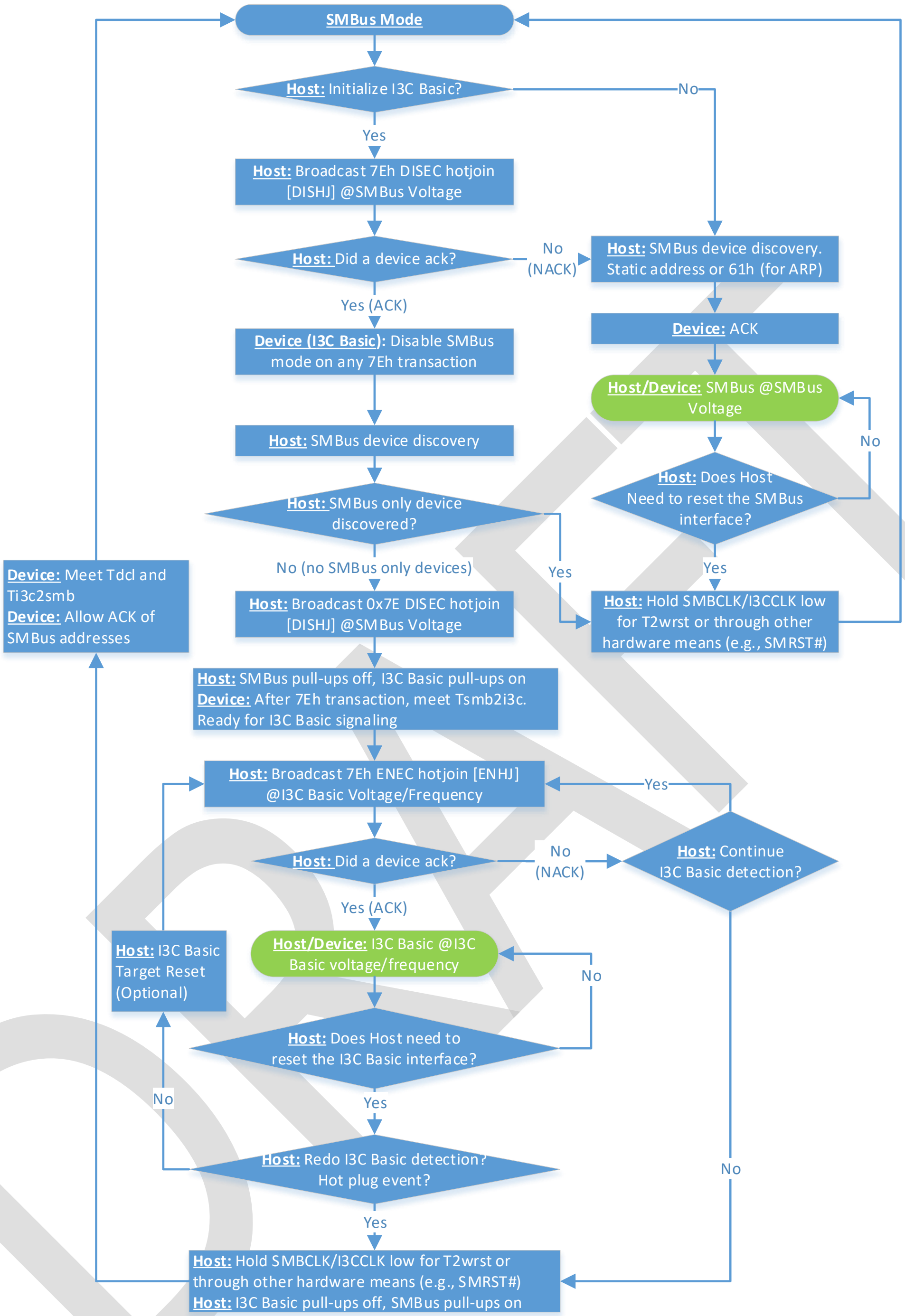


Figure 10-1. SMBus to I3C Basic transition flow