SFF-8679

Specification for

QSFP+ 4X Hardware and Electrical Specification

Rev 1.8.4 January 10, 2025

SECRETARIAT: SFF TA TWG
This draft specification is made available for public review at https://www.snia.org/sff/specifications. Comments may be submitted at https://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

This document has been released by SNIA. The SFF TWG believes that the ideas, methodologies, and technologies described in this document are technically accurate and are appropriate for widespread distribution.

The description of the connector in this specification does not assure that the specific component is available from connector suppliers. If such a connector is supplied, it should comply with this specification to achieve interoperability between suppliers.

ABSTRACT: This specification defines the contact pads, the electrical, power supply, ESD and thermal characteristics of the pluggable QSFP+ module or cable plug.

There are multiple generations of QSFP+ that reference this specification:

SFF-8635 QSFP+ 4X 10 Gb/s Pluggable Transceiver Solution (QSFP10)
SFF-8685 QSFP+ 4X 14 Gb/s Pluggable Transceiver Solution (QSFP14)
SFF-8665 QSFP+ Pluggable Transceiver Solution (QSFP+)
SFF-TA-1027 QSFP2 Cage, Connector and Module Specification

This specification supersedes the base electrical content of SFF-8436 QSFP+ 10Gb/s 4X Pluggable Transceiver.

This document provides a common specification for systems manufacturers, system integrators, and suppliers.

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Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, as well as since SFF's transition to SNIA in 2016, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/join.

Revision History

Rev 1.5:

- Moved referenced SFF specs to 2.1 Industry Documents and expanded the list.

Rev 1.6:

- Updated Figure 1 to show retimers.
- Removed two-wire interface timing diagram which is now in SFF-8636.
- Complete rewrite of power supply section to add support for Power Classes 5 to 7.
- Added section 8 "Timing Requirements".

Rev 1.7

- Editorial only, no technical changes.

Rev 1.8

- Converted to SNIA SFF template.
- Editorial updates throughout.
- Title changed to "Hardware and Electrical" to better reflect contents
- Updated abstract
- Updated editor contact information.
- Section 1 Scope – rewrote to better reflect content.
- Section 2 References – replaced several entries with updated document numbers and names.
- Section 2.3 Acronyms – deleted several unused entries and added several new ones based on content.
- Section 3 General Description – Rewrote most of this section to reflect updated content. Added several relevant applications to Table 3-1.
- Section 4 Compliance Testing – updated Figure 4-1 and corrected test point descriptions in Table 4-1.
- Section 5 Electrical Specification –
  - Updated Figure 5-1 and Table 5-1 to show the new dual-purpose signals LPMode/TxDis and IntL/RxLOSL on pads 31 and 28 respectively. Rewrote Note 2 of Table 5-1 for clarity.
  - Replaced "pin" by "pad" throughout
  - Replaced Figures 5-2 and 5-3 to better reflect current applications.
  - Extensive updates of Section 5.3 describing Low Speed Signals.
  - Updates to Table 5-2 to explain SCL and SDA electrical requirements and maximum pull-up resistor values for 400 kHz operation.
  - Significant revisions to text in 5.4 Low Speed Signal Electrical Specifications and 5.5 High Speed Signal Electrical Specifications.
  - Re-ordered and rewrote section 5.6 Power Supply Requirements including adding a new Power Class 8 with a maximum power limited only by the connector current rating.
- Section 6 Mechanical and Board Definition – cleaned up this section to reference the relevant documents instead of including non hardware/electrical features.
- Section 7 Environmental and Temperature – added a "custom" temperature class for modules that do not comply with any of the legacy case temperature ranges, e.g., hyperscale data center applications.
- Section 8 Timing Requirements
  - Major updates to Table 8-1 including re-writes of many entries in the "Conditions"

column.
    - Changed limit for "Reset Init Assert Time" from a maximum of 2 us to a minimum of 10 us.
    - Table 8-1: added new entries for "LPMode/TxDis mode change time", "IntL/RxLOSL mode change time", "RxLOSL Assert Time (Optional Fast Mode)", and "RxLOSL Deassert Time (Optional Fast Mode)".
    - Table 8-1: changed limit for "LPMode Assert Time" from 100 us to 100 ms.
    - Table 8-1: rewrote notes 1-5 and added new notes 6-7.
    - Table 8-2: changed maximum limits for "Rx Squelch Assert Time" and "Rx Squelch Deassert Time" from 80 us to 15 ms.
    - Table 8-2: added new parameters for "Tx Disable Assert Time (Optional Fast Mode)" and "Tx Disable Deassert Time (Optional Fast Mode)".
    - Table 8-2: corrected text in descriptions of Tx Squelch assert & deassert.
    - Added section 8.3 and Table 8-3 with timing for ModSelL setup and hold times, plus time for aborted sequence – bus release.
- Appendix A two-wire interface timing – Added a copy of the two-wire interface timing diagram (Figure A-1), timing parameters (Table A-1) and non-volatile memory timing specifications (Table A-2).

Rev 1.8.1 Nov 5, 2022
- Updated timing for soft control and status function.
- Updated power class table.
- Updated Fig.7 Instantaneous and sustained peak currents.
- Updated Power supply specification section for QSFP112.
- Added paragraph describing CMIS power mode control.
- Added Type 1, 2, 2A modules to Fig.6-1 and added text.
- Added CS and SN optical connectors.
- Updated Two Wire Interface Section 8 to add 1 MHz timing.

Rev 1.8.2 July 15, 2023
- Added alternative test methods for module power supply noise output and noise tolerance for QSFP-112

Rev 1.8.3 July 5th, 2024
- Replaced Fig 6-4 and Fig 6-8 per comments, changed Fig 6-9
- Editorial changes
- Edited Sections 6.6.5 and 6.6.6 –Module Power Supply Noise and Noise Tolerance test methods.

Rev 1.8.4 January 10, 2025
- Updated Fig 6-12,
- Added new voltage/current module RMS noise output specification for QSFP112/224
- Editorial changes (including to Boiler Plate)

Contents

Figures

Tables

1. Scope

This specification defines the electrical requirements for the QSFP10/14/28/56/112 pluggable 4-lane modules, hereafter referred to as QSFP+/QSFP2. The scope includes electrical contacts for the host connector; status, control and management interface signals; power supply requirements; fiber positions for optical interfaces; ESD and thermal characteristics and color coding of pluggable QSFP+ modules and cables.

This specification supersedes and extends INF-8438 QSFP (Quad SFP) 4 Gb/s 4X Transceiver and SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver by supporting higher data rates.

2. References, Conventions, Keywords, Definitions

2.1 Industry Documents

The following documents are relevant to this specification:

- ANSI/TIA-568.3-D Optical Fiber Cabling And Components Standards
- CMIS Common Management Interface Specification
- EIA-364-1000 Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Controlled Environment Applications
- ESD specifications EN61000-4-2, JEDEC JESD22-A114-B
- GR-63-CORE NEBS^{TM} Requirements: Physical Protection
- GR-253-CORE
- IEC 61754-7-1 Fibre optic interconnecting devices and passive components- Fibre optic connector interfaces - Part 7-1 Type MPO connector family - One fibre row
- IEC 61754-20 Fibre optic interconnecting devices and passive components- Fibre optic connector interfaces - Part 20 Type LC connector family
- IEEE Std 802.3
- IEEE Std 802.3ck
- INCITS 533-2016 Fibre Channel- Physical Interface - 6P (FC-PI-6P)
- INCITS 534-2019 Information Technology - Serial Attached SCSI - 4 (SAS-4)
- INCITS 559 Fibre Channel- Physical Interface - 7P (FC-PI-7P)
- INCITS 560 Fibre Channel – Physical Interfaces – 8 (FC-PI-8))
- INCITS 567-2023 Information Technology - Serial Attached SCSI - 4.1 (SAS-4.1)
- INF-8438 QSFP (Quad Small Formfactor Pluggable) Transceiver
- InfiniBand Architecture Specification
- ISO/IEC 14776-154: 2017 Information technology – Small computer system interface (SCSI) – Part 154: Serial Attached SCSI-3 (SAS-3)
- REF-TA-1011 Cross Reference to Select SFF Connectors
- SFF-8024 SFF Committee Cross Reference to Industry Products
- SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver – (EIA-964)
- SFF-8635 QSFP+ 10 Gb/s 4X Pluggable Transceiver Solution (QSFP10)
- SFF-8636 Management Interface for 4-Lane Modules
- SFF-8661 QSFP+ 28 Gb/s 4X Pluggable Module
- SFF-8662 QSFP+ 28 Gb/s 4X Connector (Style A)
- SFF-8663 QSFP+ 28 Gb/s Cage (Style A)
- SFF-8665 QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28)
- SFF-8672 QSFP+ 28 Gb/s 4X Connector (Style B)
- SFF-8682 QSFP+ 4X Connector (Style B)
- SFF-8683 QSFP+ Cage
- SFF-8685 QSFP+ 14 Gb/s 4X Pluggable Transceiver Solution (QSFP14)
- SFF-TA-1027 QSFP2 Cage, Connector and Module Specification
- TIA-604-5 FOCIS 5 Fiber Optic Connector Intermateability Standard – Type MPO
- TIA-604-10 FOCIS 10 Fiber Optic Connector Intermateability Standard – Type LC

2.2 Technical References

1. "Measuring PSNR/PSRR/PSMR to meet QSFP/OSFP high-speed Requirements", Steve Sandler, Bob Tarasewicz, Pavel Zivny, Tony Ambrose, DesignCon 2023.

2. "Power Integrity Testing Requirements Introduce Extreme Interconnect Measures", Steve Sandler, Signal Integrity Journal, February 2023 https://www.signalintegrityjournal.com/articles/2981-power-integrity-testing-requirements-introduce-extreme-interconnect-measures.

2.3 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

Other standards may be obtained from the organizations listed below:

Standard	Organization	Website
ANSI/TIA		
Electronic Industry Alliance (EIA)	Electronic Components Industry Association (ECIA)	https://www.ecianow.org/eia-technical-standards
IEC	International Electrotechnical Commission	https://webstore.iec.ch/
IEEE 802 standards	Institute of Electrical and Electronics Engineers (IEEE)	https://ieeexplore.ieee.org/browse/standards/get-program/page/series?id=68
INF	SNIA	https://www.snia.org/sff/specifications
ISO	International Organization for Standardization	
INCITS/Fibre Channel	International Committee for Information Technology Standards	INCITS: Information Technology Industry Council (ansi.org) [webstore.ansi.org]
InfiniBand	InfiniBand Trade Association (IBTA)	https://www.infinibandta.org
JEDEC	Joint Electron Deice Engineering Council (JEDEC)	https://www.jedec.org
OIF/CMIS	Optical Internetworking Forum (OIF)	https://www.oiforum.com/technical-work/implementation-agreements-ias/
PCIe	PCI-SIG	http://pcisig.com
SAS and other ANSI standards	International Committee for Information Technology Standards (INCITS)	https://www.incits.org
Telcordia (GR documents)	Ericsson	https://telecom-info.njdepot.ericsson.net

2.4 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS: Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a. red (i.e., one of the following colors):
    A. crimson; or
    B. pink;
b. blue; or
c. green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1. top;
2. middle; and
3. bottom.

Lists are associated with an introductory paragraph or phrase and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

DIMENSIONING CONVENTIONS: The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Defines the signal on a connector contact. Its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes (e.g., entities). If the context of the specification applies the restricted designation, then the restricted bit, byte, word, or field shall be treated as a value whose definition is not in scope of this document, and is not interpreted by this specification.

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

The following acronyms may be used in this specification:

ANSI	American National Standards Institute
ASIC	Application specific integrated circuit
ATM	Asynchronous transfer mode
CDR	Clock and data recovery
CML	Current mode logic
CORE	Central Office Relay Equipment
DC	Direct current
DDR	Double data rate
EDR	Extended data rate
EIA	Electronic Industries Alliance
EMI	Electromagnetic interference
ESD	Electrostatic discharge

FC	Fibre Channel
FDR	Fourteen Gb/s Data Rate
Gb/s	Gigabits per second
GbE	Gigabit Ethernet
GFC	Gigabit Fibre Channel
HDR	High Data Rate
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
ISO	International Organization for Standardization
ITU	International Telecommunications Union
JEDEC	Joint Electron Device Engineering Council
LVCMOS	Low voltage complementary metal oxide semiconductor
LVTTL	Low voltage transistor-transistor logic
MPO	Multi-fiber Push On
NEBS	Network Equipment Building System
OC	Optical Carrier
OMA	Optical Modulation Amplitude
PCB	Printed circuit board
PI	Physical Interface
QDR	Quad Data Rate
QSFP	Quad SFP
Rx	Receiver
SAS	Serial Attached SCSI
SDR	Single Data Rate
SerDes	Serializer-Deserializer
SFP	Small Formfactor Pluggable
SM	Single mode
SONET	Synchronous Optical NETwork
STM	Synchronous Transfer Mode
TIA	Telecommunications Industry Association
TTL	Transistor-transistor logic
Tx	Transmitter

3.3 Definitions

Connector: Each half of an interface that, when joined together, establishes electrical contact and mechanical retention between two components. In this specification, the term connector does not apply to any specific gender; it is used to describe the receptacle, the plug or the card edge, or the union of receptacle to plug or card edge. Other common terms include connector interface, mating interface, and separable interface.

Contact mating sequence: A term used to describe the order of electrical contact established/ terminated during mating/un-mating. Other terms include contact sequencing, contact positioning, mate first/break last, EMLB (early mate late break) staggered contacts, and long pin/short pin.

Contacts: A term used to describe connector terminals that make electrical connections across a separable interface.

Module: In this specification, module may refer to a plug assembly at the end of a copper (electrical) cable (passive or active), an active optical cable assembly, an optical transceiver, or a loopback.

Plug: A term used to describe the connector that contains the penetrating contacts of the connector interface as shown in Figure 3-1. Plugs typically contain stationary contacts. Other common terms include male, pin connector, and card edge.

Receptacle: A term used to describe the connector that contains the contacts that accept the plug contacts as shown in Figure 3-1. Receptacles typically contain spring contacts. Other common terms include female and socket connector.

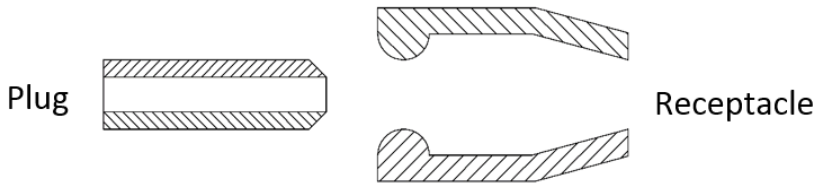


Figure 3-1 Plug and Receptacle Definition

4. General Description

4.1 Configuration Overview/Descriptions

This specification covers the following items:

- Electrical specifications for QSFP+ modules including host connector contact assignments.
- Descriptions for data, control, status and management interface signals.
- Power supply requirements.
- Electrostatic discharge (ESD) tolerance requirements.
- Color coding and labeling.
- Fiber positions for optical interfaces.
- Environmental and thermal requirements (case temperatures).
- Timing requirements.

This specification may be compatible with the example optical and electrical specifications in Table 4-1.

Table 4-1 Example uses for QSFP+

ITU-T Recommendation G.957	STM-1, STM-4, STM-16
Telcordia Technologies GR-253-CORE	OC-3, OC-12, OC-48, OC-192
IEEE Std 802.3	10 GbE, 25 GbE, 40 GbE, 50 GbE, 100 GbE, 200 GbE, 400GbE
Infiniband Architecture Specification	SDR, DDR, QDR, FDR, EDR, HDR, NDR
Fibre Channel	8GFC, 16GFC, 32GFC, 128GFC, 256GFC
Serial Attached SCSI	SAS-3, SAS-4; SAS-4.1

The Application Reference Model in Figure 4-1 shows the high-speed data interface between an ASIC (SerDes) and the module. Only one lane of the interface is shown for simplicity. Either parallel MPO or duplex LC fiber connectors can be used for the optical interface.

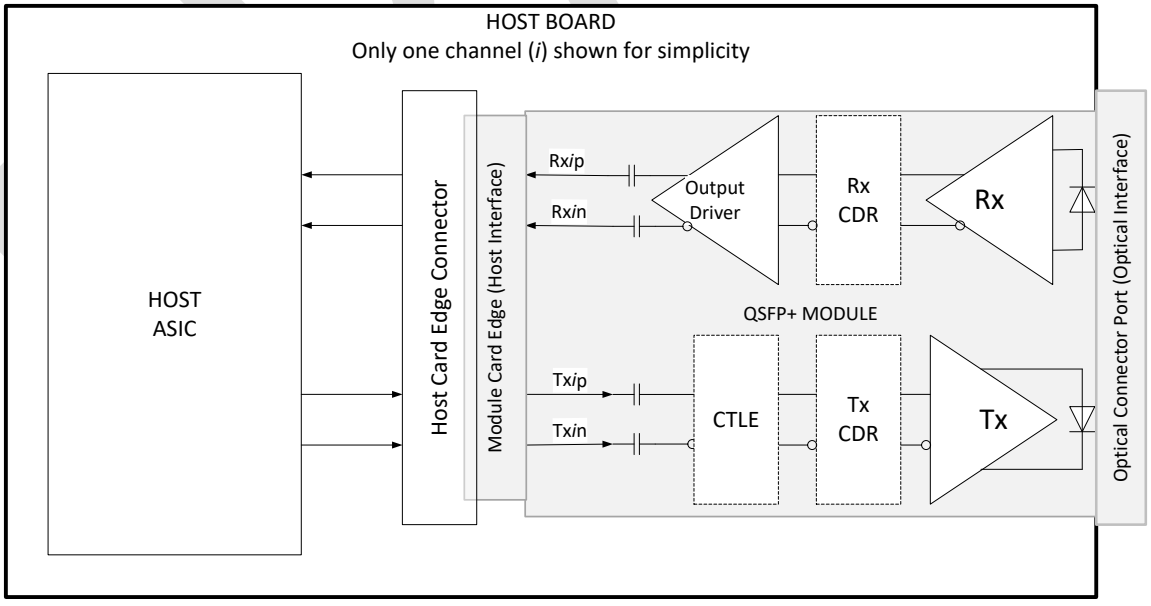


Figure 4-1 Application reference model

5. Compliance boards and reference points

The module electrical interface test points are intended to be measured using compliance boards as shown in Figure 5-1. These compliance boards are intended to connect the module under test to test equipment for verification of compliance to the appropriate standard. The Module Compliance Board is used to test the module. The electrical parameters of the compliance boards should be specified by the appropriate standard. The Module Compliance Board and Host Compliance Board can be plugged together for calibration of compliance signals and to check the electrical parameters of the compliance boards. Reference points are described in Table 5-1.

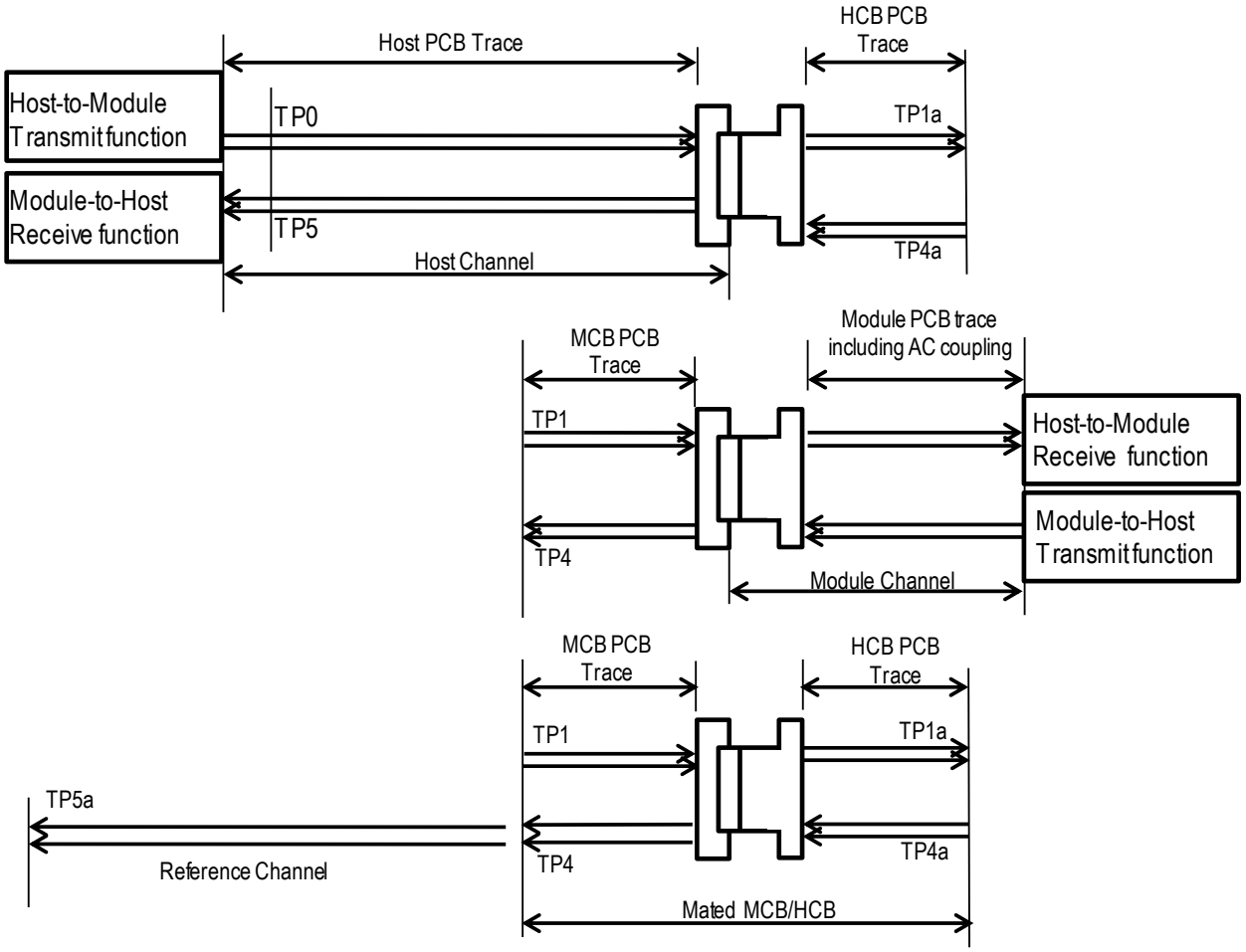


Figure 5-1 Reference Points and Compliance Boards

Table 5-1 Reference Points

Reference point	Description
TP0	Host ASIC transmitter output at ASIC package contact.
TP1	Input to Module Compliance Board. Used to test module input.
TP1a	Host ASIC transmitter output through the host board and host card edge connector at the output of the Host Compliance Board. Also used to calibrate module input compliance signals.
TP4	Module output through the compliance board connectors at the output of the Module Compliance Board. Also used to calibrate host input compliance signals.
TP4a	Input to Host Compliance Board. Used to test host input.
TP5	Input to host ASIC
TP5a	Far end module output through a reference channel
Note: Individual standards may specify unique reference points	

6. Electrical Specification

This chapter contains pad definition data for the module. The pad definition data is generic for high speed datacom applications such as Fibre Channel, Ethernet and SONET/ATM. Reference points for high-speed electrical measurements are defined in Table 5-1 and illustrated in Figure 5-1. Reference points for all other electrical signals are at comparable points at the host card edge connector.

6.1 Electrical Connector

Figure 6-1 shows the signal symbols and pad numbering for the module edge connector. The diagram shows the module PCB edge as a top and bottom view, where bottom is nearer the host PCB. There are 38 pads intended for high speed signals, low speed signals, power and ground connections. Color green identifies ground pads, color red identifies power pads, color orange identifies low speed signal/control pads, and color blue identifies high speed I/O pads. Table 6-1 provides more information about each of the 38 pads.

The module contains a printed circuit board that mates with the electrical connector. The pads are designed for a sequenced mating:

Connected first, disconnected last:	- ground contacts
Connected second, disconnected second:	- power contacts
Connected third, disconnected first:	- signal contacts

For EMI protection the signals to the connector should be shut off when the module is absent. Standard board layout practices such as connections to Vcc and GND with vias, the use of short and equal-length differential signal lines, and the use of microstrip-lines and 50 Ω terminations are recommended. The chassis ground (case common) of the module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

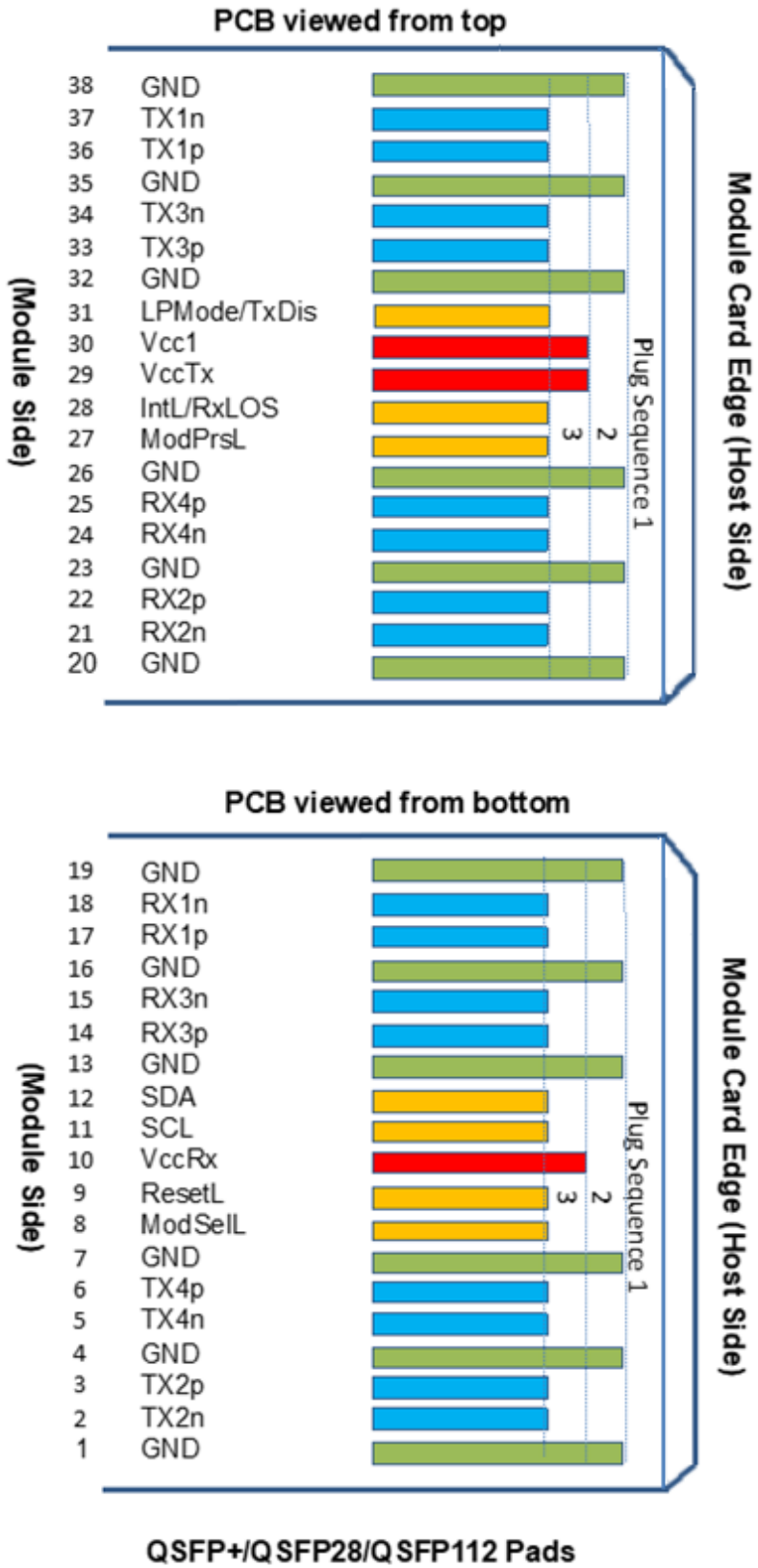


Figure 6-1 Module Pad Layout

Table 6-1 Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	Two-wire interface clock	3	
12	LVCMOS-I/O	SDA	Two-wire interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636 or CMIS).	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636 or CMIS).	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
For QSFP2, each connector GND contact is rated for a maximum current of 500 mA.

Note 2: VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1000 mA.
For QSFP2, each connector Vcc contact is rated for a maximum current of 1500 mA.
For Power Classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits.

1

6.2 QSFP Example Circuits

Figure 6-2 and Figure 6-3 provide example host board schematics for an optical QSFP+ module and for a QSFP+ copper cable plug respectively. Optical modules may have CDRs and equalizers in the module depending on the application.

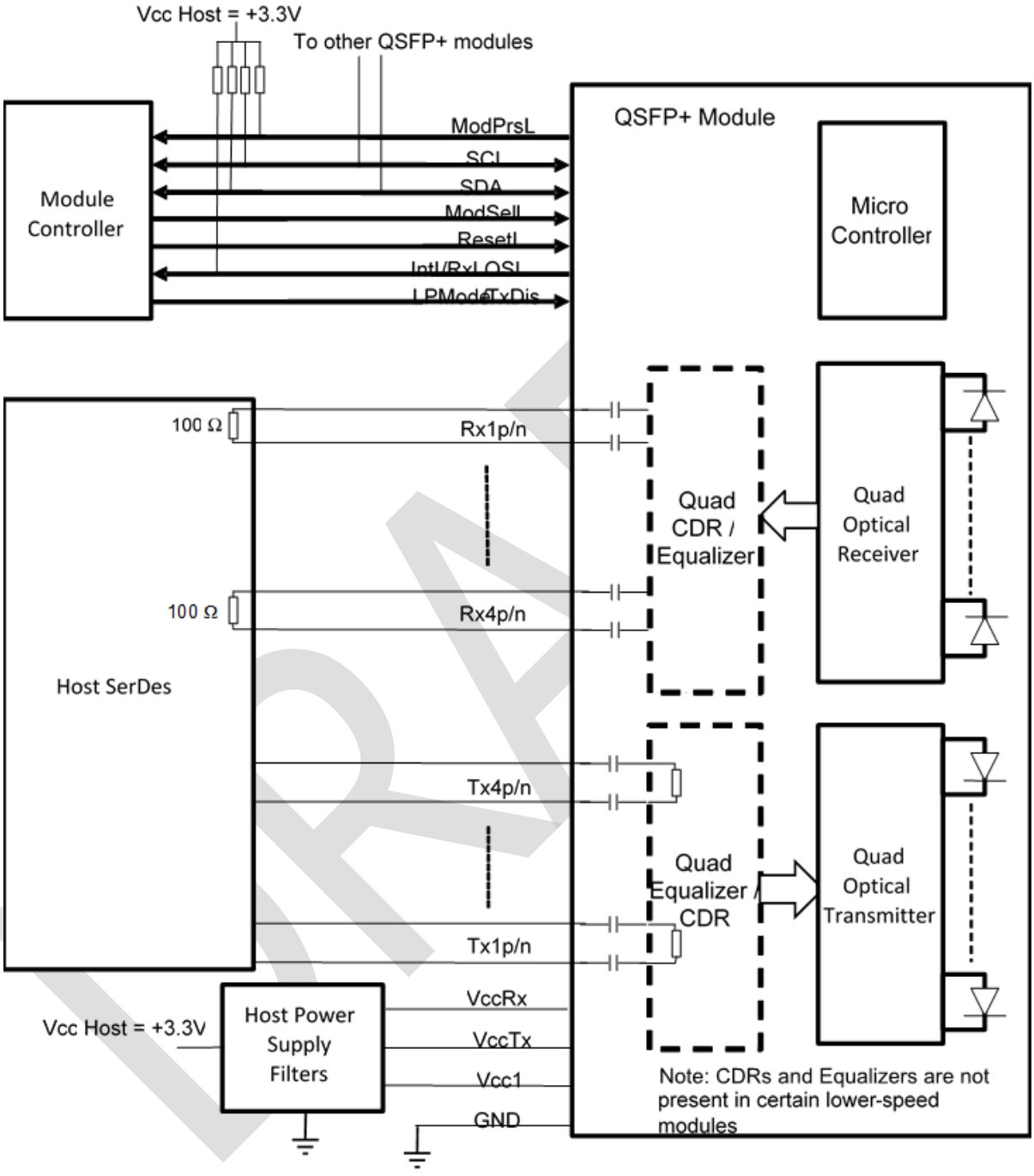


Figure 6-2 Example: Host Board Schematic for Optical Modules

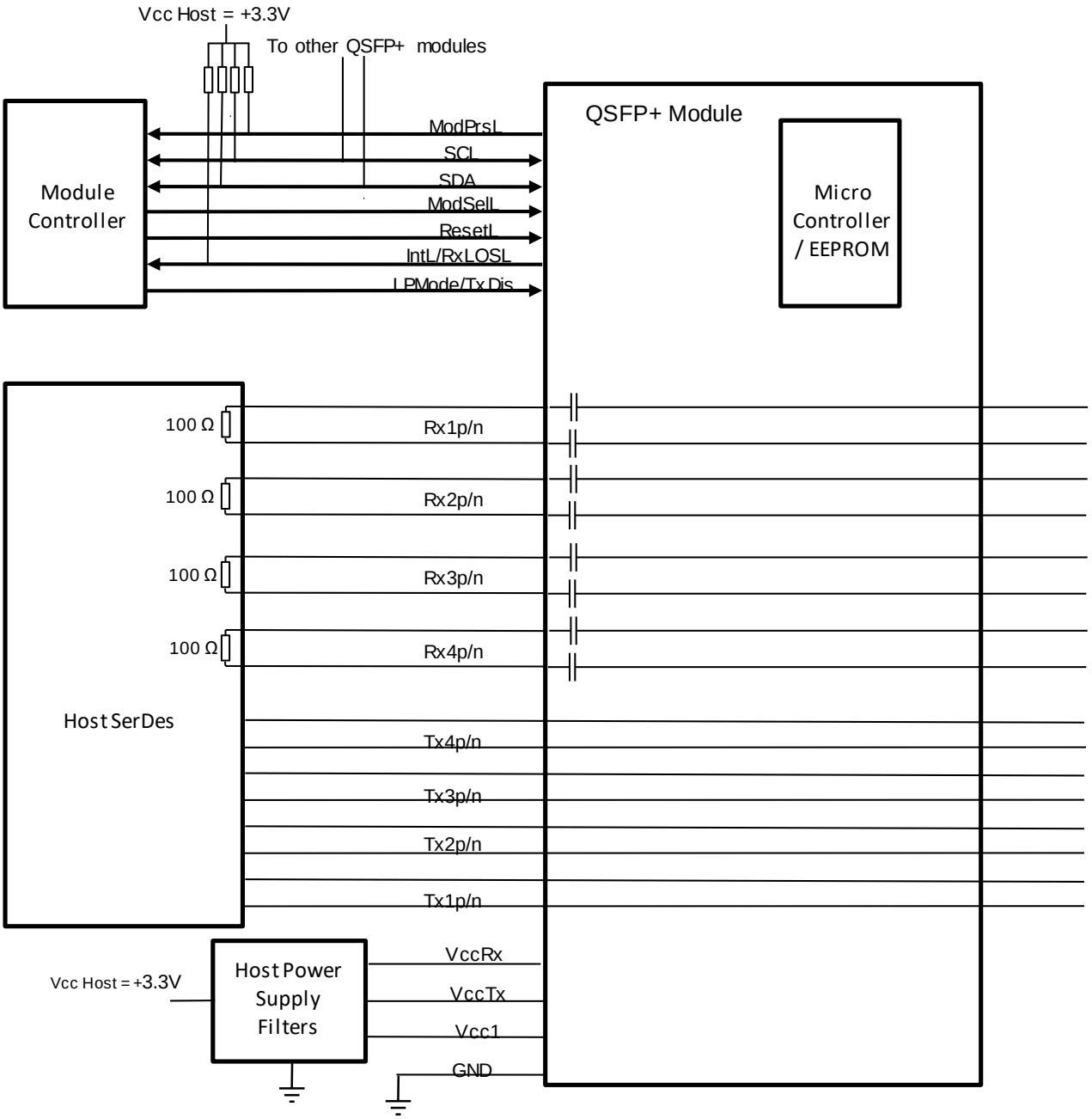


Figure 6-3 Example: Host Board Schematic for Passive Copper Cables

6.3 Low Speed Signal Descriptions

In addition to the two-wire interface the module has the following low speed signals for control and status:

- ModSelL
- ResetL
- LPMode/TxDis
- ModPrsL
- IntL/RxLOSL

The behavior of these signals is given in 6.3.1 to 6.3.5, the electrical specifications are in 6.4.1, and timing requirements are in 6.4.2 and Section 9. Timing requirements for the two-wire interface are in Appendix A.

6.3.1 ModSelL

ModSelL is an input signal. When held low by the host, the module responds to two-wire serial communication commands. The ModSelL signal allows the use of multiple modules on a single two-wire interface. When ModSelL is high, the module shall not respond to or acknowledge any two-wire interface communication from the host. The ModSelL signal input node shall be pulled towards Vcc in the module.
In order to avoid conflicts, the host system shall not attempt two-wire interface communications within the ModSelL hold time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL setup time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

6.3.2 ResetL

The ResetL signal shall be pulled towards Vcc in the module. A low level on ResetL for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level of the ResetL pad is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of reset interrupt by asserting "low" on the IntL/RxLOSL signal (see SFF-8636 or CMIS for details). However, on power up (including hot insertion) the module should post this completion of reset interrupt without the host pulling ResetL low.

6.3.3 LPMode/TxDis

LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after reset, LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the two-wire interface. TxDis provides an optional fast mode, see definition in SFF-8636 or CMIS.

When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0.

By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (SFF-8636, Address A0h, Byte 93 bits 0,1,2), the host controls how much power a module can consume. See CMIS Chapter 6.3.2 Module State Machine (MSM) on how LPMode is used in the control of the module power mode in transceivers with CMIS implementation.

See section 6.6 for more details on the power supply specifications.

When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters within the times specified in Table 9-1.

Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time. If the module is already in high power state (Power Override control bits) with transmitters already

enabled, the module shall disable all optical transmitters.

Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low, simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits.

Timing requirements for LPMode/TxDis mode changes are found in Table 9-1 .

Note that the "soft" functions of TxDis, LPMode, IntL and RxLOSL allow the host to poll or set these values over the two-wire interface as an alternative to monitoring/setting signal values. Asserting either the "hard pin" or "soft bit" (or both) for TxDis or LPMode results in that function being asserted.

6.3.4 ModPrsL

ModPrsL is pulled up towards VccHost on the host board and pulled towards ground in the module. ModPrsL is pulled low when the module is inserted and released to high when the module is physically absent from the host connector.

6.3.5 IntL/RxLOSL

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. If supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the two-wire interface. Rx LOS and RxLOSL timings, including an optional fast mode, are given in Table 9-1.

If IntL/RxLOSL is configured as IntL, a low indicates a change in module state, possible module operational fault or a module condition that sets an unmasked flag as defined in SFF-8636 or CMIS. The source of the IntL "low" can be read, cleared or masked using the two-wire interface. If the interrupt was after a module reset and SFF-8636, Page 00h, Byte 2, bit 0 (Data_Not_Ready bit) is 0, then the module releases IntL to high after the host has read the Data_Not_Ready bit. For all other interrupt causes, the module releases IntL to high after the host has read the flag associated with the cause of the interrupt.

If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. "high" indicates that there is no loss of received optical power. Rx LOS and RxLOSL timings, including an optional fast mode, are given in Table 9-1. The actual condition of loss of optical receive power is specified by other governing documents. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.

Timing requirements for IntL/RxLOSL mode change are found in Table 9-1. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.

6.4 Low Speed Signal Electrical Specifications

6.4.1 Low Speed Signaling

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, VccHost or Vcc1. Hosts shall use a pull-up toward VccHost on each of the two-wire interface SCL (clock) and SDA (data), and on the two low speed module status outputs ModPrsL and IntL/RxLOSL.

The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Compliance with Table 6-2 provides compatibility between host bus masters and the two-wire interface.

Table 6-2 Low Speed Electrical Specifications

Parameter	Symbol	Min	Max	Unit	Notes/Conditions
SCL and SDA	VOL	0	0.4	V	IOL(max)=3 mA IOL(max)=20 mA for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc + 0.5	V	
Capacitance on SCL and SDA I/O contact.	Ci		14	pF	Looking into the module SCL and SDA contacts.
Total bus capacitive load for SCL and SDA for up to 400 kHz SCL rate (includes capacitance of all elements on the bus).	Cb		100	pF	For 400 kHz clock rate use 3 kΩ pullup resistor, max For 1000kHz clock rate refer to Figure 6-4
			200	pF	For 400 kHz clock rate use 1.6 kΩ pullup resistor, max For 1000 kHz clock rate refer to Figure 6-4
LPMode/TxDis, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
	Iin	-365	125	µA	0 V ≤ Vin ≤ Vcc
IntL/RxLOSL	VOL	0	0.4	V	IOL=2 mA
	VOH	Vcc-0.5	Vcc+0.3	V	10 kΩ pull-up to VccHost
ModPrsL	VOL	0	0.4	V	IOL=2 mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

Notes:

Positive values indicate current flowing into the module. See Appendix A for management interface (SCL, SDA) timing information.

For Fast-mode Plus (SCL rate up to 1 Mbit/s), the total bus capacitive load is shown in Figure 6-4.

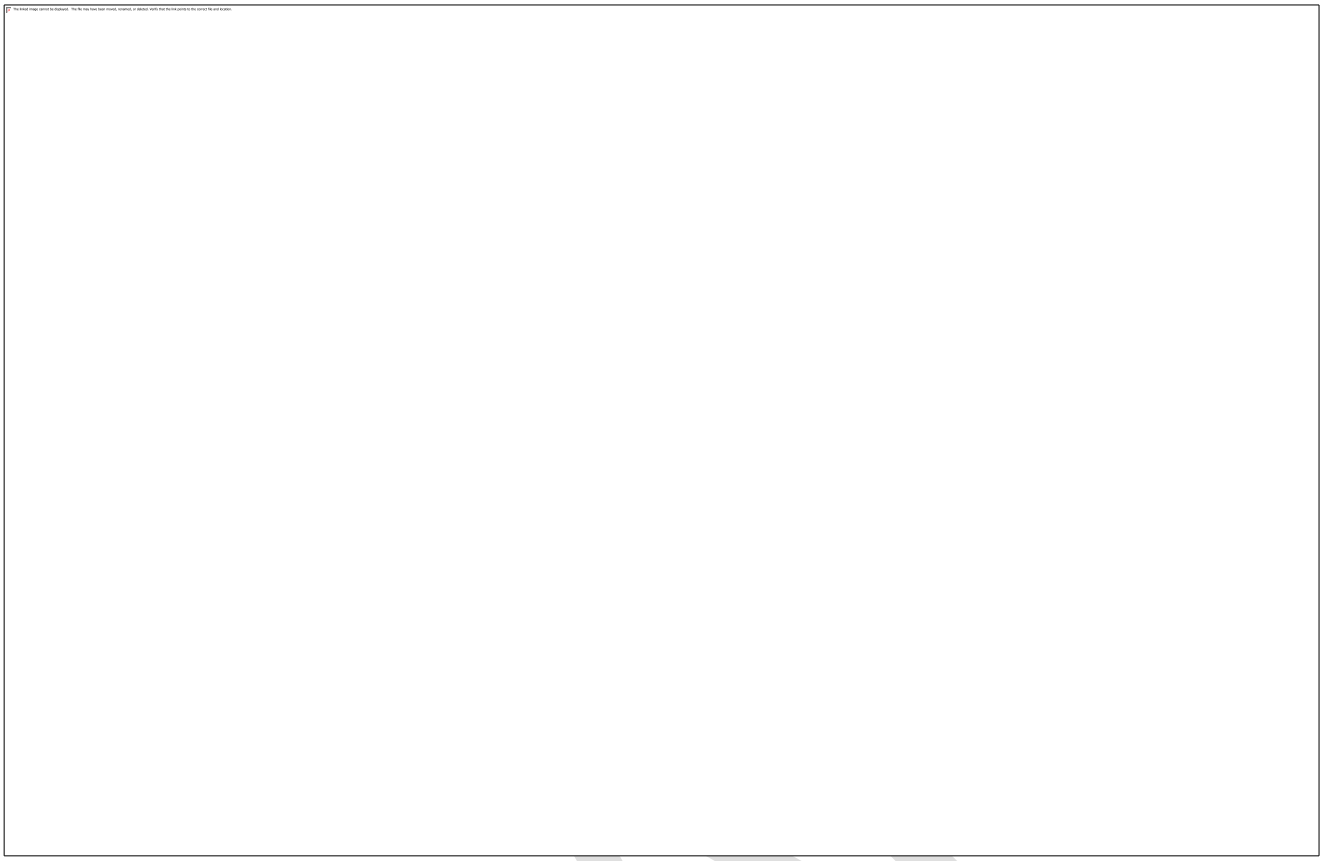


Figure 6-4 SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

6.4.2 Low Speed Signal Timing

Timing for SCL and SDA is defined in a management interface document, SFF-8636 or CMIS, and is duplicated in Appendix A for convenience. The default clock rate is a maximum of 400 kHz. An option to support up to 1 MHz clock rate may be advertised in CMIS P00h.2 (MciMaxSpeed). Initially, the host uses the 400 kHz clock rate, and does not switch to the higher data rate before it has established that it is supported by the module.

SFF-8636 and CMIS define tBUF timing, tWR timing, tNACK timing, tBPC timing.
Timing of the hardware control functions and ModSelL are specified in Table 9-1 and **31B**Table A-1.

6.5 High Speed Signal Electrical Specifications

For detailed electrical specifications for operation up to 29 GBd see e.g., IEEE Std 802.3 Annex 86A, Annex 83E, Annex 120C, or Annex 120E; Fibre Channel FC-PI-6, FC-PI-7 ; OIF CEI; InfiniBand FDR, EDR, HDR and NDR specifications. For detailed electrical specifications for operation up to 57.8 GBd see e.g., IEEE Std 802.3ck Annex 120G; OIF CEI; FC-PI-8.

Partial or complete squelch requirements may be provided in the appropriate specification. Where the relevant specification does not provide a requirement or a recommendation, the following subclauses shall apply.

6.5.1 Rx*i*p and Rx*i*n

Rx*i*p and Rx*i*n are module receiver data outputs. They are AC-coupled 100 Ω differential lines that should be terminated with 100 Ω differentially at the host ASIC (SerDes). The AC coupling is inside the module and not required on the host board.

Due to the possibility of insertion of legacy QSFP and QSFP+ modules into a host designed for higher speed operation, it is recommended that the damage threshold of the host input be at least 1600 mV peak to peak differential. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or as defined by the relevant standard, or whichever is less.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event that the optical signal on any lane becomes less than or equal to the level required to assert LOS, then the receiver data output for that lane shall be squelched or disabled and the associated RxLOS flag set. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp or the value in the relevant standard.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the two-wire interface. Rx Squelch Disable is an optional function. For specific details refer to SFF-8636 or CMIS.

6.5.2 Tx*i*p and Tx*i*n

Tx*i*p and Tx*i*n are module transmitter data inputs. They are AC-coupled 100 Ω differential lines with 100 Ω differential terminations inside the module. The AC coupling is inside the module and not required on the host board.

Due to the possibility of insertion of modules into a host designed for lower speed operation, the damage threshold of the module input shall be at least 1600 mV peak to peak differential.

Output squelch, hereafter Tx Squelch, for loss of input signal from the host, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event that the input signal becomes less than 50 mVpp or the value in the relevant standard, then the transmitter optical output for that lane shall be squelched or disabled and the associated TxLOS flag set. If multiple electrical input lanes are associated with the same optical output lanes, the loss of any of the incoming electrical input lanes causes the optical output lane to be squelched. Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm or the value(s) defined by the relevant standard. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the two-wire interface. Tx Squelch Disable is an optional function. For specific details refer to SFF-8636 or CMIS.

6.6 Power Supply Requirements

A host board together with the QSFP+ module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion or module state transitions.

The circuit card in a QSFP+ module has three designated power pads, designated VccTx, VccRx and Vcc1. When the QSFP+ module is "hot plugged" into a connector with power already present, the three pads have power applied concurrently. The module is responsible for limiting the inrush current surge from the reference power supply filtering circuit during a hot plug event. The host power supply may supply up to the maximum inrush current limits during a hot plug event without causing disturbance to other modules and components on the same power supply.

All specifications shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system. The module sequences the contacts in the order of ground, supply and signals during insertion.

6.6.1 Host Board Power Supply Filtering

The host board should use a power supply filtering network equivalent to that shown in Figure 6-5 .

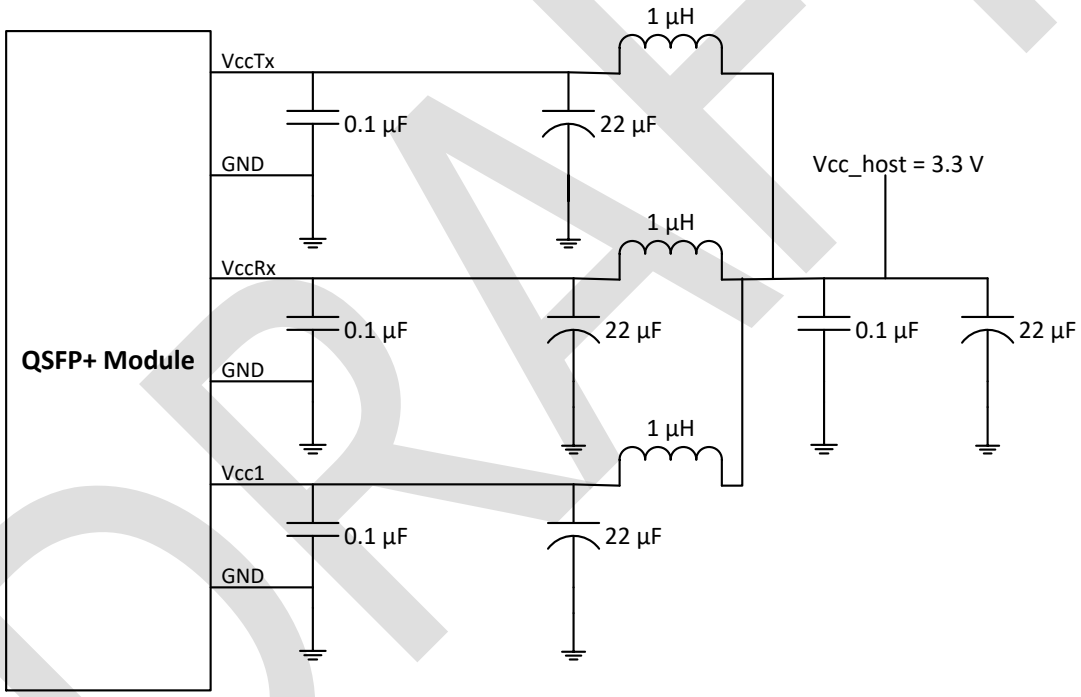


Figure 6-5 Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. System designers should choose components with appropriate DCR and ESR, in order to minimize the voltage drop and the amount of noise coupled to the module. Inductors with DC resistance of less than 0.1 Ω should be used in order to maintain the required voltage at the host edge card connector. It is recommended that the 22 µF capacitors each have an equivalent series resistance of 0.22 Ω.

The specification of the host power supply filtering network is beyond the scope of this specification, particularly because of the wide range of QSFP+ module power classes. An example current waveform into a host filter, labeled I1 in Figure 6-6 is plotted in Figure 6-7. Each power connection has a supply filter for reducing high frequency noise and ripple from host-to-module. During a hot-plug event, the filter network limits any voltage drop on the host supply so that neighboring modules sharing the same supply stay within their specified supply voltage limits.

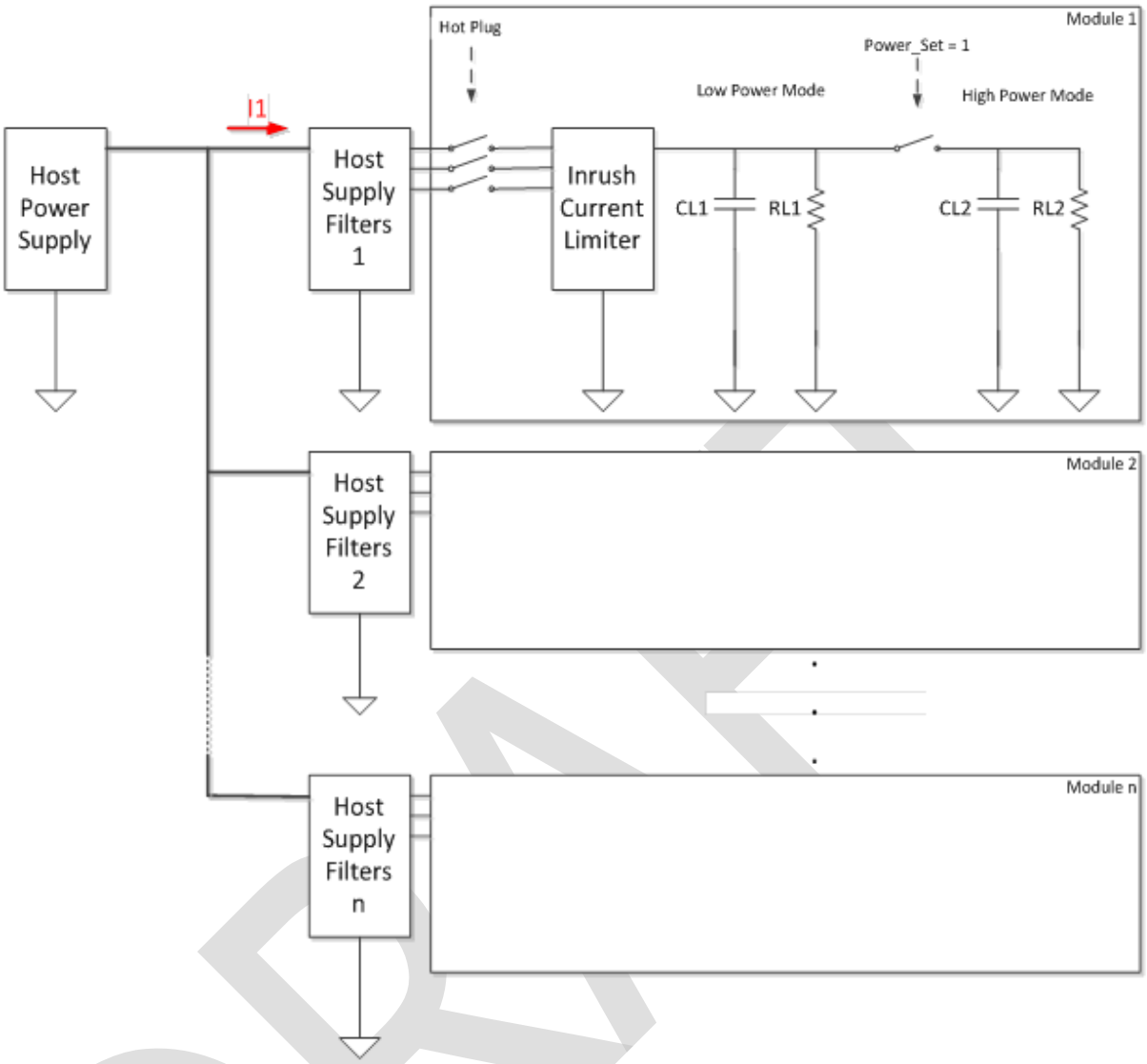


Figure 6-6 Example: Schematic of multiple QSFP+ power supply arrangement

6.6.2 Power Classes and Maximum Power Consumption

The Module Power Mode dictates the maximum power that the module is permitted to consume. The Module Power Mode is a function of the state of the Module State Machine. Two Module Power Modes are defined: Low Power Mode and High Power Mode. The maximum module power consumption in Low Power Mode for QSFP+ is 1.5W. The maximum module power consumption in High Power Mode is shown in Table 6-3.

Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the host power supply limits and cooling capacity when a module is inserted into a host designed to use only lower power modules. It is recommended that the host, through the management interface, identify the power consumption class of the module before allowing the module to go into High Power Mode.

All modules initially boot in Low Power Mode, while the module is transitioning through the initialization state. QSFP+ modules are categorized into several power classes as listed in Table 6-3. Power classes are advertised in SFF-8636, Page 00h, Byte 129 or CMIS, Page 00h, Byte 200. The maximum power consumption may be advertised in SFF-8636, Page 00h, Byte 107 or CMIS, Page 00h, Byte 201.

Table 6-3 QSFP+ Module Power Classes

Power Class	Maximum power consumption per module (W)
1	1.5
2	2.0
3	2.5
4	3.5
5	4.0
6	4.5
7	5.0
8	(Note)
Note: For Power Class 8, maximum power consumption is declared by the module in SFF-8636, Page 00h, Byte 107 or CMIS, Page 00h, Byte 201. Maximum power is limited by current rating of power supply pins.	

In order to avoid exceeding the host system power capacity and thermal management, upon hot-plug, power cycle or reset, all QSFP+ modules shall power up as if they were Power Class 1, designated as "Low Power Mode". QSFP+ modules that are Power Class 1 are fully functional after initialization and remain in Low Power Mode during operation. All other QSFP+ modules reach fully functional operation only after the host system enables "High Power Mode".

High Power Mode is defined as the power class advertised in SFF-8636, Page 00h, Byte 129 or CMIS, Page 00h, Byte 200 and is enabled by the host if the host can supply sufficient power to the module.

For QSFP+ modules managed according to SFF-8636, the host system controls whether a particular power class is enabled using the LPMode input pad and/or by writing to four control bits in SFF-8636, Page 00h, Byte 93. The management interface specification, SFF-8636 provides complete details but for explanation of power supply control, the bits are listed in Table 6-4.

Table 6-4 Power Mode Control Bits in SFF-8636, Page 00h, Byte 93)

Bit	Name	Description
7-4	Reserved	
3	High Power Class Enable (Class 8)	When set to 1 enables Power Class 8 if listed in Byte 129. When cleared to 0, modules with Power Class 8 shall dissipate less than the power specified by bit 2 but are not required to be fully functional. Refer to Table 5-5. Default=0.
2	High_Power_Class_Enable (Classes 5-7)	When set to 1 enables Power Classes 5 to 7 if listed in Byte 129. When cleared to 0, modules with Power Classes 5 to 8 shall dissipate less than 3.5 W but are not required to be fully functional. Default=0.
1	Power_set	Power set to Low Power Mode (Power Class 1). Default=0.
0	Power_override	Override of LPMode/TxDis pad state to allow power mode setting by software.

Note: Power Class 8 is managed by SFF-8636 rev 3.0 or higher.

A truth table showing the allowed power classes is shown in Table 6-5.

Table 6-5 Power Mode Truth Table

Power_override Byte 93 bit 0	Power_set Byte 93 bit 1	High_Power_ Class_Enable (Class 5-7) Byte 93 bit 2	High_Power_ Class_Enable (Class 8) Byte 93 bit 3	LPMode/TxDis pad state	Module Power Classes Enabled
Power consumption controlled by LPMode/TxDis pad state					
0	X	0	0	1	1
0	X	0	0	0	1 to 4
0	X	1	0	1	1
0	X	1	0	0	1 to 7
0	X	X	1	1	1
0	X	1	1	0	1 to 8
0	X	0	1	0	8
Power consumption controlled by Power_set bit					
1	1	0	0	X	1
1	0	0	0	X	1 to 4
1	1	1	0	X	1
1	0	1	0	X	1 to 7
1	1	X	1	X	1
1	0	1	1	X	1 to 8
1	0	0	1	X	8

For QSFP+ modules, using CMIS, the host may transition paged memory modules to High Power Mode using the conditions defined by the LowPwrS transition signal (see CMIS Table 6-12) provided that the advertised MaxPower value is supported in the host system.
If LowPwrS is FALSE when the module is in the ModuleLowPwr state, the module begins to enable High Power Mode operation, using the power up procedures defined for the ModulePwrUp state (see CMIS section 6.3.2.9). Conversely, whenever LowPwrS or LowPwrExS (as applicable) is TRUE while the module is in or moving towards High Power Mode, the module begins to return to the ModuleLowPwr state and hence to Low Power Mode operation, using the power down procedures defined for the ModulePwrDn state (see CMIS section 6.3.2.11).

6.6.3 Module Power Supply Specification

Module power supply specifications are given in Table 6-6.

QSFP+ modules operate from the host supplied voltage at the three power pads. To protect the host and system operation, each QSFP+ module during hot plug and normal operation shall follow the requirements listed in Table 6-6 and illustrated in Figure 6-7.
The test configuration for measuring the supply current is a module power compliance board with reference power supply filters, similar to the circuit shown in Appendix D and Figure 56 of SFF-8431. The current limits in Table 6-6 refer to the sum of the three currents, e.g. the equivalent of the current through the 0.1 Ω sense resistor in Figure 56 of SFF-8431.

An example current waveform into a host filter, labeled I1 in Figure 6-6 is plotted in Figure 6-7. This figure also shows the timing of the initial module turn-on in Low Power Mode, and the later transition to full power mode after the host system has enabled it via the two-wire interface. Timing for a transitional mode, when the module is in full power mode with the transmitter(s) disabled, is also shown.

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP modules shall power up in Low Power Mode if LPMode is asserted. If LPMode is not asserted the module will proceed to High Power Mode without host intervention. Figure 6-6 shows waveforms for maximum instantaneous, sustained

and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given Table 6-6.

The module shall not be affected by the instantaneous variations of the power supply caused by its own current drawing profile during all power transient events. The module shall withstand instantaneous power supply Vcc variations with a slew rate up to 175 mV/ms without traffic hits or errors on the two-wire interface.

Transmitter OFF state inrush current graph is informative. The instantaneous, sustained and steady state currents shall not exceed the high power mode transmitter ON current max values.

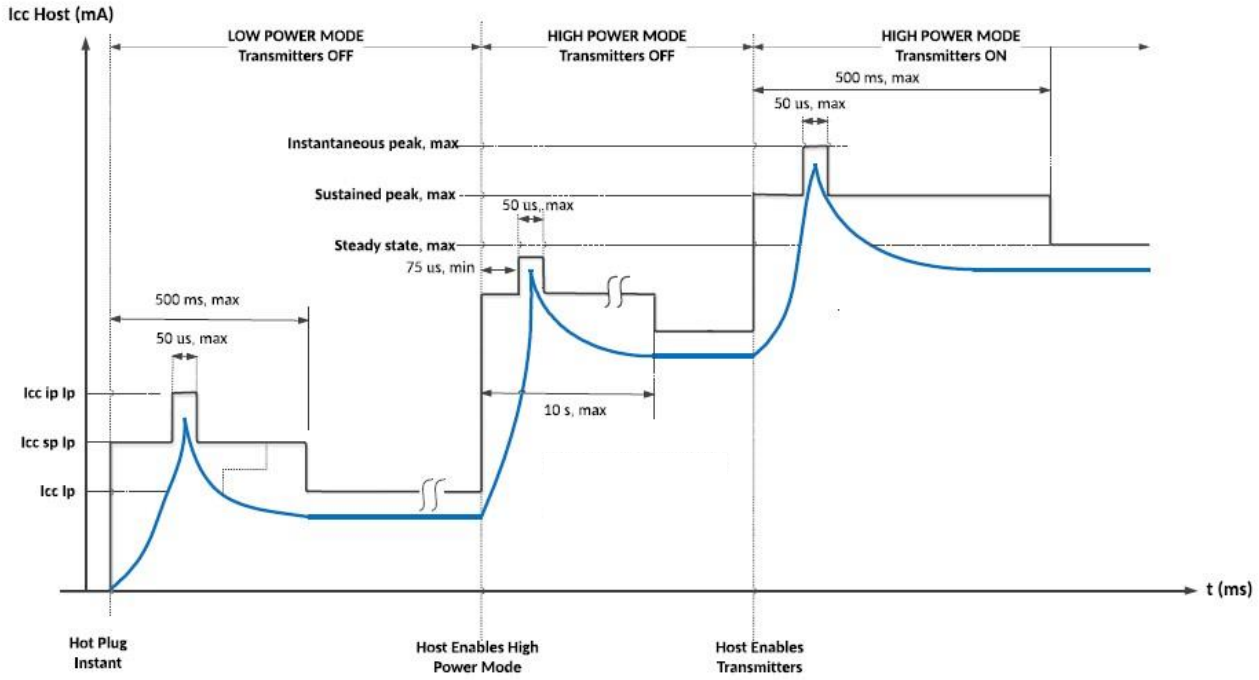


Figure 6-7 QSFP+ Inrush Current Timing

Table 6-6 QSFP+ Module Power Supply Specification

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccRx and Vcc1 including ripple, droop and noise below 100 kHz (Note 1)		3.135	3.3	3.465	V
Host RMS noise output 40 Hz to 10 MHz (eN_Host)				25	mV
Module RMS noise output 10 Hz to 10 MHz				15	mV
QSFP112/224 Module RMS noise output 40 Hz to 10 MHz (Note 2)				150	mA
Module power supply noise tolerance 40 Hz to 10 MHz (p-p)	PSNT_Mod	66			mV
Module inrush - instantaneous peak duration	T_ip	-	-	50	µs
Module inrush - initialization time	T_init	-	-	500	ms
Power Class 1 module and Low Power Mode for other modules					
Power consumption	P_1	-	-	1.5	W
Instantaneous peak current at hot plug	Icc_ip_1	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_1	-	-	495	mA
Steady state current (Note 3)	Icc_1	-	-	432.9	mA
High Power Mode Power Class 2 module					
Power consumption	P_2	-	-	2	W
Instantaneous peak current at hot plug	Icc_ip_2	-	-	800	mA
Sustained peak current at hot plug	Icc_sp_2	-	-	660	mA
Steady state current (Note 3)	Icc_2	-	-	577.2	mA
High Power Mode Power Class 3 module					
Power consumption	P_3	-	-	2.5	W
Instantaneous peak current at hot plug	Icc_ip_3	-	-	1000	mA
Sustained peak current at hot plug	Icc_sp_3	-	-	825	mA
Steady state current (Note 3)	Icc_3	-	-	721.5	mA
High Power Mode Power Class 4 module					
Power consumption	P_4	-	-	3.5	W
Instantaneous peak current at hot plug	Icc_ip_4	-	-	1400	mA
Sustained peak current at hot plug	Icc_sp_4	-	-	1155	mA
Steady state current (Note 3)	Icc_4	-	-	1010.1	mA
High Power Mode Power Class 5 module					
Power consumption	P_5	-	-	4	W
Instantaneous peak current at hot plug	Icc_ip_5	-	-	1600	mA
Sustained peak current at hot plug	Icc_sp_5	-	-	1320	mA
Steady state current (Note 3)	Icc_5	-	-	1154.4	mA
High Power Mode Power Class 6 module					
Power consumption	P_6	-	-	4.5	W
Instantaneous peak current at hot plug	Icc_ip_6	-	-	1800	mA
Sustained peak current at hot plug	Icc_sp_6	-	-	1485	mA
Steady state current (Note 3)	Icc_6	-	-	1298.7	mA
High Power Mode Power Class 7 module					
Power consumption	P_7	-	-	5	W
Instantaneous peak current at hot plug	Icc_ip_7	-	-	2000	mA
Sustained peak current at hot plug	Icc_sp_7	-	-	1650	mA
Steady state current (Note 3)	Icc_7	-	-	1443.0	mA
High Power Mode Power Class 8 module					
Power consumption (Note 4)	P_8	-	-	>5W	W
Instantaneous peak current at hot plug	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current at hot plug	Icc_sp_8	-	-	P_8/3.03	A
Steady state current (Note 3)	Icc_8	-	-	4.5	A

Note 1: Measured at VccTx, VccRx and Vcc1.
Note 2: When using the QSFP112/QSFP224 measuring method described in Section 6.6.5.2
Note 3: The module must stay within its advertised power class for all supply voltages.
Note 4: Maximum power consumption is advertised in SFF-8636, Page 00h, Byte 107 or CMIS, Page 00h, Byte 201.

6.6.4 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the eN_Host value in Table 6-6 when tested by the methods of SFF-8431, section D.17.1 with the following exceptions:

- The reference filter response H(f) is given by the equation in section D.17.1 using the coefficients from Table 6-7 below.
- The frequency response of the truncated function is illustrated in Figure 6-8.
- The resistive load for the test needs to be tailored for the QSFP power class and may be implemented using constant current sink circuits attached to each host supply filter output. The noise is measured independently on each voltage rail with the other voltage rails left open circuit.

Table 6-7 Truncated Filter Response Coefficients for Host Power Supply Noise Output

Frequency	a	b	c	d	e
10 Hz ≤ f ≤ 240.2 Hz	0	0	0	0	-0.1
240.2 Hz ≤ f ≤ 24.03 kHz	0.3784	-3.6045	12.694	-19.556	11.002
24.03 kHz ≤ f ≤ 360.4 kHz	-22.67038	430.392	-3053.779	9574.26	-11175.98
360.4 kHz ≤ f ≤ 12.6 MHz	3.692166	-91.467	838.80	-3400.38	5139.285
Note: Note: This table differs from SFF-8431 Table 32 in two ways: the frequency ranges differ because the inductor value in this specification is 1 uH, not 4.7 uH as in SFF-8431; and the sign of the value -91.467 in Column b differs, correcting an error.					

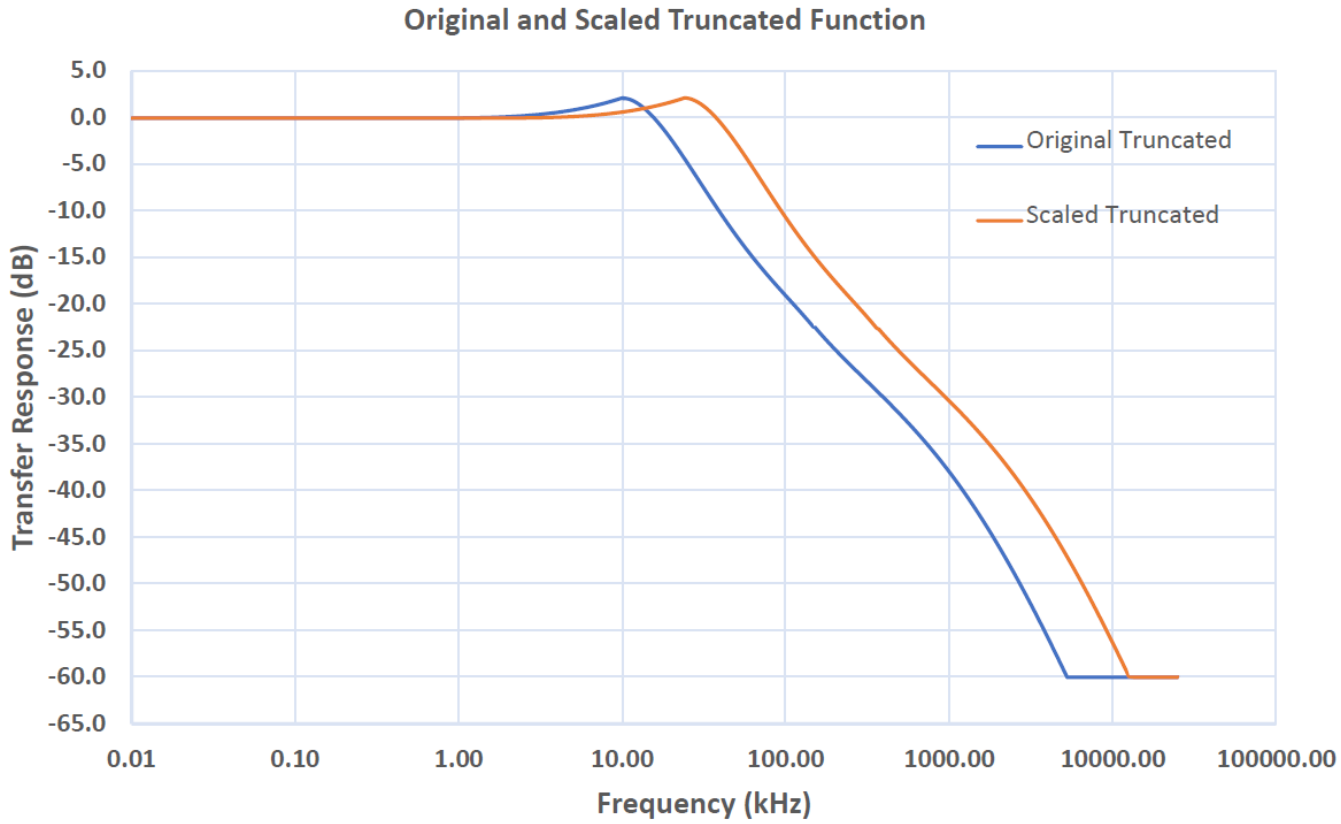


Figure 6-8 Truncated Transfer Response for Host Board Power Supply Noise Output measurement

6.6.5 Module Power Supply Noise Output

6.6.5.1 QSFP+ Module Power Supply Noise Output Test Method based on SFF-8431

The QSFP+ module shall generate less than the Module RMS noise output value in Table 6-6 when tested by the methods of SFF-8431, section D.17.2. The module noise voltage output is defined in the frequency band 10 Hz to 10 MHz at point X in Figure 6-99. The test fixture source resistor should be scaled by the ratio: (1.5 W / maximum module power consumption), where maximum module power consumption is either the maximum of the advertised power class, or the advertised maximum power. The test ensures the module will not couple excessive noise from inside the module back onto the host board. The module must pass the power supply noise output specification in all operating modes. A power meter technique, or a spectrum analyzer technique with integration of the spectrum may be used.

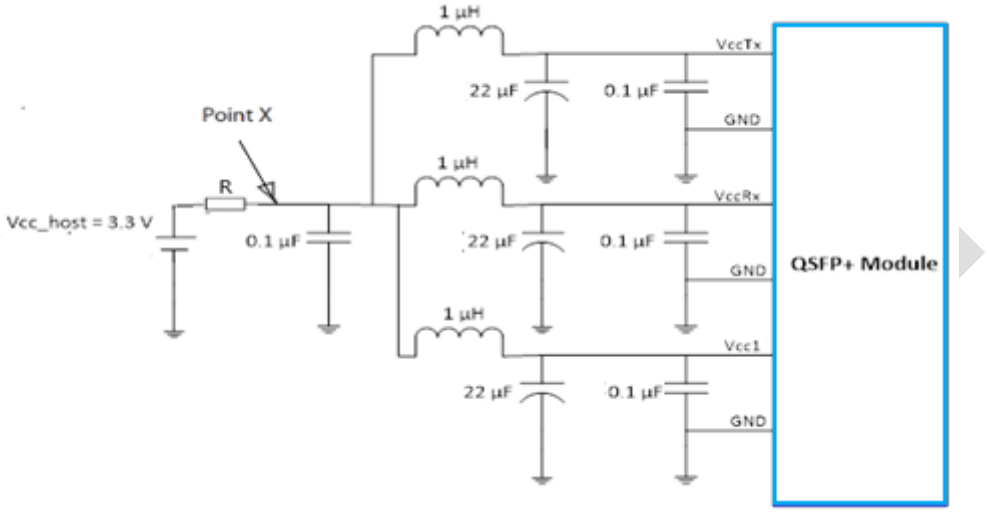


Figure 6-9 Module Compliance Board Power Supply Filters

6.6.5.2 QSFP112/QSFP224 Module Power Supply Noise Output Test Method

An alternative method was developed in the QSFP-DD MSA group for QSFP112 and QSFP224. The removal of power supply filters allows measuring actual noise generated by the module prior to any attenuation by the filter network.

This test method does not use a series resistor as in SFF-8431 and instead uses a current probe with a scope capable of integrating the current noise from 40 Hz to 10 MHz. Rogowski probes are recommended because they will minimize added interconnect inductance. Example of such probes are Tektronix TRCP series, Keysight N7042A or similar. Hall-effect current probes may also be acceptable if added interconnect is negligible, example of such probes are Tektronix TCP, Keysight N1147B.

The RMS module noise output is defined in a frequency band from 40 Hz to 10 MHz. The module noise output shall be measured with an appropriate probing technique at point Y, see **20B**Figure 6-10109. The leads from point Y to Vcc Host must be kept as short as possible to minimize the impact of added lead inductance. The module must pass the power supply noise output specification in all operating modes.

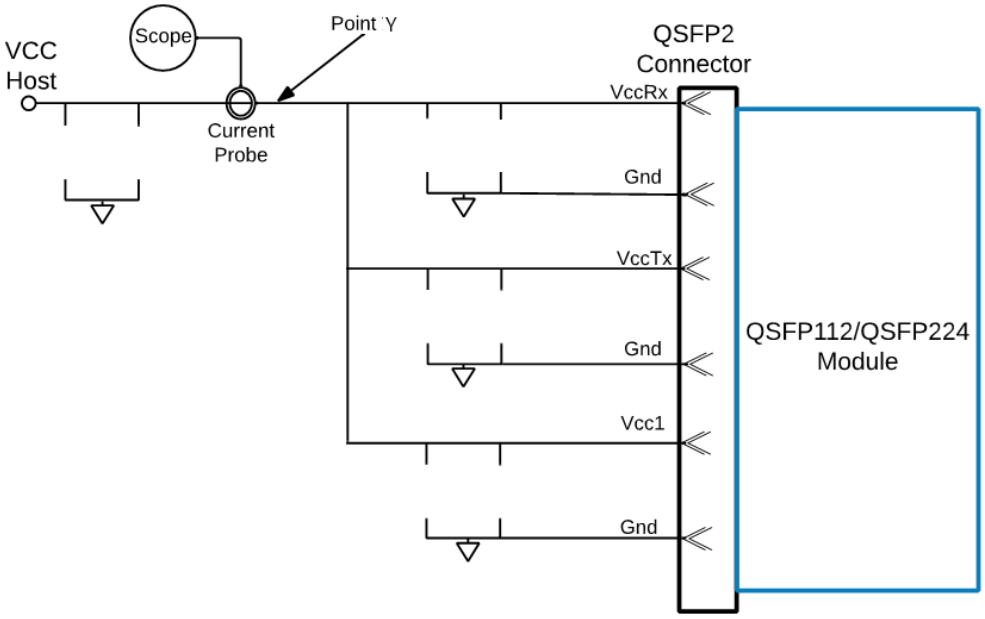


Figure 6-10 Module Noise Output measurement

6.6.6 Module Power Supply Noise Tolerance

6.6.6.1 QSFP+ Module Power Supply Noise Tolerance Test Method based on SFF-8431

The QSFP+ module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 6-6, swept from 10 Hz to 10 MHz according to the methods of SFF-8431, section D.17.3. This emulates the worst-case noise output of the host. The source resistance for the power supply and sine wave generator may need to be reduced from 0.5 Ω to a lower value for high powered modules.

In this test, a swept sinusoidal tone is applied at point X of Figure 6-99. The AC tolerance signal is created by a circuit such as a low impedance buffer amplifier between the power supply and point X. The impedance of the PSU and sine wave generator is less than 0.5 Ω. The amplitude of the sine wave is calibrated at each frequency at point X with the module replaced with a 12 Ω load between Vcc and Vee.
NOTES -- It may be desirable to remove the 0.1 uF capacitors on the host side of the reference filters for this test, to reduce the power needed by the sine wave generator. The calibration of the sine wave is not expected to be significantly different if the module were in place rather than the test resistor.
Alternatively, the test may be performed separately for VccT and VccR with the other supply filter connected directly to the power supply. It is not necessary to show compliance with both separate and common Vcc modulation.
This test applies at minimum and maximum DC setpoint levels. Note that the DC level is inset to the limits in Table 6-6 by the peak of the sinusoidal voltage at the input to the module (which is frequency dependent).
The source frequency is varied over the range specified by Table 6-6 to determine if any frequency causes a parameter to fall out of the specification limit. In all cases, the parameters measured shall pass the optical standards with the tone present over all frequencies specified.

6.6.6.2 QSFP112/QSFP224 Module Power Supply Noise Tolerance Test Method

An alternative method was developed in the QSFP-DD MSA group for QSFP112 and QSFP224. It is intended for easier compliance board setup and implementation. The removal of power supply filters simplifies the test and reduces the amplitude by as much as 1000x where off the shelf Power OpAmp can be used.

The QSFP112/QSFP224 modules shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 6-6.

The reference noise waveform consists of a sinusoidal 40 Hz to 10 MHz noise generated by Osc1, amplified by the Power OpAmp and added to Vcc PSU through a bias tee, see Figure 6-10. The injected power supply noise is

calibrated at point Y. Example of suitable Power OpAmps are Analog Devices ADA4870, LT1210, TI THS3491. Since most of these power OpAmps are limited to 1 A peak, the interconnecting impedance of the bias tee must be greater than 33 mV pk / 1 A pk or 33 mΩ minimum. Based on the minimum suggested frequency of 100 kHz, this can be resistive (33 mΩ minimum) or reactive (47 nH minimum). The bias tee effective capacitor needs to be greater than 47 uF, so a stable tantalum capacitor with 30 mΩ ESR is recommended.

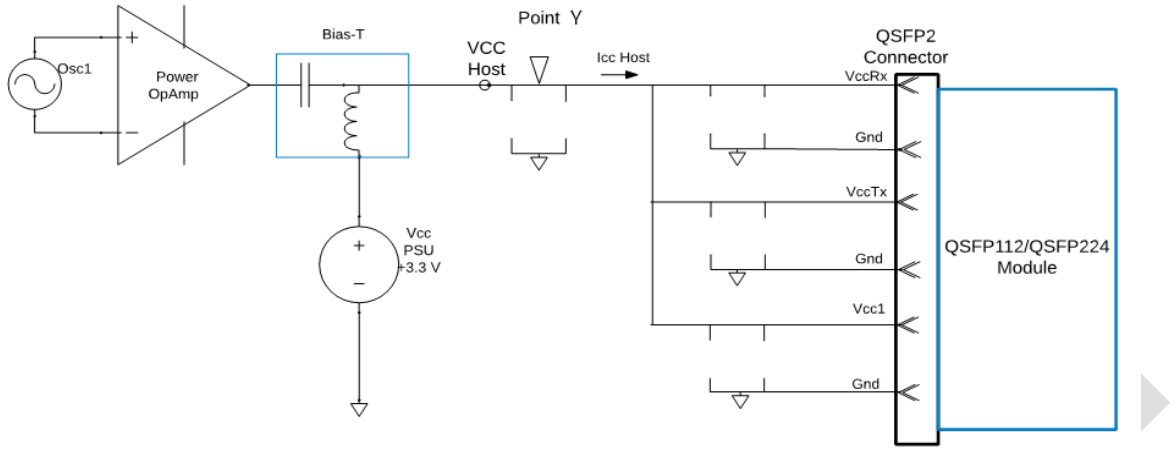


Figure 6-11 Module High Frequency Noise Tolerance

To facilitate power supply tolerance testing at frequencies < ~100 kHz due to Power OpAmp interaction with PSU and low frequency response of the Bias-T, it is recommended to use noise source Osc2 modulating PSU sense line to generate sinusoidal noise directly on the PSU output, see Figure 6-121211. Osc2 amplitude level is adjusted while observing point Y amplitude level as defined in Table 6-6 for module in low power and high-power modes. To modulate the PSU sense lines, the PSU must have high speed sense tracking. An example of PSU with high-speed sense tracking are Keysight N6700 Series, Kikusui PBZ series, or supply controllers, such as the TI TPSM5D1806.
The user is responsible for the calibration and the validation of the setup across the whole frequency range. The user may need to consider alternative proposed solutions if the electrical characteristics of the fixture and setup requires any component to work beyond its rated operating conditions.

Osc1 and Osc2 are adjusted to produce the value of PSNT_Mod PSNR given in Table 6-6 at point Y with resistive loads drawing the same power as the module in low and high-power modes. The resistive loads are then replaced with the module under test with the same Osc1/Osc2 amplitude settings that produced the max PSNR with the resistive loads.

An appropriate probing technique (such as transmission line probe) is required for noise measurement at point Y.

For modules with limited or no decoupling directly connected to host PSU, the PSNR can be directly measured at point Y with the module plugged into the host and the module operating in low power and high power modes. Osc1 or Osc2 are adjusted to provide maximum PSNR at point Y for a given module in low power and full power modes. Depending on the measurement setup, a ground loop isolator may be required to provide common mode rejection as described in Technical Reference 2 in Section 2.2 .

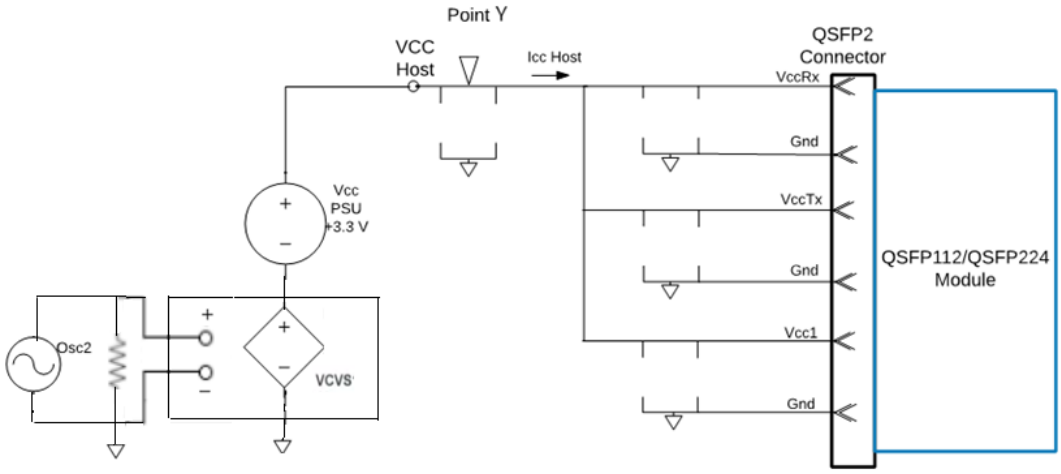


Figure 6-12 Module Low Frequency Noise Tolerance

Notes:

1. Module must be tested in low and high power modes.
2. Recommended test frequencies are below. Frequency sweep is suggested.

40, 50, 63, 80, 100, 125, 160, 200, 250, 315, 400, 500, 630, 800 Hz

1.0, 1.25, 1.6, 2.0, 2.5, 3.2, 4.0, 5.0, 6.3, 8.0, 10, 12.5, 16, 20, 25, 32, 40, 50, 63, 80, 100, 125, 160, 200, 250, 320, 400, 500, 630, 800 kHz

1.0, 1.25, 1.6, 2.0, 2.5, 3.2, 4.0, 5.0, 6.3, 8.0, 10 MHz

6.6.6.3 Module Power Supply Noise Tolerance Test Method using Commercial Injector Probe

Module Power Supply Noise Tolerance implementation of 6.6.6.2 can be replaced with commercially produced injector probes, an example of such injector probe is Picotest P2124A. Injector probe combines a power rail voltage (input voltage) with a modulation signal and injects the noisy bus voltage into the DUT being tested for noise immunity (PSNR). The form factor of injector probe is such that it can be positioned at the card edge, eliminating power cables and the inductance that can limit the modulation amplitude and bandwidth. This modulation scheme supports the full range from 40 Hz-10 MHz without having to change setups at ~100 kHz.

The probe-based implementation supports the requirements by getting close enough to the DUT to allow the 10 MHz modulation with little attenuation. The DC input power supply voltage at the host can be held constant using a supplied remote sense filter. The remote sense filter allows the user to switch between different operating modes (high power, low power etc.) while keeping the operating point stable across every power state transition. With the appropriate PSU unit and remote filtering, the injector probe will compensate for any additional voltage drop due to the modulator and the interconnects.

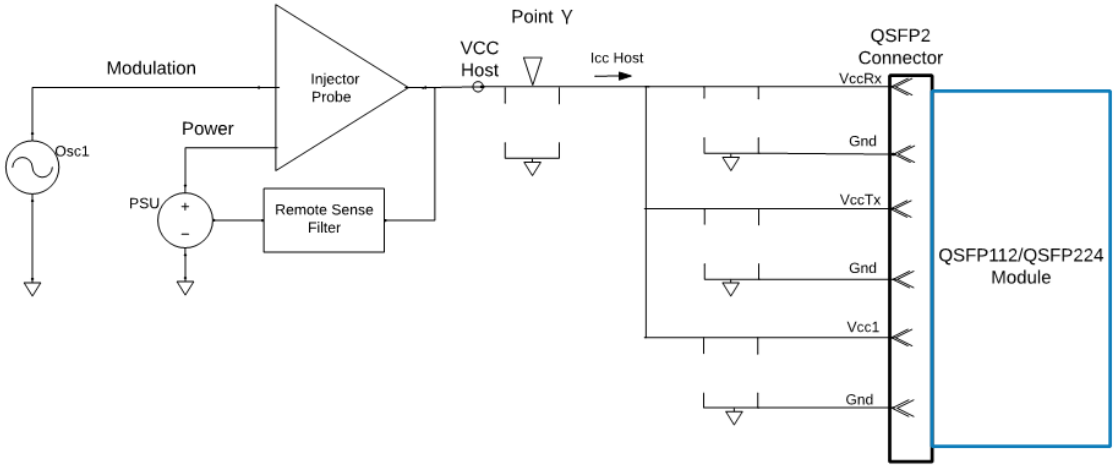


Figure 6-13 Broadband Noise Tolerance Injection Probe Setup

Injection Probe Setup

- Injection probe may have sense line for optional remote sense.
- The modulated RF signal can be any from any 50 Ω generator.
- Usage of a remote sense filter to adjust the power supply voltage level is recommended.
- Benchtop power supply with greater than 3.6 V output range with sufficient current capabilities and with sense line.

6.7 ESD

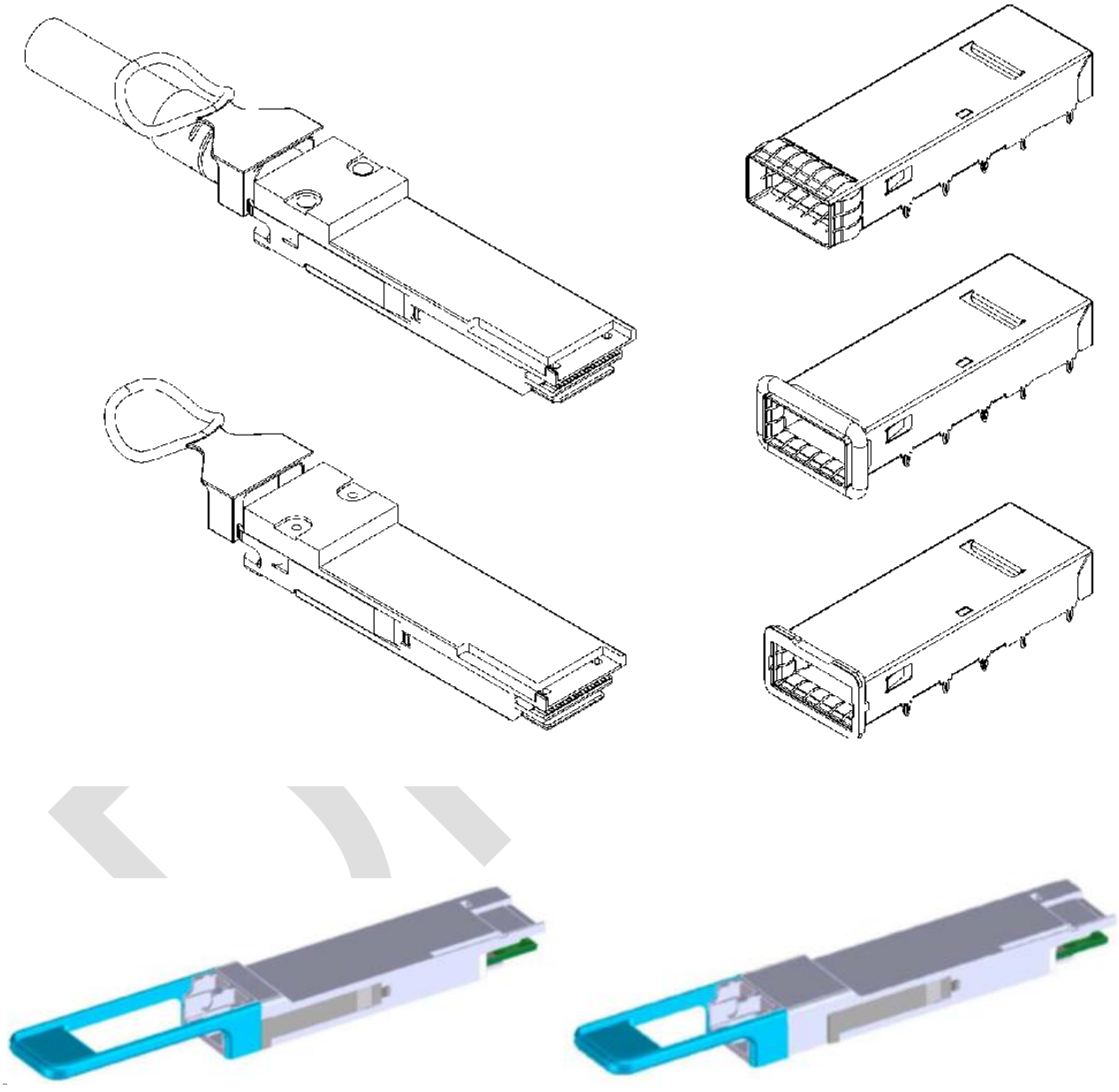
Where ESD performance is not otherwise specified, e.g. in the InfiniBand, Ethernet specifications, the module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case.

The module and host shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B for all pins.

7. Mechanical and Board Definition

7.1 Mechanical general

The overall module defined in this clause is illustrated in Figure 7-1. The optical interface is described in Section 7.3. Several cage-to-bezel options are possible. Both metal spring finger and elastomeric EMI solutions are permitted. Heat sink/clip thermal designs are not defined by this specification; however, general designs are described in SFF-8663, SFF-8683 and SFF-1027.



Type 1 Pluggable module **Type 2 Pluggable module**

Figure 7-1 Pluggable Module and Cable Plug Rendering

7.2 Color Coding and Labeling of Modules

An exposed feature of the module (a feature or surface visible when the module is fully inserted in the host) shall be color coded. Unless industry specifications apply, the following colors should be used.

- Beige for 850 nm
- Blue for 1310 nm
- White for 1550 nm

Each module shall be clearly labeled. The complete labeling need not be visible when the module is installed. The bottom of the module is the recommended location for the label, unless otherwise specified in the mechanical specification. Labeling shall include:

- Appropriate manufacturing and part number identification
- Appropriate regulatory compliance labeling
- A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

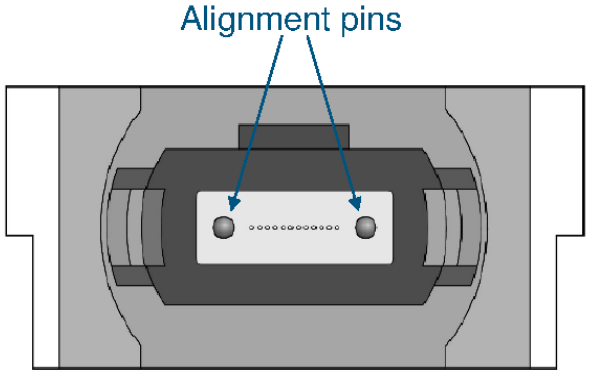
- Interface standard(s) supported
- and/or
- Optical wavelength
- Required fiber characteristics
- Operating data rate
- Link length supported

The labeling shall not interfere with the mechanical, thermal or EMI features.

7.3 Optical Interface

Unless specified in the relevant standard, the recommended connectors are: a male MPO connector as specified in IEC 61754-7 (see Figure 7-4) or a dual LC as specified in IEC 61754-20 (see Figure 7-5). The assignment of transmit and receive directions is shown in Figure 7-22 and Figure 7-3.

The four fiber positions on the left as shown in Figure 7-22, with the key up, are used for the optical transmit signals (Lane 1 to 4). The fiber positions on the right are used for the optical receive signals (Lane 4 to 1). The central four fibers may be physically present. Two alignment pins are present.



Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1

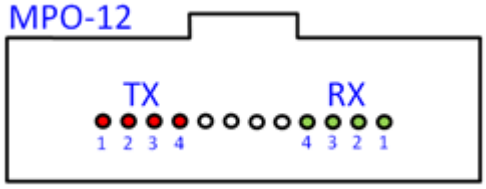
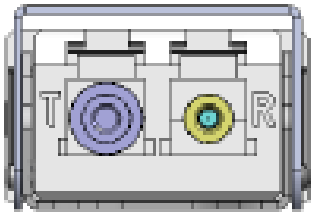


Figure 7-2 Optical Receptacle and Lane Orientation for MPO connector



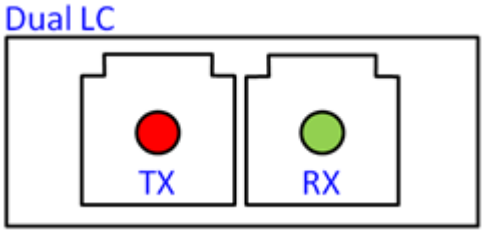


Figure 7-3 Optical Receptacle for Dual LC Connector

7.3.1 MPO Optical Cable Connection

Aligned key (Type B) MPO patch cords should be used to ensure alignment of the signals between the modules. The aligned key patch cord is defined in IEC 61754-7 and shown in Figure 7-4. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.

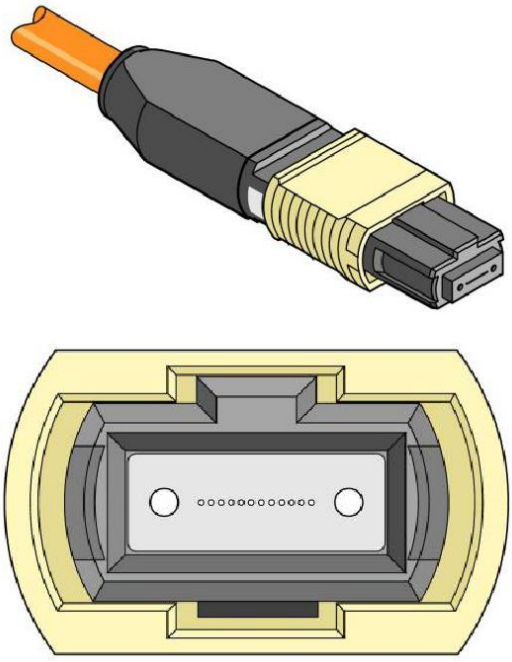


Figure 7-4 MPO Optical Patch Cord

7.3.2 Dual LC Optical Cable Connection

The Dual LC optical connector plug is defined in IEC 61754-20 and also in TIA-604-10 and is shown in Figure 7-5.

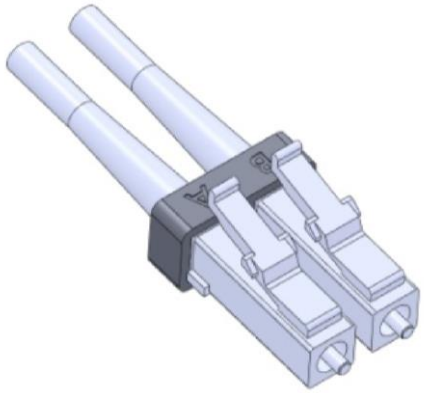


Figure 7-5 Dual LC Optical Connector Plug

8. Environmental and Temperature

8.1 Temperature Requirements

The module shall operate within one or more of the case temperatures ranges defined in Table 8-1 or the relevant specification if different. The temperature ranges are applicable between 60 m below sea level and 1800 m above sea level, (Ref. Telcordia GR-63-CORE) utilizing the host's designed airflow.

Table 8-1 Temperature Range Class of Operation

Class	Case Temperature Range
Standard	0 to 70 ºC
Extended	-5 to 85 ºC
Industrial	-40 to 85 ºC
Custom	Reported by two-wire interface (see SFF-8636 or CMIS)

9. Timing Requirements

A block diagram illustrating the control and status signals between a host system and a QSFP+ module is shown in Figure 9-1. Timing requirements for the signals SCL and SDA are provided in the SFF-8636 specification. Timing requirements for: ResetL, LPMode/TxDis, ModSelL, IntL/RxLOSL signals are provided in this section. In addition, the timing of control and status functions implemented via the two-wire interface are provided.

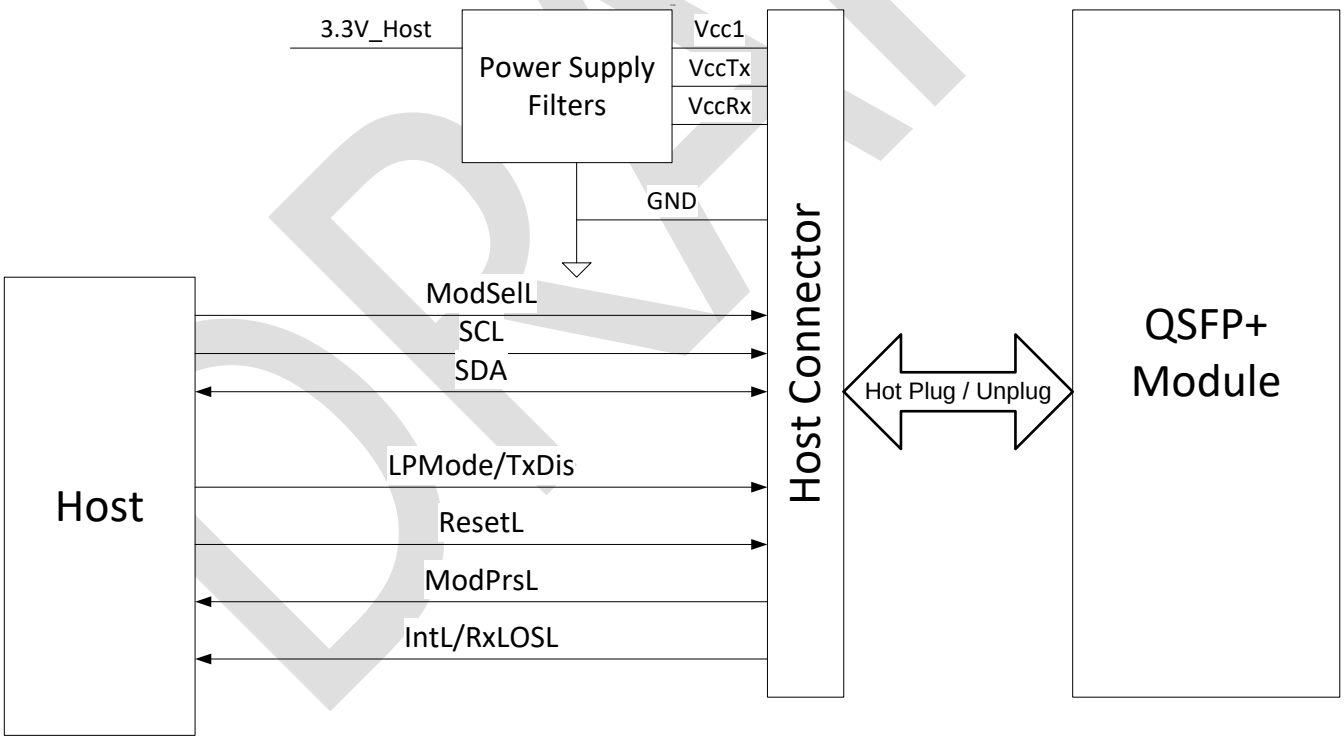


Figure 9-1 Block diagram of module control signals

9.1 Control and Status Timing Requirements

Table 9-1 Control and Status Timing Requirements

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
Initialization time	t_init		2	s	Time from power on or hot plug until the module is fully functional. This time applies to Power Class 2 or higher modules when LPMode is pulled low by the host, and to all Power Class 1 modules.	2,3,6
MgmtInit Duration	tMgmtInit		2	s	Time from power on[1], hot plug or rising edge of reset until completion of the MgmtInit State as defined in CMIS.	8
Two-wire Interface Ready Time	t_serial		2	s	Time from power on until the module responds to data transmission on the two-wire interface.	2
Monitor Data Ready Time	t_data		2	s	Time from power on to Data_Not_Ready, Byte 2 bit 0, cleared to 0 and IntL output pulled low.	2
Reset Init Assert Time	t_reset_init	10	-	µs	Host is required to provide a reset pulse of at least the minimum value for the module to guarantee a reset sequence. Shorter pulses may reset the module depending on implementation.	
Reset Assert Time	t_reset		2	s	Time from a rising edge on the ResetL input until the module is fully functional.	3
LPMode/TxDis mode change time	t_LPMode/TxDis		100	ms	Time to change between LPMode and TxDis modes of the dual-mode signal LPMode/TxDis	
LPMode Assert Time	ton_LPMode		100	ms	Time from when the host releases LPMode to high until module power consumption reaches Power Class 1.	
LPMode Deassert Time	toff_LPMode		300	ms	Time from when the host pulls LPMode low until the module is fully functional.	3,5,6
IntL/RxLOSL mode change time	t_IntL/RxLOSL		100	ms	Time to change between IntL and RxLOSL modes of the dual-mode signal IntL/RxLOSL.	
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering an interrupt until IntL is low.	
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read operation of associated flag until module releases IntL to high. This includes the time to clear Rx LOS, Tx Fault and other flag bits.	4

RxLOSL Assert Time (Optional Fast Mode)	ton_f_LOS		1	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from optical loss of signal to RxLOSL signal pulled low by the module.	
RxLOSL Deassert Time (Optional Fast Mode)	toff_f_LOS		3	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high.	
Rx LOS Assert Time	ton_LOS		100	ms	Time from Rx optical signal loss to Rx LOS bit set to 1 and IntL pulled low by the module.	
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set to 1 and IntL pulled low by the module.	
Flag Assert Time	ton_flag		200	ms	Time from condition triggering flag to associated flag bit set to 1 and IntL pulled low by the module.	
Mask Assert Time	ton_mask		100	ms	Time from mask bit set to 1 until the module is prevented from pulling IntL low when the associated flag is set high.	1
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared to 0 until module is enabled to pull IntL low when the associated flag is set high.	1
Application or Rate Select Change Time	t_ratesel		100	ms	Time from change of Application Select Byte or Rate Select bit until module is in conformance with the appropriate specifications for the new application or rate.	1,7,9,6
Power_override or Power_set Assert Time	ton_Pdown		100	ms	Time from Power override or Power set bit set to 1 until module power consumption reaches Power Class 1.	1,9
Power_override or Power_set Deassert Time	toff_Pdown		300	ms	Time from Power override or Power set bit cleared to 0 until the module is fully functional.	1,9,6
DataPathDeinit_MaxDuration					See CMIS memory P01h.144	1,8
DataPathInit_MaxDuration					See CMIS memory P01h.144	1,8
ModulePwrUp_MaxDuration					See CMIS memory P01h.167	4,8
ModulePwrDn_MaxDuration					See CMIS memory P01h.167	4,8
DataPathTxTurnOn_MaxDuration					See CMIS memory P01h.168	1,6,8
DataPathTxTurnOff_MaxDuration					See CMIS memory P01h.168	1,8

Note 1: Measured from rising edge of SDA during STOP sequence of write transaction.

Note 2: Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 5-6.

Note 3: Fully functional is defined as the module being ready to transmit and receive valid signals and all management interface data, including monitors, being valid. It is indicated after Reset or hot plug by the module releasing IntL to high after

the host has read a 0 from the Data_Not_Ready flag bit.

Note 4: Measured from rising edge of SDA during STOP sequence of read transaction.

Note 5: Does not apply to Power Class 1 modules.

Note 6: For some modules this limit is overridden via the management interface, SFF-8636, CMIS or by custom product specifications.

Note 7: For Fibre Channel speed negotiation, the 100 ms limit is too slow. See the relevant standard for details of the timing requirements.

Note 8: As defined in CMIS

Note 9: As defined in SFF-8636

9.2 Squelch and Tx/Rx Disable Assert, Deassert and Enable/Disable Timing

Table 8-2 lists the required timing performance for assert, deassert, enable and disable of the Tx Squelch, Rx Squelch, Tx Disable and Rx Output Disable functions.

Table 9-2 QSFP+ Squelch and Tx/Rx Disable timing

Parameter	Symbol	Max	Unit	Conditions	Note
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached. See 6.5.1.	
Rx Squelch Deassert Time	toff_Rxsq	15	ms	Time from resumption of Rx input signals until normal Rx output condition is reached. See 6.5.1.	3
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See 6.5.2.	
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached. See 6.5.2.	3
Tx Disable Assert Time	ton_TxDis	100	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.	1,2
Tx Disable Deassert Time	toff_TxDis	400	ms	Time from Tx Disable bit cleared to 0 until optical output rises above 90% of nominal.	1,2
Tx Disable Assert Time (Optional Fast Mode)	ton_f_TxDis	3	ms	Optional fast mode is advertised via the management interface (SFF-8636/CMIS). Time from TxDis signal high to the optical output reaching the disabled level.	1,2
Tx Disable Deassert Time (Optional Fast Mode)	Toff_f_TxDis	10	ms	Optional fast mode is advertised via the management interface (SFF-8636/CMIS). Time from TxDis signal low to the optical output reaching the enabled level.	1,2
Rx Output Disable Assert Time	ton_RxDis	100	ms	Time from Rx Output Disable bit set to 1 until Rx output falls below 10% of nominal.	1
Rx Output Disable Deassert Time	toff_RxDis	100	ms	Time from Rx Output Disable bit cleared to 0 until Rx output rises above 90% of nominal.	1
Squelch Disable Assert Time	ton_sqDIS	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared to 0 until squelch functionality is disabled.	1
Squelch Disable Deassert Time	toff_RxDis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set to 1 until squelch functionality is enabled.	1

Note 1: Measured from rising edge of SDA during STOP sequence of write transaction.
Note 2: In CMIS 4.0 and beyond the listed values are superseded by the advertised MaxDurationDPTxTurnOff and MaxDurationDPTxTurnOn times in P01h.168. The above listed values place a limit on the MaxDurationDPTxTurnOff and MaxDurationDPTxTurnOn times (P01h.168) that can be advertised by such modules.
Note 3: These limits can be superseded by appropriate standards.

Appendix A. Two-wire Interface Timing

A.1 Timing Diagram

The diagram in Figure A-1 illustrates the timing parameters for the two-wire interface clock (SCL) and data (SDA) signals.

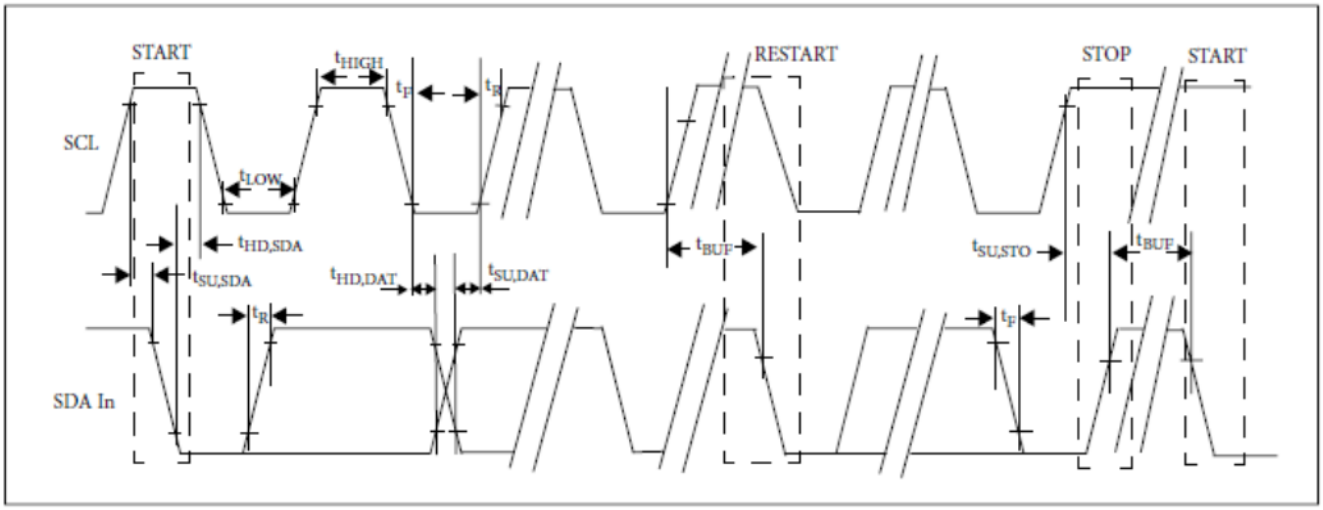


Figure A-1 Two-wire Interface Timing Diagram

A.2 Timing Parameters

The minimum and maximum limits for the timing parameters are provided in Table A-33.

Table A-3 Management interface timing parameters

		Fast Mode (SCL 400 kHz)		Fast Mode+ (SCL 1 MHz)			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3		0.50		us	
Clock Pulse Width High	tHIGH	0.6		0.26		us	
Time bus free before new transmission can start	tBUF	20		20		us	Between STOP and START and between ACK and Restart
START Hold Time	tHD.STA	0.6		0.26		us	
START Set-up Time	tSU.STA	0.6		0.26		us	
Data in Hold Time	tHD.DAT	0		0		us	
Data in Set-up Time	tSU.DAT	0.1		0.1		us	
Input Rise Time	tR		300		120	ns	From (VIL, MAX-0.15) to (VIH, MIN +0.15)
Input Fall Time	tF		300		120	ns	From (VIH, MIN + 0.15) to (VIL, MAX - 0.15)
STOP Set-up Time	tSU.STO	0.6		0.26		us	
STOP Hold-up Time	tHD_STO	0.6		0.26		us	
Clock Holdoff Time (Clock Stretching)	T_clock_hold		500		500	us	Maximum time the module may hold SCL low before completing a read or write operation
Aborted sequence – bus release	Deselect_Abort		2		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the module releasing SCL and SDA
ModSelL Setup Time[1]	tSU.ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host-initiated TWI serial bus sequence.
ModSelL Hold Time[1]	tHD.ModSelL	0.01[2] 0.5[3]		2		ms	ModSelL Hold Time is the delay from completion of TWI serial bus sequence to ModSelL rising edge.
Complete single or sequential write to non-volatile registers	tWR		40[2] 80[3]		80	ms	Time to complete a single or sequential write of up to four bytes to non-volatile registers.
Accept a single or sequential write to volatile memory	tNACK		10[3]		10[3]	ms	Time to complete a single or sequential write to volatile registers.
Time to complete a change of memory page or bank	tBPC		10[3]		10[3]	ms	Time to complete a change of memory page or bank.
Endurance (Write Cycles)		50k		50k		cycles	Module Case Temperature = 70 ºC

Note 1: Support for the setup and hold times are required for all modules. In CMIS transceivers, once the module has initialized the management interface, management registers can be read to determine alternate ModSelL set up and hold times. See CMIS 8.4.5, Durations Advertisement or SFF-8636 6.2.9, Free Side Device Properties (Page 00h, Bytes 107-117).
Note 2: For transceivers implementing SFF-8636
Note 3: For transceivers implementing CMIS

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