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2  
3 SFF-8679

4 Specification for

5 **QSFP+ 4X Hardware and Electrical Specification**

6 Draft 1.7.4 August 6, 2018

7 Secretariat: SFF TA TWG

8 Abstract: This specification defines the contact pads, the electrical, power  
9 supply, ESD and thermal characteristics of the pluggable QSFP+ module or cable  
10 plug.

11 There are multiple generations of QSFP+ that reference this specification:

12 SFF-8635 QSFP+ 4X 10 Gb/s Pluggable Transceiver Solution (QSFP10)

13 SFF-8685 QSFP+ 4X 14 Gb/s Pluggable Transceiver Solution (QSFP14)

14 SFF-8665 QSFP+ 4X 28 Gb/s Pluggable Transceiver Solution (QSFP+)

15 This specification supersedes the base electrical content of SFF-8436 QSFP+ 10Gb/s  
16 4X Pluggable Transceiver.

17 This document provides a common specification for systems manufacturers, system  
18 integrators, and suppliers.

19 This draft specification is made available for public review, and written comments  
20 are solicited from readers. Comments received at <http://www.snia.org/feedback> will  
21 be considered for inclusion in future revisions of this specification.

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25 Public feedback: <http://www.snia.org/feedback>

## 1 Change History

### 2 Rev 1.5:

- 3 - Moved referenced SFF specs to 2.1 Industry Documents and expanded the list.

### 4 Rev 1.6:

- 5 - Updated Figure 1 to show retimers.
- 6 - Removed two-wire interface timing diagram which is now in SFF-8636.
- 7 - Complete rewrite of power supply section to add support for Power Classes 5
- 8 to 7.
- 9 - Added section 8 "Timing Requirements".

### 10 Rev 1.7

- 11 - Editorial only, no technical changes.

### 12 Rev 1.7.1-4 (working drafts)

- 13 - Converted to SNIA SFF template.
- 14 - Editorial updates throughout
- 15 - Title changed to "Hardware and Electrical" to better reflect contents
- 16 - Updated abstract
- 17 - Updated editor contact information.
- 18 - Section 1 Scope - rewrote to better reflect content.
- 19 - Section 2 References - replaced several entries with updated document
- 20 numbers and names.
- 21 - Section 2.3 Acronyms - deleted several unused entries and added several
- 22 new ones based on content.
- 23 - Section 3 General Description - Rewrote most of this section to reflect
- 24 updated content. Added several relevant applications to Table 3-1.
- 25 - Section 4 Compliance Testing - updated Figure 4-1 and corrected test point
- 26 descriptions in Table 4-1.
- 27 - Section 5 Electrical Specification -
  - 28 ○ Updated Figure 5-1 and Table 5-1 to show the new dual-purpose
  - 29 signals LPMode/TxDis and IntL/RxLOSL on pads 31 and 28
  - 30 respectively. Rewrote Note 2 of Table 5-1 for clarity.
  - 31 ○ Replaced "pin" by "pad" throughout
  - 32 ○ Replaced Figures 5-2 and 5-3 to better reflect current
  - 33 applications.
  - 34 ○ Extensive updates of Section 5.3 describing Low Speed Signals.
  - 35 ○ Updates to Table 5-2 to explain SCL and SDA electrical
  - 36 requirements and maximum pull-up resistor values for 400 kHz
  - 37 operation.
  - 38 ○ Significant revisions to text in 5.4 Low Speed Signal Electrical
  - 39 Specifications and 5.5 High Speed Signal Electrical
  - 40 Specifications.
  - 41 ○ Re-ordered and rewrote section 5.6 Power Supply Requirements
  - 42 including adding a new Power Class 8 with a maximum power limited
  - 43 only by the connector current rating.
- 44 - Section 6 Mechanical and Board Definition - cleaned up this section to
- 45 reference the relevant documents instead of including non
- 46 hardware/electrical features.
- 47 - Section 7 Environmental and Temperature - added a "custom" temperature
- 48 class for modules that do not comply with any of the legacy case
- 49 temperature ranges, e.g., hyperscale data center applications.
- 50 - Section 8 Timing Requirements
  - 51 ○ Major updates to Table 8-1 including re-writes of many entries in
  - 52 the "Conditions" column.
  - 53 ○ Changed limit for "Reset Init Assert Time" from a maximum of 2 us

- 1 to a minimum of 10 us.
- 2 ○ Table 8-1: added new entries for “LPMode/TxDis mode change time”,
- 3 “IntL/RxLOSL mode change time”, “RxLOSL Assert Time (Optional
- 4 Fast Mode)”, and “RxLOSL Deassert Time (Optional Fast Mode)”.
- 5 ○ Table 8-1: changed limit for “LPMode Assert Time” from 100 us to
- 6 100 ms.
- 7 ○ Table 8-1: rewrote notes 1-5 and added new notes 6-7.
- 8 ○ Table 8-2: changed maximum limits for “Rx Squelch Assert Time”
- 9 and “Rx Squelch Deassert Time” from 80 us to 15 ms.
- 10 ○ Table 8-2: added new parameters for “Tx Disable Assert Time
- 11 (Optional Fast Mode)” and “Tx Disable Deassert Time (Optional
- 12 Fast Mode)”.
- 13 ○ Table 8-2: corrected text in descriptions of Tx Squelch assert &
- 14 deassert.
- 15 ○ Added section 8.3 and Table 8-3 with timing for ModSelL setup and
- 16 hold times, plus time for aborted sequence – bus release.
- 17 - Appendix A two-wire interface timing – Added a copy of the two-wire
- 18 interface timing diagram (Figure A-1), timing parameters (Table A-1)
- 19 and non-volatile memory timing specifications (Table A-2).
- 20

## 1 Foreword

2 The development work on this specification was done by the SNIA SFF TWG, an  
3 industry group. Since its formation as the SFF Committee in August 1990, the  
4 membership has included a mix of companies which are leaders across the industry.

5 When 2 1/2" diameter disk drives were introduced, there was no commonality on  
6 external dimensions e.g. physical size, mounting locations, connector type,  
7 connector location, between vendors. The SFF Committee provided a forum for system  
8 integrators and vendors to define the form factor of disk drives.

9 During their definition, other activities were suggested because participants in  
10 SFF faced more challenges than the form factors. In November 1992, the charter was  
11 expanded to address any issues of general interest and concern to the storage  
12 industry. The SFF Committee became a forum for resolving industry issues that are  
13 either not addressed by the standards process or need an immediate solution.

14 In July 2016, the SFF Committee transitioned to SNIA (Storage Networking Industry  
15 Association), as a TA (Technology Affiliate) TWG (Technical Work Group).

16 Industry consensus is not a requirement to publish a specification because it is  
17 recognized that in an emerging product area, there is room for more than one  
18 approach. By making the documentation on competing proposals available, an  
19 integrator can examine the alternatives available and select the product that is  
20 felt to be most suitable.

21 SFF meets during the T10 (see <http://www.incits.org/committees/t10>) and T11 (see  
22 <http://www.incits.org/committees/t11>) weeks, and SSWGs (Specific Subject Working  
23 Groups) are held at the convenience of the participants.

24 Many of the specifications developed by SFF have either been incorporated into  
25 standards or adopted as standards by ANSI, EIA, JEDEC and SAE.

26 For those who wish to participate in the activities of the SFF TWG, the sign up for  
27 membership can be found at: <http://www.snia.org/sff/join>

28 The complete list of SFF Specifications which have been completed or are currently  
29 being worked on by the SFF Committee can be found at:  
30 <http://www.snia.org/sff/specifications>

31 Suggestions for improvement of this specification will be welcome, they should be  
32 submitted to: <http://www.snia.org/feedback>

33

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## 1 1 Scope

2 This document specifies the electrical requirements for the QSFP10/14/28 pluggable  
3 4-lane interfaces, hereafter referred to as QSFP+. The scope includes: electrical  
4 contacts for the host connector; status, control and management interface signals;  
5 power supply requirements; fiber positions for optical interfaces; ESD and thermal  
6 characteristics and color coding of pluggable QSFP+ modules and cables.

7 This specification supersedes and extends INF-8438 QSFP (Quad SFP) 4 Gb/s 4X  
8 Transceiver and SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver by supporting  
9 higher transfer rates.

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28 description of the purpose, nature, and scope of the requested use. Permission for  
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30 granted if the Exception request is not acknowledged within ten (10) business days  
31 of SNIA's receipt. Any denial of permission for the Exception shall include an  
32 explanation of such refusal.

### 33 1.2 Disclaimer

34 The information contained in this publication is subject to change without notice.  
35 The SNIA makes no warranty of any kind with regard to this specification,  
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37 fitness for a particular purpose. The SNIA shall not be liable for errors contained  
38 herein or for incidental or consequential damages in connection with the  
39 furnishing, performance, or use of this specification.

40

## 1 2 References

### 2 2.1 Industry Documents

3 The following interface standards and specifications are relevant to this  
4 Specification.

- 5 - GR-253-CORE
- 6 - ESD specifications EN61000-4-2, JEDEC JESD22-A114-B
- 7 - IEC 61754-7-1:2014 Fibre optic interconnecting devices and passive
- 8 components- Fibre optic connector interfaces - Part 7-1: Type MPO connector
- 9 family - One fibre row
- 10 - IEC 61754-20:2012 Fibre optic interconnecting devices and passive components-
- 11 Fibre optic connector interfaces - Part 20: Type LC connector family
- 12 - ANSI/TIA-568.3-D Optical Fiber Cabling And Components Standards
- 13 - TIA-604-5 FOCIS 5 Fiber Optic Connector Intermateability Standard - Type MPO
- 14 - TIA-604-10 FOCIS 10B Fiber Optic Connector Intermateability Standard - Type
- 15 LC
- 16 - Telcordia GR-63-CORE, Issue 4, April 2012, NEBS™ Requirements: Physical
- 17 Protection
- 18 - IEEE Std 802.3-2015
- 19 - IEEE Std 802.3bs-2017
- 20 - IEEE Std 802.3cc-2017
- 21 - IEEE P802.3cd
- 22 - InfiniBand Architecture Specification
- 23 - INCITS 479-2011 Fibre Channel- Physical Interface -5 (FC-PI-5)
- 24 - INCITS 512-2015 Fibre Channel- Physical Interface -6 (FC-PI-6)
- 25 - INCITS 533-2016 Fibre Channel- Physical Interface -6P (FC-PI-6P)
- 26 - INCITS 543: Information technology - Fibre Channel - Physical Interfaces - 7
- 27 (FC-PI-7)
- 28 - INCITS 559: Information technology - Fibre Channel - Physical Interfaces - 7P
- 29 (FC-PI-7P)
- 30 - ISO/IEC 14776-154:2017 Information technology - Small computer system
- 31 interface (SCSI) - Part 154: Serial Attached SCSI-3 (SAS-3)
- 32 - INCITS 534: Information technology - Serial Attached SCSI-4 (SAS-4)
- 33

#### 34 2.1.1 Relevant SFF Specifications

35 SFF specifications are available from <http://www.snia.org/sff/specifications>

- 36 - SFF-8024 SFF Committee Cross Reference to Industry Products
- 37 - SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver - (EIA-964)
- 38 - INF-8438 QSFP (Quad Small Formfactor Pluggable) Transceiver
- 39 - SFF-8635 QSFP+ 10 Gb/s 4X Pluggable Transceiver Solution (QSFP10)
- 40 - SFF-8636 Management Interface for Cabled Environments
- 41 - SFF-8661 QSFP+ 28 Gb/s 4X Pluggable Module
- 42 - SFF-8662 QSFP+ 28 Gb/s 4X Connector (Style A)
- 43 - SFF-8663 QSFP+ 28 Gb/s Cage (Style A)
- 44 - SFF-8665 QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28)
- 45 - SFF-8672 QSFP+ 28 Gb/s 4X Connector (Style B)
- 46 - SFF-8679 QSFP+ 4X Hardware and Electrical Specification
- 47 - SFF-8682 QSFP+ 14 Gb/s 4X Connector (Style B)
- 48 - SFF-8683 QSFP+ Cage
- 49 - SFF-8685 QSFP+ 14 Gb/s 4X Pluggable Transceiver Solution (QSFP14)

50

51



## 1 2.2 Conventions

2 The ISO convention of numbering is used i.e., the thousands and higher multiples  
3 are separated by a space and a period is used as the decimal point. This is  
4 equivalent to the English/American convention of a comma and a period.

5

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

6

## 7 2.3 Acronyms and Abbreviations

8 The following acronyms may be used in this specification.

9	ANSI	American National Standards Institute
10	ASIC	Application Specific Integrated Circuit
11	ATM	Asynchronous Transfer Mode
12	CDR	Clock and Data Recovery
13	CML	Current Mode Logic
14	CORE	Central Office Relay Equipment
15	CTLE	Continuous Time Linear Equalizer
16	DC	Direct Current
17	DDR	Double Data Rate
18	EDR	Extended Data Rate
19	EIA	Electronic Industries Alliance
20	EMI	Electromagnetic Interference
21	ESD	Electrostatic Discharge
22	FC	Fibre Channel
23	FDR	Fourteen Gb/s Data Rate
24	Gb/s	Gigabits per second
25	GbE	Gigabit Ethernet
26	GFC	Gigabit Fibre Channel
27	HCB	Host Compliance Board
28	HDR	High Data Rate
29	IEC	International Electrotechnical Commission
30	IEEE	Institute for Electrical and Electronics Engineers
31	ISO	Organization for International Standards
32	ITU	International Telecommunications Union
33	JEDEC	Joint Electron Device Engineering Council
34	LVC MOS	Low Voltage Complementary Metal Oxide Semiconductor
35	LVTTTL	Low Voltage Transistor Transistor Logic
36	MCB	Module Compliance Board
37	MPO	Multi-fiber Push On
38	NEBS	Network Equipment Building System
39	OC	Optical Carrier
40	OMA	Optical Modulation Amplitude
41	PCB	Printed Circuit Board
42	PI	Physical Interface
43	QDR	Quad Data Rate
44	QSFP	Quad SFP
45	Rx	Receiver
46	SAS	Serial Attached SCSI
47	SDH	Synchronous Digital Hierarchy

1	SDR	Single Data Rate
2	SerDes	Serializer-Deserializer
3	SFP	Small Formfactor Pluggable
4	SM	Single Mode
5	SONET	Synchronous Optical Network
6	STM	Synchronous Transfer Mode
7	TIA	Telecommunications Industry Association
8	TTL	Transistor-Transistor Logic
9	Tx	Transmitter
10		

Working Draft

### 1 3 General Description

2 This specification covers the following items:

- 3 — Electrical specifications for QSFP+ modules including host connector contact
- 4 assignments.
- 5 — Descriptions for data, control, status and management interface signals.
- 6 — Power supply requirements.
- 7 — Electrostatic discharge (ESD) tolerance requirements.
- 8 — Color coding and labeling.
- 9 — Fiber positions for optical interfaces.
- 10 — Environmental and thermal requirements (case temperatures).
- 11 — Timing requirements.

12

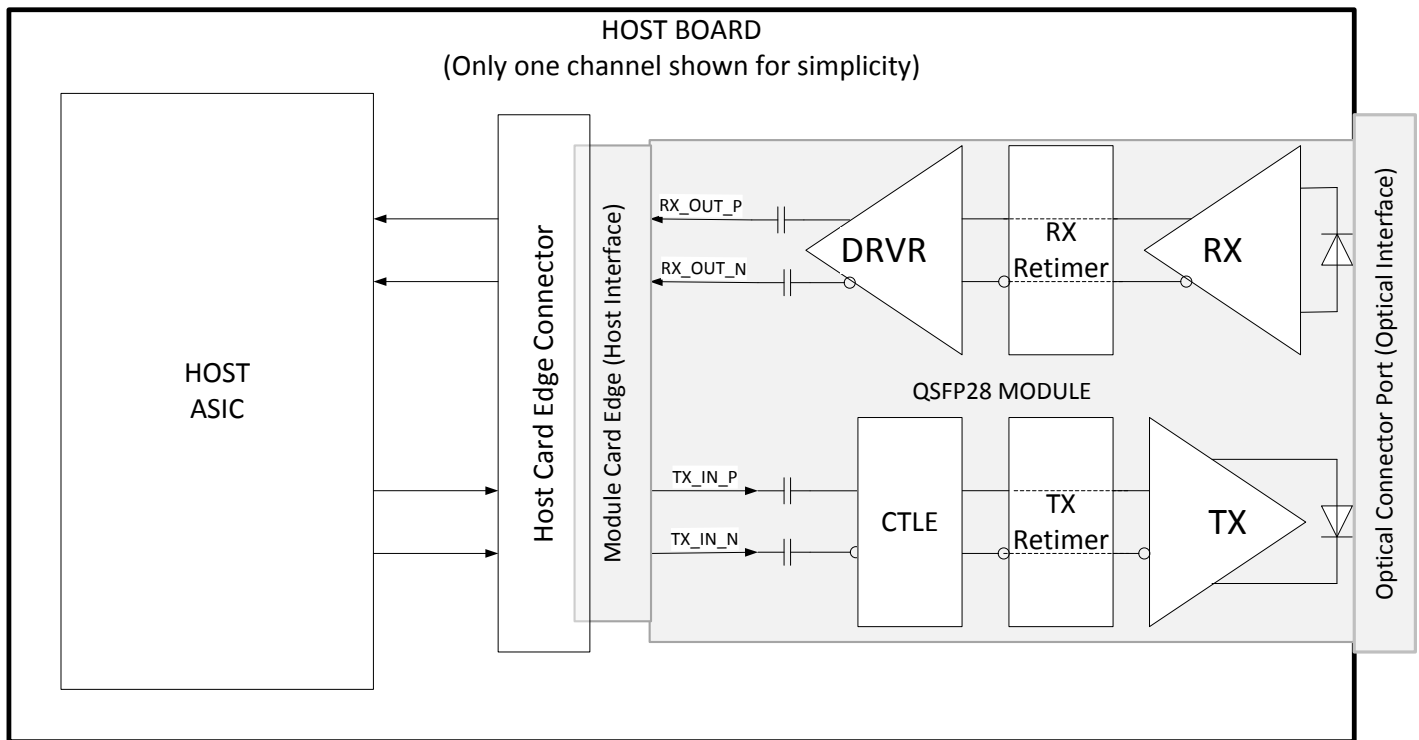
13 The electrical and optical specifications may be compatible with the examples in  
14 Table 3-1.

**TABLE 3-1 EXAMPLES OF APPLICATIONS**

ITU-T Recommendation G.957	STM-1, STM-4, STM-16
Telcordia Technologies GR-253-CORE	OC-3, OC-12, OC-48, OC-192
IEEE Std. 802.3	10 GbE, 25 GbE, 40 GbE, 50 GbE, 100 GbE, 200 GbE
Infiniband Architecture Specification	SDR, DDR, QDR, FDR, EDR, HDR
Fibre Channel	8GFC, 16GFC, 32GFC, 128GFC
Serial Attached SCSI	SAS-3, SAS-4

15

16 The Application Reference Model in Figure 3-1 shows the high-speed data interface  
17 between an ASIC (SerDes) and the module. Only one data channel of the interface is  
18 shown for simplicity. Either parallel MPO or duplex LC fiber connectors can be used  
19 for the optical interface.



1

FIGURE 3-1 APPLICATION REFERENCE MODEL

2 **4 Compliance Testing**

3 The module electrical interface test points are intended to be measured using  
 4 compliance boards as shown in Figure 4-1. These compliance boards are intended to  
 5 connect the module under test to test equipment for verification of compliance to  
 6 the appropriate standard. The Module Compliance Board is used to test the module.  
 7 The electrical parameters of the compliance boards should be specified by the  
 8 appropriate standard. The Module Compliance Board and Host Compliance Board can be  
 9 plugged together for calibration of compliance signals and to check the electrical  
 10 parameters of the compliance boards. Reference points are described in Table 4-1.

11

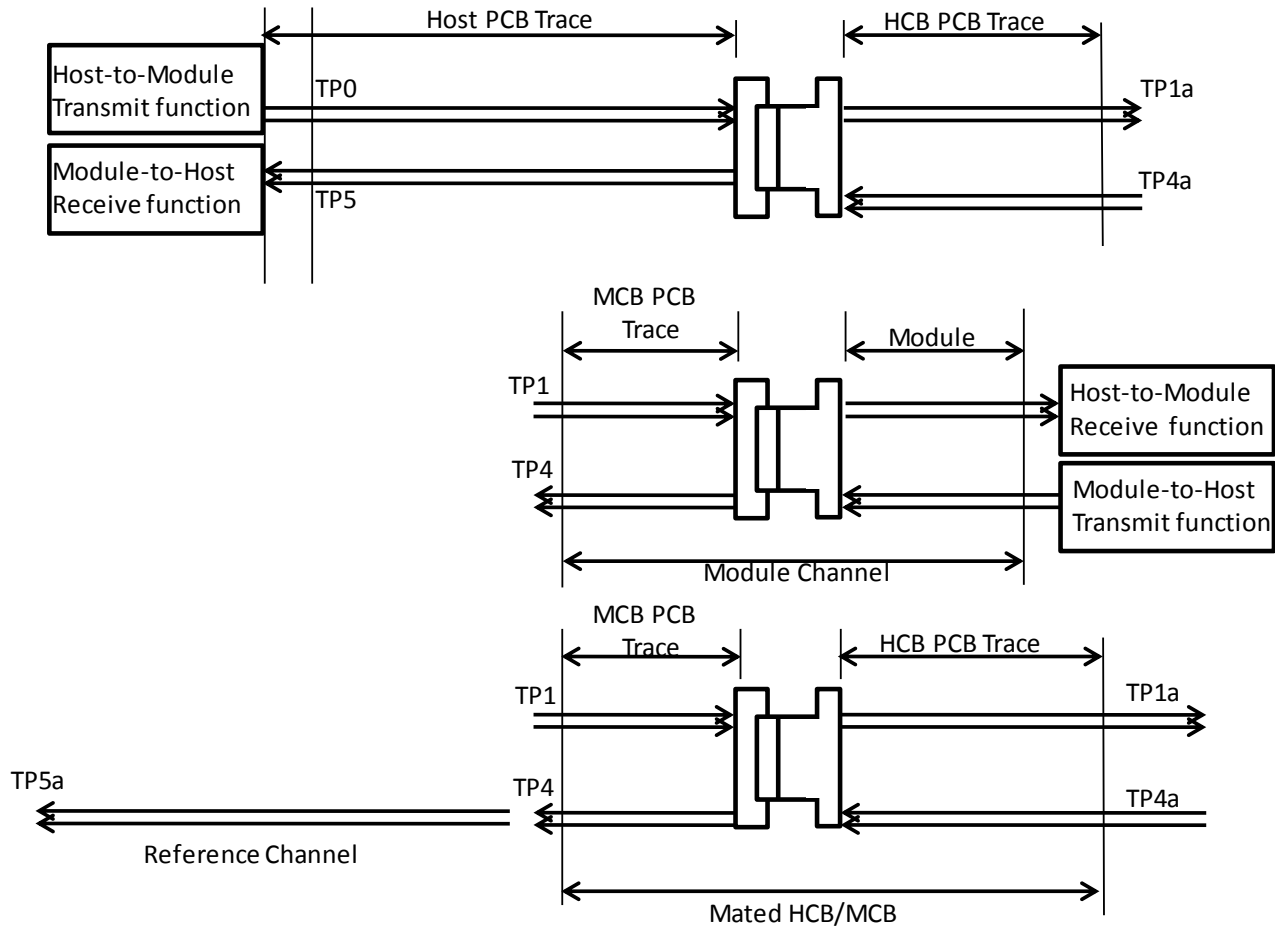


FIGURE 4-1 REFERENCE POINTS AND COMPLIANCE BOARDS

TABLE 4-1 REFERENCE POINTS

Reference point	Description
TP0	Host ASIC transmitter output at ASIC package contact.
TP1	Input to Module Compliance Board. Used to test module input.
TP1a	Host ASIC transmitter output through the host board and host card edge connector at the output of the Host Compliance Board. Also used to calibrate module input compliance signals.
TP4	Module output through the compliance board connectors at the output of the Module Compliance Board. Also used to calibrate host input compliance signals.
TP4a	Input to Host Compliance Board. Used to test host input.
TP5	Input to host ASIC
TP5a	Far end module output through a reference channel

Note: Individual standards may specify unique reference points

1  
2

3

1 **5 Electrical Specification**

2 This clause contains pad definition data for the module. The pad definition data is  
 3 generic for high speed datacom applications such as Fibre Channel, Ethernet and  
 4 SONET/ATM. Compliance Points for high-speed electrical measurements are defined in  
 5 Table 4-1 and illustrated in Figure 4-1. Compliance Points for all other electrical  
 6 signals are at comparable points at the host card edge connector.

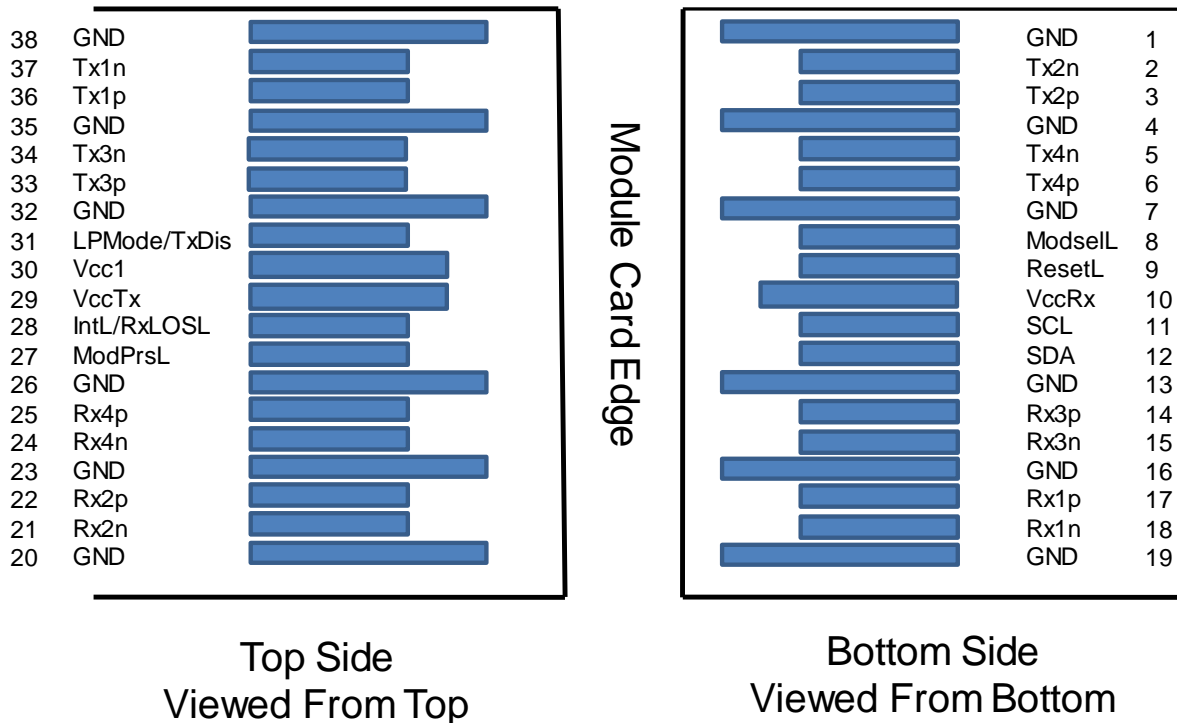
7 **5.1 Electrical Connector**

8 Figure 5-1 shows the signal symbols and pad numbering for the module edge  
 9 connector. The diagram shows the module PCB edge as a top and bottom view, where  
 10 bottom is nearer the host PCB. There are 38 pads intended for high speed signals,  
 11 low speed signals, power and ground connections. Table 5-1 provides more  
 12 information about each of the 38 pads.

13 The module contains a printed circuit board that mates with the electrical  
 14 connector. The pads are designed for a sequenced mating:

- 15 First mate - ground contacts
- 16 Second mate - power contacts
- 17 Third mate - signal contacts

18 For EMI protection the signals to the connector should be shut off when the module  
 19 is absent. Standard board layout practices such as connections to Vcc and GND with  
 20 vias, the use of short and equal-length differential signal lines, and the use of  
 21 microstrip-lines and 50 Ω terminations are recommended. The chassis ground (case  
 22 common) of the module should be isolated from the module's circuit ground, GND, to  
 23 provide the equipment designer flexibility regarding connections between external  
 24 electromagnetic interference shields and circuit ground, GND, of the module.



25 **FIGURE 5-1 MODULE PAD LAYOUT**

26

1

TABLE 5-1 PAD FUNCTION DEFINITION

Pad	Logic	Symbol	Description	Plug Sequence	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	two-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	two-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636).	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

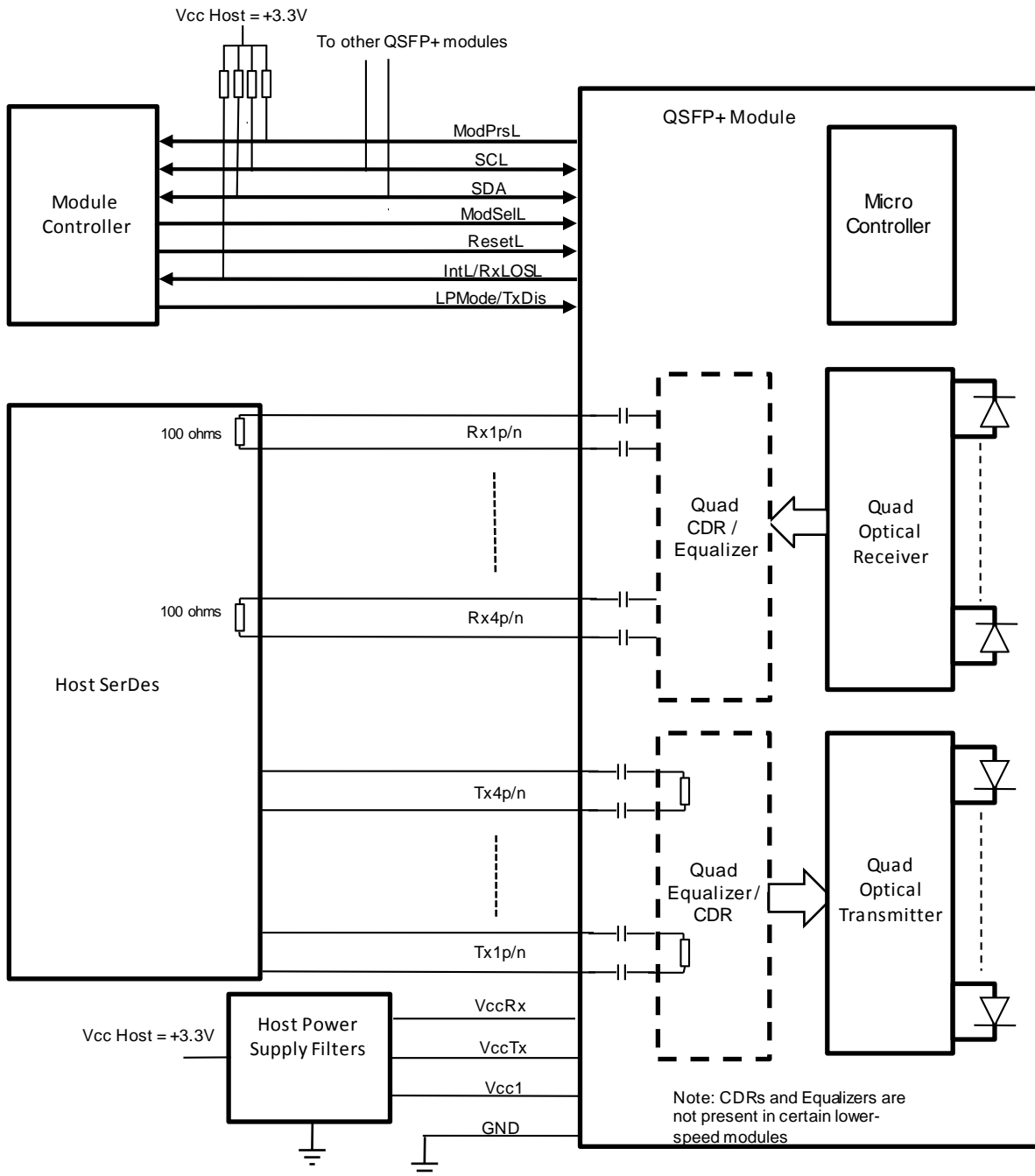
Note 2: VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1 A.

2

3

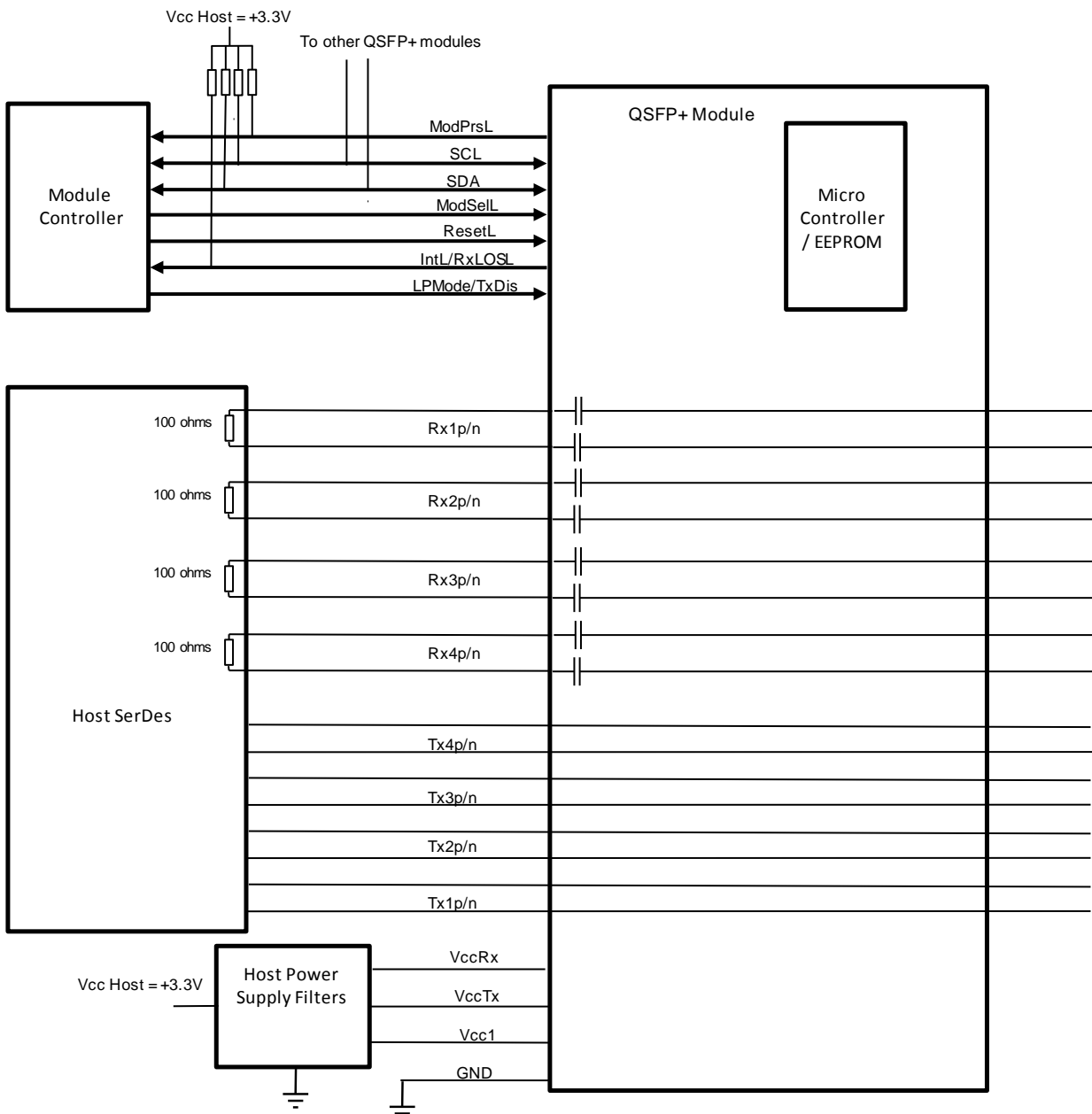
1 5.2 QSFP Example Circuits

2 Figure 5-2 and Figure 5-3 provide example host board schematics for an optical  
 3 QSFP+ module and for a QSFP+ copper cable plug respectively. Optical modules may  
 4 have CDRs and equalizers in the module depending on the application.



5  
 6  
 FIGURE 5-2 EXAMPLE: HOST BOARD SCHEMATIC FOR OPTICAL MODULES





1  
2 **FIGURE 5-3 EXAMPLE: HOST BOARD SCHEMATIC FOR PASSIVE COPPER CABLES**

## 1 5.3 Low Speed Signal Descriptions

2 In addition to the two-wire serial interface the module has the following low speed  
3 signals for control and status:

4 ModSelL  
5 ResetL  
6 LPMode/TxDis  
7 ModPrsL  
8 IntL/RxLOSL

9 The behavior of these signals is given in 5.3.1 to 5.3.5, the electrical  
10 specifications are in 5.4.1, and timing requirements are in 5.4.2 and 8. Timing  
11 requirements for the two-wire serial interface are in Appendix A.

### 12 5.3.1 ModSelL

13 ModSelL is an input signal. When held low by the host, the module responds to two-  
14 wire serial communication commands. The ModSelL signal allows the use of multiple  
15 modules on a single two-wire interface bus. When ModSelL is "high", the module  
16 shall not respond to or acknowledge any two-wire interface communication from the  
17 host. The ModSelL signal input node shall be pulled towards Vcc in the module.

18 In order to avoid conflicts, the host system shall not attempt two-wire interface  
19 communications within the ModSelL de-assert time after any modules are deselected.  
20 Similarly, the host shall wait at least for the period of the ModSelL assert time  
21 before communicating with the newly selected module. The assertion and de-assertion  
22 periods of different modules may overlap as long as the above timing requirements  
23 are met.

### 24 5.3.2 ResetL

25 The ResetL signal shall be pulled towards Vcc in the module. A low level on ResetL  
26 for longer than the minimum pulse length ( $t_{\text{Reset\_init}}$ ) initiates a complete module  
27 reset, returning all user module settings to their default state. Module Reset  
28 Assert Time ( $t_{\text{init}}$ ) starts on the rising edge after the low level of the ResetL  
29 pad is released. During the execution of a reset ( $t_{\text{init}}$ ) the host shall disregard  
30 all status bits until the module indicates a completion of reset interrupt by  
31 asserting "low" on the IntL/RxLOSL signal (see SFF-8636 for details). Note that on  
32 power up (including hot insertion) the module should post this completion of reset  
33 interrupt without the host pulling ResetL low.

### 34 5.3.3 LPMode/TxDis

35 LPMode/TxDis is a dual-mode input signal from the host operating with active high  
36 logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is  
37 deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be  
38 configured as TxDis using the two-wire management interface except during the  
39 execution of a reset. TxDis provides an optional fast mode, see definition in SFF-  
40 8636.

41 When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By  
42 using the LPMode signal and a combination of the Power\_override, Power\_set and  
43 High\_Power\_Class\_Enable software control bits (SFF-8636, Address A0h, Byte 93 bits  
44 0,1,2), the host controls how much power a module can consume. See section 5.6 for  
45 more details on the power supply specifications.

46 When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0.  
47 In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical

- 1 transmitters within the times specified in Table 8-2.
- 2 Changing LPMoDe/TxDiS mode from LPMoDe to TxDiS when the LPMoDe/TxDiS state is high  
3 disables all optical transmitters. If the module was in low power mode, then the  
4 module transitions out of low power mode at the same time. If the module is already  
5 in high power state (Power Override control bits) with transmitters already  
6 enabled, the module shall disable all optical transmitters.
- 7 Changing the LPMoDe/TxDiS mode from LPMoDe to TxDiS when the LPMoDe/TxDiS state is  
8 low, simply changes the behavior of the mode of LPMoDe/TxDiS. The behavior of the  
9 module depends on the Power Override control bits.

10 Timing requirements for LPMoDe/TxDiS mode changes are found in Table 8-1.

11 Note that the “soft” functions of TxDiS, LPMoDe, IntL and RxLOSL allow the host to  
12 poll or set these values over the two-wire interface as an alternative to  
13 monitoring/setting signal values. Asserting either the “hard pin” or “soft bit”  
14 (or both) for TxDiS or LPMoDe results in that function being asserted.

#### 15 5.3.4 ModPrsL

16 ModPrsL is pulled up towards Vcc\_Host on the host board and pulled towards ground  
17 in the module. ModPrsL is asserted "low" when inserted and deasserted "high" when  
18 the module is physically absent from the host connector.

#### 19 5.3.5 IntL/RxLOSL

20 IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the  
21 module. It shall be pulled up towards Vcc on the host board. At power-up or after  
22 ResetL is deasserted, IntL/RxLOSL is configured as IntL. If supported, IntL/RxLOSL  
23 can be optionally programmed as RxLOSL using the two-wire management interface  
24 except during the execution of a reset. See definition in SFF-8636. Rx LOS and  
25 RxLOSL timings, including an optional fast mode, are given in 8.1.

26 If IntL/RxLOSL is configured as IntL, a low indicates a possible module  
27 operational fault or a module condition that sets an unmasked flag as defined  
28 in SFF-8636. The source of the IntL “low” can be read, cleared or masked using  
29 the two-wire serial interface. If the interrupt was after a module reset and  
30 SFF-8636, Page 00h, Byte 2, bit 0 (Data\_Not\_Ready bit) is 0, then the module  
31 releases IntL to high after the host has read the Data\_Not\_Ready bit. For all  
32 other interrupt causes, the module releases IntL to high after the host has  
33 read the flag associated with the cause of the interrupt.

34 If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss  
35 of received optical power on at least one lane. “high” indicates that there is  
36 no loss of received optical power. Rx LOS and RxLOSL timings, including an  
37 optional fast mode, are given in Table 8-2. The actual condition of loss of  
38 optical receive power is specified by other governing documents, as the alarm  
39 threshold level is application specific. The module shall pull RxLOSL to low  
40 if any lane in a multiple lane module or cable has a LOS condition and shall  
41 release RxLOSL to high only if no lane has a LOS condition.

42 Timing requirements for IntL/RxLOSL mode change are found in Table 8-1. If the  
43 module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no  
44 change in IntL/RxLOSL states after the mode change.

## 1 5.4 Low Speed Signal Electrical Specifications

### 2 5.4.1 Low Speed Signaling

3 Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTTL)  
 4 operating at  $V_{cc}$ .  $V_{cc}$  refers to the generic supply voltages of  $V_{ccTx}$ ,  $V_{ccRx}$ ,  
 5  $V_{cc\_host}$  or  $V_{cc1}$ . Hosts shall use a pull-up resistor connected to  $V_{cc\_host}$  on each  
 6 of the two-wire interface SCL (clock), SDA (data), and all low speed status  
 7 outputs.

8 The SCL and SDA is a hot plug interface that may support a bus topology. During  
 9 module insertion or removal, the module may implement a pre-charge circuit which  
 10 prevents corrupting data transfers from other modules that are already using the  
 11 bus.

12 Compliance with Table 5-2 provides compatibility between host bus masters and the  
 13 two-wire interface.

TABLE 5-2 LOW SPEED ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min	Max	Unit	Notes/Conditions
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0 mA
	VOH	$V_{cc}-0.5$	$V_{cc}+0.3$	V	
SCL and SDA	VIL	-0.3	$V_{cc}*0.3$	V	
	VIH	$V_{cc}*0.7$	$V_{cc} + 0.5$	V	
Capacitance on SCL and SDA I/O contact.	$C_i$		14	pF	Looking into the module SCL and SDA contacts.
Total bus capacitive load for SCL and SDA for up to 400 kHz SCL rate (includes capacitance of all elements on the bus).	$C_b$		100	pF	3.0 k $\Omega$ pullup resistor
			200	pF	1.6 k $\Omega$ pullup resistor
LPMode/TxDis, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	$V_{cc}+0.3$	V	
	$I_{in}$	-365	125	$\mu$ A	$0V \leq V_{in} \leq V_{cc}$
ModPrsL and IntL/RxLOSL	VOL	0	0.4	V	IOL=2.0mA
	VOH	$V_{cc}-0.5$	$V_{cc}+0.3$	V	

14 Notes: Positive values indicate current flowing into the module. See Appendix A  
 15 for management interface (SCL, SDA) timing information.

### 16 5.4.2 Low Speed Signal Timing

17 Timing for SCL and SDA is defined in a management interface document, SFF-8636 and  
 18 is duplicated in Appendix A for convenience. Timing of the hardware control  
 19 functions and ModSelL are specified in section 8.

## 20 5.5 High Speed Signal Electrical Specifications

21 For detailed high-speed requirements see the appropriate specification, e.g. IEEE  
 22 Std 802.3, Fibre Channel, OIF-CEI or InfiniBand. Partial or complete squelch  
 23 requirements may be provided in the appropriate specification. Where the relevant  
 24 specification does not provide a requirement or a recommendation, the following  
 25 subclauses shall apply.

### 26 5.5.1 Rx $i_p$ and Rx $i_n$

27 Rx $i_p$  and Rx $i_n$  are module receiver data outputs. They are AC-coupled 100  $\Omega$

1 differential lines that should be terminated with 100  $\Omega$  differentially at the host  
2 ASIC (SerDes). The AC coupling is inside the module and not required on the Host  
3 board.

4 Note: Due to the possibility of insertion of legacy QSFP and QSFP+ modules into a  
5 host designed for higher speed operation, it is recommended that the damage  
6 threshold of the host input be at least 1600 mV peak to peak differential.

7 Output squelch for loss of optical input signal, hereafter Rx Squelch, is required  
8 and shall function as follows. In the event that the optical signal on any channel  
9 becomes less than or equal to the level required to assert LOS, then the receiver  
10 data output for that channel shall be squelched or disabled and the associated  
11 RxLOS flag set. In the squelched or disabled state output impedance levels are  
12 maintained while the differential voltage swing shall be less than 50 mVpp or the  
13 value in the relevant standard.

14 In normal operation the default case has Rx Squelch active. Rx Squelch can be  
15 deactivated using Rx Squelch Disable through the two-wire serial interface. Rx  
16 Squelch Disable is an optional function. For specific details refer to SFF-8636.

### 17 5.5.2 Tx<sub>ip</sub> and Tx<sub>in</sub>

18 Tx<sub>ip</sub> and Tx<sub>in</sub> are module transmitter data inputs. They are AC-coupled 100  $\Omega$   
19 differential lines with 100  $\Omega$  differential terminations inside the module. The AC  
20 coupling is inside the module and not required on the Host board.

21 Due to the possibility of insertion of modules into a host designed for lower speed  
22 operation, the damage threshold of the module input shall be at least 1600 mV peak  
23 to peak differential.

24 Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS,  
25 is an optional function. Where implemented it shall function as follows. In the  
26 event that the input signal becomes less than 50 mVpp or the value in the relevant  
27 standard, then the transmitter optical output for that channel shall be squelched  
28 or disabled and the associated TxLOS flag set.

29 Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and  
30 when disabled the transmitter power shall be less than or equal to -30 dBm or the  
31 value(s) defined by the relevant standard. For applications, e.g. Ethernet, where  
32 the transmitter off condition is defined in terms of average power, disabling the  
33 transmitter is recommended and for applications, e.g. InfiniBand, where the  
34 transmitter off condition is defined in terms of OMA, squelching the transmitter is  
35 recommended.

36 In module operation, where Tx Squelch is implemented, the default case has Tx  
37 Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the  
38 two-wire serial interface. Tx Squelch Disable is an optional function. For specific  
39 details refer to SFF-8636.

### 40 5.6 Power Supply Requirements

41 A host board together with the QSFP+ module(s) forms an integrated power system. The  
42 host supplies stable power to the module. The module limits electrical noise coupled  
43 back into the host system and limits inrush charge/current during hot plug insertion.

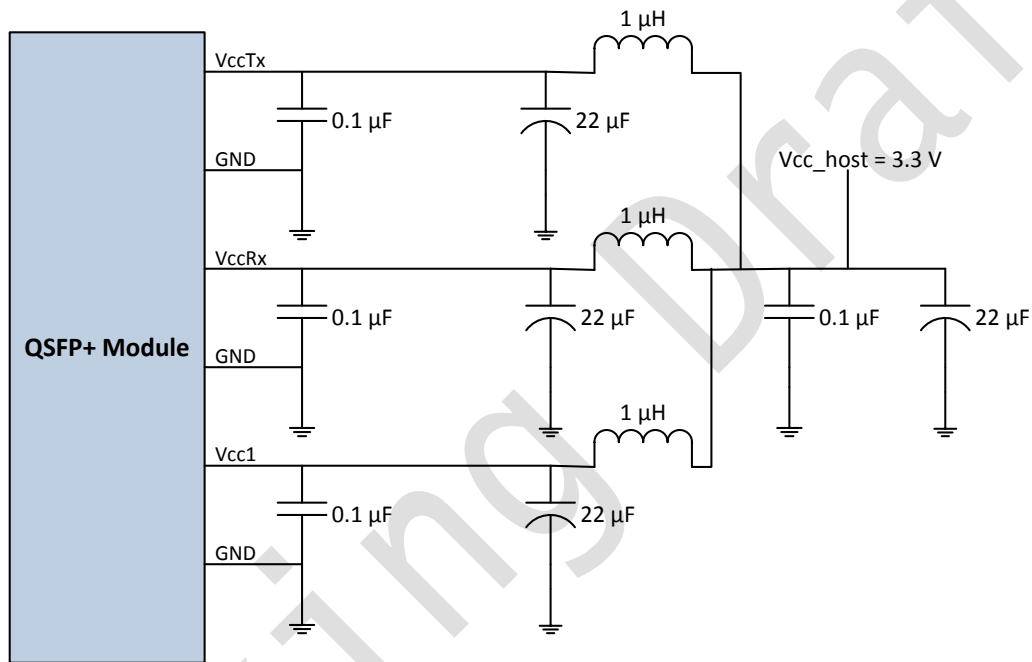
44 The circuit card in a QSFP+ module has three designated power pads, designated VccTx,  
45 VccRx and Vcc1. When the QSFP+ module is "hot plugged" into a connector with power  
46 already present, the three pads have power applied concurrently. The module is

1 responsible for limiting the inrush current surge from the reference power supply  
 2 filtering circuit during a hot plug event. The host power supply may supply up to the  
 3 maximum inrush current limits during a hot plug event without causing disturbance to  
 4 other modules and components on the same power supply.

5 All specifications shall be met at the maximum power supply current. No power  
 6 sequencing of the power supply is required of the host system. The module sequences  
 7 the contacts in the order of ground, supply and signals during insertion.

### 8 5.6.1 Host Board Power Supply Filtering

9 The host board should use a power supply filtering network equivalent to that shown  
 10 in Figure 5-4.



11 **FIGURE 5-4 RECOMMENDED HOST BOARD POWER SUPPLY FILTERING**

12 Any voltage drop across a filter network on the host is counted against the host DC  
 13 set point accuracy specification. Inductors with DC resistance of less than 0.1  $\Omega$   
 14 should be used in order to maintain the required voltage at the host edge card  
 15 connector. It is recommended that the 22  $\mu$ F capacitors each have an equivalent series  
 16 resistance of 0.22  $\Omega$ .

17 The specification of the host power supply filtering network is beyond the scope of  
 18 this specification, particularly because of the wide range of QSF+ module Power  
 19 Classes. An example current waveform into a host filter, labeled I1 in Figure 5-5 is  
 20 plotted in Figure 5-6. Each power connection has a supply filter for reducing high  
 21 frequency noise and ripple from host-to-module. During a hot-plug event, the filter  
 22 network limits any voltage drop on the host supply so that neighboring modules sharing  
 23 the same supply stay within their specified supply voltage limits.

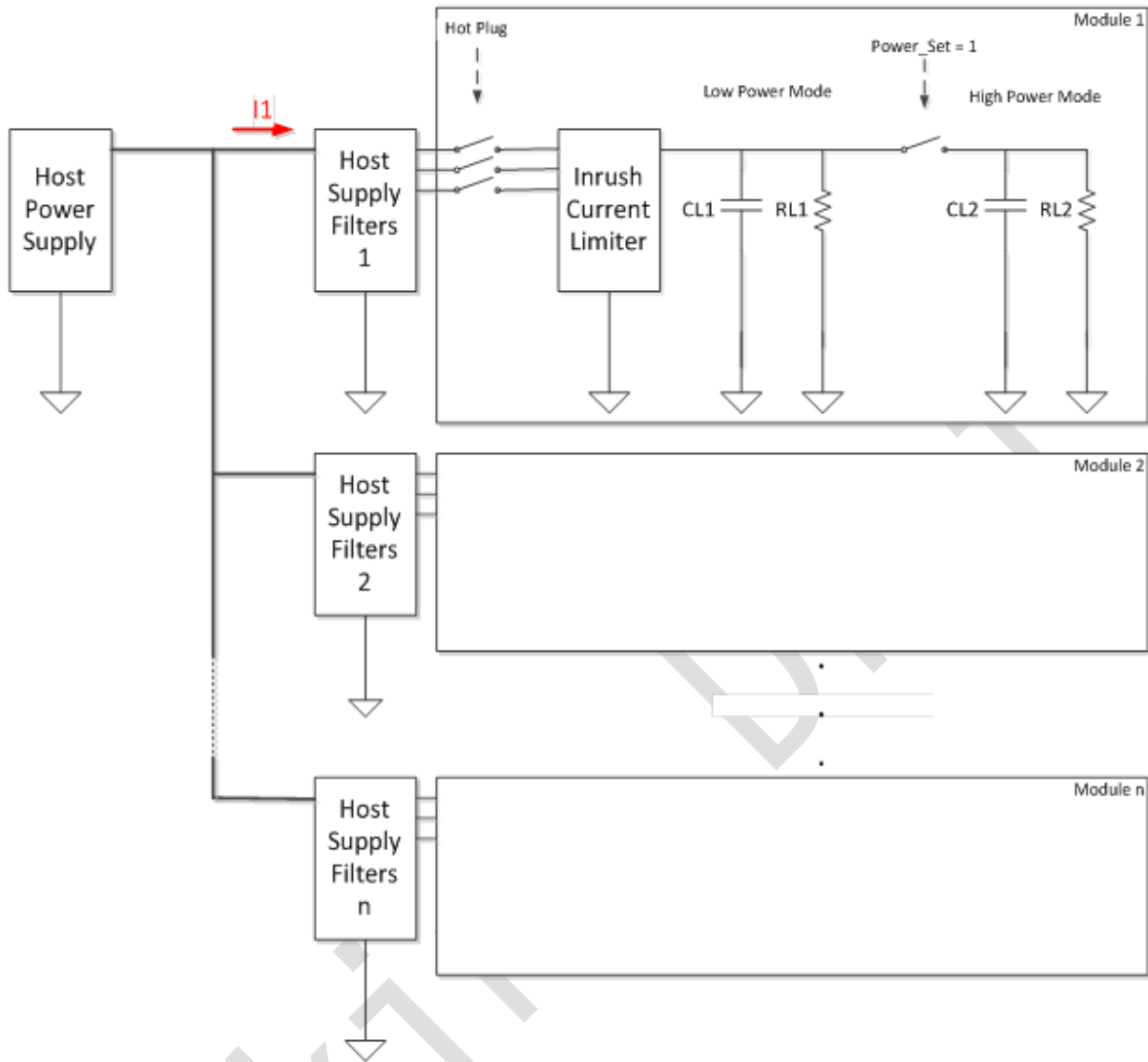


FIGURE 5-5 EXAMPLE: SCHEMATIC OF MULTIPLE QSFP28 POWER SUPPLY ARRANGEMENT

1

2 **5.6.2 Power Classes and Maximum Power Consumption**

3 Since different classes of modules exist with pre-defined maximum power consumption  
 4 limits, it is necessary to avoid exceeding the host power supply limits and cooling  
 5 capacity when a module is inserted into a host designed to use only lower power  
 6 modules. It is recommended that the host, through the management interface, identify  
 7 the power consumption class of the module before allowing the module to go into High  
 8 Power Mode.

9 QSFP+ modules are categorized into several Power Classes as listed in Table 5-3.  
 10 Power Classes are advertised in SFF-8636, Page 00h, Byte 129 (81h).

11

1

TABLE 5-3 QSFP+ – MODULE POWER CLASSES

Power Class	Maximum power consumption per module (W)
1	1.5
2	2.0
3	2.5
4	3.5
5	4.0
6	4.5
7	5.0
8	10.0 (Note)

2 Note: Maximum power is declared by the module in SFF-8436, Page 00h, Byte 129.

3 In order to avoid exceeding the host system power capacity, upon hot-plug, power  
 4 cycle or reset, all QSFP+ modules shall power up in Power Class 1, designated as "Low  
 5 Power Mode". QSFP+ modules that are Power Class 1 are fully functional after  
 6 initialization and remain in Low Power Mode during operation. All other QSFP+ modules  
 7 reach fully functional operation only after the host system enables High Power Mode".

8 High Power Mode is defined as the Power Class advertised in SFF-8636, Page 00h, Byte  
 9 129 and is enabled by the host if the host can supply sufficient power to the module.  
 10 The host system controls whether a particular Power Class is enabled using the LPMode  
 11 input pad and/or by writing to four control bits in SFF-8636, Page 00h, Byte 93. The  
 12 management interface specification, SFF-8636 provides complete details but for  
 13 explanation of power supply control, the bits are listed in Table 5-4.

TABLE 5-4 POWER MODE CONTROL BITS (SEE SFF-8636)

Addr	Bit	Name	Description
93	7-4	Reserved	
	3	High Power Class Enable (Class 8)	When set to 1 enables Power Class 8 if listed in Byte 129. When cleared to 0, modules with Power Class 8 shall dissipate less than the power specified by bit 2, but are not required to be fully functional. Refer to Table 5-5. Default=0.
	2	High_Power_Class_Enable (Classes 5-7)	When set to 1 enables Power Classes 5 to 7 if listed in Byte 129. When cleared to 0, modules with Power Classes 5 to 8 shall dissipate less than 3.5 W, but are not required to be fully functional. Default=0.
	1	Power_set	Power set to Low Power Mode (Power Class 1). Default=0.
	0	Power_override	Override of LPMode/TxDis pad state to allow power mode setting by software.

14 **Note: Power Class 8 relies on future changes to the management specification**  
 15 **(beyond SFF-8636 rev 2.9)**

16



- 1 A truth table showing the allowed Power Classes is shown in Table 5-5.

TABLE 5-5 POWER MODE TRUTH TABLE

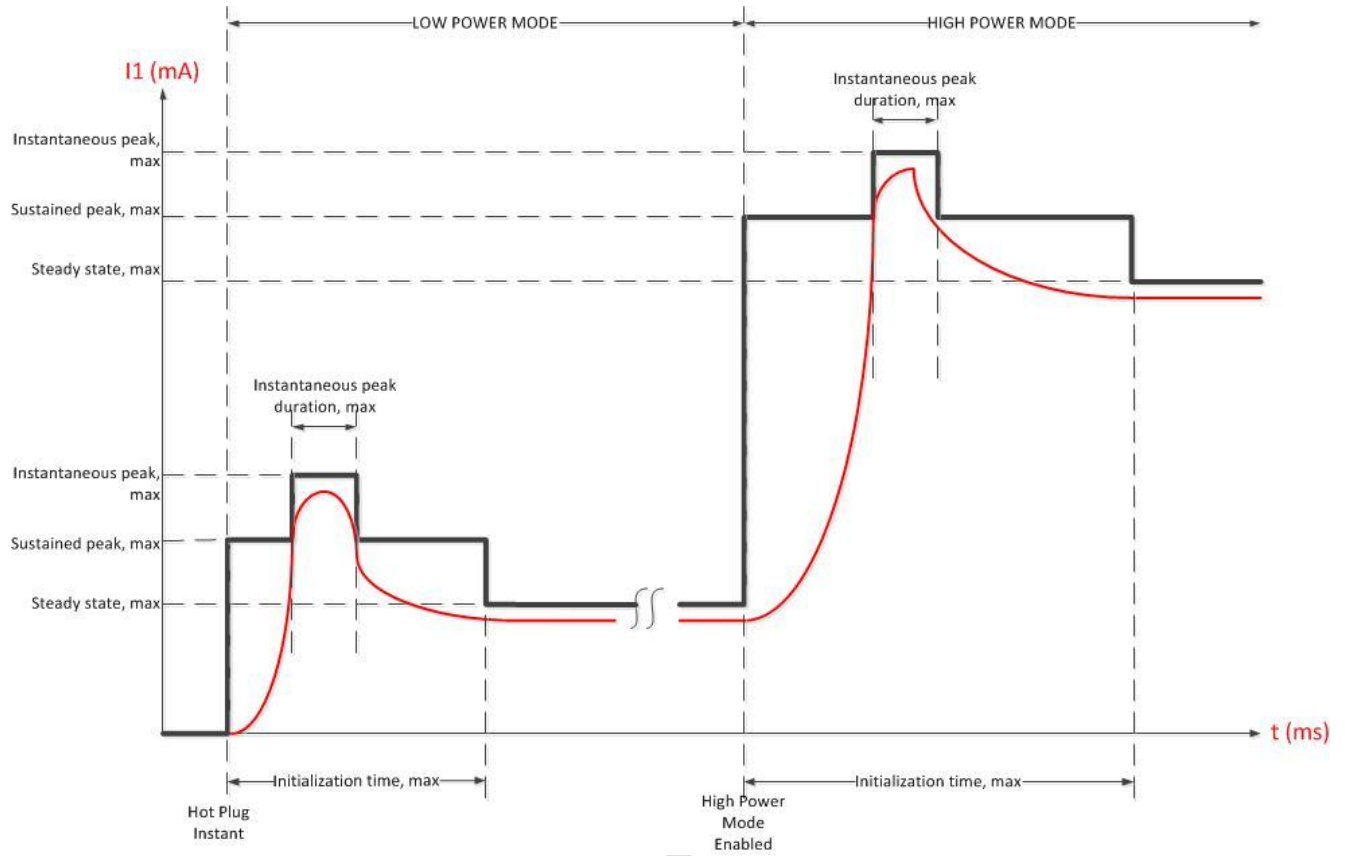
Power_override Byte 93 bit 0	Power_set Byte 93 bit 1	High_Power_ Class_Enable (Class 5-7) Byte 93 bit 2	High_Power_ Class_Enable (Class 8) Byte 93 bit 3	LPMode/TxDis pad state	Module Power Classes Enabled
<i>Power consumption controlled by LPMode/TxDis pad state</i>					
0	X	0	0	1	1
0	X	0	0	0	1 to 4
0	X	1	0	1	1
0	X	1	0	0	1 to 7
0	X	X	1	1	1
0	x	1	1	0	1 to 8
0	X	0	1	0	8
<i>Power consumption controlled by Power_set bit</i>					
1	1	0	0	X	1
1	0	0	0	X	1 to 4
1	1	1	0	X	1
1	0	1	0	X	1 to 7
1	1	X	1	X	1
1	0	1	1	x	1 to 8
1	0	0	1	X	8

- 2
- 3 **5.6.3 Module Power Supply Specification**
- 4 Module power supply specifications are given in Table 5-6.

5 QSFP+ modules operate from the host supplied voltage at the three power pads. To  
6 protect the host and system operation, each QSFP+ module during hot plug and normal  
7 operation shall follow the requirements listed in Table 5-5 and illustrated in  
8 Figure 5-6.

9 The test configuration for measuring the supply current is a module power compliance  
10 board with reference power supply filters, similar to the circuit shown in Appendix  
11 D and Figure 56 of SFF-8431. The current limits in Table 5-6 refer to the sum of the  
12 three currents, e.g. the equivalent of the current through the 0.1  $\Omega$  sense resistor  
13 in Figure 56 of SFF-8431.

14 An example current waveform into a host filter, labeled I1 in Figure 5-5 is plotted  
15 in Figure 5-6. This figure also shows the timing of the initial module turn-on in Low  
16 Power Mode, and the later transition to full power mode after the host system has  
17 enabled it via the two-wire interface.



1

FIGURE 5-6 QSF+ INRUSH CURRENT TIMING

2

TABLE 5-6 QSFP+ MODULE POWER SUPPLY SPECIFICATION

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccRx and Vcc1 including ripple, droop and noise below 100 kHz (Note 1)		3.135	3.3	3.465	V
Host RMS noise output 10 Hz to 10 MHz				25	mV
Module RMS noise output 10 Hz to 10 MHz (Note 2)				15	mV
Module power supply noise tolerance 10 Hz to 10 MHz (peak-to-peak)	PSNR_Mod			66	mV
Module inrush - instantaneous peak duration	T_ip	-	-	50	μs
Module inrush - initialization time	T_init	-	-	500	ms
<b>Power Class 1 module and Low Power Mode for other modules</b>					
Power consumption	P_1	-	-	1.5	W
Instantaneous peak current at hot plug	Icc_ip_1	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_1	-	-	495	mA
Steady state current (Note 3)	Icc_1	-	-	432.9	mA
<b>High Power Mode Power Class 2 module</b>					
Power consumption	P_2	-	-	2	W
Instantaneous peak current at hot plug	Icc_ip_2	-	-	800	mA
Sustained peak current at hot plug	Icc_sp_2	-	-	660	mA
Steady state current (Note 3)	Icc_2	-	-	577.2	mA
<b>High Power Mode Power Class 3 module</b>					
Power consumption	P_3	-	-	2.5	W
Instantaneous peak current at hot plug	Icc_ip_3	-	-	1000	mA
Sustained peak current at hot plug	Icc_sp_3	-	-	825	mA
Steady state current (Note 3)	Icc_3	-	-	721.5	mA
<b>High Power Mode Power Class 4 module</b>					
Power consumption	P_4	-	-	3.5	W
Instantaneous peak current at hot plug	Icc_ip_4	-	-	1400	mA
Sustained peak current at hot plug	Icc_sp_4	-	-	1155	mA
Steady state current (Note 3)	Icc_4	-	-	1010.1	mA
<b>High Power Mode Power Class 5 module</b>					
Power consumption	P_5	-	-	4	W
Instantaneous peak current at hot plug	Icc_ip_5	-	-	1600	mA
Sustained peak current at hot plug	Icc_sp_5	-	-	1320	mA
Steady state current (Note 3)	Icc_5	-	-	1154.4	mA
<b>High Power Mode Power Class 6 module</b>					
Power consumption	P_6	-	-	4.5	W
Instantaneous peak current at hot plug	Icc_ip_6	-	-	1800	mA
Sustained peak current at hot plug	Icc_sp_6	-	-	1485	mA
Steady state current (Note 3)	Icc_6	-	-	1298.7	mA
<b>High Power Mode Power Class 7 module</b>					
Power consumption	P_7	-	-	5	W
Instantaneous peak current at hot plug	Icc_ip_7	-	-	2000	mA
Sustained peak current at hot plug	Icc_sp_7	-	-	1650	mA
Steady state current (Note 3)	Icc_7	-	-	1443.0	mA

Parameter	Symbol	Min	Nom	Max	Unit
<b>High Power Mode Power Class 8 module</b>					
Power consumption (Note 4)	P_8	-	-	10	W
Instantaneous peak current at hot plug	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current at hot plug	Icc_sp_8	-	-	P_8/3.03	A
Steady state current (Note 3)	Icc_8	-	-	3	A
Note 1: Measured at VccTx, VccRx and Vcc1.					
Note 2: See 5.6.5					
Note 3: The module must stay within its declared power class for all supply voltages.					
Note 4: User must read management register for maximum power consumption.					

1

#### 2 5.6.4 Host Board Power Supply Noise Output

3 The host shall generate an effective weighted integrated spectrum RMS noise less  
4 than the value in Table 5-6 when tested by the methods of SFF-8431, section D.17.1.  
5 The resistive load for the test needs to be tailored for the QSFP power class and  
6 may be implemented using constant current sink circuits attached to each host  
7 supply filter output.

#### 8 5.6.5 Module Power Supply Noise Output

9 The QSFP+ module shall generate less than the value in Table 5-6 when tested by the  
10 methods of SFF-8431, section D.17.2. The test fixture source resistor should be  
11 scaled by the ratio: (1.5W / maximum module power consumption), where maximum  
12 module power consumption is either the maximum of the advertised power class, or  
13 the advertised maximum power.

#### 14 5.6.6 Module Power Supply Noise Tolerance

15 The QSFP+ module shall meet all requirements and remain fully operational in the  
16 presence of a sinusoidal tolerance signal of amplitude given by Table 5-6, swept  
17 from 10 Hz to 10 MHz according to the methods of SFF-8431, section D.17.3. This  
18 emulates the worst-case noise output of the host. The source resistance for the  
19 power supply and sine wave generator may need to be reduced from 0.5  $\Omega$  to a lower  
20 value for high powered modules.

#### 21 5.7 ESD

22 Where ESD performance is not otherwise specified, e.g. in the InfiniBand  
23 specification, the module shall meet ESD requirements given in EN61000-4-2,  
24 criterion B test specification when installed in a properly grounded cage and  
25 chassis. The units are subjected to 15 kV air discharges during operation and 8 kV  
26 direct contact discharges to the case.

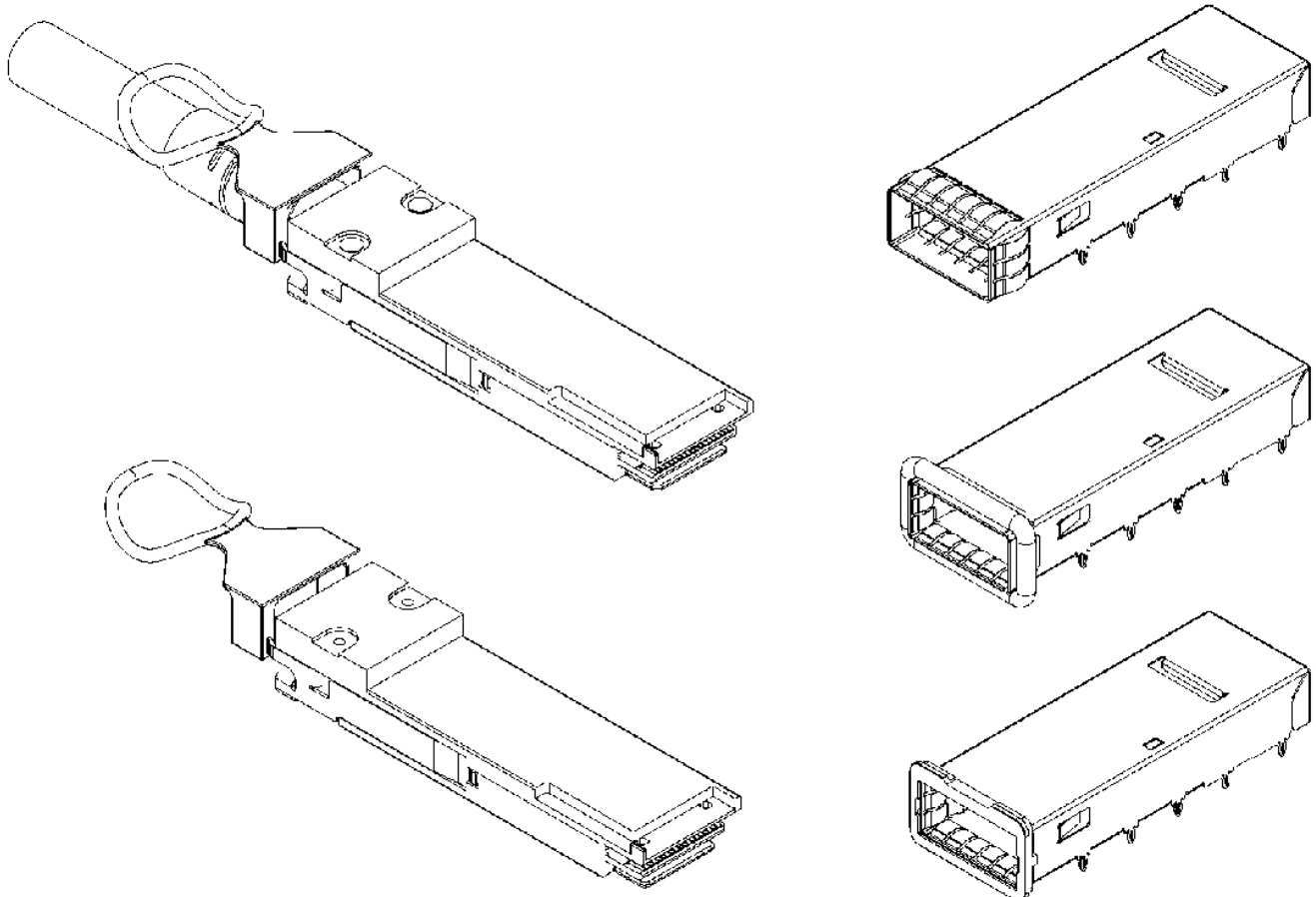
27 The module and host shall withstand 1000 V electrostatic discharge based on Human  
28 Body Model per JEDEC JESD22-A114-B for all pins.

29

## 1 6 Mechanical and Board Definition

### 2 6.1 Mechanical general

3 The overall module defined in this clause is illustrated in Figure 6-1. The optical  
 4 interface is described in section 6.3. Several cage-to-bezel options are possible.  
 5 Both metal spring finger and elastomeric EMI solutions are permitted. Heat  
 6 sink/clip thermal designs are not defined by this specification; however, general  
 7 designs are described in SFF-8663 and SFF-8683.



8  
 9 **FIGURE 6-1 PLUGGABLE MODULE AND CABLE PLUG RENDERING**

### 10 6.2 Color Coding and Labeling of Modules

11 An exposed feature of the module (a feature or surface visible when the module is  
 12 fully inserted in the host) shall be color coded. Unless industry specifications  
 13 apply, the following colors should be used.

- 14 Beige for 850 nm
- 15 Blue for 1310 nm
- 16 White for 1550 nm

17

18 Each module shall be clearly labeled. The complete labeling need not be visible

1 when the module is installed. The bottom of the module is the recommended location  
2 for the label. Labeling shall include:

- 3           Appropriate manufacturing and part number identification
- 4           Appropriate regulatory compliance labeling
- 5           A manufacturing traceability code

7 The label should also include clear specification of the external port  
8 characteristics such as:

- 9           Interface standard(s) supported
- 10          and/or
- 11          Optical wavelength
- 12          Required fiber characteristics
- 13          Operating data rate
- 14          Link length supported

16 The labeling shall not interfere with the mechanical, thermal or EMI features.

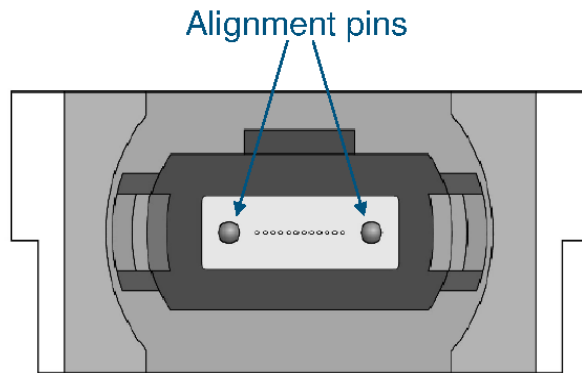
17 **6.3 Optical Interface**

18 Unless specified in the relevant standard, the recommended connectors are: a male  
19 MPO connector as specified in IEC 61754-7 (see Figure 6-4) or a dual LC as  
20 specified in IEC 61754-20 (see Figure 6-5). The assignment of transmit and receive  
21 directions is shown in Figure 6-2 and Figure 6-3.

22 The four fiber positions on the left as shown in Figure 6-2, with the key up, are  
23 used for the optical transmit signals (Channel 1 to 4). The fiber positions on the  
24 right are used for the optical receive signals (Channel 4 to 1).

25   The central four fibers may be physically present.

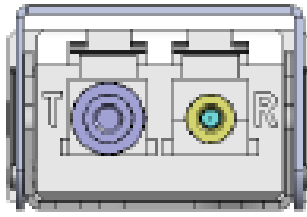
26   Two alignment pins are present.



Transmit Channels: 1 2 3 4  
 Unused positions: x x x x  
 Receive Channels: 4 3 2 1

27

**FIGURE 6-2 OPTICAL RECEPTACLE AND CHANNEL ORIENTATION FOR MPO CONNECTOR**



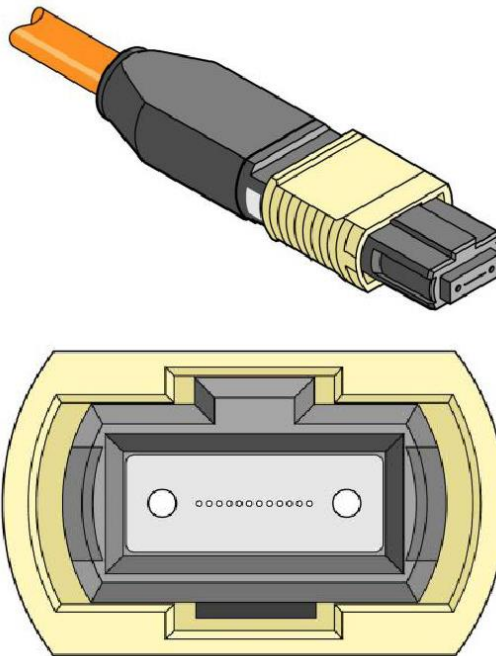
1

FIGURE 6-3 OPTICAL RECEPTACLE AND CHANNEL ORIENTATION FOR DUAL LC CONNECTOR

2

### 3 6.3.1 MPO Optical Cable Connection

4 Aligned key (Type B) MPO patch cords should be used to ensure alignment of the  
 5 signals between the modules. The aligned key patch cord is defined in IEC 61754-7  
 6 and shown in Figure 6-4. The optical connector is orientated such that the keying  
 7 feature of the MPO receptacle is on the top.

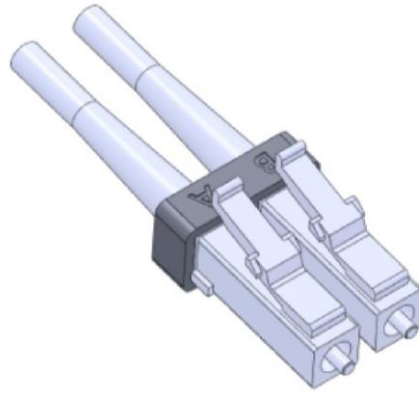


8

FIGURE 6-4 MPO OPTICAL PATCH CORD

### 9 6.3.2 Dual LC Optical Cable Connection

10 The Dual LC optical connector plug is defined in IEC 61754-20 and also in TIA/EIA-  
 11 604-10A and is shown in Figure 6-5.



1  
2  
3  
4  
5  
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7

FIGURE 6-5 DUAL LC OPTICAL CONNECTOR PLUG

2 7 Environmental and Temperature

3 7.1 Temperature Requirements

4 The module shall operate within one or more of the case temperature ranges defined  
5 in Table 7-1. The temperature ranges are applicable between 60 m below sea level  
6 and 1800 m above sea level, (Ref. NEBS GR-63) utilizing the host's designed  
7 airflow.

8  
9

TABLE 7-1 TEMPERATURE RANGE CLASS OF OPERATION

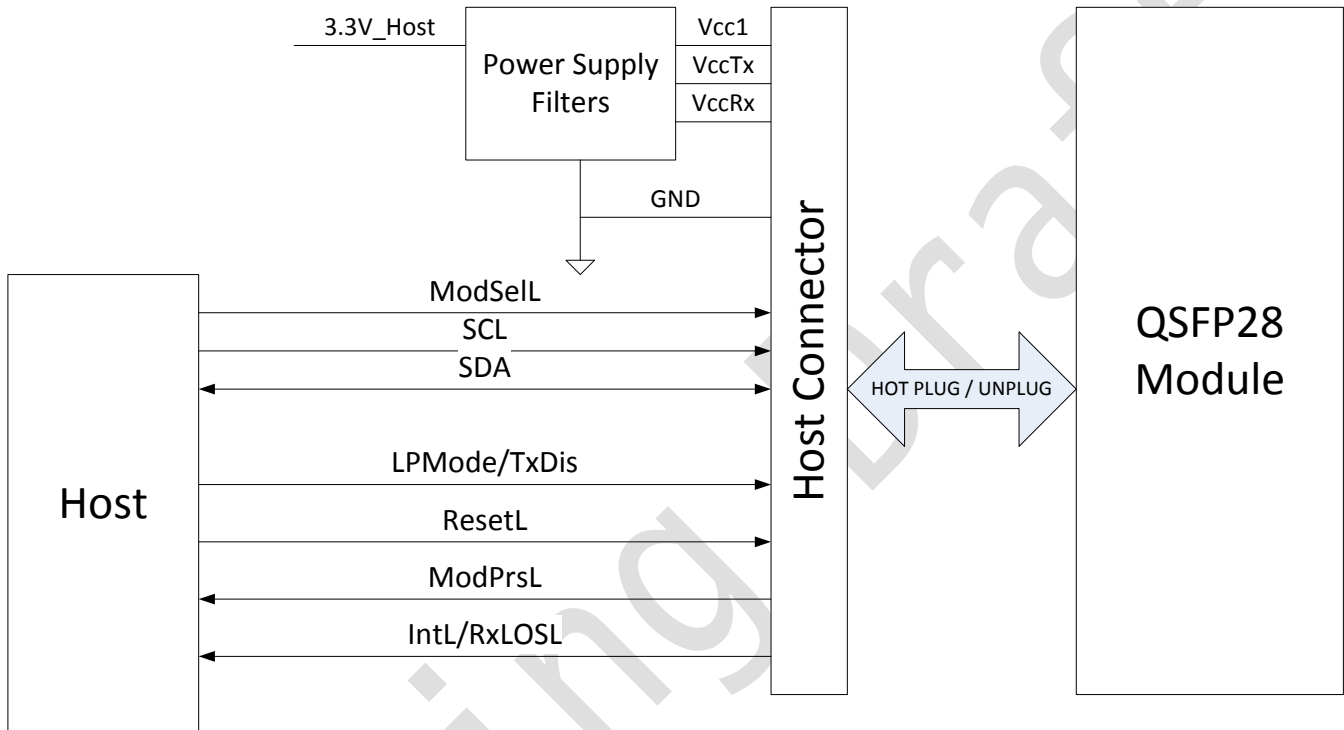
Class	Case Temperature Range
Standard	0 to 70 °C
Extended	-5 to 85 °C
Industrial	-40 to 85 °C
Custom	Reported by two-wire interface (see SFF-8636)



1 **8 Timing Requirements**

2 A block diagram illustrating the control and status signals between a host system  
3 and a QSFP+ module is shown in Figure 8-1. Timing requirements for the signals SCL  
4 and SDA are provided in the SFF-8636 specification. Timing requirements for:  
5 ResetL, LPMode/TxDis, ModSelL, IntL/RxLOSL signals are provided in this section. In  
6 addition, the timing of control and status functions implemented via the two-wire  
7 interface are provided.

8



9

FIGURE 8-1 BLOCK DIAGRAM OF MODULE CONTROL SIGNALS

10

## 1 8.1 Control and Status Timing Requirements

TABLE 8-1 CONTROL AND STATUS TIMING REQUIREMENTS

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
Initialization time	t_init		2	s	Time from power on, hot plug or rising edge of ResetL until the module is fully functional. This time applies to Power Class 2 or higher modules when LPMODE is pulled low by the host, and to all Power Class 1 modules.	2,3,6
Reset Init Assert Time	t_reset_init	10	-	µs	Host is required to provide a reset pulse of at least the minimum value for the module to guarantee a reset sequence. Shorter pulses may reset the module depending on implementation.	
Serial Bus Hardware Ready Time	t_serial		2	s	Time from power on until the module responds to data transmission over the two-wire serial bus.	2
Monitor Data Ready Time	t_data		2	s	Time from power on to Data_Not_Ready, Byte 2 bit 0, cleared to 0 and IntL output pulled low.	2
Reset Assert Time	t_reset		2	s	Time from a rising edge on the ResetL input until the module is fully functional.	3
LPMODE/TxDis mode change time	t_LPMODE/TxDis		100	ms	Time to change between LPMODE and TxDis modes of the dual-mode signal LPMODE/TxDis	
LPMODE Assert Time	ton_LPMODE		100	ms	Time from when the host releases LPMODE to high until module power consumption reaches Power Class 1.	
LPMODE Deassert Time	toff_LPMODE		300	ms	Time from when the host pulls LPMODE low until the module is fully functional.	3, 5
IntL/RxLOSL mode change time	t_IntL/RxLOSL		100	ms	Time to change between IntL and RxLOSL modes of the dual-mode signal IntL/RxLOSL.	
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering an interrupt until IntL is low.	
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read operation of associated flag until module releases IntL to high. This includes the time to clear Rx LOS, Tx Fault and other flag bits.	4
RxLOSL Assert Time (Optional Fast Mode)	ton_f_LOS		1	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from optical loss of signal to RxLOSL signal pulled low by the module.	

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
RxLOSL Deassert Time (Optional Fast Mode)	toff_f_LOS		3	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high.	
Rx LOS Assert Time	ton_LOS		100	ms	Time from Rx optical signal loss to Rx LOS bit set to 1 and Intl pulled low by the module.	
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set to 1 and Intl pulled low by the module.	
Flag Assert Time	ton_flag		200	ms	Time from condition triggering flag to associated flag bit set to 1 and Intl pulled low by the module.	
Mask Assert Time	ton_mask		100	ms	Time from mask bit set to 1 until the module is prevented from pulling Intl low when the associated flag is set high.	1
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared to 0 until module is enabled to pull Intl low when the associated flag is set high.	1
Application or Rate Select Change Time	t_ratesel		100	ms	Time from change of Application Select Byte or Rate Select bit until module is in conformance with the appropriate specifications for the new application or rate.	1,7
Power_override or Power_set Assert Time	ton_Pdown		100	ms	Time from Power_override or Power_Set bit set to 1 until module power consumption reaches Power Class 1.	1
Power_override or Power_set Deassert Time	toff_Pdown		300	ms	Time from Power_override or Power_Set bit cleared to 0 until the module is fully functional.	1

- 1 Note 1: Measured from rising edge of SDA during STOP sequence of write transaction.  
2 Note 2: Power on is defined as the instant when supply voltages reach and remain at or above  
3 the minimum level specified in Table 5-6.  
4 Note 3: Fully functional is defined as the module being ready to transmit and receive valid  
5 signals and all management interface data, including monitors, being valid. It is  
6 indicated after Reset or hot plug by asserting Intl with the Data\_Not\_Ready bit  
7 being 0.  
8 Note 4: Measured from rising edge of SDA during STOP sequence of read transaction.  
9 Note 5: Does not apply to Power Class 1 modules.  
10 Note 6: For some modules this limit is overridden via the management interface, SFF-8636, or  
11 by custom product specifications.  
12 Note 7: For Fibre Channel speed negotiation, the 100 ms limit is too slow. See the relevant  
13 standard for details of the timing requirements.  
14  
15

## 1 8.2 Squelch and Tx/Rx Disable Assert, Deassert and Enable/Disable Timing

2 Table 8-2 lists the required timing performance for assert, deassert, enable and  
 3 disable of the Tx Squelch, Rx Squelch, Tx Disable and Rx Output Disable functions.

TABLE 8-2 QSFP+ SQUELCH AND TX/RX DISABLE TIMING

Parameter	Symbol	Max	Unit	Conditions	Note
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached. See 5.5.1.	
Rx Squelch Deassert Time	toff_Rxsq	15	ms	Time from resumption of Rx input signals until normal Rx output condition is reached. See 5.5.1.	
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See 5.5.2.	
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached. See 5.5.2.	
Tx Disable Assert Time	ton_TxDis	100	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.	1
Tx Disable Deassert Time	toff_TxDis	400	ms	Time from Tx Disable bit cleared to 0 until optical output rises above 90% of nominal.	1
Tx Disable Assert Time (Optional Fast Mode)	ton_f_TxDis	3	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from TxDis signal high to the optical output reaching the disabled level.	
Tx Disable Deassert Time (Optional Fast Mode)	Toff_f_TxDis	10	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from TxDis signal low to the optical output reaching the enabled level.	
Rx Output Disable Assert Time	ton_RxDis	100	ms	Time from Rx Output Disable bit set to 1 until Rx output falls below 10% of nominal.	1
Rx Output Disable Deassert Time	toff_RxDis	100	ms	Time from Rx Output Disable bit cleared to 0 until Rx output rises above 90% of nominal.	1
Squelch Disable Assert Time	ton_sqDIS	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared to 0 until squelch functionality is disabled.	1
Squelch Disable Deassert Time	toff_RxDis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set to 1 until squelch functionality is enabled.	1
Note 1: Measured from rising edge of SDA during STOP sequence of write transaction.					

4

5

## 1 8.3 QSFP Management Interface Timing Parameters

2 The ModSelL pad and the aborted sequence behavior are specific to QSFP/QSFP+/QSFP+  
 3 modules. Other timing for the SCL and SDA lines can be found in the SFF-8636  
 4 Common Management Interface document.

TABLE 8-3 QSFP MANAGEMENT INTERFACE TIMING PARAMETERS

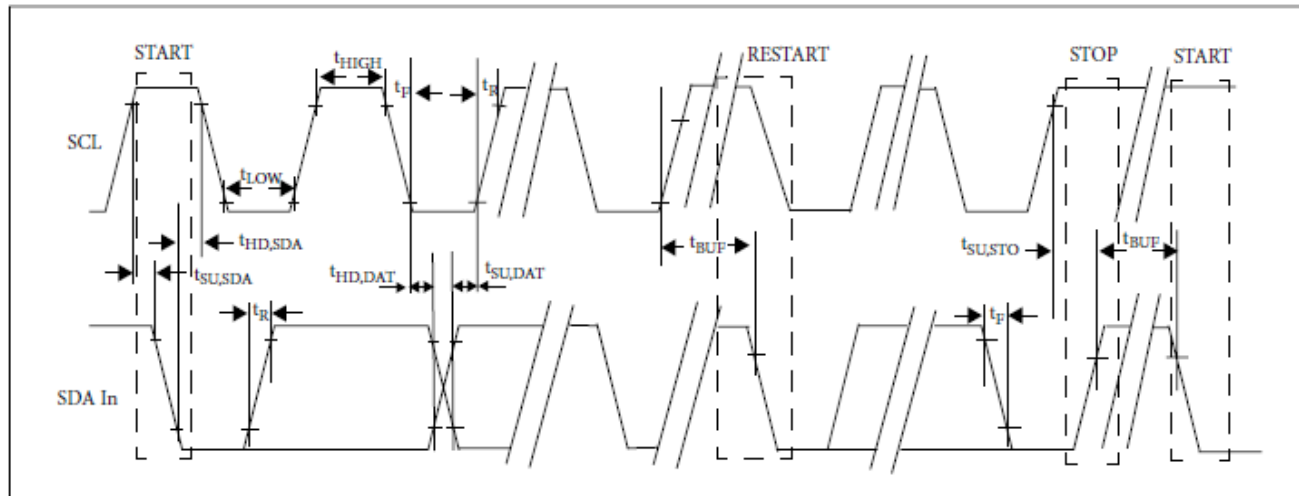
Parameter	Symbol	Min	Max	Unit	Conditions
ModSelL Setup Time (Note 1)	Host_select_setup	2		ms	Setup time on the select lines before start of a host initiated serial bus sequence
ModSelL Hold Time (Note 1)	Host_select_hold	10		us	Delay from completion of a serial bus sequence to ModSelL rising edge.
Aborted sequence - bus release	Deselect_Abort		2	ms	Delay from a host setting ModSelL to high (at any point in a bus sequence) to the QSFP module releasing SCL and SDA

5 Note 1: ModeSelL Setup and Hold times are requirements on the host system.

6

# 1 Appendix A two-wire Interface Timing

## 2 A.1 Timing Diagram



3 **FIGURE A-1 TIMING DIAGRAM**

## 4 A.2 Timing Parameters

**TABLE A-1 MANAGEMENT INTERFACE TIMING PARAMETERS**

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	kHz	
Clock Pulse Width Low	tLOW	1.3		us	
Clock Pulse Width High	tHIGH	0.6		us	
Time bus free before new transmission can start	tBUF	20		us	Between STOP and START and between ACK and Restart
START Hold Time	tHD.STA	0.6		us	
START Set-up Time	tSU.STA	0.6		us	
Data in Hold Time	tHD.DAT	0		us	
Data in Set-up Time	tSU.DAT	0.1		us	
Input Rise Time (400 kHz)	tR.400		300	ns	From (VIL, MAX-0.15) to (VIH, MIN +0.15)
Input Fall Time (400 kHz)	tF.400		300	ns	From (VIH, MIN + 0.15) to (VIL, MAX - 0.15)
STOP Set-up Time	tSU.STO	0.6		us	
Serial Clock Holdoff (Clock Stretching)	T_clock_hold		500	us	Maximum time the slave may hold the SCL line low before continuing with a read or write operation

5

6

TABLE A-2 NON-VOLATILE MEMORY SPECIFICATION

1

Parameter	Symbol	Min	Max	Unit	Conditions
Complete Single or Sequential Write	tWR		40	ms	Complete a sequential write of up to four bytes.
Endurance (Write Cycles)		50,000		cycles	70 °C

2

3

\_\_\_\_\_ END OF DOCUMENT \_\_\_\_\_