SFF-8636

Specification for

Management Interface for 4-lane Modules and Cables
Rev 2.12 April 29, 2026

SECRETARIAT: SFF TWG

This specification is made available for public review at https://www.snia.org/sff/specifications. Comments may be submitted at https://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

ABSTRACT: This specification defines a common management interface for 4-lane pluggable transceiver modules and cable assemblies. Physical layer and mechanical details of the connector interface are outside the scope of this document.

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Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, as well as since SFF's transition to SNIA in 2016, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/join.

Revision History

Rev 0.9

- Clarified wording in 6.2.2

Rev 1.0

- Added missing reservation entries (Bytes 133, 134, and 220). Modified bit entry labels (Bytes 93 and 136).

Rev 1.2

- Editorial: Formatted Word controls to improve pagination breaks and comply with style guide.

Rev 1.3

- Table 20 Identifier Values and Table 24 Encoding Values modified to point to SFF-8024 as the reference for later values and codes.

Rev 1.4

- Added Revision Compliance Byte. Changed Bytes 1, 131, 138, 146, 164, 188, and 189 to comply with latest SFF-8436 map. Added 12 Gbps SAS bit in Byte 133. Various grammatical changes made.

Rev 1.5

- Added functionality for QSFP28 (4x25G, 4x28G) transceivers per the requirements of 100GE, EDR InfiniBand and 128GFC Fibre Channel. Tables 7, 8, 10, 12, 13, 17, 19, 20, 21, 23, 29, 29A, 32A, 36, 37, 41 and section 6.2.5, 6.3.6, 6.3.12, 6.3.27.

Rev 1.6

- Abstract and Scope corrected to include transceiver modules as well as shielded cables as intended applications.

Rev 1.7 **January 24, 2014**

- Editorial: Expanded 2.1 to include specifications referenced in the body. Near-invisible superscripts were modified to be visible text and cross-references made dynamic.
- Reference to SFF-8078 in Table 13 Control Function Bytes corrected to SFF-8079.
- Table 20 Identifier Values and Table 24 Encoding Values which had been retained in the text for information were removed.
- Table 23 Specification Compliance and Table 29A Extended Ethernet Compliance Codes tables were moved to SFF-8024.

Rev 1.9 **January 27, 2014:**

- Clarified Address 5 Loss of Lock indicators as latched
- Added Address 93 bit 2 High Power Class Enable lockout feature
- Clarified Address 98 CDR controls as 1b=On and 0b=Off (i.e. bypassed)
- Clarified Table 21 for Address 129 bits 1-0 to refer to Address 93 bit 2
- Added Adaptive EQ indicator in Address 193 bit 3.
- Clarified Address 194 bits 7-6 setting as 1b=Controllable, 0b=Fixed
- Added Address 220 bit 2 to identify Tx Power diagnostic monitoring supported
- Added Page 03h Address 224 to define magnitude of Tx EQ and Rx Emph supported
- Added Tx Adaptive EQ capability indicator, Page 00h, Address 193 bit 3
- Added Tx Adaptive EQ (per ch) control bits in Page 03h, Address 241 bits 3-0
- Added Tx Adaptive EQ Fault flag in Address 6 and masking bits in Address 101
- Added Rx output amplitude support indicators in Page 03h Byte 225
- Added text to section 6.3.2 indicating that the power class identifiers specify worst case maximum power dissipation.
- Added Initialization complete flag to Byte 6 bit 0.

Rev 2.0 **August 6, 2014:**

- Changed the amplitude setting 0 from 200-400 to 100-400mv.

- Added Version 2 to address 141.
- Added Version 2 Rate Select table to Table 14 with: 00 as under 12Gb/s, 01 as between 12Gb/s and 24Gb/s, 10 as between 24Gb/s and 26Gb/s and 11 is above 26Gb/s
- Changed revision register compliance bit for revision 1.9 to 2.0 (1.9 was never released)
- Editorial changes to fix spelling and maintain consistent naming.

Rev 2.1 **August 21, 2014:**

- Assigned Page 00h Bytes 111-112 for use by PCI-SIG
- Restored Table 23 and Table 24 from SFF-8024
- Replaced 'See SFF-8024 Table 4-x' with 'See SFF-8024 Transceiver Management'
- Made Page/Address Byte, Page/Address, Page/Byte synonyms common: as Page/Byte
- Added Page/Byte/Bit location to those table titles which did not have it
- Alphabetized abbreviations and added some that were missing
- Deleted 'Ethernet' in respect to Extended Specification Compliance Codes
- Replaced Figure 13 with current use of memory
- Other minor corrections e.g. added 'h' as in Page 00h when it was missing

Rev 2.2

- During the review of Rev 2.1 it was recommended that:
- the contents of Table 22 Connector Type be moved to SFF-8024.
- the contents of Table 24 Encoding Values be returned to SFF-8024.
- Other minor editing improvements

Rev 2.3

- Nomenclature of 10e in Section 2.5 Abbreviations replaced by 10^

Rev 2.4 **November 7, 2014:**

- Adopted Figure/Table numbering style of current template
- To make correlation of previous Change History easier for readers, a Cross Reference of Figures and Tables was prepared.

Rev 2.5 **April 18, 2015:**

-Table 6-30 split creating new Table 6-31. Old Tables 6-31 to 6-35 become new Tables 6-32 to 6-36.
Figure 1-1 updated to reference SFF-8665 (QSFP28)
2.1 Industry Documents - added SFF-8665
Table 5-3 updated to include Bytes 93, 98, 99 and 107
Table 5-6 updated to include sub-headings with page numbers and to add Bytes 94-97, 100-104, 105-106, 111-112, 114-118. Changed description of Page 03h Bytes 226-241 to Optional Channel Controls. Added Page 03h Bytes 254-255.
6.1 Overview. Added fourth paragraph explaining details of non-implemented pages.
Figure 6-1. Updated Page 00h descriptions for Bytes 22-33, 100-104, 105-106, 108-110, 111-112, 113 and 114. Removed '(Cable Assemblies)' from Page 03h sub-heading.
6.1.1.1 shortened column descriptions by removing 'applications' from each one.
Table 6-1. Updated descriptions at Bytes 22-33, 86-98, 99, 100-104, 105-106, 108-110, 111-112, 113, 114-118.
6.2.2 Status Indicators. Added text to third sentence of first paragraph to emphasize that both the IntL pin and bit are asserted upon completion of a power up reset.
Table 6-3. Added value 07h for rev 2.5. Added text to value 00h - 'Do not use for...'. Updated value 01h to say SFF-8436 rev 4.8 or earlier.
Table 6-5. Additional description for Byte 6 bit 0 Initialization Complete Flag referencing Table 6-25 for the new Initialization Complete Implemented bit.
6.2.4 Free Side Device Monitors. Added fifth paragraph to explain placement of temperature sensor.
Table 6-8. Added Bytes 66-73 description for reserved channel monitor set 5.
Table 6-13. Corrected Byte 101 bits 7-4 names from L-Tx… to M-Tx…
6.2.9 Free Side Device Properties. Added paragraphs 5 and 6 to explain the purpose of Byte 113 bits 3-0 and Byte 113 bits 6-4. This byte is added for breakout cables.
Table 6-14. Added Byte 113 bits 6-4 Far End Implementation and bits 3-0 Near End Implementation descriptions.
6.2.11 Page Select. Added last sentence to define behavior when the host writes an unsupported

page value.
Table 6-15. Removed sub-headers for Base ID, Extended ID and Vendor Specific ID Fields. Changed Name of Byte 130 from 'Connector, Media' to 'Connector Type'. Updated description of Byte 146 to clarify that all cable assemblies are in units of 1m and OM4 fiber lengths are in units of 2m.
6.3.8 through 6.3.12. Added words to clarify usage for separable modules and for cable assemblies.
6.3.13. Additional sentence referencing Byte 130 (connector type) to distinguish active optical cable (AOC) from separable module (SM).
Table 6-20. Added '/ Undefined' to value 1000b.
6.3.27 Diagnostic Monitoring Type. Added additional words to fourth and fifth paragraphs to explain the treatment of Byte 220 bits 3-2 when not set.
Table 6-25. Added Byte 221 bit 4 Initialization Complete Flag Implemented, with explanation.
Table 6-29. Reformatted with # Bytes column and updated descriptions.
Table 6-31. Added Byte 225 bits 5-4 Rx output emphasis type with description.
Table 6-32. Bytes 226-233 from Vendor Specific to Reserved. Added descriptions for Byte 241 bits 3-0 to specify that adaptive equalization is the default if it is implemented.
Table 6-35. Code 1xxx from Vendor Specific to Reserved.
6.6.2 Optional Channel Controls. Added 2 sentences at the end of first paragraph to explain that free side devices can limit the maximum emphasis supported using Byte 224.

Rev 2.6 **June 19, 2015:**

Title changed per request to comply with the lexicon
Table 5-4 and other content consolidated into Table 5-3.

Rev 2.7 **January 26, 2016:**

Updates as per "bucket list" comment resolution.
Editorial corrections throughout.
Added SAS 24.0 Gbps bit in Table 6-17.

Rev 2.9 **April 21, 2017:**

Published version incorporating editorial comments received during approval ballot.
Cover Page: added David Lewis to Points of Contact.
Expressions of Support by Manufacturers: Removed names pending new ballot.
Cross Reference of Figures and Tables: Added new Table 6-10 and incremented all Table numbers from 6-11 to 6-37
2.1 Industry Documents: added SFF-8436, INF-8438, SFF-8679.
Figure 6-1 Common Memory Map: changed description of bytes 100-104 to match other places in the document.
Table 6-2 Status Indicators: Byte 2, bits 7-4 now reserved for microQSFP MSA module state field. Improved descriptions for byte 2 bits 1-0.
Table 6-3 Revision Compliance: Added 08h for SFF-8636 Rev 2.8.
Table 6-5 Free Side Monitor Interrupt Flags: Added byte 6, bit 1 for TEC readiness flag.
Table 6-9 Control Function Bytes: New descriptions for Byte 93, bit 2-0.
6.2.6 Control Functions: 4 new paragraphs describing power levels and related control functions. New Table 6-10 Truth Table for Enabling Power Classes. All following table numbers increased by 1.
6.2.7.2 Extended Rate Selection: Modified first sentence to clarify that page 00h, byte 195 bit 5 needs to be set for rate selection to be supported.
Table 6-14 Hardware Interrupt Pin Masking Bits: Added byte 103, bit 1 for TEC readiness flag masking bit.
Table 6-15 Free-Side Device Properties: Byte 114 removed from reserved and assigned for microQSFP MSA maximum duration fields.
Table 6-16 Upper Page 00h Memory Map: Added definition to byte 142 Length (SMF) to say that a value of 1 shall be used for reaches from 0 to 1 km. Added a new use for byte 145 Length (OM1 62.5 um) or Copper Cable Attenuation. Corrected byte 189 copper cable attenuation frequency from 12 to 12.9 GHz.
Table 6-19 Extended Rate Select Compliance Tag Assignment: Modified description of byte 141 bits 1-0.
6.3.11 Length (OM1) or Copper Cable Attenuation: Added new paragraph describing support for

copper cable assemblies.
Table 6-22 Extended Module Code Values: Added byte 164 bit 5 for HDR module code.
6.3.20: corrected section title to Wavelength Tolerance or Copper Cable Attenuation.
Table 6-23 Option Values: Byte 195 bit 0 used to indicate support for pages 20h-21h.
voltage monitoring.
Table 6-26 Enhanced Options: Added byte 221 bit 1 for TEC readiness flag implemented.
6.6 Upper page 03h: first paragraph modified to say that page 03h includes ability registers for optional equalizer, emphasis and amplitude.
6.6.1 Free-Side Device and Channel Thresholds: Added paragraph after Table 6-31.
Table 6-33 Optional Channel Controls: Added byte 228 Maximum TEC stabilization time and byte 229 Maximum CTLE settling time. Improved descriptions for bytes 238-239 Rx Output Amplitude Controls.
6.6.3 Optional Channel Controls: Added paragraph after Table 6-36 to clarify that Rx amplitude and emphasis are measured at the relevant test point.
Added new section 6.7 for Tables 20h-21h.
Added Annex A – alternative text for section 6.2.7 Rate Select and Configuration for Multi-Rate Modules.
Table 5-3 Added pages 20-21h
Figure 6-1 Replaced with new figure that includes pages 20-21h
Table 6-2 Replaced (O) with (-) in byte 2 bits 7-4
Table 6-2 Removed (if pin supported) from description of IntL bit
Table 6-2 Made the IntL bit (R) for all free side devices
Table 6-5 Updated the description of TC readiness flag to reflect correct reassert behavior
6.2.4 Removed reference to an external temperature control location
Table 6-9 Changed all entries from (O) to (-) for PC free side device
Table 6-15 Updated descriptions of Advanced Low Power bits and Min. Operating Voltage bits
Table 6-15 Provided names of PCI SIG specifications that use bytes 111-112
Table 6-16 Updated descriptions of bytes 142-146 to say that the link lengths apply at the stated bit rate
Table 6-23 Changed byte 193 bit 4 from reserved to "Tx Input Adaptive Equalizer Freeze Capable" bit.
Table 6-32 Moved Max. TC Stabilization Time and Max. CTLE Settling Time bytes from Table 6-33 to end of Table 6-32. Added units to descriptions. Changed table title to include timing.
Table 6-33 Changed byte 233 bits 4-0 from reserved to Tx Adaptive Equalizer Freeze control bits.
Section 6.7 Reorganization and rewording throughout.
Editorial changes for bucket list items that were missed in rev 2.8.2

Rev 2.10 **September 18, 2019:**

Deprecated Table 01h and associated advertising and control bits for "Application Select Table per SFF-8079". This feature is considered obsolete.
- Bytes 89-92 and 94-97 now reserved (were controls for SFF-8079).
- Advertising bit at Page 00h, Byte 221, bit 2, is now reserved.

Added **SW reset** control at byte 93, bit 7 and advertising bit at Page 00h, Byte 221, bit 0.
Added support for **power class 8** as described in SFF-8679 including:
- Control for High Power Class 8 at byte 93, bit 3.
- Advertising Max Power Consumption at byte 107.

Added support for **reconfiguration of LPMode/TxDis and IntL/RxLOSL** dual-purpose signals as described in SFF-8679.
- Controls for reconfiguration at byte 99, bits 1-0.
- Advertising bits at Page 00h, Byte 193, bits 6-5.

Added **ModSelL wait time** advertising field (byte 116) and text description at section 6.2.9.
Added a **Secondary Extended Spec Compliance Code** byte (byte 116).
Reworded description of bytes 140 and Page 00h, byte 222 from "BR, nominal" to "Signaling rate, nominal" and changed units from Mb/s to MBd.
Added advertising and controls for optional **Controllable Host-side FEC** support, and

Controllable Media-side FEC support for modules with FEC inside the module. Advertising bits at Page 03h, byte 227, bits 7-6. Controls at Page 03h, byte 230, bits 7-6.
Added controls for per-lane **Tx forced squelch** at Page 03h, byte 231, bits 3-0 and an advertising bit at Page 03h, byte 227, bit 3.
Added advertising bits for **Fast RxLOS and Fast TxDis** capabilities as specified in SFF-8679. Page 03h, byte 227, bits 2-1.
Updated list of industry documents at 2.1 and added a note to say that SFF-8431 is archived and is replaced by SFF-8418 and SFF-8419.
Improved description of byte 2, bit 2 in Table 6-2.
Added notes to Table 6-13 referring the reader to SFF-8449 for SAS applications.
Editorial improvements throughout.

Rev 2.10a **September 24, 2019:**
Removed "draft" from cover page of published document.

Rev 2.11 **January 03, 2023:**
Replaced master/slave with controller/target throughout the document.
Added Transceiver Subtype code and Fiber Face type code Page 00h, byte 117.
Re-labeled Figure 6-1 as Table 6-1 and renumbered consecutive tables and figures
Replaced master/slave with controller/target in figures 5-1 through 5-6. Replaced the tables with editable format (were images)
Moved byte 117 from Reserved to Free Side Device Properties group in Table 6-1 and Table 5-3
Added text describing the new fields in register 117.
Several editorial changes
To avoid confusion for PAM4 based transceivers, replaced "bit rate" with "signaling rate "or "rate"
To avoid confusion with information transfer rate, data rate, and signaling rate changed "data rate" to "rate "in few places in Appendix A.

Rev 2.12 **April 29, 2026:**
Update to new boilerplate.
Removed reserved bytes for lanes 2-4 in order to be able to accommodate future 8 lanes
Made new references in alphabetic order in section 2.1
Updates formatting and adds missing part of the title of IEEE 1588
Changed indication of inclusive registers from comma to -. i.e. N(1,4) changed to N(1-4)
Added codes to Table 6-4 (Revision compliance)
Added new section 7 with optional High Accuracy Timing registers using page 22h (extending the single lane features from SFF-8472 to four lanes)

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1 Scope

This specification defines a common memory map and protocol that can be used to manage both 4-channel pluggable transceiver modules and 4-channel managed external cable interface implementations. Physical layer and mechanical details of the interface are outside the scope of this document. Memory map details and communication protocol used to transfer the information are described within this document. This approach facilitates a common memory map and management interface for modules or cable assemblies with different mechanical, physical layer, and other characteristics. Examples include the QSFP+ family and mini multilane connectors for SAS (see REF-TA-1011).

This specification does not apply to the CFP MSA family of modules, which use the MDIO interface and a different memory map.

2 References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:

- IEEE Std 1588 IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems
- IEEE Std 802.3cx-2023 Improved PTP timestamping accuracy
- INF-8074 SFP (Small Formfactor Pluggable) Transceiver
- INF-8438 QSFP (Quad Small Formfactor Pluggable) Transceiver
- REF-TA-1011 Cross Reference to Select SFF Connectors and Modules
- SFF-8024 SFF Module Management Reference Code Tables
- SFF-8079 SFP Rate and Application Selection
- SFF-8418 SFP+ 10 Gb/s Electrical Interface
- SFF-8419 SFP+ Power and Low Speed Interface
- SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface [Archived, replaced by SFF-8418 and SFF-8419]
- SFF-8436 QSFP+ 10 Gbs 4X Pluggable Transceiver
- SFF-8449 Management Interface for SAS Shielded Cables
- SFF-8472 Management Interface for SFP+
- SFF-8665 QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28)
- SFF-8679 QSFP+ 4X Hardware and Electrical Specification

2.2 Sources

The complete list of SFF documents which have been published are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

NUMERALS CONSTANTS: Numerals without suffix are understood as numbers in decimal notation (e.g. 16). Hexadecimal literals are marked with a suffix 'h' (e.g. 10h), often written with leading zeroes (0010h). Binary literals are marked with a suffix 'b' (e.g. 10000b), often written with leading zeroes (00010000b). The suffixes may be omitted for unambiguous cases like 0=0b=0h and 1=1b=1h. Spaces may be inserted to make long hexadecimal or binary digit strings readable (e.g. 0001 0000b).

3 Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be implemented as defined by the specification. Describing a feature as optional in the text is an informational callout to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Where the term is used for a signal on a connector contact, the function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies to the restricted designation, then the restricted bit, byte, word, or field shall be treated as a value whose definition is not in scope of this document, and is not interpreted by this specification.

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

AC	active cable
AO	active optical cable
b	binary (suffix to preceding binary based number)
ºC	degrees Celsius (thermal unit associated with a value)
C	conditional upon another parameter which is optional
CDR	clock and data recovery
dB	decibel (base 10 logarithmic unit)
dBm	decibels above one milliwatt
Gbps	gigabits per second (i.e., 10^9 bits per second)
GHz	gigahertz (i.e., 10^9 cycles per second)
h	hexadecimal (suffix to preceding hexadecimal based number)
Hz	hertz (i.e., cycles per second)
kHz	kilohertz (i.e., 10^3 cycles per second)

km	kilometer (i.e., 10^3 meters)
LSB	least significant bit
m	meter (unit of length)
mA	milliampere (i.e., 10^-3 amperes)
Mbps	megabits per second (i.e., 10^6 bits per second)
MHz	megahertz (i.e., 10^6 cycles per second)
ms	millisecond (i.e., 10^-3 seconds)
MSB	most significant bit
mV	millivolt (i.e., 10^-3 volts)
mW	milliwatt (i.e., 10^-3 watts)
nm	nanometer (i.e., 10^-9 meters)
ns	nanosecond (i.e., 10^-9 seconds)
O	optional
P-P	peak-to-peak
PAM4	four-level pulse amplitude modulation
PC	passive cable
ps	picosecond (i.e., 10^-12 seconds)
R	required
Rx	receiver
s	second (unit of time)
SM	separable module
TC	temperature controller (e.g. thermo-electric cooler)
Tx	transmitter
µA	microampere (i.e., 10^-6 amperes)
µm	micrometer (i.e., 10^-6 meters)
µs	microsecond (i.e., 10^-6 seconds)
µV	microvolt (i.e., 10^-6 volts)
µW	microwatt (i.e., 10^-6 watts)
V	volt (unit of electrical potential)
W	watt (unit of electrical power)

3.3 Definitions

Bit Organization: 8-bit fields have the most significant bit at bit 7, and 16-bit fields have the most significant bit at bit 15. See Figure 3-1.

								MSB			**8-bit Field**				**LSB**
MSB								**16-bit Field**							**LSB**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 3-1 Bit Organization

Fixed: The terminology "fixed" is used to describe the gender of the mating side of the connector that accepts its mate upon mating. This gender is frequently, but not always, associated with the common terminology "receptacle". Other terms commonly used are "female" and "socket connector". The term "fixed" is adopted from EIA standard terminology as the gender that most commonly exists on the fixed end of a connection, for example, on the board or bulkhead side. In this document, the terms “fixed”, “fixed-side”, and “host” are equivalent.

Free: The terminology "free" is used to describe the gender of the mating side of the connector that penetrates its mate upon mating. This gender is frequently, but not always, associated with the common terminology "plug". Other terms commonly used are "male" and "pin connector". The term "free" is adopted from EIA standard terminology as the gender that most commonly exists on the free end of a connection, for example, on the cable side. In this document, the terms “free”, “free-side”, and “module” are equivalent.

Passive Cable: In this specification, a passive cable requires power only to operate the management interface circuitry.

Active Cable: In this specification, an active cable requires power for circuitry that is used to transmit and receive high-speed signals. In addition, power is required to operate the management interface. The high-speed electrical interface of the cable may contain equalizers and retimers (CDRs) which are managed by registers defined in this management interface specification.

Pluggable Transceiver Module: In this specification, a pluggable transceiver module, also known as a separable module (SM), requires power for the management interface and for the circuitry integral to the Tx/Rx high-speed serial channels supported by the module. The module also has a media dependent interface (MDI), such as a duplex single mode fiber or a parallel multimode fiber connector. The high-speed electrical interface of the module may contain equalizers and retimers (CDRs) which are managed by registers defined in this management interface specification. In this document, the terms “free”, “free-side”, and “module” are equivalent.

4 General Description

The management interface provides a method for the fixed side to determine the characteristics and status of the free side through a memory map. In some implementations, the interface also provides a mechanism to control the operation of the free side circuitry. For the case where the module is an end of a cable assembly, the host can determine if the cable assembly is passive, active copper, or active optical. For the case where the module is a transceiver, the host can determine if the module is used with single-mode or multimode fiber, or a copper cable assembly, and which industry standards are supported. Parameters such as supplier, part number, propagation delay and loss (for passive cable assemblies) can also be determined.

4.1 Fixed-to-Free Side Block Diagram

Note, in Figure 4-1, the limitations in the scope of SFF-8636 to the fixed-to-free side management interface.

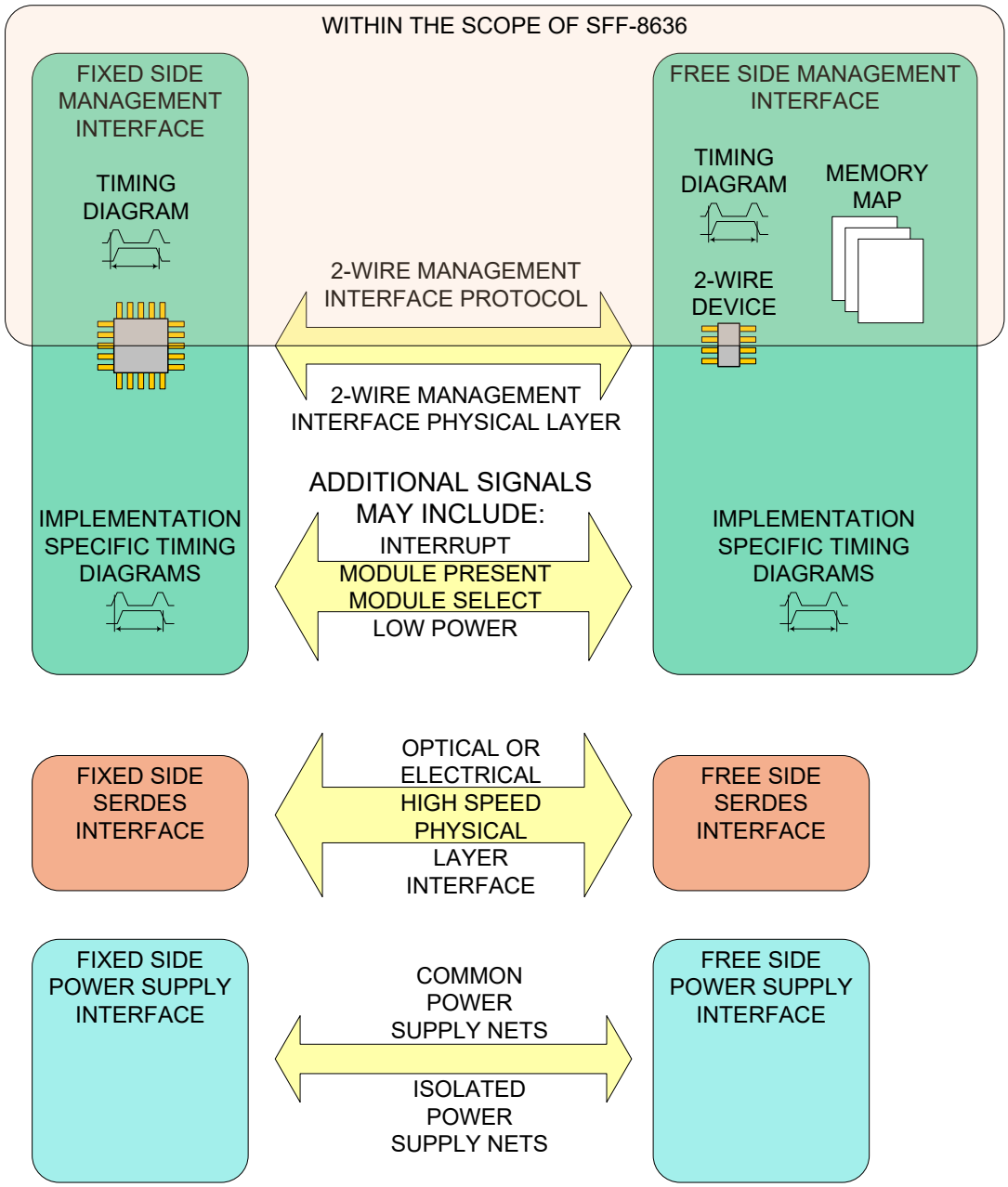

Figure 4-1 Common Management Interface Block Diagram

4.2 Signal Definition

The 2-wire management interface includes the following signals.

4.2.1 SCL

2-wire interface clock.

4.2.2 SDA

2-wire interface data.

4.2.3 Other Signals

Additional signals such as power, module present, interrupt, reset, and low-power mode may be implemented but are beyond the scope of SFF-8636. Refer to the relevant hardware specification for information on these signals.

4.3 Physical Implementation

4.3.1 Cable Assembly

The interconnect implementation may be a passive or active copper cable assembly or an active optical cable assembly, as illustrated in Figure 4-2.

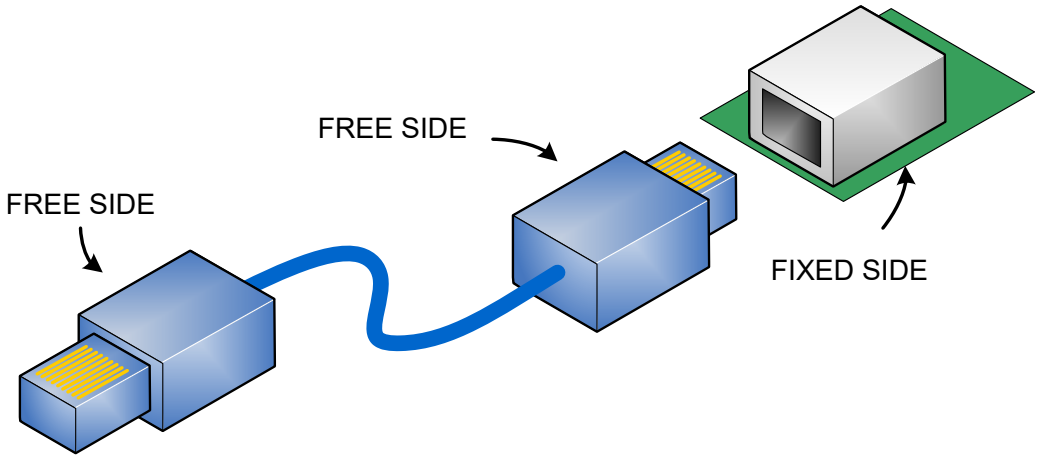

Figure 4-2 Cable Assembly Implementation

4.3.2 Separable Transceiver Modules

Figure 4-3 depicts a separable active copper or optical transceiver interconnect implementation. Only the management interface between the fixed and free side is within the scope of this document.

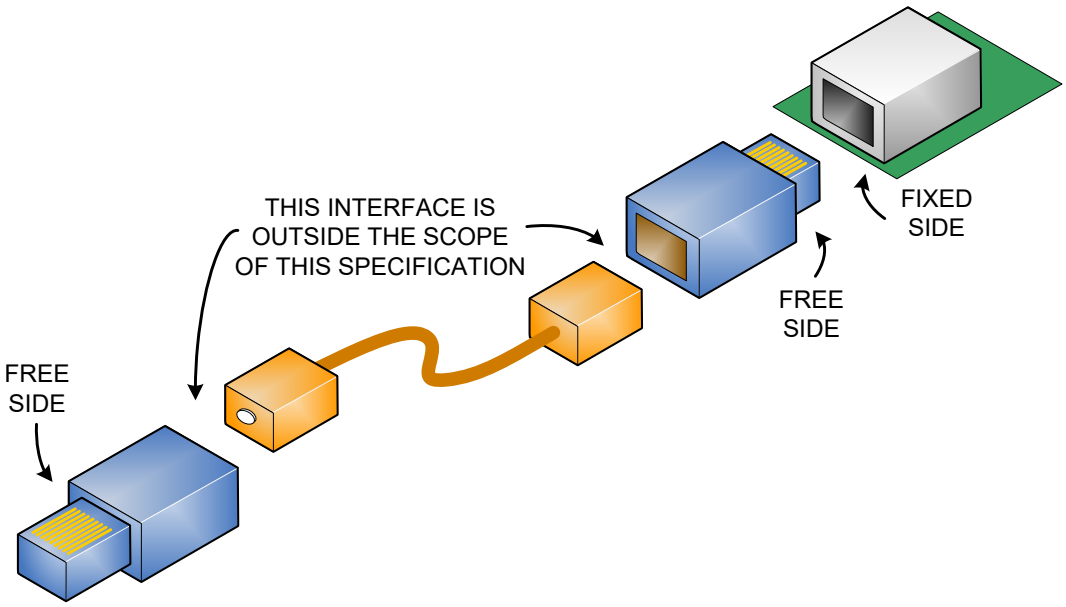

Figure 4-3 Separable Transceiver Module Implementation

4.3.3 Management Interface Scope

The scope of the management and active cable power interfaces is limited. Note that management and power interfaces do not extend from one free side end of the cable to the other.

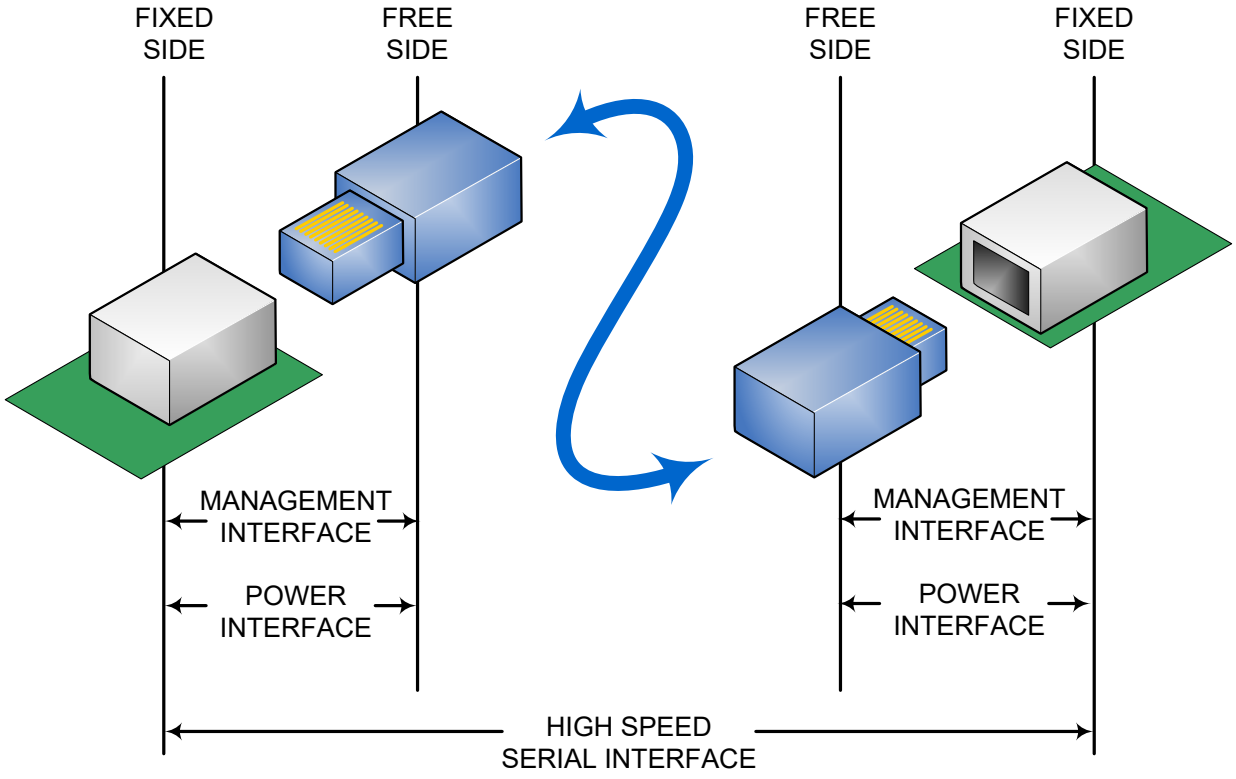

Figure 4-4 Management Interface Scope

4.4 Reset Behavior

4.4.1 Protocol Reset

Synchronization issues may cause the controller and target state machines to disagree on the specific bit location currently being transferred. See 5.2.2.

4.4.2 Power On Reset

When power is applied, the module will set all registers to their default values and reset the 2-wire interface. The timing is specified in the relevant hardware specification.

4.4.3 Reset Signals

Some implementations may include a reset pin (ResetL) and/or the optional software reset bit (see Page 00h Byte 93 bit 7). If provided, upon assertion of either signal the module will set all registers to their default values and reset the 2-wire interface. The timing is specified in the relevant hardware specification.

5 2-wire Bus Interface

5.1 Signal Interface

The 2-wire interface shall consist of a controller and a target. The fixed side shall be the controller and the free side shall be the target. Control and data are transferred serially. The controller shall initiate all data transfers. Data can be transferred from the controller to the target and from the target to the controller. The 2-wire interface shall consist of the clock (SCL) and data (SDA) signals.

The controller utilizes SCL to clock data and control information on the 2-wire bus. The controller and target shall latch the state of SDA on the positive transitioning edge of SCL.

The SDA signal is bi-directional. During data transfer, the SDA signal shall transition when SCL is low. A transition on the SDA signal, while SCL is high, shall indicate a stop or start condition.

5.2 2-wire Bus Protocol

5.2.1 The operational States and State Transitions

5.2.1.1 Start

A high-to-low transition of SDA with SCL high is a START condition. All 2-wire bus operations shall begin with a START condition.

5.2.1.2 Stop

A low-to-high transition of SDA with SCL high is a STOP condition. All 2-wire bus operations shall end with a STOP condition

5.2.1.3 Acknowledge

After sending each 8-bit word, the side driving the 2-wire bus releases the SDA line for one-bit time, during which the monitoring side of the 2-wire bus is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Write data operations shall be acknowledged by the target for all bytes. Read data operations shall be acknowledged by the controller for all but the final byte read, for which the controller shall respond with a non-acknowledge (NACK) by permitting SDA to remain high and followed by a STOP.

5.2.1.4 Clock Stretching

To extend the transfer the target asserts clock low. This can be used by the target to delay completion of the operation.

5.2.2 Protocol Reset

Synchronization issues may cause the controller and target state machines to disagree on the specific bit location currently being transferred, the type of operation or even if an operation is in progress. The 2-wire interface protocol has no explicitly defined reset mechanism. The following procedure may force completion of the current operation and cause the target to release SDA.

a) The controller shall provide up to nine SCL clock cycles (drive low, then high) to the target.
b) The controller shall monitor SDA while SCL is high on each cycle.
c) If the target releases SDA, it will be high and the controller shall initiate a START condition.
d) If SDA remains low after a full nine clock cycles the protocol reset has failed.

5.2.3 Format

5.2.3.1 Control

After the start condition, the first 8-bit word of a 2-wire bus operation shall consist of the 7-bit target address '1010000' followed by a read/write control bit.

1	0	1	0	0	0	0	R/W
MSB							LSB

The least significant bit indicates if the operation is a data read or write. A read operation is performed if this bit is high and a write operation is executed if this bit is set low. Upon completion of the control word transmission, the target shall assert the SDA signal low to acknowledge delivery (ACK) of the control/address word.

5.2.3.2 Address and Data

Following the read/write control bit, and acknowledgment by the target, addresses and data words are transmitted in 8-bit words with the most significant bit (MSB) first.

5.3 Read/Write Operations

5.3.1 Target Memory Address Counter (Read and Write Operations)

All 2-wire targets maintain an internal data word address counter containing the address accessed by the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the target. This address remains valid between operations as long as the power to the target is maintained. Upon loss of power to or reset of the free side device, the target address counter contents may be indeterminate. The address rolls over from the last byte of the 128-byte memory page to the first byte of the same page.

5.3.2 Write Operations (BYTE Write)

For a write operation the controller sends the target write control byte (10100000), monitors acknowledgment and then sends an 8-bit data word address. Upon receipt of the address, the target responds with a zero (ACK) to acknowledge and then clocks in the first 8-bit data word. Following the receipt of the 8-bit data word, the target shall output a zero (ACK) and the controller must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the 2-wire interface specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the target enters an internally timed write cycle, tWR, to internal memory. The target disables its management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the internal memory write is complete.

Note that 2-wire interface 'Combined Format' using repeated START conditions is not supported on write commands.

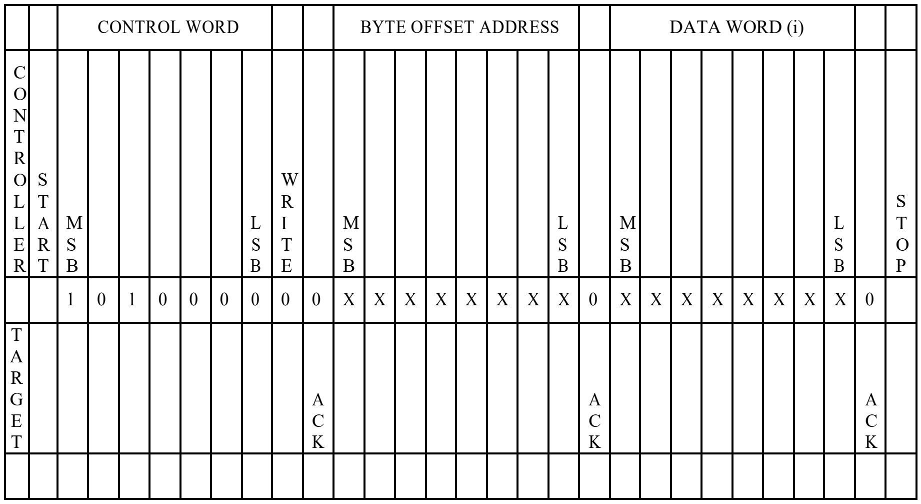

Figure 5-1 Write Byte Operation

5.3.3 Write Operations (Sequential Write)

The 2-wire target shall support a write of up to four sequential bytes without repeated target address and memory address information. A sequential write is initiated the same way as a single byte write, but the host controller does not send a stop condition after the first word is clocked in. Instead, after the target acknowledges receipt of the first data word, the controller can transmit up to three more data words. The target shall send an acknowledge after each data word received. The controller must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that 2-wire interface 'combined format' using repeated START conditions is not supported on write commands.

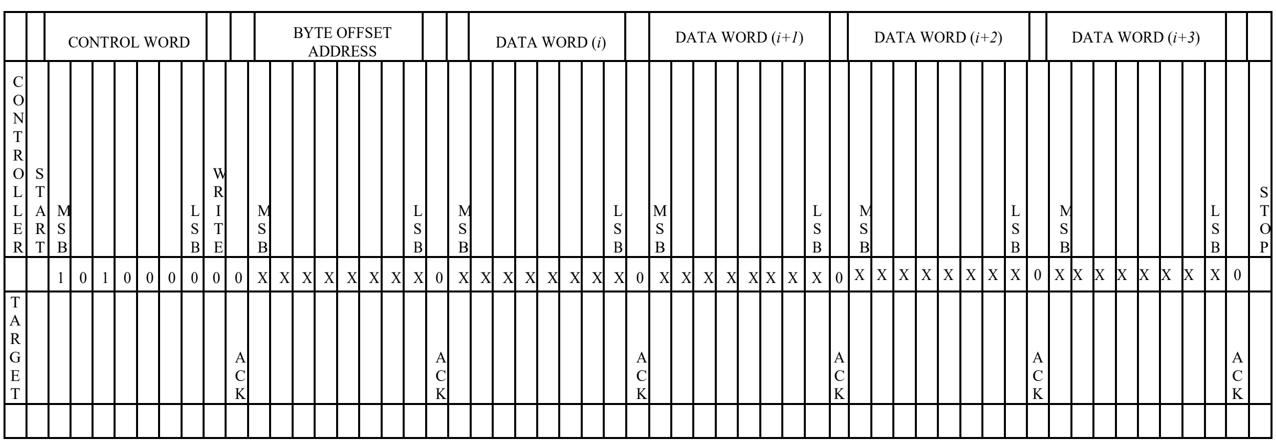

Figure 5-2 Sequential Write Operation

5.3.4 Write Operations (Acknowledge Polling)

Once the target internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. When the internal write cycle is complete the target shall respond to subsequent commands with an acknowledge indicating that read or write operations may continue.

5.3.5 Read Operations (Current Address Read)

A current address read operation requires only the target address read word (10100001) be sent. Once acknowledged by the target, the current address data word is serially clocked out. The transfer is terminated when the controller responds with a NACK and a STOP instead of an acknowledge.

		CONTROL WORD																			
CONTROLLER	START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	0	1	0	X	X	X	X	X	X	X	X	1	
TARGET										ACK	MSB							LSB		
											DATA WORD (*i*)									

Figure 5-3 Current Address Read

5.3.6 Read Operations (Random Read)

A random read operation requires a dummy write operation to load in the target byte address. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the target. The controller then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The target acknowledges the device address and serially clocks out the requested data word. The transfer is terminated when the controller responds with a NACK and a STOP instead of an acknowledge.

		CONTROL WORD									BYTE OFFSET ADDRESS									CONTROL WORD																					
CONTROLLER	START	MSB							LSB	WRITE		MSB							LSB		START	MSB							LSB	READ												NACK	STOP
		1	0	1	0	0	0	0	0	0	X	X	X	X	X	X	X	X	0		1	0	1	0	0	0	0	1	0	X	X	X	X	X	X	X	X	1	
TARGET											ACK									ACK									ACK	MSB								LSB			
																														DATA WORD (*i*)											

Figure 5-4 Random Read

5.3.7 Read Operations (Sequential Read)

Sequential reads are initiated by either a current address read or a random address read. To specify a sequential read, the controller responds with an acknowledge (instead of a STOP) after each data word. As long as the target receives an acknowledge, it shall serially clock out sequential data words. The transfer is terminated when the controller responds with a NACK and a STOP instead of an acknowledge.

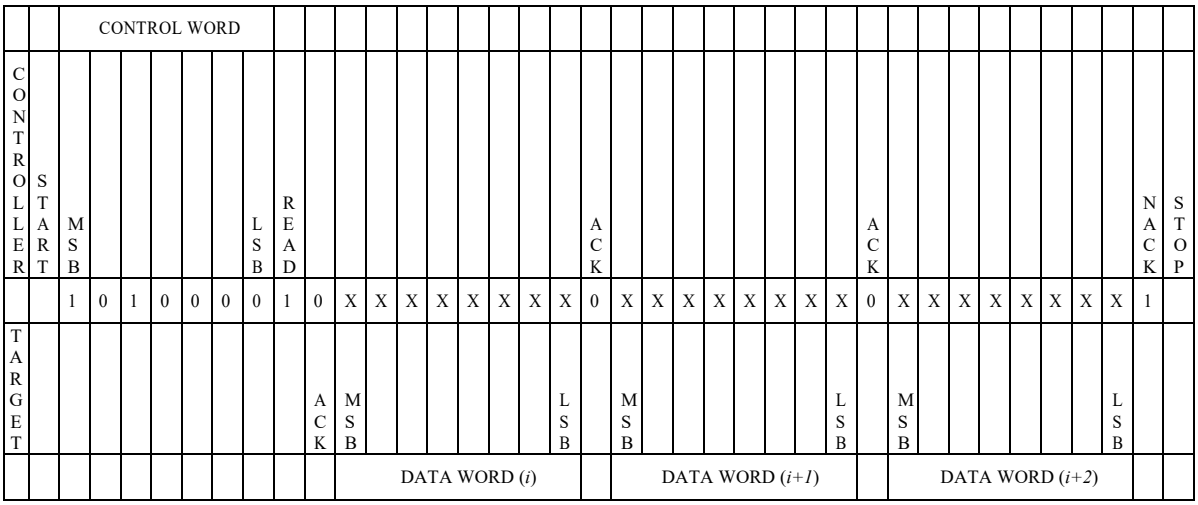

Figure 5-5 Sequential Address Read Starting at Current Address

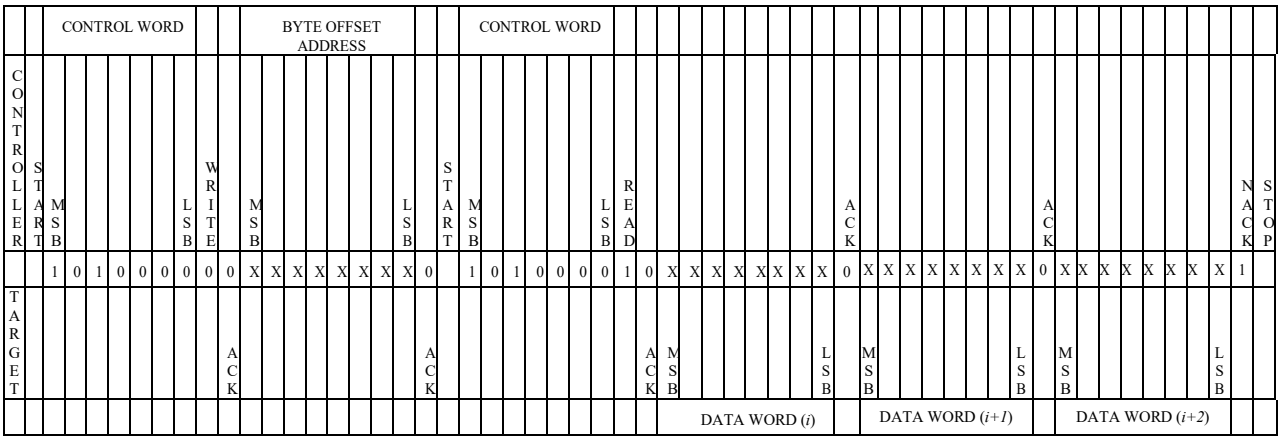

Figure 5-6 Sequential Address Read Starting with Random Read

5.4 2-wire Interface Timing

5.4.1 Timing Diagram

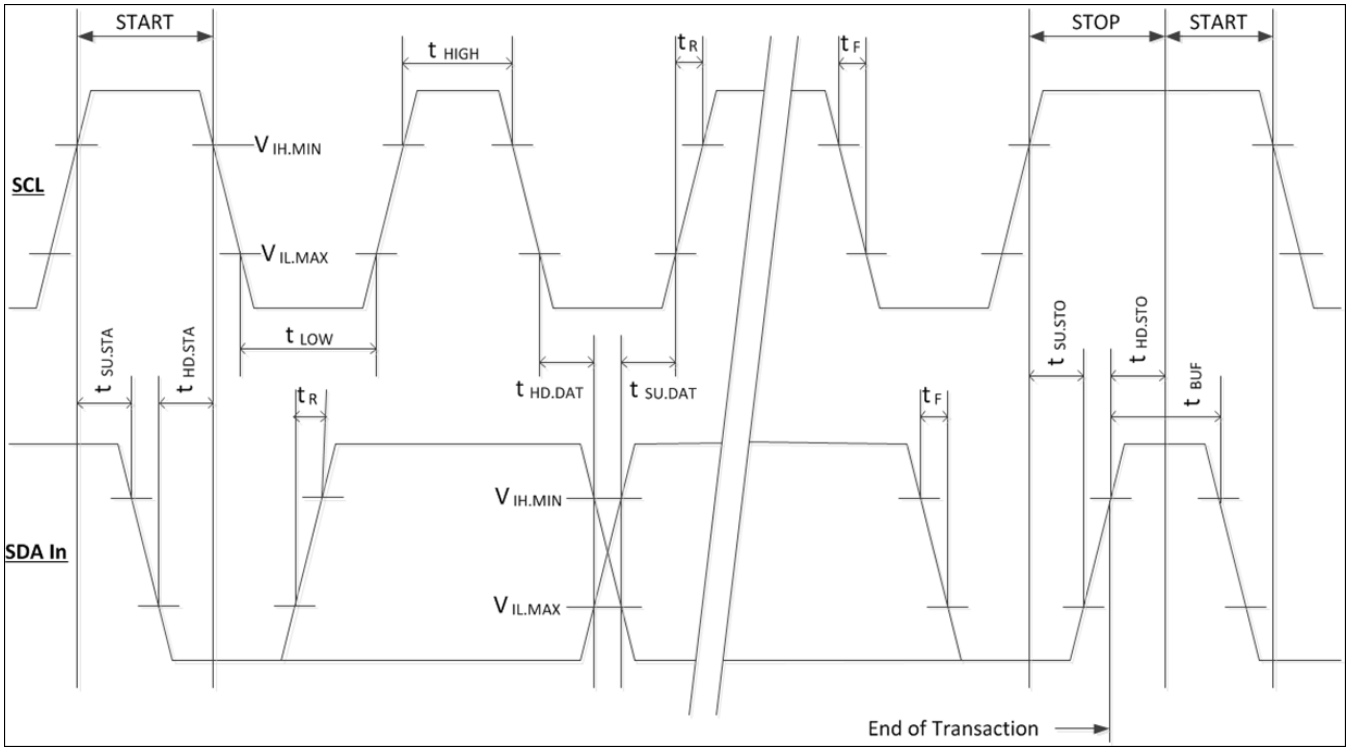

Figure 5-7 Timing Diagram

5.4.2 Timing Parameters

Table 5-1 Management Interface timing parameters

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3		µs	
Clock Pulse Width High	t_{HIGH}	0.6		µs	
Time bus free before new transmission can start	t_{BUF}	20		µs	Between STOP and START and between ACK and Restart
START Hold Time	$t_{HD.STA}$	0.6		µs	
START Set-up Time	$t_{SU.STA}$	0.6		µs	
Data In Hold Time	$t_{HD.DAT}$	0		µs	
Data in Set-up Time	$t_{SU.DAT}$	0.1		µs	
Input Rise Time (400 kHz)	$t_{R.400}$		300	ns	From (V_{IL} (max) -0.15) to (V_{IH} (min) +0.15)
Input Fall Time (400 kHz)	$t_{F.400}$		300	ns	From (V_{IH} (min) + 0.15) to (V_{IL} (max) - 0.15)
STOP Set-up Time	$t_{SU.STO}$	0.6		µs	
Serial Interface Clock Holdoff (Clock Stretching)	T_clock_hold		500	µs	Maximum time the target may hold the SCL line low before continuing with a read or write operation

Table 5-2 Non-Volatile Memory Specification

Parameter	Symbol	Min	Max	Unit	Conditions
Complete single or sequential write	t_{WR}		40	ms	Complete (up to) 4-byte Write
Endurance (Write Cycles)		50,000		cycles	70ºC

5.5 Write Operation Restrictions

The 1-byte locations shall be written with single byte write operations, and those >1 byte may be written with multi-byte write operations. The contents of writable memory blocks defined in Table 5-3, except Page 02h, are volatile with all bits set to zero at power on.

Table 5-3 Writable Memory Blocks

Byte	# Bytes	Operation	Description
Page 00h			**Volatile**
86	1	Read/Write	Control Register
87	1	Read/Write	Rx Rate select Register
88	1	Read/Write	Tx Rate select Register
89-92	4	Read/Write	Reserved (was assigned to SFF-8079 in Rev 2.9 and earlier).
93	1	Read/Write	SW Reset / High Power Class Enable / Power Set / Power Override
94-97	4	Read/Write	Reserved (was assigned to SFF-8079 in Rev 2.9 and earlier).
98	1	Read/Write	Tx and Rx CDR Controls
99	1	Read/Write	Hardware Signal Configuration Controls
100-104	5	Read/Write	Hardware Interrupt Pin Masking Bits
105-106	2	Read/Write	Vendor Specific
111-112	2	Read/Write	Assigned for use by PCI Express
118	1	Read/Write	Reserved
119-122	4	Write-Only	Password Change Entry Area (Optional)
123-126	4	Write-Only	Password Entry Area (Optional)
127	1	Read/Write	Page Select Byte
Page 02h			**Non-Volatile**
128-255	128	Read/Write	User Writable Memory
Page 03h			**Volatile**
230-241	12	Read/Write	Optional Channel Controls
242-251	10	Read/Write	Channel Monitor Masks
252-255	4	Read/Write	Reserved
Page 20h			**Volatile**
140-151	12	Read/Write	Interrupt mask bits for monitored parameters
250	1	Read/Write	Counters reset function

6 Memory Map

6.1 Overview

The memory map is utilized for status, ID, monitoring and control functions.

The map is arranged into a single lower page address space of 128 bytes and multiple upper address pages of 128 bytes each. This structure permits timely access to information in the lower page such as interrupt flags and monitors. Less time-critical entries such as serial ID information and threshold settings are available with the page select function.

Lower Page 00h is required and includes interrupt flags and monitor results arranged to enable single block read operations for time-critical data.

Upper Page 00h is required and provides static module identity and capabilities information.

Page 01h is optional, was used to support SFF-8079, is deprecated as of SFF-8636 Rev 2.10 and is now reserved memory. Implementation of Page 01h is advertised in Page 00h, Byte 195, bit 6.

Page 02h is optional and provides a user read/write space. Implementation of Page 02h is advertised in Page 00h, Byte 195, bit 7.

Page 03h is optional and includes static monitor thresholds, advertising, and various channel controls including interrupt masks. Implementation of Page 03h is advertised in Page 00h, Byte 2, bit 2.

Pages 20h-21h contain support for additional monitored parameters for modules that have PAM4 modulation and/or have optical transmission at multiple wavelengths on a DWDM grid. Page 20h provides the alarms, warnings, masks, parameter values, and configuration. Page 21h provides the alarm and warning thresholds. Implementation of Pages 20h and 21h is advertised in Page 00, Byte 195, bit 0.

Pages 22-7Fh are reserved for future use. Pages 04-1Fh and 80-FFh are for vendor-specific functions.

Writing the value of a non-supported page shall not be accepted by the target. The Page Select byte shall revert to 0h and read/write operations shall be to Upper Page 00h. Because Upper Page 00h is read-only, this scheme prevents the inadvertent corruption of module memory by a host attempting to write to a non-supported location.

Table 6-1 Common Memory Map

From	To	Content	No. of bytes	Type
2-Wire Serial Address 1010000x				
Lower Page 00h				
0	2	ID and Status	3	Read-Only
3	21	Interrupt Flags (Clear on read)	19	Read-Only
22	33	Free Side Device Monitors	12	Read-Only
34	81	Channel Monitors	48	Read-Only
82	85	Reserved	4	Read-Only
86	99	Control	14	Read/Write
100	106	Free Side Interrupt Masks	7	Read/Write
107	110	Free Side Device Properties	4	Read-Only
111	112	Assigned to PCI Express	2	Read/Write
113	117	Free Side Device Properties	5	Read-Only
118	118	Reserved	1	Read/Write
119	122	Optional Password Change	4	Write-Only
123	126	Optional Password Entry	4	Write-Only
127	127	Page Select Byte	1	Read/Write
Upper Page 00h				
128	128	Identifier	1	Read-Only
129	191	Base ID Fields	63	Read-Only
192	223	Extended ID	32	Read-Only
224	255	Vendor Specific ID	32	Read-Only
Page 01h (Optional)				
128	255	Reserved (previously for SFF-8079 support)	128	Read-Only
Page 02h (Optional)				
128	255	User EEPROM Data	128	Read/Write
Page 03h (Optional)				
128	175	Free Side Device Thresholds	48	Read-Only
176	223	Channel Thresholds	48	Read-Only
224	229	Tx EQ, Rx Output and TC Support	6	Read-Only
230	241	Channel Controls	12	Read/Write
242	251	Channel Monitor Masks	10	Read/Write
252	255	Reserved	4	Read/Write
Pages 04h-1Fh (Optional)				
128	255	Vendor Specific	128	Read/Write
Pages 20h-21h (Optional)				
128	255	PAM-4 and WDM Features	128	Read/Write
Pages 22h (Optional)				
128	**255**	High Accuracy Timing	**128**	**Read/Write**
Pages 23h-7Fh (Optional)				
128	255	Reserved	128	Read/Write
Pages 80h-FFh (Optional)				
128	255	Vendor Specific	128	Read/Write

Note: Unless specifically stated otherwise, all informative ID fields must contain accurate data. Using a value of 0 to indicate a field is unspecified (as is common in the SFP definition) is not permitted. Reserved memory locations are to be filled with logic zeros in all bit locations for reserved bytes, and in reserved bit locations for partially specified byte locations.

6.1.1 Required Versus Optional Functionality

The memory map tables contained within this section include columns for passive cables (PC), active cables (AC), active optical cables (AO) and separable modules (SM). Depending on the free side device type, some common memory map parameters are optional. In each column, one of three options is specified: required (R), optional (O) or conditional upon another parameter which is optional (C). Entries with a dash (-) indicate that whether the byte or bit is required is not relevant.

6.2 Lower Page 00h

Lower Page 00h is used to access a variety of measurement, diagnostic and control functions. In addition, a mechanism to select upper memory map pages is provided. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

Table 6-2 Lower Page 00h Memory Map

Byte	Description	Type	PC	AC	AO	SM
0	Identifier (See SFF-8024 Transceiver Management)	Read-Only	R	R	R	R
1-2	Status	Read-Only	See Table 6-3			
3-21	Interrupt Flags	Read-Only	See Table 6-5, Table 6-6 and Table 6-7			
22-33	Free Side Device Monitors	Read-Only	See Table 6-8			
34-81	Channel Monitors	Read-Only	See Table 6-9			
82-85	Reserved	Read-Only	-			
86-99	Control	Read/Write	See Table 6-10			
100-106	Free Side Device and Channel Masks	Read/Write	See Table 6-13			
107-110	Free Side Device Properties	Read-Only	See Table 6-14			
111-112	Assigned for use by PCI Express	Read/Write	See Table 6-14			
113-117	Free Side Device Properties	Read-Only	See Table 6-14			
118	Reserved	Read/Write	-			
119-122	Password Change Entry Area	Write-Only	O	O	O	O
123-126	Password Entry Area	Write-Only	O	O	O	O
127	Page Select Byte	Read/Write	R	R	R	R

6.2.1 Identifier

Page 00h Byte 0 and Page 00h Byte 128 shall contain the same parameter values. See 6.3.1 for parameter description. See document SFF-8024 Transceiver Management section for the definition of valid values.

6.2.2 Status Indicators (Page 00h, Bytes 1-2)

Table 6-3 Status Indicators (Page 00h Bytes 1-2)

Byte	Bit	Name	Description	PC	AC	AO	SM
1	All	Revision Compliance	See Table 6-4.	R	R	R	R
2	7-4	Reserved	Module State Code – reserved for microQSFP MSA.	-	-	-	-
	3	Reserved		-	-	-	-
	2	Flat_mem	Upper memory flat or paged. Bit 2 = 1b: Flat memory (lower and upper pages 00h only), Bit 2 = 0b: Paging (at least upper page 03h implemented), See Page 00h, Byte 195 for additional advertising.	R	R	R	R
	1	IntL	Digital state of the IntL Interrupt output pin. 1 = IntL not asserted, 0 = IntL asserted. Default = 1.	R	R	R	R
	0	Data_Not_Ready	Indicates free-side does not yet have valid monitor data. The bit remains high until valid data can be read at which time the bit goes low.	R	R	R	R

The Data_Not_Ready bit shall be asserted high during free-side device reset, power up reset and prior to a valid suite of monitor readings. Once all monitor readings are valid, the bit is set low until the device is powered down

or reset. Upon completion of power-up reset, the free-side device shall assert the IntL output signal and bit (if supported) low while de-asserting the Data_Not_Ready bit low. The IntL bit will remain asserted until a read is performed of the Data_Not_Ready bit (Byte 2).

Table 6-4 Revision Compliance (Page 00h Byte 1)

Value	Memory Map Version
00h	Revision not specified. Do not use for SFF-8636 rev 2.5 or higher.
01h	SFF-8436 Rev 4.8 or earlier
02h	Includes functionality described in revision 4.8 or earlier of SFF-8436, except that this byte and Bytes 186-189 are as defined in this document
03h	SFF-8636 Rev 1.3 or earlier
04h	SFF-8636 Rev 1.4
05h	SFF-8636 Rev 1.5
06h	SFF-8636 Rev 2.0
07h	SFF-8636 Rev 2.5, 2.6 and 2.7
08h	SFF-8636 Rev 2.8, 2.9 and 2.10
09h	SFF-8636 Rev 2.11
0Ah	SFF-8636 Rev 2.12
0B-FFh	Reserved

6.2.3 Interrupt Flags (Page 00h, Bytes 3-21)

Bytes 3-21 consist of interrupt flags for LOS, Tx Fault, warnings and alarms. The non-asserted state shall be 0b. If an interrupt flag condition is true, the free side shall assert the corresponding flag bit to 1b. The flag bit shall remain set until the fixed-side performs a read operation of the bit or the free side is reset. Flag bits cleared while underlying interrupt condition remains true may be immediately set again by the free side device. During this process, the IntL output signal may be re-asserted if the associated mask bit is not set. These flags may be masked.

Table 6-5 Channel Status Interrupt Flags (Page 00h Bytes 3-5)

Byte	Bit	Name	Description	PC	AC	AO	SM
3	7	L-Tx4 LOS	Latched Tx4 LOS indicator	O	O	O	O
	6	L-Tx3 LOS	Latched Tx3 LOS indicator	O	O	O	O
	5	L-Tx2 LOS	Latched Tx2 LOS indicator	O	O	O	O
	4	L-Tx1 LOS	Latched Tx1 LOS indicator	O	O	O	O
	3	L-Rx4 LOS	Latched Rx4 LOS indicator	O	O	O	O
	2	L-Rx3 LOS	Latched Rx3 LOS indicator	O	O	O	O
	1	L-Rx2 LOS	Latched Rx2 LOS indicator	O	O	O	O
	0	L-Rx1 LOS	Latched Rx1 LOS indicator	O	O	O	O
4	7	L-Tx4 Adapt EQ Fault	Latched Tx4 input Adaptive EQ fault indicator	O	O	O	O
	6	L-Tx3 Adapt EQ Fault	Latched Tx3 input Adaptive EQ fault indicator	O	O	O	O
	5	L-Tx2 Adapt EQ Fault	Latched Tx2 input Adaptive EQ fault indicator	O	O	O	O
	4	L-Tx1 Adapt EQ Fault	Latched Tx1 input Adaptive EQ fault indicator	O	O	O	O
	3	L-Tx4 Fault	Latched Tx4 Transmitter/Laser fault indicator	O	O	O	R
	2	L-Tx3 Fault	Latched Tx3 Transmitter/Laser fault indicator	O	O	O	R
	1	L-Tx2 Fault	Latched Tx2 Transmitter/Laser fault indicator	O	O	O	R
	0	L-Tx1 Fault	Latched Tx1 Transmitter/Laser fault indicator	O	O	O	R
5	7	L-Tx4 LOL	Latched Tx4 CDR LOL indicator	O	O	O	O
	6	L-Tx3 LOL	Latched Tx3 CDR LOL indicator	O	O	O	O
	5	L-Tx2 LOL	Latched Tx2 CDR LOL indicator	O	O	O	O
	4	L-Tx1 LOL	Latched Tx1 CDR LOL indicator	O	O	O	O
	3	L-Rx4 LOL	Latched Rx4 CDR LOL indicator	O	O	O	O
	2	L-Rx3 LOL	Latched Rx3 CDR LOL indicator	O	O	O	O
	1	L-Rx2 LOL	Latched Rx2 CDR LOL indicator	O	O	O	O
	0	L-Rx1 LOL	Latched Rx1 CDR LOL indicator	O	O	O	O

Table 6-6 Free Side Monitor Interrupt Flags (Page 00h Bytes 6-8)

Byte	Bit	Name	Description	PC	AC	AO	SM
6	7	L-Temp High Alarm	Latched high-temperature alarm	O	O	O	R
	6	L-Temp Low Alarm	Latched low-temperature alarm	O	O	O	O
	5	L-Temp High Warning	Latched high-temperature warning	O	O	O	O
	4	L-Temp Low Warning	Latched low-temperature warning	O	O	O	O
	3-2	Reserved		-	-	-	-
	1	TC readiness flag	Asserted (one) after TC has stabilized. Returns to zero when read. Does not reassert until the module is reset or re-enters high power mode from low power mode. See Table 6-25 for the TC Readiness Implemented bit.	O	O	O	O
	0	Initialization complete flag	Asserted (one) after initialization and/or reset has completed. Returns to zero when read. Does not reassert unless reset. See Table 6-25 for the Initialization Complete Implemented bit.	O	O	O	O
7	7	L-Vcc High Alarm	Latched high supply voltage alarm	O	O	O	O
	6	L-Vcc Low Alarm	Latched low supply voltage alarm	O	O	O	O
	5	L-Vcc High Warning	Latched high supply voltage warning	O	O	O	O
	4	L-Vcc Low Warning	Latched low supply voltage warning	O	O	O	O
	3-0	Reserved		-	-	-	-
8	All	Vendor Specific		-	-	-	-

Table 6-7 Channel Monitor Interrupt Flags (Page 00h Bytes 9-21)

Byte	Bit	Name	Description	PC	AC	AO	SM
9	7	L-Rx1 Power High Alarm	Latched Rx1 high power alarm	O	O	O	O
	6	L-Rx1 Power Low Alarm	Latched Rx1 low power alarm	O	O	O	O
	5	L-Rx1 Power High Warning	Latched Rx1 high power warning	O	O	O	O
	4	L-Rx1 Power Low Warning	Latched Rx1 low power warning	O	O	O	O
	3	L-Rx2 Power High Alarm	Latched Rx2 high power alarm	O	O	O	O
	2	L-Rx2 Power Low Alarm	Latched Rx2 low power alarm	O	O	O	O
	1	L-Rx2 Power High Warning	Latched Rx2 high power warning	O	O	O	O
	0	L-Rx2 Power Low Warning	Latched Rx2 low power warning	O	O	O	O
10	7	L-Rx3 Power High Alarm	Latched Rx3 high power alarm	O	O	O	O
	6	L-Rx3 Power Low Alarm	Latched Rx3 low power alarm	O	O	O	O
	5	L-Rx3 Power High Warning	Latched Rx3 high power warning	O	O	O	O
	4	L-Rx3 Power Low Warning	Latched Rx3 low power warning	O	O	O	O
	3	L-Rx4 Power High Alarm	Latched Rx4 high power alarm	O	O	O	O
	2	L-Rx4 Power low Alarm	Latched Rx4 low power alarm	O	O	O	O
	1	L-Rx4 Power high Warning	Latched Rx4 high power warning	O	O	O	O
	0	L-Rx4 Power low warning	Latched Rx4 low power warning	O	O	O	O
11	7	L-Tx1 Bias High Alarm	Latched Tx1 high bias alarm	O	O	O	O
	6	L-Tx1 Bias Low Alarm	Latched Tx1 low bias alarm	O	O	O	O
	5	L-Tx1 Bias high Warning	Latched Tx1 high bias warning	O	O	O	O
	4	L-Tx1 Bias Low Warning	Latched Tx1 low bias warning	O	O	O	O
	3	L-Tx2 Bias High Alarm	Latched Tx2 high bias alarm	O	O	O	O
	2	L-Tx2 Bias Low Alarm	Latched Tx2 low bias alarm	O	O	O	O
	1	L-Tx2 Bias High Warning	Latched Tx2 high bias warning	O	O	O	O
	0	L-Tx2 Bias Low Warning	Latched Tx2 low bias warning	O	O	O	O
12	7	L-Tx3 Bias High Alarm	Latched Tx3 high bias alarm	O	O	O	O
	6	L-Tx3 Bias Low Alarm	Latched Tx3 low bias alarm	O	O	O	O
	5	L-Tx3 Bias High Warning	Latched Tx3 high bias warning	O	O	O	O
	4	L-Tx3 Bias Low Warning	Latched Tx3 low bias warning	O	O	O	O
	3	L-Tx4 Bias High Alarm	Latched Tx4 high bias alarm	O	O	O	O
	2	L-Tx4 Bias Low Alarm	Latched Tx4 low bias alarm	O	O	O	O
	1	L-Tx4 Bias High Warning	Latched Tx4 high bias warning	O	O	O	O
	0	L-Tx4 Bias Low Warning	Latched Tx4 low bias warning	O	O	O	O
13	7	L-Tx1 Power High Alarm	Latched Tx1 high power alarm	O	O	O	O
	6	L-Tx1 Power Low Alarm	Latched Tx1 low power alarm	O	O	O	O
	5	L-Tx1 Power High Warning	Latched Tx1 high power warning	O	O	O	O
	4	L-Tx1 Power Low Warning	Latched Tx1 low power warning	O	O	O	O
	3	L-Tx2 Power High Alarm	Latched Tx2 high power alarm	O	O	O	O
	2	L-Tx2 Power Low Alarm	Latched Tx2 low power alarm	O	O	O	O
	1	L-Tx2 Power High Warning	Latched Tx2 high power warning	O	O	O	O
	0	L-Tx2 Power Low Warning	Latched Tx2 low power warning	O	O	O	O
14	7	L-Tx3 Power High Alarm	Latched Tx3 high power alarm	O	O	O	O
	6	L-Tx3 Power Low Alarm	Latched Tx3 low power alarm	O	O	O	O
	5	L-Tx3 Power High Warning	Latched Tx3 high power warning	O	O	O	O
	4	L-Tx3 Power Low Warning	Latched Tx3 low power warning	O	O	O	O
	3	L-Tx4 Power High Alarm	Latched Tx4 high power alarm	O	O	O	O
	2	L-Tx4 Power Low Alarm	Latched Tx4 low power alarm	O	O	O	O
	1	L-Tx4 Power High Warning	Latched Tx4 high power warning	O	O	O	O
	0	L-Tx4 Power Low Warning	Latched Tx4 low power warning	O	O	O	O
15-16	All	Reserved	Reserved channel monitor flags, set 4	-	-	-	-
17-18	All	Reserved	Reserved channel monitor flags, set 5	-	-	-	-
19-21	All	Vendor Specific		-	-	-	-

6.2.4 Free Side Device Monitors (Page 00h, Bytes 22-33)

Real-time monitoring for the free side device includes internal temperature and supply voltage. In addition there are optional monitors for the optical lanes of separable modules.

The fixed side shall use 2-byte reads to retrieve the 16-bit measurements to guarantee data coherency. The free side device shall prevent the host from acquiring partially updated multi-byte data during a 2-byte read. Clock stretching provides one mechanism to delay the delivery of data until both bytes of a field are updated. The data format may facilitate greater resolution and range than required. Reference of the specific product specification of the free side device or interoperability standard is necessary to determine the measurement accuracy.

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real-time 16-bit data.

Table 6-8 Free Side Monitoring Values (Page 00h Bytes 22-33)

Byte	Bit	Name	Description	PC	AC	AO	SM
22	All	Temperature MSB	Internally measured temperature (MSB)	O	O	O	R
23	All	Temperature LSB	Internally measured temperature (LSB)	O	O	O	R
24-25	All	Reserved		-	-	-	-
26	All	Supply Voltage MSB	Internally measured supply voltage (MSB)	O	O	O	O
27	All	Supply Voltage LSB	Internally measured supply voltage (LSB)	O	O	O	O
28-29	All	Reserved		-	-	-	-
30-33	All	Vendor Specific		-	-	-	-

Internally measured free side device temperatures are represented as a 16-bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of -128 ºC to +127 ºC that is considered valid between -40 ºC and +125 ºC. Temperature accuracy is vendor specific but must be better than +/-3 ºC over the specified operating temperature and voltage. Placement of the temperature sensor is vendor specific.

Internally measured free side device supply voltages are represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 to 65535) with LSB equal to 100 µV, yielding a total measurement range of 0 to +6.55 V. Practical considerations to be defined by free side device manufacturer will tend to limit the actual bounds of the supply voltage measurement. Accuracy is Vendor Specific but must be better than +/-3% of the manufacturer's nominal value over specified operating temperature and voltage.

6.2.5 Channel Monitors (Page 00h, Bytes 34-81)

Real-time channel monitoring for each transmit and receive channel includes optical input power and Tx bias current.

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real-time 16-bit data.

Table 6-9 Channel Monitoring Values (Page 00h Bytes 34-81)

Byte	Bit	Name	Description	PC	AC	AO	SM
34	All	Rx1 Power MSB	Internally measured Rx1 input power	O	O	O	O
35	All	Rx1 Power LSB		O	O	O	O
36	All	Rx2 Power MSB	Internally measured Rx2 input power	O	O	O	O
37	All	Rx2 Power LSB		O	O	O	O
38	All	Rx3 Power MSB	Internally measured Rx3 input power	O	O	O	O
39	All	Rx3 Power LSB		O	O	O	O
40	All	Rx4 Power MSB	Internally measured Rx4 input power	O	O	O	O
41	All	Rx4 Power LSB		O	O	O	O
42	All	Tx1 Bias MSB	Internally measured Tx1 bias	O	O	O	O
43	All	Tx1 Bias LSB		O	O	O	O
44	All	Tx2 Bias MSB	Internally measured Tx2 bias	O	O	O	O
45	All	Tx2 Bias LSB		O	O	O	O
46	All	Tx3 Bias MSB	Internally measured Tx3 bias	O	O	O	O
47	All	Tx3 Bias LSB		O	O	O	O
48	All	Tx4 Bias MSB	Internally measured Tx4 bias	O	O	O	O
49	All	Tx4 Bias LSB		O	O	O	O
50	All	Tx1 Power MSB	Internally measured Tx1 Power	O	O	O	O
51	All	Tx1 Power LSB		O	O	O	O
52	All	Tx2 Power MSB	Internally measured Tx2 Power	O	O	O	O
53	All	Tx2 Power LSB		O	O	O	O
54	All	Tx3 Power MSB	Internally measured Tx3 Power	O	O	O	O
55	All	Tx3 Power LSB		O	O	O	O
56	All	Tx4 Power MSB	Internally measured Tx4 Power	O	O	O	O
57	All	Tx4 Power LSB		O	O	O	O
58-65		Reserved channel monitor set 4		-	-	-	-
66-73		Reserved channel monitor set 5		-	-	-	-
74-81		Vendor Specific		-	-	-	-

Measured Tx bias current is represented in mA as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 to 65535) with LSB equal to 2 µA, yielding a total measurement range of 0 to 131 mA. Accuracy is Vendor Specific but must be better than +/-10% of the manufacturer's nominal value over specified operating temperature and voltage.

Measured Rx received optical power is represented in mW as either an average received power or OMA depending upon how Page 00h Byte 220 bit 3 is set. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 µW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.

Measured Tx optical power is the average power represented in mW. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 0.1 µW, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage.

6.2.6 Control Functions (Page 00h, Bytes 86-99)

Table 6-10 Control Function Bytes (Page 00h Bytes 86-99)

Byte	Bit	Name	Description	PC	AC	AO	SM
86	7-4	Reserved		-	-	-	-
	3	Tx4 Disable	Read/Write bit for software disable of Tx4 *	-	O	O	R
	2	Tx3 Disable	Read/Write bit for software disable of Tx3 *	-	O	O	R
	1	Tx2 Disable	Read/Write bit for software disable of Tx2 *	-	O	O	R
	0	Tx1 Disable	Read/Write bit for software disable of Tx1 *	-	O	O	R
	* For the case of an electrical/optical transceiver, writing '1' disables the laser of the channel						
87	7	Rx4_Rate_select	Software rate select. Rx Channel 4 MSB	-	O	O	O
	6	Rx4_Rate_select	Software rate select. Rx Channel 4 LSB	-	O	O	O
	5	Rx3_Rate_select	Software rate select. Rx Channel 3 MSB	-	O	O	O
	4	Rx3_Rate_select	Software rate select. Rx Channel 3 LSB	-	O	O	O
	3	Rx2_Rate_select	Software rate select. Rx Channel 2 MSB	-	O	O	O
	2	Rx2_Rate_select	Software rate select. Rx Channel 2 LSB	-	O	O	O
	1	Rx1_Rate_select	Software rate select. Rx Channel 1 MSB	-	O	O	O
	0	Rx1_Rate_select	Software rate select. Rx Channel 1 LSB	-	O	O	O
88	7	Tx4_Rate_select	Software rate select. Tx Channel 4 MSB	-	O	O	O
	6	Tx4_Rate_select	Software rate select. Tx Channel 4 LSB	-	O	O	O
	5	Tx3_Rate_select	Software rate select. Tx Channel 3 MSB	-	O	O	O
	4	Tx3_Rate_select	Software rate select. Tx Channel 3 LSB	-	O	O	O
	3	Tx2_Rate_select	Software rate select. Tx Channel 2 MSB	-	O	O	O
	2	Tx2_Rate_select	Software rate select. Tx Channel 2 LSB	-	O	O	O
	1	Tx1_Rate_select	Software rate select. Tx Channel 1 MSB	-	O	O	O
	0	Tx1_Rate_select	Software rate select. Tx Channel 1 LSB	-	O	O	O
89 – 92	All	Reserved	Prior to Rev 2.10 used for SFF-8079 – now deprecated.	-	-	-	-
93	7	SW Reset	Software reset is a self-clearing bit that causes the module to be reset. The effect shall be the same as asserting the ResetL signal for the hold time in the module hardware specification, followed by its deassertion 0b=not in reset 1b=trigger a reset See Page 00h Byte 221 bit 0 for implementation indicator	-	O	O	O
	6-4	Reserved		-	-	-	-
	3	High Power Class Enable (Class 8)	When set to 1 enables Power Class 8 if listed in Byte 129. When cleared to 0, modules with Power Class 8 shall consume less than the power specified by bit 2, but are not required to be fully functional. Refer to Table 6-11. Default = 0.	-	O	O	O
	2	High Power Class Enable (Classes 5-7)	When set to 1 enables Power Classes 5 to 7 if listed in Byte 129. When cleared to 0, modules with Power Classes 5 to 8 shall consume less than 3.5 W, but are not required to be fully functional. Refer to Table 6-11. Default = 0.	-	O	O	O
	1	Power set	For QSFP+/QSFP28: Power set to Low Power Mode (Power Class 1). Default 0. For microQSFP: Redefined as Low Power Mode. Default=1.	-	R	R	R

Byte	Bit	Name	Description	PC	AC	AO	SM
	0	Power override	Override of LPMode/TxDis pad state to allow power mode setting by software. Default 0.	-	R	R	R
94-97	All	Reserved		-	-	-	-
98	7	Tx4_CDR_control	Channel 4 Tx CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	6	Tx3_CDR_control	Channel 3 Tx CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	5	Tx2_CDR_control	Channel 2 Tx CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	4	Tx1_CDR_control	Channel 1 Tx CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	3	Rx4_CDR_control	Channel 4 Rx CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	2	Rx3_CDR_control	Channel 3 Rx CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	1	Rx2_CDR_control	Channel 2 Rx CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
	0	Rx1_CDR_control	Channel 1 Rx CDR Control (1b = CDR on, 0b = CDR off)	-	O	O	O
99	7-2	Reserved		-	-	-	-
	1	LP/TxDis ctrl	LPMode/TxDis input signal control. See SFF-8679 for a complete description. 0b = LPMode 1b = TxDis	-	O	O	O
	0	IntL/LOSL ctrl	IntL/LOSL output signal control. See SFF-8679 for a complete description. 0b = IntL 1b = LOSL	-	O	O	O

For transceivers with CDR capability, setting the CDR to ON engages the internal retiming function. Setting the CDR to OFF enables an internal bypassing mode, which directs traffic around the internal CDR. The two most common reasons to turn a CDR off (i.e. internally bypass it) are to run at rates not supported by a particular CDR or to save the thermal power in applications where CDR jitter mitigation is not required. Jitter specifications of the high-speed interfaces are outside the scope of this specification.

QSFP+ and QSFP28 modules have the LPMode input signal (see SFF-8679) that can be used by the host system to force the module into Low Power Mode. Low Power Mode for those modules is defined as maximum power consumption of 1.5W. If the LPMode input signal is pulled low by the host system, the module is then capable of entering High Power Mode. The maximum power consumption in High Power Mode depends on the module Power Class as advertised in the Extended Identifier (see 6.3.2), Page 00h, byte 129, bits 1-0 and 7-6.

The operation of the LPMode input signal can be overridden by the host writing a '1' to byte 93, bit 0. In that case, the function of the LPMode input signal is replaced by byte 93, bit 1.

SFF-8436 has 4 power classes from 1.5 to 3.5 W. Only bits 7-6 are used to define those power classes. At revision 1.9 of this specification, 3 new higher power classes, 4.0 W, 4.5 W, and 5.0 W were added. These power classes, designated power classes 5, 6 and 7, are designated using bits 1-0 of the Extended Identifier byte, page 00h byte 129. In order to protect legacy host systems designed to support only the original 4 power classes, the High Power Class Enable control was defined at byte 93, bit 2. Modules in power classes 5, 6, 7 or 8 are required to limit power consumption to no more than a power class 4 module if the High Power Class Enable, byte 93 bit 2 control is not set. They are not required to be functional in this situation.

Starting with SFF-8636 Rev 2.10, a new Power Class 8 is introduced. It is enabled using byte 93, bit 3 and is advertised using upper page 00h, byte 129, bit 5. Power Class 8 modules use byte 107 to advertise the maximum power consumption of the module. For Power Class 8 advertising see page 00h, byte 129. Modules in power class 8 are required to limit power consumption to no more than a power class 7 module if the High Power Class Enable, byte 93 bit 3 control is not set. They are not required to be functional in this situation.

A truth table for the power controls in byte 93 bits 0, 1, 2 and 3, is shown in Table 6-11.

Power class limits and controls for microQSFP modules are different from the description here. Refer to the MSA specification for details.

Table 6-11 Truth table for enabling power classes (Page 00h Byte 93)

(The maximum consumption limits in this table are based on SFF-8679 for QSFP modules).

LPMode (*)	Power Override B93 bit 0	Power Set B93 bit 1	High Pwr Class Enable B93 bit2	High Pwr Class Enable B93 bit3	Enabled Power Classes
0	0	X	0	0	1 to 4
0	0	X	1	0	1 to 7
0	0	X	1	1	1 to 8
0	0	X	0	1	8
1	0	X	X	X	1
X	1	0	0	0	1 to 4
X	1	0	1	0	1 to 7
X	1	0	1	1	1 to 8
X	1	0	0	1	8
X	1	1	X	X	1

(*) LPMode is a signal carried on a dual-purpose contact. When the dual-purpose contact is not programmed as LPMode, the module behaves as though LPMode = 0. Refer to SFF-8679 section 5.3.3 for details.

6.2.7 Rate Select

Rate Select is an optional control used to limit the receiver bandwidth for compatibility with multiple signaling rates. In addition, rate selection allows the transmitter and receiver to be tuned for specific rates. For more information, see Appendix A Rate Select and Configuration for Multi-rate Modules (Informative)

The free side device shall implement one of two options:

a) Provide no support for rate selection
b) Rate selection using extended rate select

6.2.7.1 No Rate Selection Support

When no rate selection is supported, (Page 00h Byte 221 bits 2 and 3) have a value of 0 and Options (Page 00h Byte 195 bit 5) has a value of 0. Lack of implementation does not indicate a lack of simultaneous compliance with multiple standard rates. See 6.3.4 for the description of how compliance with particular standards should be determined.

6.2.7.2 Extended Rate Selection

When Page 00h Byte 195 bit 5 is 1 and Rate Select declaration bits (Page 00h Byte 221 bits 2 and 3) have the values of 0 and 1 respectively and at least one of the bits in the Extended Rate Compliance byte (Page 00h Byte 141) has a value of one, the free side device supports extended rate select. For extended rate selection, two bits are assigned to each receiver in Byte 87 (Rxn_Rate_Select) and two bits for each transmitter in Byte 88 (Txn_Rate_Select) to specify up to four rates. See Table 6-12 for the functionality when Byte 141 bits 0-1 are set. All other values of the Extended Rate Compliance byte are reserved.

Table 6-12 xN_Rate_Select with Extended Rate Selection

xN_Rate_Select (MSB Value)	xN_Rate_Select (LSB Value)	Description
Version 1 - Page 00h Byte 141 Bit 0 = 1		
0	0	Optimized for signaling rates less than 2.2 GBd
0	1	Optimized for signaling rates from 2.2 up to 6.6 GBd
1	0	Optimized for 6.6 GBd signaling rates and above
1	1	Reserved
Version 2 - Page 00h Byte 141 Bit 1 = 1		
0	0	Optimized for signaling rates less than 12 GBd
0	1	Optimized for signaling rates from 12 up to 24 GBd
1	0	Optimized for signaling rates from 24 up to 26 GBd
1	1	Optimized for 26 GBd signaling rates and above

6.2.8 Free Side Device Indicators and Channel Masks (Page 00h, Bytes 100-106)

The fixed side may control which flags result in a hardware interrupt by setting high individual bits from a set of masking bits in Page 00h Bytes 100-104 for free side device flags, and Page 03h Bytes 242-251 for channel flags. See Table 6-13 and Table 6-35. A 1 value in a masking bit prevents the assertion of the hardware interrupt pin, if one exists, by the corresponding latched flag bit. Masking bits are volatile and startup with all unmasked (masking bits 0).

The mask bits may be used to prevent continued interruption from on-going conditions, which would otherwise continually reassert the hardware interrupt pin. A mask bit is allocated for each flag bit.

Table 6-13 Hardware Interrupt Pin Masking Bits (Page 00h Bytes 100-106)

Byte	Bit	Name	Description	PC	AC	AO	SM
100	7	M-Tx4 LOS Mask	Masking bit for Tx4 LOS indicator	C	C	C	C
	6	M-Tx3 LOS Mask	Masking bit for Tx3 LOS indicator	C	C	C	C
	5	M-Tx2 LOS Mask	Masking bit for Tx2 LOS indicator	C	C	C	C
	4	M-Tx1 LOS Mask	Masking bit for Tx1 LOS indicator	C	C	C	C
	3	M-Rx4 LOS Mask	Masking bit for Rx4 LOS indicator	C	C	C	C
	2	M-Rx3 LOS Mask	Masking bit for Rx3 LOS indicator	C	C	C	C
	1	M-Rx2 LOS Mask	Masking bit for Rx2 LOS indicator	C	C	C	C
	0	M-Rx1 LOS Mask	Masking bit for Rx1 LOS indicator	C	C	C	C
101	7	M-Tx4 Adapt EQ Fault Mask	Masking bit for Tx4 Adaptive EQ fault	C	C	C	C
	6	M-Tx3 Adapt EQ Fault Mask	Masking bit for Tx3 Adaptive EQ fault	C	C	C	C
	5	M-Tx2 Adapt EQ Fault Mask	Masking bit for Tx2 Adaptive EQ fault	C	C	C	C
	4	M-Tx1 Adapt EQ Fault Mask	Masking bit for Tx1 Adaptive EQ fault	C	C	C	C
	3	M-Tx4 Transmitter Fault Mask	Masking bit for Tx4 Transmitter fault	C	C	C	R
	2	M-Tx3 Transmitter Fault Mask	Masking bit for Tx3 Transmitter fault	C	C	C	R
	1	M-Tx2 Transmitter Fault Mask	Masking bit for Tx2 Transmitter fault	C	C	C	R
	0	M-Tx1 Transmitter Fault Mask	Masking bit for Tx1 Transmitter fault	C	C	C	R
102	7	M-Tx4 CDR LOL Mask	Masking bit for Tx4 CDR Loss of Lock	C	C	C	C
	6	M-Tx3 CDR LOL Mask	Masking bit for Tx3 CDR Loss of Lock	C	C	C	C
	5	M-Tx2 CDR LOL Mask	Masking bit for Tx2 CDR Loss of Lock	C	C	C	C
	4	M-Tx1 CDR LOL Mask	Masking bit for Tx1 CDR Loss of Lock	C	C	C	C
	3	M-Rx4 CDR LOL Mask	Masking bit for Rx4 CDR Loss of Lock	C	C	C	C
	2	M-Rx3 CDR LOL Mask	Masking bit for Rx3 CDR Loss of Lock	C	C	C	C
	1	M-Rx2 CDR LOL Mask	Masking bit for Rx2 CDR Loss of Lock	C	C	C	C
	0	M-Rx1 CDR LOL Mask	Masking bit for Rx1 CDR Loss of Lock	C	C	C	C
103	7	M-Temp High Alarm	Masking bit for high-temperature alarm	C	C	C	C
	6	M-Temp Low Alarm	Masking bit for low-temperature alarm	C	C	C	C
	5	M- Temp High Warning	Masking bit for high-temperature warning	C	C	C	C
	4	M-Temp Low Warning	Masking bit for low-temperature warning	C	C	C	C
	3-2	Reserved		-	-	-	-
	1	M-TC readiness flag	Masking bit for TC readiness flag	C	C	C	C
	0	Reserved		-	-	-	-
104	7	M-Vcc High alarm	Masking bit for Vcc high alarm	C	C	C	C
	6	M-Vcc Low alarm	Masking bit for Vcc low alarm	C	C	C	C
	5	M-Vcc High Warning	Masking bit for Vcc high warning	C	C	C	C

Byte	Bit	Name	Description	PC	AC	AO	SM
	4	M-Vcc Low Warning	Masking bit for Vcc low warning	C	C	C	C
	3-0	Reserved		-	-	-	-
105-106	All	Vendor Specific		-	-	-	-

6.2.9 Free Side Device Properties (Page 00h, Bytes 107-117)

Byte 107 indicates the maximum module power consumption in 0.1 W increments. This field shall be populated if the module advertises Power Class 8 in Page 00h Byte 129 (see Table 6-16). However, non-Power Class 8 modules may also report their maximum module power consumption in this field. Modules that do not report their maximum power consumption shall populate this field with 00h.

The unsigned 16-bit value in Bytes 108-109 indicates the propagation delay of the non-separable free side device. Byte 108 bit 7 is the most significant bit and Byte 109 bit 0 is the least significant. Each unit of the combined value corresponds to 10 ns with fractional values rounded up to the next unit.

Byte 110 bits 7-4 specify the free-side device power consumption levels below 1.5 W. A value of 0000 shall indicate that a power consumption limit below 1.5 W is not available. A value of 0001 shall indicate the free-side device shall consume no more than 1 W, 0010 indicates no more than 0.75 W and 0011 indicates no more than 0.5 W.

A value of 1 in Byte 110 bit 3 shall indicate that both ends of the free-side device comply with the SFF-8636 specification. A value of 0 shall be utilized for all other cases including the use of other management interfaces specifications and separable applications where the free-side device ends and media can be physically separated from each other. Byte 110 bits 2-0 indicate that the free-side device can operate properly from less than nominal 3.3 V on the Vcc pins. A value of 000 indicates the feature is disabled. The free-side device shall operate properly from nominal 2.5 V with a value of 001 and nominal 1.8 V with a value of 010.

The use of Bytes 111-112 is not defined in this specification.

Byte 113 bits 3-0 specify which channels of the free side device at the near end are implemented. A value of 0 indicates that the channel is implemented and a value of 1 indicates that the channel is not implemented.

Byte 113 bits 6-4 are used to indicate what type of device(s) are implemented at the far end(s) of a cable or module. A separable free side device or a device that does not specify the far end implementation is coded 000.

The ModSelL wait time fields define the minimum supported setup time for the ModSelL signal, defined as the elapsed time between host assertion of ModSelL and the start of a two-wire serial bus transaction and the required delay from completion of a two-wire serial bus transaction until the host can de-assert the ModSelL signal. For example, if the module wait time is 1.6 ms, the mantissa field (bits 4-0) will be 11001b and the exponent field (bits 7-5) will be 110b indicating six binary zeroes after the 11001b, for a net result of 11001000000b, or 1600 decimal.

Host implementers should note that the host must use the worst-case ModSelL wait time for all modules on the same shared two-wire serial bus. For example, when a new module is hot swapped onto the shared serial bus, the host must use the wait time specified in the hardware specification for all modules on that serial bus, until the supported ModSelL wait time for that new module can be identified.

The secondary extended specification compliance code in Byte 116 identifies an electrical or optical interface that is not included in Table 6-17 Specification Compliance Codes, and is an additional supported specification relative to Page 00h, Byte 192 (see 6.3.23).

An additional sub-type identifier in Byte 117 bits 7-4 can be used to provide information to the host on mechanical and thermal implementation. Refer to SFF-8024 for possible values and the hardware specification for more information on the listed sub-types. When applicable, the Fiber Face Type, byte 117, bits 1-0 are used to identify the fiber face type for the specific connector type. The values are listed in SFF-8024.

Table 6-14 Free Side Device Properties (Page 00h Bytes 107-116)

Byte	Bit	Name	Description	PC	AC	AO	SM
107	All	Max Power Consumption	Maximum power consumption of module. Unsigned integer with LSB = 0.1 W.	O	O	O	O
108	All	Propagation Delay MSB	The most significant byte of propagation delay	R	R	R	O
109	All	Propagation Delay LSB	The least significant byte of propagation delay	R	R	R	O
110	7-4	Advanced Low Power Mode	The code indicates maximum power consumption less than 1.5 W. For SAS applications refer to SFF-8449. 0000 1.5W or higher 0001 no more than 1 W 0010 no more than 0.75 W 0011 no more than 0.5 W	R	R	R	O
	3	Far Side Managed	A value of 1 indicates that the far end is managed and complies with SFF-8636.	R	R	R	O
	2-0	Min Operating Voltage	The code indicates nominal supply voltages lower than 3.3 V. For SAS applications refer to SFF-8449. 000 3.3 V 001 2.5 V 010 1.8 V	R	R	R	O
111-112	All	Assigned for use by PCI Express	Used for: - The PCI Express External Cable Specification - The PCI Express OCuLink Specification	-	-	-	-
113	7	Reserved		-	-	-	-
	6-4	Far-End Implementation	=000 Far end is unspecified =001 Cable with single far-end with 4 channels implemented, or separable module with a 4-channel connector =010 Cable with single far-end with 2 channels implemented, or separable module with a 2-channel connector =011 Cable with single far-end with 1 channel implemented, or separable module with a 1-channel connector =100 4 far-ends with 1 channel implemented in each (i.e. 4x1 break out) =101 2 far-ends with 2 channels implemented in each (i.e. 2x2 break out) =110 2 far-ends with 1 channel implemented in each (i.e. 2x1 break out)	R	R	R	O
	3-0	Near-End Implementation	Bit 0 =0 Channel 1 implemented =1 Channel 1 not implemented Bit 1 =0 Channel 2 implemented =1 Channel 2 not implemented Bit 2 =0 Channel 3 implemented =1 Channel 3 not implemented Bit 3 =0 Channel 4 implemented =1 Channel 4 not implemented	R	R	R	O
114	7-4	Tx_TurnOn MaxDuration	Tx_TurnOn_MaxDuration for microQSFP MSA. 0000b=Not implemented.	R	R	R	R
	3-0	DataPathInit MaxDuration	DataPathInit_MaxDuration for microQSFP MSA. 0000b=Not implemented.	R	R	R	R

Byte	Bit	Name	Description	PC	AC	AO	SM
115	7-5	ModSelL wait time exponent	The ModSelL wait time is the mantissa x 2^exponent expressed in microseconds. In other words, the mantissa field is shifted up by the number of bits indicated in the exponent field (time = mantissa << exponent). A value of 00h indicates these fields are not implemented.	O	O	O	O
	4-0	ModSelL wait time mantissa					
116	All	Secondary Extended Spec Compliance	Secondary Extended Specification Compliance Codes (See SFF-8024 Transceiver Management)	R	R	R	R
117	7-4	Transceiver Sub-type	Transceiver Sub-type code (See SFF-8024 Transceiver Management)	R	R	R	R
	3-2	Reserved		R	R	R	R
	1-0	Fiber Face Type	Fiber Face Type code (See SFF-8024 Transceiver Management)	R	R	R	R

6.2.10 Password Entry and Change (Page 00h, Bytes 119-126)

Bytes 119-126 are reserved for an optional password entry function. The Password entry bytes are write-only and will be retained until power down, reset, or rewritten by fixed side. This function may be used to control read/write access to Vendor Specific Page 02h. Additionally, free side device vendors may use this function to implement write protection of Serial ID and other read-only information. Passwords may be supplied to and used by fixed side system manufacturers to limit write access in the User EEPROM Page 02h.

Password access shall not be required to access free side device data in the lower memory Page 00h or in Upper Page 00h, 02h, and 03h. Note that multiple manufacturer passwords may be defined to allow selective access to read or write to various sections of memory as allowed above.

Fixed side manufacturer and free side device manufacturer passwords shall be distinguished by the high order bit (bit 7, Byte 123). All fixed side manufacturer passwords shall fall in the range of 00000000h to 7FFFFFFFh and all free side device manufacturer passwords in the range of 80000000h to FFFFFFFFh. Fixed side system manufacturer passwords shall be initially set to 00001011h in new free side devices.

Fixed side system manufacturer passwords may be changed by writing a new password in Bytes 119-122 when the correct current fixed side manufacture password has been entered in 123-126, with the high order bit being ignored and forced to a value of 0 in the new password. The password entry field shall be set to 00000000h on power-up and reset.

6.2.11 Page Select (Page 00h, Byte 127)

Byte 127 is used to select the upper page. A value of 00h indicates upper memory Page 00h is mapped to Bytes 128-255 and a value of 01h indicates that upper Page 01h if available is mapped to Bytes 128-255. Similarly, values of 02h, 03h, 20h, and 21h indicate which upper page is mapped to Bytes 128-255. If the host attempts to write a page select value which is not supported in a particular module, the Page Select byte will revert to 00h.

6.3 Upper Page 00h

Upper Page 00h consists of the Serial ID and is used for read-only identification information.

Table 6-15 Upper Page 00h Memory Map

Byte	Size	Name	Description	PC	AC	AO	SM
128	1	Identifier	Identifier Type of free side device (See SFF-8024 Transceiver Management)	R	R	R	R
129	1	Ext. Identifier	Extended Identifier of free side device. Includes power classes, CLEI codes, CDR capability (See Table 6-16)	R	R	R	R
130	1	Connector Type	Code for media connector type (See SFF-8024 Transceiver Management)	R	R	R	R
131-138	8	Specification Compliance	Code for electronic or optical compatibility (See Table 6-17)	R	R	R	R
139	1	Encoding	Code for serial encoding algorithm. (See SFF-8024 Transceiver Management)	R	R	R	R
140	1	Signaling rate, nominal	Nominal signaling rate, units of 100 MBd. For rate > 25.4 GBd, set this to FFh and use Byte 222.	R	R	R	R
141	1	Extended Rate Select Compliance	Tags for extended rate select compliance. See Table 6-18.	R	R	R	R
142	1	Length (SMF)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for SMF fiber in km [*]. A value of 1 shall be used for reaches from 0 to 1 km.	R	R	R	R
143	1	Length (OM3 50 um)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for EBW 50/125 um fiber (OM3), units of 2 m [*]	R	R	R	R
144	1	Length (OM2 50 um)	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for 50/125 um fiber (OM2), units of 1 m [*]	R	R	R	R
145	1	Length (OM1 62.5 um) or Copper Cable Attenuation	Link length supported at the signaling rate in byte 140 or page 00h byte 222, for 62.5/125 um fiber (OM1), units of 1 m [*], or copper cable attenuation in dB at 25.78 GHz.	R	R	R	R
146	1	Length (passive copper or active cable or OM4 50 um)	Length of passive or active cable assembly (units of 1 m) or link length supported at the signaling rate in byte 140 or page 00h byte 222, for OM4 50/125 um fiber (units of 2 m) as indicated by Byte 147. See 6.3.12.	R	R	R	R
147	1	Device technology	Device technology (Table 6-19 and Table 6-20).	R	R	R	R
148-163	16	Vendor name	Free side device vendor name (ASCII)	R	R	R	R
164	1	Extended Module	Extended Module codes for InfiniBand (See Table 6-21)	R	R	R	R
165-167	3	Vendor OUI	Free side device vendor IEEE company ID	R	R	R	R
168-183	16	Vendor PN	Part number provided by free side device vendor(ASCII)	R	R	R	R
184-185	2	Vendor rev	Revision level for part number provided by the vendor(ASCII)	R	R	R	R

Byte	Size	Name	Description	PC	AC	AO	SM
186-187	2	Wavelength or Copper Cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5 GHz (Byte 186) and 5.0 GHz (Byte 187)	R	R	R	R
188-189	2	Wavelength tolerance or Copper Cable Attenuation	The range of laser wavelength (+/- value) from nominal wavelength. (wavelength Tol. =value/200 in nm) or copper cable attenuation in dB at 7.0 GHz (Byte 188) and 12.9 GHz (Byte 189)	R	R	R	R
190	1	Max case temp.	Maximum case temperature	R	R	R	R
191	1	CC_BASE	Check code for base ID fields (Bytes 128-190)	R	R	R	R
192	1	Link codes	Extended Specification Compliance Codes (See SFF-8024)	R	R	R	R
193-195	3	Options	Optional features implemented. See Table 6-22.	R	R	R	R
196-211	16	Vendor SN	Serial number provided by vendor (ASCII)	R	R	R	R
212-219	8	Date Code	Vendor's manufacturing date code	R	R	R	R
220	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the free side device. Bit 1,0 Reserved. See Table 6-24.	R	R	R	R
221	1	Enhanced Options	Indicates which optional enhanced features are implemented in the free side device. See Table 6-25.	R	R	R	R
222	1	Baud Rate, nominal	Nominal baud rate per channel, units of 250 MBd. Complements Byte 140. See Table 6-26.	R	R	R	R
223	1	CC_EXT	Check code for the Extended ID Fields (Bytes 192-222)	R	R	R	R
224-255	32	Vendor Specific	Vendor Specific EEPROM	-	-	-	-
* A value of zero means that the free side device does not support the specified technology or that the length information must be determined from the free side device technology.							

6.3.1 Identifier (00h 128)

The Identifier Values at Byte 128 specify the physical device described by the serial information. This value shall be included in the serial data. These values are maintained in the Transceiver Management section of SFF-8024.

6.3.2 Extended Identifier (00h 129)

The extended identifier provides additional information about the free side device. For example, the identifier indicates if the free side device contains a CDR function and identifies the power consumption class it belongs to.

Power classes 5, 6 and 7 were added in rev 1.9 of this specification to enable modules requiring more than 3.5W of consumption. However, legacy systems were designed for a maximum of 3.5W. To ensure that those systems were not harmed by power classes 5, 6 or 7 a lockout feature was added in Byte 93 bit 2 to enable high power mode for those modules. A legacy system does not know about Byte 129 bits 1-0 or about Byte 93 bit 2. New systems know about both and can configure power class 5 through 7 support accordingly. The power class identifiers specify maximum power consumption over operating conditions and life with all supported settings set to worst case values.

Power Class 8 is introduced by rev 2.10 of this specification. Class 8 modules advertise a fine-grained value of power consumption in Page 00h, Byte 107. See SFF-8679 for QSFP+/QSFP28 power consumption values. If byte 129, bit 5 is set a module may also indicate one of the other power classes using bits 7-6 and 1-0, if it complies with that class. It should set bits 7-6 and 1-0 to all 1's if the maximum power consumption is greater than or equal to Power Class 7.

Table 6-16 Extended Identifier Values (Page 00h Byte 129)

Bit	Device Type
7-6	00: Power Class 1 (1.5 W max.)
	01: Power Class 2 (2.0 W max.)
	10: Power Class 3 (2.5 W max.)
	11: Power Class 4 (3.5 W max.) and Power Classes 5, 6 or 7
5	Power Class 8 implemented (Max power declared in byte 107)
4	0: No CLEI code present in Page 02h
	1: CLEI code present in Page 02h
3	0: No CDR in Tx, 1: CDR present in Tx
2	0: No CDR in Rx, 1: CDR present in Rx
1-0	00: Power Classes 1 to 4
	01: Power Class 5 (4.0 W max.) See Byte 93 bit 2 to enable.
	10: Power Class 6 (4.5 W max.) See Byte 93 bit 2 to enable.
	11: Power Class 7 (5.0 W max.) See Byte 93 bit 2 to enable.

6.3.3 Connector Type (00h 130)

The Connector Type entry at Page 00H Byte 130 indicates the connector type for the separable portion of the free side device (see 4.3.2). This value shall be included in the serial data. These values are maintained in the Transceiver Management section of SFF-8024.

6.3.4 Specification Compliance (00h 131-138)

The bit significant indicators define the electronic or optical interfaces that are supported by the free side device. At least one bit shall be set in this field, and if more than one bit is applicable (as in the case of Fibre Channel), all shall be set accordingly. Except where stated, the interface supports 4 lanes of the standard.

Table 6-17 Specification Compliance Codes (Page 00h Bytes 131-138)

Byte	Bit	Module Capability
10/40G/100G Ethernet Compliance Codes		
131	7	Extended: See section 6.3.23. The Extended Specification Compliance Codes are maintained in the Transceiver Management section of SFF-8024.
	6	10GBASE-LRM
	5	10GBASE-LR
	4	10GBASE-SR
	3	40GBASE-CR4
	2	40GBASE-SR4
	1	40GBASE-LR4
	0	40G Active Cable (XLPPI)
SONET Compliance Codes		
132	7-3	Reserved
	2	OC 48, long reach
	1	OC 48, intermediate reach
	0	OC 48 short reach
SAS/SATA Compliance Codes		
133	7	SAS 24.0 Gbps
	6	SAS 12.0 Gbps
	5	SAS 6.0 Gbps
	4	SAS 3.0 Gbps
	3-0	Reserved
Gigabit Ethernet Compliance Codes		
134	7-4	Reserved
	3	1000BASE-T
	2	1000BASE-CX
	1	1000BASE-LX
	0	1000BASE-SX
Fibre Channel Link Length		
135	7	Very long distance (V)
	6	Short distance (S)
	5	Intermediate distance (I)
	4	Long distance (L)
	3	Medium (M)
Fibre Channel Transmitter Technology		
135	2	Reserved
	1	Longwave laser (LC)
	0	Electrical inter-enclosure (EL)
136	7	Electrical intra-enclosure
	6	Shortwave laser w/o OFC (SN)
	5	Shortwave laser w OFC (SL)
	4	Longwave Laser (LL)
	3-0	Reserved
Fibre Channel Transmission Media		
137	7	Twin Axial Pair (TW)
	6	Shielded Twisted Pair (TP)

Byte	Bit	Module Capability
	5	Miniature Coax (MI)
	4	Video Coax (TV)
	3	Multi-mode 62.5 um (M6)
	2	Multi-mode 50 um (M5)
	1	Multi-mode 50 um (OM3)
	0	Single Mode (SM)
Fibre Channel Speed		
138	7	1200 MBps (per channel)
	6	800 MBps
	5	1600 MBps (per channel)
	4	400 MBps
	3	3200 MBps (per channel)
	2	200 MBps
	1	Extended: See section 6.3.23. The Extended Specification Compliance Codes are maintained in the Transceiver Management section of SFF-8024.
	0	100 MBps

6.3.5 Encoding (00h 139)

The Encoding Values at Page 00h Byte 139 indicate the serial encoding mechanism for the high-speed serial interface. The value shall be contained in the serial data. These values are maintained in the Transceiver Management section of SFF-8024.

6.3.6 Nominal Signaling Rate (00h 140)

The nominal signaling rate per channel (BR, nominal) is specified in units of 100 Megabaud in byte 140 and in units of 250 Megabaud in byte 222. The baud rate includes overhead necessary to encode and delimit the signal as well as symbols carrying data information. A value of 0 indicates the baud rate is not specified and must be determined from the module technology. A value of FFh in byte 140 means the baud rate exceeds 25.4 GBd and byte 222 must be used to determine nominal baud rate. The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value (byte 139).

6.3.7 Extended Rate Select Compliance (00h 141)

The Extended Rate Select Compliance field is used to allow a single free side device the flexibility to comply with single or multiple Extended Rate Select definitions. A definition is indicated by the presence of a '1' in the specified bit. If exclusive, non-overlapping definitions are used, Page 00h Byte 141 will allow compliance to 8 distinct multi-rate definitions.

Table 6-18 Extended Rate Select Compliance Tag Assignment (Page 00h Byte 141)

Byte	Bits	Description
141	7-2	Reserved
	1-0	Rate Select Version. This functionality is different from SFF-8472 and SFF-8431. 10b: Rate Select Version 2 01b: Rate Select Version 1 00b, 11b: Reserved
Note: See 6.2.7 for further details of the use of this field		

6.3.8 Length (Standard SM Fiber) -km (00h 142)

In addition to EEPROM data from original GBIC definition, this value specifies the link length that is supported by a separable module free side device while operating in compliance with the applicable standards using single mode fiber. Supported link length is as specified in INF-8074. The value is in units of kilometers. A value of zero means

that the free side device does not support single mode fiber or that the length information must be determined from the free side device technology. For all cable assemblies, including active optical cables, the value shall be zero.

6.3.9 Length (OM3) (00h 143)

This value specifies the link length that is supported by a separable module free side device while operating in compliance with the applicable standards using 2000 MHz*km (850 nm) extended bandwidth 50-micron multi-mode fiber. The value is in units of 2 meters. A value of zero means that the free side device does not support OM3 fiber or that the length information must be determined from the free side device technology. For all cable assemblies, including active optical cables, the value shall be zero.

6.3.10 Length (OM2) (00h 144)

This value specifies the link length that is supported by a separable module free side device while operating in compliance with the applicable standards using 500 MHz*km (850 nm and 1310 nm) 50-micron multi-mode fiber. The value is in units of 1 meter. A value of zero means that the free side device does not support OM2 fiber or that the length information must be determined from the free side device technology. For all cable assemblies, including active optical cables, the value shall be zero.

6.3.11 Length (OM1) or Copper Cable Attenuation (00h 145)

This value specifies the link length that is supported by a separable module free side device while operating in compliance with the applicable standards using 200 MHz*km (850 nm) and 500 MHz*km (1310 nm) 62.5-micron multi-mode fiber. The value is in units of 1 meter. A value of zero means that the free side device does not support OM1 fiber or that the length information must be determined from the free side device technology.

For copper cable assemblies, where page 00h byte 147 bits 7-4 are 1010b, 1011b, 1101b or 1111b, this register is used to record the cable attenuation (or apparent attenuation from the near end of the cable for active cables) at 25.78 GHz in units of 1 dB. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable. For active optical cables or copper cables not listed in this paragraph, the value shall be zero.

6.3.12 Length: Cable Assembly or Optical Fiber (OM4) (00h 146)

If a separable module (as indicated by a value other than 23h in Byte 130) free side device transmitter technology is 850nm VCSEL (indicated by Byte 147 bits 7-4) then this value specifies the link length supported while operating in compliance with the applicable standards using 4700 MHz*km (850nm) extended bandwidth 50-micron multi-mode fiber (OM4). The value is in units of 2 meters.

Otherwise, this value specifies the link length of a Cable assembly (copper or AOC) in units of 1 meter. Link length is as specified in the INF-8074. Link lengths less than 1 meter shall indicate 1 meter.

A value of zero means the free side device is not a cable assembly or the length information must be determined from the separable free side device technology. A value of 255 means a separable module VCSEL free side device supports a link length greater than 508 meters or the cable assembly has a link length greater than 254 meters.

6.3.13 Device Technology (00h 147)

Aspects of the device or cable technology used are described by the Device Technology byte. An active optical cable may be distinguished from a separable module by reading Byte 130 (Connector Type).

Table 6-19 Device Technology (Page 00h Byte 147)

Bits	Description
7-4	Transmitter technology (See Table 6-20)
3	0: No wavelength control 1: Active wavelength control
2	0: Uncooled transmitter device 1: Cooled transmitter
1	0: Pin detector 1: APD detector
0	0: Transmitter not tunable 1: Transmitter tunable

Table 6-20 Transmitter Technology (Page 00h Byte 147 Bits 7-4)

Value	Description
0000b	850 nm VCSEL
0001b	1310 nm VCSEL
0010b	1550 nm VCSEL
0011b	1310 nm FP
0100b	1310 nm DFB
0101b	1550 nm DFB
0110b	1310 nm EML
0111b	1550 nm EML
1000b	Other / Undefined
1001b	1490 nm DFB
1010b	Copper cable unequalized
1011b	Copper cable passive equalized
1100b	Copper cable, near and far end limiting active equalizers
1101b	Copper cable, far end limiting active equalizers
1110b	Copper cable, near end limiting active equalizers
1111b	Copper cable, linear active equalizers

6.3.14 Vendor Name (00h 148-163)

The vendor name is a 16-character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

6.3.15 Extended Module Codes (00h 164)

The Extended Module Codes define the electronic or optical interfaces for InfiniBand that are supported by the free side device.

Table 6-21 Extended Module Code Values (Page 00h Byte 164)

Byte	Bit	Module Code
InfiniBand Data Rate codes		
164	7-6	Reserved
	5	HDR
	4	EDR
	3	FDR
	2	QDR
	1	DDR
	0	SDR

6.3.16 Vendor Organizationally Unique Identifier Field (00h 165-167)

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

6.3.17 Vendor Part Number (00h 168-183)

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

6.3.18 Vendor Revision Number (00h 184-185)

The vendor revision number (vendor rev) is a 2-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the field indicates that the vendor Rev is unspecified.

6.3.19 Wavelength or Copper Cable Attenuation (00h 186-187)

For optical free side devices, this parameter identifies the nominal transmitter output wavelength at room temperature. This parameter is a 16-bit hex value with Byte 186 as high order byte and Byte 187 as low order byte. The laser wavelength is equal to the 16-bit integer value divided by 20 in nm (units of 0.05 nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected DWDM applications. For an accurate representation of controlled wavelength applications, this value should represent the center of the guaranteed wavelength range.

If the free side device is identified as copper cable these registers are used to define the cable attenuation. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

Byte 186 (00-FFh) is the copper cable attenuation at 2.5 GHz in units of 1 dB.

Byte 187 (00-FFh) is the copper cable attenuation at 5.0 GHz in units of 1 dB.

6.3.20 Wavelength Tolerance or Copper Cable Attenuation (00h 188-189)

The guaranteed tolerance of transmitter output wavelength under all normal operating conditions. For copper cable assemblies, the value is zero. This parameter is a 16-bit value with Byte 188 as high order byte and Byte 189 as low order byte. The laser wavelength is equal to the 16-bit integer value divided by 200 in nm (units of 0.005 nm). Thus, the following two examples:

Example 1:

10GBASE-LR Wavelength Range = 1260 to 1355 nm
Nominal Wavelength in Bytes 186-187 = 1307.5 nm.
Represented as INT(1307.5 nm * 20) = 26150 = 6626h
Wavelength Tolerance in Bytes 188-189 = 47.5 nm.
Represented as INT(47.5 nm * 200) = 9500 = 251Ch

Example 2:

ITU-T Grid Wavelength = 1534.25 nm (195.4 THz) with 0.236 nm (30 GHz) Tolerance
Nominal Wavelength in Bytes 186-187 = 1534.25 nm.
Represented as INT(1534.25 nm * 20) = 30685 = 77DDh
Wavelength Tolerance in Bytes 188-189 = 0.236 nm.
Represented as INT(0.236 nm * 200) = 47 = 002Fh

If the free side device is identified as copper cable these registers are used to define the cable attenuation. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

Byte 188 (00-FFh) is the copper cable attenuation at 7.0 GHz in units of 1 dB.

Byte 189 (00-FFh) is the copper cable attenuation at 12.9 GHz in units of 1 dB.

6.3.21 Maximum Case Temperature (00h 190)

This parameter allows specification of a maximum case temperature other than the standard 70C. Maximum case temperature is an 8-bit value in degrees C. A value of 00h indicates 70C.

6.3.22 CC_BASE (00h 191)

The check code is a 1-byte code that can be used to verify that the first 63 bytes of serial information in the free side device are valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from 128 to 190, inclusive.

6.3.23 Extended Specification Compliance Codes (00h 192)

The Extended Specification Compliance Codes in Byte 192 identify the electronic or optical interfaces which are not included in Table 6-17 Specification Compliance Codes. These values are maintained in the Transceiver Management section of SFF-8024

6.3.24 Options (00h 193-195)

The bits in the options field shall specify the options implemented in the free side device.

Variable transceiver Tx input EQ and Rx output emphasis have been added, defined as the EQ and Emphasis capability designed into the transceiver in support of TP1a and TP4, respectively as defined in IEE802.3 Clause 86. Transceiver support of programmable EQ and Emphasis is found in Byte 193 bits 1 to 3 and shown below in Table 6-22. The default host control mechanism is "Fixed Position Programmable", found in Page 03h, Bytes 234-237 and documented in Table 6-30, Table 6-32 and Table 6-33. If a transceiver supports "Adaptive EQ", defined as transceiver automatic internal control of EQ position setting (without host intervention), it can be so identified in Byte 193 bit 3. Adaptive EQ algorithms and periodicity are implementation specific. Control of "Adaptive EQ" is done using Upper Page 03h Byte 241 bits 3-0 (per channel controls).

The magnitude of Tx input EQ and Rx output emphasis supported by the transceiver is identified in Page 03h Byte 224. This applies to either Fixed Position Programmable or Adaptive EQ modes.

CDR status and control functions are identified in Byte 194 bits 4 to 7. If Loss of Lock indicators (flags) are implemented bits 4 and 5 are set high. If CDR On/Off control is implemented bits 6 and 7 are set high. For transceivers with CDR capability, setting the CDR to ON engages the internal retiming function. Setting the CDR to OFF enables an internal bypassing mode, which directs traffic around the internal CDR. The two most common reasons to turn a CDR off (i.e. internally bypass it) are to run at rates not supported by a particular CDR or to save the thermal power in applications where CDR jitter mitigation is not required.

Table 6-22 Option Values (Page 00h Bytes 193-195)

Byte	Bit	Description	PC	AC	AO	SM
193	7	Reserved	-	-	-	-
	6	LPMode/TxDis input signal is configurable using byte 99, bit 1. See SFF-8679 for a complete description.				
	5	IntL/RxLOSL output signal is configurable using byte 99, bit 0. See SFF-8679 for a complete description.				
	4	Tx input adaptive equalizers freeze capable. 1 if implemented, else 0.	R	R	R	R
	3	Tx input equalizers auto-adaptive capable. 1 if implemented, else 0.	R	R	R	R
	2	Tx input equalizers fixed-programmable settings. 1 if implemented, else 0.	R	R	R	R
	1	Rx output emphasis fixed-programmable settings. 1 if implemented, else 0.	R	R	R	R
	0	Rx output amplitude fixed-programmable settings. 1 if implemented, else 0.	R	R	R	R
194	7	Tx CDR On/Off Control implemented. 1 if controllable, else 0.	R	R	R	R
	6	Rx CDR On/Off Control implemented. 1 if controllable, else 0.	R	R	R	R
	5	Tx CDR Loss of Lock (LOL) flag implemented. 1 if implemented, else 0.	R	R	R	R
	4	Rx CDR Loss of Lock (LOL) flag implemented. 1 if implemented, else 0.	R	R	R	R
	3	Rx Squelch Disable implemented. 1 if implemented, else 0.	R	R	R	R
	2	Rx Output Disable implemented. 1 if implemented, else 0.	R	R	R	R
	1	Tx Squelch Disable implemented. 1 if implemented, else 0.	R	R	R	R
	0	Tx Squelch implemented. 1 if implemented, else 0.	R	R	R	R
195	7	Memory Page 02 provided. 1 if implemented, else 0.	R	R	R	R
	6	Memory Page 01h provided. 1 if implemented, else 0.	R	R	R	R
	5	Rate select is implemented as defined in 6.2.7. If the bit is set to 1 then refer to that section for multi-rate operation description.	C	C	C	C
	4	Tx_Disable is implemented and disables the serial output as defined by the relevant transmitter specification.	R	R	R	R
	3	Tx_Fault signal implemented. 1 if implemented, else 0	R	R	R	R
	2	Tx Squelch implemented to reduce OMA coded 0, implemented to reduce Pave coded 1.	R	R	R	R
	1	Tx Loss of Signal implemented. 1 if implemented, else 0	R	R	R	R
	0	Pages 20-21h implemented. Default = 0 (not implemented).	R	R	R	R

6.3.25 Vendor Serial Number (00h 196-211)

The vendor serial number (vendor SN) is a 16-character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the free side device. A value of 0000h in the 16-byte field indicates that the vendor SN is unspecified.

6.3.26 Date Code (00h 212-219)

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory and shall be in the specified format.

Table 6-23 Date Codes (Page 00h Bytes 212-219)

Byte	Description	PC	AC	AO	SM
212-213	ASCII code, two low order digits of the year. (00=2000)	R	R	R	R
214-215	ASCII code digits of the month (01=Jan through 12=Dec	R	R	R	R
216-217	ASCII code day of the month (01-31)	R	R	R	R
218-219	ASCII code, Vendor Specific lot code, may be blank	R	R	R	R

6.3.27 Diagnostic Monitoring Type (00h 220)

'Diagnostic Monitoring Type' is a 1-byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the free side device.

Table 6-24 Diagnostic Monitoring Type (Page 00h Byte 220)

Byte	Bits	Description	PC	AC	AO	SM
220	7-6	Reserved	-	-	-	-
	5	Temperature monitoring implemented (0b=Not implemented or pre-Rev 2.8, 1b=Implemented)	R	R	R	R
	4	Supply voltage monitoring implemented (0b=Not implemented or pre-Rev 2.8, 1b=Implemented)	R	R	R	R
	3	Received power measurements type. 0=OMA, 1=Average Power	R	R	R	R
	2	Transmitter power measurement. 0=Not supported, 1=Supported	R	R	R	R
	1-0	Reserved	-	-	-	-

Digital Diagnostic Monitors monitor received power, bias current, supply voltage, and temperature. Additionally, alarm and warning thresholds must be written as specified in this document. Auxiliary monitoring fields are optional extensions to Digital Diagnostics.

All digital monitoring values must be internally calibrated and reported in the units defined in 6.2.5.

Bit 2 indicates whether a transmitted power measurement is supported. The indication is required, however, support of transmitter power measurement is optional (see Table 6-9). If the bit is set, the transmitted power measurement is supported, and the module will monitor the average optical power. If not, transmitted power measurement is not supported.

Bit 3 indicates whether the received power measurement represents average input optical power or OMA. The indication is required, however, support of received power measurement is optional (see Table 6-9). If the bit is set, the average power is monitored. If not, received power measurement is not supported, or OMA is monitored.

6.3.28 Enhanced Options (00h 221)

See Table 6-25 for use of the Enhanced Options field. The state where the Rate Select declaration bits both have a value of 1 is reserved and should not be used.

Table 6-25 Enhanced Options (Page 00h Byte 221)

Byte	Bit	Description	PC	AC	AO	SM
221	7-5	Reserved	-	-	-	-
	4	Initialization Complete Flag implemented. This flag was introduced in rev 2.5. When this bit is 1, the initialization complete flag at Byte 6 bit 0 is implemented independently of t_init. When this bit is 0, the initialization complete flag is either not implemented or if implemented has a response time less than t_init, max as specified for the module.	R	R	R	R
	3	Rate Selection Declaration: When this Declaration bit is 0 the free side device does not support rate selection. When this Declaration bit is 1, rate selection is implemented using extended rate selection. See 6.2.7.2	R	R	R	R
	2	This bit is reserved and reads 0. It was used for SFF-8079 support in revisions of this document before 2.10.	-	-	-	-
	1	TC readiness flag implemented. 0= TC readiness flag not implemented. 1= TC readiness flag is implemented.	R	R	R	R
	0	Software reset is implemented. Use byte 93, bit 7. 0b = not implemented.	O	O	O	O

To enable baud rates in excess of 25.4 GBd, an extended baud rate field has been added in byte 222 to supplement the existing values in byte 140. Byte 140 contains baud rate at 100 MBd resolution, which is limited to 25.4 GBd. Byte 222 contains baud rate at 250 MBd resolution, enabling up to 63.5 GBd. A value of zero means this field is unspecified.

Table 6-26 Extended Baud Rate: Nominal (Page 00h Byte 222)

Byte	Bits	Description	PC	AC	AO	SM
222	7-0	Nominal baud rate, units of 250 MBd. See Byte 140 description.	R	R	R	R

6.3.29 Check Code Extension (00h 223)

The check code is a 1-byte code that can be used to verify that the first 32 bytes of extended serial information in the free side device is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from 192 to 222, inclusive.

6.3.30 Vendor Specific (00h 224-255)

This area may contain Vendor Specific information, which can be read from the free side device. The data is read-only. Page 00h Bytes 224-255 may be used for Vendor Specific ID functions.

6.4 Upper Page 01h (Optional)

Page 01h was previously used for an Application Select Table specified in SFF-8079. This feature is now considered obsolete and so starting with SFF-8636 rev 2.10 this use of the page is deprecated. It is now reserved.

6.5 Upper Page 02h (Optional)

Page 02 is optionally provided as user-writable EEPROM. The fixed side may read or write this memory for any purpose. If Page 00h Byte 129 bit 4 is set, however, the first 10 bytes of Page 02h Bytes 128-137 are used to store the CLEI code for the free side device.

6.6 Upper Page 03h (Optional)

Upper Page 03h contains free side device thresholds, channel thresholds and masks, ability registers for the optional equalizer, emphasis and amplitude, and optional channel controls. See 6.6.1, 0, 6.6.3 and 6.6.4 for detailed descriptions of their use.

Table 6-27 Upper Page 03h Memory Map

Byte	# Bytes	Description	Type
128-175	48	Thresholds	Read-Only
176-223	48	Channel Thresholds	Read-Only
224	1	Tx EQ & Rx Emphasis Magnitude ID	Read-Only
225	1	Rx output amplitude support indicators	Read-Only
226-229	4	Control options advertising	Read-Only
230-241	12	Optional Channel Controls	Read/Write
242-251	10	Channel Monitor Masks	Read/Write
252-255	4	Reserved	Read/Write

6.6.1 Free Side Device and Channel Thresholds (Page 03h, Bytes 128-223)

Each monitor value has a corresponding high alarm, low alarm, high warning, and low warning thresholds. For each monitor that is implemented, high and low alarm thresholds are required. These factory-preset values allow the user to determine when a particular value is outside of normal limits as determined by the free side device manufacturer. It is assumed that these values will vary with different technologies and different implementations. These values are stored in read-only memory in Page 03h Bytes 128-223.

Table 6-28 Free Side Device and Channel Thresholds (Page 03h Bytes 128-223)

Byte	# Bytes	Name	Description	PC	AC	AO	SM
128-129	2	Temp High Alarm	MSB at lower byte address	C	C	C	C
130-131	2	Temp Low Alarm	MSB at lower byte address	C	C	C	C
132-133	2	Temp High Warning	MSB at lower byte address	O	O	O	O
134-135	2	Temp Low Warning	MSB at lower byte address	O	O	O	O
136-143	8	Reserved		-	-	-	-
144-145	2	Vcc High Alarm	MSB at lower byte address	C	C	C	C
146-147	2	Vcc Low Alarm	MSB at lower byte address	C	C	C	C
148-149	2	Vcc High Warning	MSB at lower byte address	O	O	O	O
150-151	2	Vcc Low Warning	MSB at lower byte address	O	O	O	O
152-159	8	Reserved		-	-	-	-
160-175	16	Vendor Specific		-	-	-	-
176-177	2	Rx Power High Alarm	MSB at lower byte address	C	C	C	C
178-179	2	Rx Power Low Alarm	MSB at lower byte address	C	C	C	C
180-181	2	Rx Power High Warning	MSB at lower byte address	O	O	O	O
182-183	2	Rx Power Low Warning	MSB at lower byte address	O	O	O	O
184-185	2	Tx Bias High Alarm	MSB at lower byte address	C	C	C	C
186-187	2	Tx Bias Low Alarm	MSB at lower byte address	C	C	C	C
188-189	2	Tx Bias High Warning	MSB at lower byte address	O	O	O	O
190-191	2	Tx Bias Low Warning	MSB at lower byte address	O	O	O	O
192-193	2	Tx Power High Alarm	MSB at lower byte address	C	C	C	C
194-195	2	Tx Power Low Alarm	MSB at lower byte address	C	C	C	C
196-197	2	Tx Power High Warning	MSB at lower byte address	O	O	O	O
198-199	2	Tx Power Low Warning	MSB at lower byte address	O	O	O	O

Byte	# Bytes	Name	Description	PC	AC	AO	SM
200-207	8	Reserved	Reserved thresholds for channel parameter set 4	-	-	-	-
208-215	8	Reserved	Reserved thresholds for channel parameter set 5	-	-	-	-
216-223	8	Vendor Specific		-	-	-	-

The values reported in the Alarm and Warning Thresholds area may be typical values at some chosen nominal operating conditions and may be temperature compensated or otherwise adjusted when setting warning and/or alarm flags. Any threshold compensation or adjustment is Vendor Specific and optional. Refer to the vendor's data sheet for use of alarm and warning thresholds.

6.6.2 Optional Equalizer, Emphasis and Amplitude Indicators (Page 03h, Bytes 224-229)

Table 6-29 **Equalizer, Emphasis, Amplitude and Timing (Page 03h Bytes 224-229)**

Byte	Bit	Name	Description	PC	AC	AO	SM
224	7-4	Max Tx input equalization	Max Tx input equalization supported (controls are in bytes 234-235 and codes are in Table 6-32)	O	O	O	O
	3-0	Max Rx output emphasis	Max Rx output emphasis supported (controls are in bytes 236-237 and codes are in Table 6-33)	O	O	O	O
225	7-6	Reserved		-	-	-	-
	5-4	Rx output emphasis type	=00b Peak-to-peak amplitude stays constant, or not implemented, or no information =01b Steady state amplitude stays constant stays constant =10b Average of peak-to-peak and steady state amplitudes stays constant =11b Reserved	O	O	O	O
	3	Rx output amplitude support	=0 Amplitude 0011 not supported or no information =1 Amplitude 0011 supported (see Table 6-31)	O	O	O	O
	2		=0 Amplitude 0010 not supported or no information =1 Amplitude 0010 supported (see Table 6-31)	O	O	O	O
	1		=0 Amplitude 0001 not supported or no information =1 Amplitude 0001 supported (see Table 6-31)	O	O	O	O
	0		=0 Amplitude 0000 not supported or no information =1 Amplitude 0000 supported (see Table 6-31)	O	O	O	O
226	All	Reserved		-	-	-	-
227	7	Controllable Host-Side FEC support	=0 Module's host-side FEC, if any, is not controllable by the host. =1 Module can terminate and generate FEC encoding from and to the host under control of the host. See Page 03h, Byte 230, bit 7 for the control bit.	-	O	O	O
	6	Controllable Media-Side FEC support	=0 Module's media-side FEC, if any, is not controllable by the host. =1 Module can generate and terminate FEC encoding from and to the media under control of the host. See Page 03h, Byte 230, bit 6 for the control bit.	-	O	O	O
	5-4	Reserved		-	-	-	-
	3	Tx Force Squelch Implemented	0 = Tx Force Squelch not implemented 1 = Tx Force Squelch implemented. See page 03h, byte 231, bits 3-0 for control bits.	-	O	O	O
	2	RxLOSL Fast Mode Supported	0 = RxLOSL fast mode is not supported. 1 = Complies with timing requirements of SFF-8679 optional RxLOSL fast mode.	-	O	O	O
	1	TxDis Fast Mode Supported	0 = TxDis fast mode is not supported. 1 = Complies with timing requirements of SFF-8679 optional TxDis fast mode.	-	O	O	O
	0	Reserved		-	-	-	-
228	All	Maximum TC stabilization time	Maximum time for the TC to reach its target working point under worst-case conditions. LSB = 1 s.	O	O	O	O
229	All	Maximum CTLE settling time	Maximum time needed by CTLE adaptive algorithm to converge to an appropriate value under worst-	O	O	O	O

Byte	Bit	Name	Description	PC	AC	AO	SM
			case conditions. LSB = 100 ms.				

6.6.3 Optional Channel Controls (Page 03h, Bytes 230-241)

Upper Memory Page Control Bits are used to define the optional channel controls.

Table 6-30 Optional Channel Controls (Page 03h Bytes 230-241)

Byte	Bit	Name	Description	PC	AC	AO	SM
230	7	Host-Side FEC enable	Enables host-side FEC termination on the Tx electrical inputs and host-side FEC generation on the Rx electrical outputs. 0b = disable, 1b = enable. Default = 0.	-	O	O	O
	6	Media-Side FEC enable	Enables media-side FEC generation on the Tx outputs and media-side FEC termination on the Rx inputs. 0b = enable, 1b = disable. Default = 0.	-	O	O	O
	5-0	Reserved		-	-	-	-
231	7-4	Reserved		-	-	-	-
	3	Tx4 Force Squelch	Software squelch of transmitter output, per media lane. Note that the transmitter output may be disabled, which overrides the behaviors of this control 0b = No impact on Tx behavior 1b = Tx output squelched See Page 03h Byte 227 bit 3 for implementation indicator.	-	O	O	O
	2	Tx3 Force Squelch		-	O	O	O
	1	Tx2 Force Squelch		-	O	O	O
	0	Tx1 Force Squelch		-	O	O	O
232	All	Reserved		-	-	-	-
233	7-4	Reserved		-	-	-	-
	3	Tx1AEFreeze	Controls to freeze Tx input adaptive equalizers. 1 to freeze, else 0. See page 00h byte 193 bit 4 for support indicator.	O	O	O	O
	2	Tx2AEFreeze		O	O	O	O
	1	Tx3AEFreeze		O	O	O	O
	0	Tx4AEFreeze		O	O	O	O
234	7-4	Tx1 input equalizer control	Tx input equalizer controls (see Page 03h Byte 224 and Table 6-32)	O	O	O	O
	3-0	Tx2 input equalizer control		O	O	O	O
235	7-4	Tx3 input equalizer control		O	O	O	O
	3-0	Tx4 input equalizer control		O	O	O	O
236	7-4	Rx1 output emphasis control	Rx output emphasis controls (see Page 03h Byte 224 and Table 6-33)	O	O	O	O
	3-0	Rx2 output emphasis control		O	O	O	O
237	7-4	Rx3 output emphasis control		O	O	O	O
	3-0	Rx4 output emphasis control		O	O	O	O
238	7-4	Rx1 output amplitude control	Controls for Rx output differential amplitude. (See Table 6-31)	O	O	O	O
	3-0	Rx2 output amplitude control		O	O	O	O
239	7-4	Rx3 output amplitude control		O	O	O	O
	3-0	Rx4 output amplitude control		O	O	O	O
240	7	Rx4 SQ Disable	Controls to disable squelch of Rx outputs. 1 = Disabled, 0 = Enabled Default = 0.	O	O	O	O
	6	Rx3 SQ Disable		O	O	O	O
	5	Rx2 SQ Disable		O	O	O	O
	4	Rx1 SQ Disable		O	O	O	O
	3	Tx4 SQ Disable	Controls to disable squelch of Tx outputs. 1 = Disabled, 0 = Enabled	O	O	O	O
	2	Tx3 SQ Disable		O	O	O	O
	1	Tx2 SQ Disable		O	O	O	O

Byte	Bit	Name	Description	PC	AC	AO	SM
	0	Tx1 SQ Disable	Default = 0.	O	O	O	O
241	7	Rx4 Output Disable	Controls to disable Rx outputs.	O	O	O	O
	6	Rx3 Output Disable	1 = Disabled, 0 = Enabled	O	O	O	O
	5	Rx2 Output Disable	Default = 0.	O	O	O	O
	4	Rx1 Output Disable		O	O	O	O
	3	Tx4 adaptive equalization control	Controls for Tx input adaptive equalizers.	-	O	O	O
	2	Tx3 adaptive equalization control	1b=Enable (default)	-	O	O	O
	1	Tx2 adaptive equalization control	0b=Disable (use manual EQ) See 00h 193 bit 3 for implementation indicator.	-	O	O	O
	0	Tx1 adaptive equalization control		-	O	O	O

Table 6-31 Output Differential Amplitude Control (Page 03h Bytes 238-239)

Value	Receiver Output Amplitude No Output Equalization	
	Nominal	Units
1xxxb	Reserved	
0111b		
0110b		
0101b		
0100b		
0011b	600-1200	mV (p-p)
0010b	400-800	
0001b	300-600	
0000b	100-400	

Table 6-32 Tx Input Equalizer Controls (Page 03h Bytes 234-235)

Value	Transmitter Input Equalization	
	Nominal	Units
11xxb	Reserved	
1011b		
1010b	10	dB
1001b	9	
1000b	8	
0111b	7	
0110b	6	
0101b	5	
0100b	4	
0011b	3	
0010b	2	
0001b	1	
0000b	0	No EQ

Table 6-33 Rx Output Emphasis Controls (Page 03h Bytes 236-237)

Value	Receiver Output Emphasis At nominal Output Amplitude	
	Nominal	**Units**
1xxxb	Reserved	
0111b	7	dB
0110b	6	
0101b	5	
0100b	4	
0011b	3	
0010b	2	
0001b	1	
0000b	0	No Emphasis

Output amplitude and output emphasis are defined at the appropriate test points defined by the relevant standard. There is an illustration of reference test points in SFF-8679.

Because receiver emphasis settings can affect receiver output amplitude (and vice versa) Table 6-31 and Table 6-33 define the variable parameter at a nominal condition of the other. For instance, Table 6-31 defines output amplitude at a zero output emphasis setting and Table 6-33 defines output emphasis at a nominal output amplitude setting (implementation dependent). The maximum emphasis supported is defined in section 0, Table 6-29 byte 224. If an implementation does not support all levels up to and including the maximum, the nearest value shall be used.

Squelch and output control functionality is optional. If implemented, squelch and output disable is controlled for each channel using Page 03h Bytes 231 and 240-241. Writing a '1' in the Squelch Disable register (Page 03h Byte 240) disables the squelch for the associated channel. Writing a '1' in the Output Disable register (Page 03h Byte 241) disables the output of the associated channel. When a '1' is written in both registers for a channel, the associated output is disabled. The registers read all '0's upon power-up. Note that the Tx Forced Squelch controls in page 03h, byte 231, override the Tx Squelch Disable settings (see Table 6-30). All other squelch functionality details are outside the scope of this document.

Table 6-34 Tx Squelch Truth Table

Tx Force Squelch (Byte 231)	Tx Squelch Disable (Byte 240)	Output Amplitude
1	x	Squelched
0	1	Normal
0	0	Auto-squelch enabled if implemented (see page 00h, byte 194, bit 0).

6.6.4 Channel Monitor Masks (Page 03h, Bytes 242-251)

Table 6-35 Channel Monitor Masks (Page 03h Bytes 242-251)

Byte	Bit	Name	Description	PC	AC	AO	SM
242	7	M-Rx1 Power High Alarm	Masking bits for Rx input power alarms and warnings.	C	C	C	C
	6	M-Rx1 Power Low Alarm		C	C	C	C
	5	M-Rx1 Power High Warning		C	C	C	C
	4	M-Rx1 Power Low Warning		C	C	C	C
	3	M-Rx2 Power High Alarm		C	C	C	C
	2	M-Rx2 Power Low Alarm		C	C	C	C
	1	M-Rx2 Power High Warning		C	C	C	C
	0	M-Rx2 Power Low Warning		C	C	C	C
243	7	M-Rx3 Power High Alarm		C	C	C	C
	6	M-Rx3 Power Low Alarm		C	C	C	C
	5	M-Rx3 Power High Warning		C	C	C	C
	4	M-Rx3 Power Low Warning		C	C	C	C
	3	M-Rx4 Power High Alarm		C	C	C	C
	2	M-Rx4 Power Low Alarm		C	C	C	C
	1	M-Rx4 Power High Warning		C	C	C	C
	0	M-Rx4 Power Low Warning		C	C	C	C
244	7	M-Tx1 Bias High Alarm	Masking bits for Tx bias alarms and warnings.	C	C	C	C
	6	M-Tx1 Bias Low Alarm		C	C	C	C
	5	M-Tx1 Bias High Warning		C	C	C	C
	4	M-Tx1 Bias Low Warning		C	C	C	C
	3	M-Tx2 Bias High Alarm		C	C	C	C
	2	M-Tx2 Bias Low Alarm		C	C	C	C
	1	M-Tx2 Bias High Warning		C	C	C	C
	0	M-Tx2 Bias Low Warning		C	C	C	C
245	7	M-Tx3 Bias High Alarm		C	C	C	C
	6	M-Tx3 Bias Low Alarm		C	C	C	C
	5	M-Tx3 Bias High Warning		C	C	C	C
	4	M-Tx3 Bias Low Warning		C	C	C	C
	3	M-Tx4 Bias High Alarm		C	C	C	C
	2	M-Tx4 Bias Low Alarm		C	C	C	C
	1	M-Tx4 Bias High Warning		C	C	C	C
	0	M-Tx4 Bias Low Warning		C	C	C	C
246	7	M-Tx1 Power High Alarm	Masking bits for Tx output power alarms and warnings.	C	C	C	C
	6	M-Tx1 Power Low Alarm		C	C	C	C
	5	M-Tx1 Power High Warning		C	C	C	C
	4	M-Tx1 Power Low Warning		C	C	C	C
	3	M-Tx2 Power High Alarm		C	C	C	C
	2	M-Tx2 Power Low Alarm		C	C	C	C
	1	M-Tx2 Power High Warning		C	C	C	C
	0	M-Tx2 Power Low Warning		C	C	C	C
247	7	M-Tx3 Power High Alarm		C	C	C	C
	6	M-Tx3 Power Low Alarm		C	C	C	C
	5	M-Tx3 Power High Warning		C	C	C	C
	4	M-Tx3 Power Low Warning		C	C	C	C
	3	M-Tx4 Power High Alarm		C	C	C	C
	2	M-Tx4 Power Low Alarm		C	C	C	C
	1	M-Tx4 Power High Warning		C	C	C	C
	0	M-Tx4 Power Low Warning		C	C	C	C

Byte	Bit	Name	Description	PC	AC	AO	SM
248-249	All	Reserved	Reserved channel monitor masks set 4	-	-	-	-
250-251	All	Reserved	Reserved channel monitor masks set 5	-	-	-	-

6.7 Upper Page 20h and Upper Page 21h (Optional)

The Upper Page 20h and Upper Page 21h contain support for additional monitored parameters for modules that have PAM4 modulation and/or have optical transmission wavelengths on a DWDM grid.

6.7.1 Overview

Many additional parameters may be supported by a QSFP with advanced modulation techniques. Pages 20h and 21h in the SFF-8436/SFF-8636 memory space are assigned for monitoring of these parameters. The basic monitoring techniques are the same as for other monitored parameters (i.e., they support current value, latched warning/alarm status, masks, and thresholds). To indicate to the host device whether pages 20h and 21h are supported, page 00h byte 195 bit 0 is used. A value of 1b indicates that page 20h and 21h are supported as described in this section. A value of 0b indicates that pages 20h and 21h are not supported by the module.

For a PAM4 signal, several additional parameters are very useful to determine the health of the module and the line environment. These include bit error ratio and frame error rate calculations, a signal-to-noise ratio measurement and a level transition measurement that characterize the PAM eye, and a residual dispersion measurement.

For a module implementing a Dense Wavelength Division Multiplexing optical interface, there is a significant benefit in providing access to additional diagnostic monitoring parameters specifically for a DWDM module. In DWDM the wavelength or frequency of the laser is an extremely important parameter and monitoring it allows the health of the laser to be known. When a direct measurement of the error in the frequency is not available, the laser temperature deviation from the target is often used as a proxy. In addition, DWDM modules typically use a thermo-electric cooler (TEC) to control the laser temperature. The current flowing through the TEC is a strong indicator of the health of the module. A warning or error indication in any of these parameters can be an early indication of pending module failure.

Other modules may require additional parameters to be defined in the future.

It is expected that not all possible features will be supported by all modules or on all channels. To address this situation, this specification allows the module to determine which parameters are being monitored. Some parameters may be module-level in scope, and some may be channel-specific. This information is conveyed by the module to the host in the 2-byte parameter configuration registers (page 20h bytes 200-248). To indicate that one or more parameters are not supported the module reports 00h in both bytes of the configuration register for that parameter.

Up to 24 different parameters can be monitored, each providing a real-time value as well as alarm and warning flags. 16 threshold value sets are provided, and each of the 24 parameters is associated by the module with one of the threshold value sets. The parameter configuration registers indicate which threshold set is to be used with each parameter. Note that this implies that multiple parameters may share the same threshold set (for example, if the same parameter is measured on multiple channels).

To facilitate future functionality without major specification changes, the parameter configuration registers provide an enumerated value for the specific parameter to be monitored.

In addition to parameter monitoring, this specification includes a read-only logical mapping indication feature which associates electrical channels with optical channels when that mapping is defined.

6.7.2 Registers for Page 20h and 21h

6.7.2.1 Overview

Table 6-36 Register overview for page 20h

Byte	Size	Name	Description	PC	AC	AO	SM
128-139	12	Param Alarms	Latched alarm/warning flags for monitored parameters (see 6.7.2.2)	O	O	O	O
140-151	12	Param Masks	Interrupt mask values for monitored parameters (see 6.7.2.3)	O	O	O	O
152-199	48	Param Values	Real-time values for monitored parameters (see 6.7.2.4)	O	O	O	O
200-247	48	Param Configuration	Parameter configuration registers (see 6.7.2.5)	O	O	O	O
248-249	2	Lane mapping	Lane mapping (see 6.7.2.6)	O	O	O	O
250-255	6	Other configuration	Error counter reset and other configurations (see 6.7.2.7)	O	O	O	O

Table 6-37 Register overview for page 21h

Byte	Size	Name	Description	PC	AC	AO	SM
128-255	128	Param Thresholds	Parameter alarm and warning thresholds (page 21h, see 6.7.2.8)	O	O	O	O

6.7.2.2 Latched Alarm/Warning Flags for Monitored Parameters

These 12 bytes cover the latched alarm and warning flags for the monitored parameters specified by the parameter configuration registers. Each parameter has 4 bits with the most-significant bit representing the alarm high error, followed by alarm low, warning high and warning low as with other alarm and warning flags. Note that the threshold against which the real-time value is compared to generate these alarms and warnings is specified in the Parameter Configuration Registers.

Table 6-38 Latched Alarm/Warning Flags (Page 20h Bytes 128-139)

Byte	Bit	Name	Description	PC	AC	AO	SM
128	7-4	L-Param1 Alarm/Warning	Latched alarm/warning flags for monitored parameter 1	O	O	O	O
	3-0	L-Param2 Alarm/Warning	Latched alarm/warning flags for monitored parameter 2	O	O	O	O
129	7-4	L-Param3 Alarm/Warning	Latched alarm/warning flags for monitored parameter 3	O	O	O	O
	3-0	L-Param4 Alarm/Warning	Latched alarm/warning flags for monitored parameter 4	O	O	O	O
130	7-4	L-Param5 Alarm/Warning	Latched alarm/warning flags for monitored parameter 5	O	O	O	O
	3-0	L-Param6 Alarm/Warning	Latched alarm/warning flags for monitored parameter 6	O	O	O	O
131	7-4	L-Param7 Alarm/Warning	Latched alarm/warning flags for monitored parameter 7	O	O	O	O
	3-0	L-Param8 Alarm/Warning	Latched alarm/warning flags for monitored parameter 8	O	O	O	O
132	7-4	L-Param9 Alarm/Warning	Latched alarm/warning flags for monitored parameter 9	O	O	O	O
	3-0	L-Param10 Alarm/Warning	Latched alarm/warning flags for monitored parameter 10	O	O	O	O

Byte	Bit	Name	Description	PC	AC	AO	SM
133	7-4	L-Param11 Alarm/Warning	Latched alarm/warning flags for monitored parameter 11	O	O	O	O
	3-0	L-Param12 Alarm/Warning	Latched alarm/warning flags for monitored parameter 12	O	O	O	O
134	7-4	L-Param13 Alarm/Warning	Latched alarm/warning flags for monitored parameter 13	O	O	O	O
	3-0	L-Param14 Alarm/Warning	Latched alarm/warning flags for monitored parameter 14	O	O	O	O
135	7-4	L-Param15 Alarm/Warning	Latched alarm/warning flags for monitored parameter 15	O	O	O	O
	3-0	L-Param16 Alarm/Warning	Latched alarm/warning flags for monitored parameter 16	O	O	O	O
136	7-4	L-Param17 Alarm/Warning	Latched alarm/warning flags for monitored parameter 17	O	O	O	O
	3-0	L-Param18 Alarm/Warning	Latched alarm/warning flags for monitored parameter 18	O	O	O	O
137	7-4	L-Param19 Alarm/Warning	Latched alarm/warning flags for monitored parameter 19	O	O	O	O
	3-0	L-Param20 Alarm/Warning	Latched alarm/warning flags for monitored parameter 20	O	O	O	O
138	7-4	L-Param21 Alarm/Warning	Latched alarm/warning flags for monitored parameter 21	O	O	O	O
	3-0	L-Param22 Alarm/Warning	Latched alarm/warning flags for monitored parameter 22	O	O	O	O
139	7-4	L-Param23 Alarm/Warning	Latched alarm/warning flags for monitored parameter 23	O	O	O	O
	3-0	L-Param24 Alarm/Warning	Latched alarm/warning flags for monitored parameter 24	O	O	O	O

6.7.2.3 Mask Registers for Monitored Parameters

These 12 bytes cover the interrupt masks for the latched alarm and warning flags. Each parameter has 4 bits with the most-significant bit representing the alarm high error, followed by low alarm, high warning and low warning as with other alarm and warning parameters. When a particular bit is 0, then the corresponding flag generates an interrupt. If the bit is 1 then an interrupt is not generated. As with the alarm and warning flags, for each parameter the highest bit number represents alarm high followed by alarm low, warning high and warning low masks.

Table 6-39 Interrupt Mask Registers (Page 20h Bytes 140-151)

Byte	Bit	Name	Description	PC	AC	AO	SM
140	7-4	M-Param1 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 1	O	O	O	O
	3-0	M-Param2 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 2	O	O	O	O
141	7-4	M-Param3 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 3	O	O	O	O
	3-0	M-Param4 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 4	O	O	O	O
142	7-4	M-Param5 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 5	O	O	O	O

Byte	Bit	Name	Description	PC	AC	AO	SM
	3-0	M-Param6 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 6	O	O	O	O
143	7-4	M-Param7 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 7	O	O	O	O
	3-0	M-Param8 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 8	O	O	O	O
144	7-4	M-Param9 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 9	O	O	O	O
	3-0	M-Param10 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 10	O	O	O	O
145	7-4	M-Param11 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 11	O	O	O	O
	3-0	M-Param12 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 12	O	O	O	O
146	7-4	M-Param13 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 13	O	O	O	O
	3-0	M-Param14 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 14	O	O	O	O
147	7-4	M-Param15 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 15	O	O	O	O
	3-0	M-Param16 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 16	O	O	O	O
148	7-4	M-Param17 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 17	O	O	O	O
	3-0	M-Param18 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 18	O	O	O	O
149	7-4	M-Param19 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 19	O	O	O	O
	3-0	M-Param20 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 20	O	O	O	O
150	7-4	M-Param21 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 21	O	O	O	O
	3-0	M-Param22 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 22	O	O	O	O
151	7-4	M-Param23 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 23	O	O	O	O
	3-0	M-Param24 Alarm/Warning	Masking bits for alarm/warning flags for monitored parameter 24	O	O	O	O

6.7.2.4 Real-Time Value of Monitored Parameters

These 48 bytes contain the real-time value of the monitored parameters. They are to be interpreted as specified in the Parameter Configuration Registers. In addition, the module will compare these values to the corresponding thresholds indicated in the Parameter Configuration Registers to generate the appropriate alarms and/or warnings in the registers above. As with the rest of SFF-8636, these parameters are all stored with the most significant byte in the lower numbered address.

Table 6-40 Real-Time Value Registers (Page 20h Bytes 152-199)

Byte	Bit	Name	Description	PC	AC	AO	SM
152	All	Param 1 MSB	Real-time value of parameter 1 (MSB)	O	O	O	O
153	All	Param 1 LSB	Real-time value of parameter 1 (LSB)	O	O	O	O
154	All	Param 2 MSB	Real-time value of parameter 2 (MSB)	O	O	O	O
155	All	Param 2 LSB	Real-time value of parameter 2 (LSB)	O	O	O	O
156	All	Param 3 MSB	Real-time value of parameter 3 (MSB)	O	O	O	O
157	All	Param 3 LSB	Real-time value of parameter 3 (LSB)	O	O	O	O
158	All	Param 4 MSB	Real-time value of parameter 4 (MSB)	O	O	O	O
159	All	Param 4 LSB	Real-time value of parameter 4 (LSB)	O	O	O	O
160	All	Param 5 MSB	Real-time value of parameter 5 (MSB)	O	O	O	O
161	All	Param 5 LSB	Real-time value of parameter 5 (LSB)	O	O	O	O
162	All	Param 6 MSB	Real-time value of parameter 6 (MSB)	O	O	O	O
163	All	Param 6 LSB	Real-time value of parameter 6 (LSB)	O	O	O	O
164	All	Param 7 MSB	Real-time value of parameter 7 (MSB)	O	O	O	O
165	All	Param 7 LSB	Real-time value of parameter 7 (LSB)	O	O	O	O
166	All	Param 8 MSB	Real-time value of parameter 8 (MSB)	O	O	O	O
167	All	Param 8 LSB	Real-time value of parameter 8 (LSB)	O	O	O	O
168	All	Param 9 MSB	Real-time value of parameter 9 (MSB)	O	O	O	O
169	All	Param 9 LSB	Real-time value of parameter 9 (LSB)	O	O	O	O
170	All	Param 10 MSB	Real-time value of parameter 10 (MSB)	O	O	O	O
171	All	Param 10 LSB	Real-time value of parameter 10 (LSB)	O	O	O	O
172	All	Param 11 MSB	Real-time value of parameter 11 (MSB)	O	O	O	O
173	All	Param 11 LSB	Real-time value of parameter 11 (LSB)	O	O	O	O
174	All	Param 12 MSB	Real-time value of parameter 12 (MSB)	O	O	O	O
175	All	Param 12 LSB	Real-time value of parameter 12 (LSB)	O	O	O	O
176	All	Param 13 MSB	Real-time value of parameter 13 (MSB)	O	O	O	O
177	All	Param 13 LSB	Real-time value of parameter 13 (LSB)	O	O	O	O
178	All	Param 14 MSB	Real-time value of parameter 14 (MSB)	O	O	O	O
179	All	Param 14 LSB	Real-time value of parameter 14 (LSB)	O	O	O	O
180	All	Param 15 MSB	Real-time value of parameter 15 (MSB)	O	O	O	O
181	All	Param 15 LSB	Real-time value of parameter 15 (LSB)	O	O	O	O
182	All	Param 16 MSB	Real-time value of parameter 16 (MSB)	O	O	O	O
183	All	Param 16 LSB	Real-time value of parameter 16 (LSB)	O	O	O	O
184	All	Param 17 MSB	Real-time value of parameter 17 (MSB)	O	O	O	O
185	All	Param 17 LSB	Real-time value of parameter 17 (LSB)	O	O	O	O
186	All	Param 18 MSB	Real-time value of parameter 18 (MSB)	O	O	O	O
187	All	Param 18 LSB	Real-time value of parameter 18 (LSB)	O	O	O	O
188	All	Param 19 MSB	Real-time value of parameter 19 (MSB)	O	O	O	O
189	All	Param 19 LSB	Real-time value of parameter 19 (LSB)	O	O	O	O
190	All	Param 20 MSB	Real-time value of parameter 20 (MSB)	O	O	O	O
191	All	Param 20 LSB	Real-time value of parameter 20 (LSB)	O	O	O	O
192	All	Param 21 MSB	Real-time value of parameter 21 (MSB)	O	O	O	O
193	All	Param 21 LSB	Real-time value of parameter 21 (LSB)	O	O	O	O
194	All	Param 22 MSB	Real-time value of parameter 22 (MSB)	O	O	O	O
195	All	Param 22 LSB	Real-time value of parameter 22 (LSB)	O	O	O	O
196	All	Param 23 MSB	Real-time value of parameter 23 (MSB)	O	O	O	O
197	All	Param 23 LSB	Real-time value of parameter 23 (LSB)	O	O	O	O
198	All	Param 24 MSB	Real-time value of parameter 24 (MSB)	O	O	O	O
199	All	Param 24 LSB	Real-time value of parameter 24 (LSB)	O	O	O	O

6.7.2.5 Parameter Configuration Registers

These 48 bytes determine how the real-time value registers, alarms and warnings, masks and thresholds are to be interpreted by the host. For each of the 24 possible monitored parameters the monitoring point, parameter type and threshold location are provided by the module. The parameter configuration is a 2-byte field which is described below.

Table 6-41 Parameter Configuration Registers (Page 20h Bytes 200-247)

Byte	Bit	Name	Description	PC	AC	AO	SM
200	All	Config 1 MSB	Configuration for parameter 1 (MSB)	O	O	O	O
201	All	Config 1 LSB	Configuration for parameter 1 (LSB)	O	O	O	O
202	All	Config 2 MSB	Configuration for parameter 2 (MSB)	O	O	O	O
203	All	Config 2 LSB	Configuration for parameter 2 (LSB)	O	O	O	O
204	All	Config 3 MSB	Configuration for parameter 3 (MSB)	O	O	O	O
205	All	Config 3 LSB	Configuration for parameter 3 (LSB)	O	O	O	O
206	All	Config 4 MSB	Configuration for parameter 4 (MSB)	O	O	O	O
207	All	Config 4 LSB	Configuration for parameter 4 (LSB)	O	O	O	O
208	All	Config 5 MSB	Configuration for parameter 5 (MSB)	O	O	O	O
209	All	Config 5 LSB	Configuration for parameter 5 (LSB)	O	O	O	O
210	All	Config 6 MSB	Configuration for parameter 6 (MSB)	O	O	O	O
211	All	Config 6 LSB	Configuration for parameter 6 (LSB)	O	O	O	O
212	All	Config 7 MSB	Configuration for parameter 7 (MSB)	O	O	O	O
213	All	Config 7 LSB	Configuration for parameter 7 (LSB)	O	O	O	O
214	All	Config 8 MSB	Configuration for parameter 8 (MSB)	O	O	O	O
215	All	Config 8 LSB	Configuration for parameter 8 (LSB)	O	O	O	O
216	All	Config 9 MSB	Configuration for parameter 9 (MSB)	O	O	O	O
217	All	Config 9 LSB	Configuration for parameter 9 (LSB)	O	O	O	O
218	All	Config 10 MSB	Configuration for parameter 10 (MSB)	O	O	O	O
219	All	Config 10 LSB	Configuration for parameter 10 (LSB)	O	O	O	O
220	All	Config 11 MSB	Configuration for parameter 11 (MSB)	O	O	O	O
221	All	Config 11 LSB	Configuration for parameter 11 (LSB)	O	O	O	O
222	All	Config 12 MSB	Configuration for parameter 12 (MSB)	O	O	O	O
223	All	Config 12 LSB	Configuration for parameter 12 (LSB)	O	O	O	O
224	All	Config 13 MSB	Configuration for parameter 13 (MSB)	O	O	O	O
225	All	Config 13 LSB	Configuration for parameter 13 (LSB)	O	O	O	O
226	All	Config 14 MSB	Configuration for parameter 14 (MSB)	O	O	O	O
227	All	Config 14 LSB	Configuration for parameter 14 (LSB)	O	O	O	O
228	All	Config 15 MSB	Configuration for parameter 15 (MSB)	O	O	O	O
229	All	Config 15 LSB	Configuration for parameter 15 (LSB)	O	O	O	O
230	All	Config 16 MSB	Configuration for parameter 16 (MSB)	O	O	O	O
231	All	Config 16 LSB	Configuration for parameter 16 (LSB)	O	O	O	O
232	All	Config 17 MSB	Configuration for parameter 17 (MSB)	O	O	O	O
233	All	Config 17 LSB	Configuration for parameter 17 (LSB)	O	O	O	O
234	All	Config 18 MSB	Configuration for parameter 18 (MSB)	O	O	O	O
235	All	Config 18 LSB	Configuration for parameter 18 (LSB)	O	O	O	O
236	All	Config 19 MSB	Configuration for parameter 19 (MSB)	O	O	O	O
237	All	Config 19 LSB	Configuration for parameter 19 (LSB)	O	O	O	O
238	All	Config 20 MSB	Configuration for parameter 20 (MSB)	O	O	O	O
239	All	Config 20 LSB	Configuration for parameter 20 (LSB)	O	O	O	O
240	All	Config 21 MSB	Configuration for parameter 21 (MSB)	O	O	O	O

Byte	Bit	Name	Description	PC	AC	AO	SM
241	All	Config 21 LSB	Configuration for parameter 21 (LSB)	O	O	O	O
242	All	Config 22 MSB	Configuration for parameter 22 (MSB)	O	O	O	O
243	All	Config 22 LSB	Configuration for parameter 22 (LSB)	O	O	O	O
244	All	Config 23 MSB	Configuration for parameter 23 (MSB)	O	O	O	O
245	All	Config 23 LSB	Configuration for parameter 23 (LSB)	O	O	O	O
246	All	Config 24 MSB	Configuration for parameter 24 (MSB)	O	O	O	O
247	All	Config 24 LSB	Configuration for parameter 24 (LSB)	O	O	O	O

The two bytes of parameter are stored most significant byte-first with the following definition:

Table 6-42 Parameter Configuration Details

Byte	Bits	Description
MSB	7:4	Threshold ID. This number corresponds to which threshold set (1-16) is to be used for this parameter.
	3	Reserved
	2	Parameter monitored at: 0b = Global module 1b = Channel-specific (see bits 1:0)
	1:0	Channel number, if the parameter is monitored channel-specific, per bit 2.
LSB	7:0	Parameter type (see Table 6-43)

The parameter type value is taken from the following table:

Table 6-43 Parameter Type Enumeration

Value	Description
0	Parameter not supported. This value means that the module is not presenting any data on the corresponding real-time value, or latched flag registers.
1	SNR, line ingress (see section 6.7.4.1)
2	Residual ISI/Dispersion, line ingress (see section 6.7.4.2)
3	PAM4 Level Transition Parameter, line ingress (see section 6.7.4.3)
4	Pre-FEC BER, average, line ingress (see section 6.7.4.4)
5	FER, average, line ingress (see section 6.7.4.4)
6	TEC Current (see section 6.7.5.1)
7	Laser Frequency (see section 6.7.5.2)
8	Laser Temperature (see section 6.7.5.3)
9	Pre-FEC BER, latched minimum value since last read, line ingress (see section 6.7.4.4)
10	Pre-FEC BER, latched maximum value since last read, line ingress (see section 6.7.4.4)
11	Pre-FEC BER, prior period, line ingress (see section 6.7.4.4)
12	Pre-FEC BER, current, line ingress (see section 6.7.4.4)
13	FER, latched minimum value since last read, line ingress (see section 6.7.4.4)
14	FER, latched maximum value since last read, line ingress (see section 6.7.4.4)
15	FER, prior period, line ingress (see section 6.7.4.4)
16	FER, current, line ingress (see section 6.7.4.4)
17-191	Reserved
192-255	Vendor-specific

6.7.2.6 Electrical/Optical Lane Mapping

This read-only feature allows the host to retrieve the electrical to optical channel mapping. For a PAM4 encoding, the electrical channel can be either mapped to the MSB or the LSB of the optical channel. This parameter is read-only. Each electrical channel has a 4-bit register in register 183 or 184 to define this mapping:

Table 6-44 Lane Mapping Registers (Table 20h Bytes 248-249)

Byte	Bit	Name	Description	PC	AC	AO	SM
248	7-4	Mapping Lane 1	Line side mapping for electrical channel 1 (see Table 6-45)	O	O	O	O
	3-0	Mapping Lane 2	Line side mapping for electrical channel 2 (see Table 6-45)	O	O	O	O
249	7-4	Mapping Lane 3	Line side mapping for electrical channel 3 (see Table 6-45)	O	O	O	O
	3-0	Mapping Lane 4	Line side mapping for electrical channel 4 (see Table 6-45)	O	O	O	O

And the mapping is defined in Table 6-45.

Table 6-45 Lane Mapping Enumeration

Value	Description
0	Not determined or not supported. This means that the data from the electrical lane could be spread amongst any optical lane and between LSB and MSB. This may be the case for example, in FEC encoded data or Gray mapped data. Use this value also to mean that lane mapping is not supported.
1	Optical Lane 1, LSB. This means that all of the data from the electrical lane appears on optical lane 1 in the LSB.
2	Optical Lane 1, MSB. This means that all of the data from the electrical lane appears on optical lane 1 in the MSB.
3	Optical Lane 2, LSB. This means that all of the data from the electrical lane appears on optical lane 2 in the LSB.
4	Optical Lane 2, MSB. This means that all of the data from the electrical lane appears on optical lane 2 in the MSB.
5	Optical Lane 1. This means that all of the data from the electrical lane appears on optical lane 1, but it might be LSB or MSB or spread between the two based on encoding.
6	Optical Lane 2. This means that all of the data from the electrical lane appears on optical lane 2, but it might be LSB or MSB or spread between the two based on encoding.
7-12	Reserved
13-15	Vendor specific mapping

6.7.2.7 Other Configuration Registers

This section contains a single bit that enables the host to reset the module error counters so that a recent BER can be presented. Other bits and registers are reserved.

Table 6-46 Other Configuration Registers (Table 20h Bytes 250-255)

Byte	Bit	Name	Description	PC	AC	AO	SM
250	7	Error Reset	1b = Reset error counters (clears back to zero automatically when the counters have been reset)	O	O	O	O
	6-0	Reserved	Reserved	-	-	-	-
251-255	All	Reserved	Reserved	-	-	-	-

6.7.2.8 Threshold Registers

This section contains the 16 threshold register sets against which the various parameters are to be compared to determine if an alarm or warning flag should be generated. Each threshold set has 4 2-Byte registers ordered most significant byte-first, and the registers are in the same order as other threshold registers in SFF-8636: alarm high threshold, alarm low threshold, warning high threshold, warning low threshold. The units of the threshold values are identified by the corresponding parameter value which is assigned to the threshold set.

Table 6-47 Threshold Registers (Page 21h Bytes 128-255)

Byte	Bit	Name	Description	PC	AC	AO	SM
128-135	All	Param Threshold Set 1	Threshold set 1, same order as other SFF-8636 threshold sets	O	O	O	O
136-143	All	Param Threshold Set 2	Threshold set 2, same order as other SFF-8636 threshold sets	O	O	O	O
144-151	All	Param Threshold Set 3	Threshold set 3, same order as other SFF-8636 threshold sets	O	O	O	O
152-159	All	Param Threshold Set 4	Threshold set 4, same order as other SFF-8636 threshold sets	O	O	O	O
160-167	All	Param Threshold Set 5	Threshold set 5, same order as other SFF-8636 threshold sets	O	O	O	O
168-175	All	Param Threshold Set 6	Threshold set 6, same order as other SFF-8636 threshold sets	O	O	O	O
176-183	All	Param Threshold Set 7	Threshold set 7, same order as other SFF-8636 threshold sets	O	O	O	O
184-191	All	Param Threshold Set 8	Threshold set 8, same order as other SFF-8636 threshold sets	O	O	O	O
192-199	All	Param Threshold Set 9	Threshold set 9, same order as other SFF-8636 threshold sets	O	O	O	O
200-207	All	Param Threshold Set 10	Threshold set 10, same order as other SFF-8636 threshold sets	O	O	O	O
208-215	All	Param Threshold Set 11	Threshold set 11, same order as other SFF-8636 threshold sets	O	O	O	O
216-223	All	Param Threshold Set 12	Threshold set 12, same order as other SFF-8636 threshold sets	O	O	O	O
224-231	All	Param Threshold Set 13	Threshold set 13, same order as other SFF-8636 threshold sets	O	O	O	O
232-239	All	Param Threshold Set 14	Threshold set 14, same order as other SFF-8636 threshold sets	O	O	O	O
240-247	All	Param Threshold Set 15	Threshold set 15, same order as other SFF-8636 threshold sets	O	O	O	O
248-255	All	Param Threshold Set 16	Threshold set 16, same order as other SFF-8636 threshold sets	O	O	O	O

6.7.3 Diagrams for PAM4 Monitored Parameters

Figure 6-1 below shows a general block diagram of the optical ingress path of a module showing the location where the SNR and level transition parameters are measured.

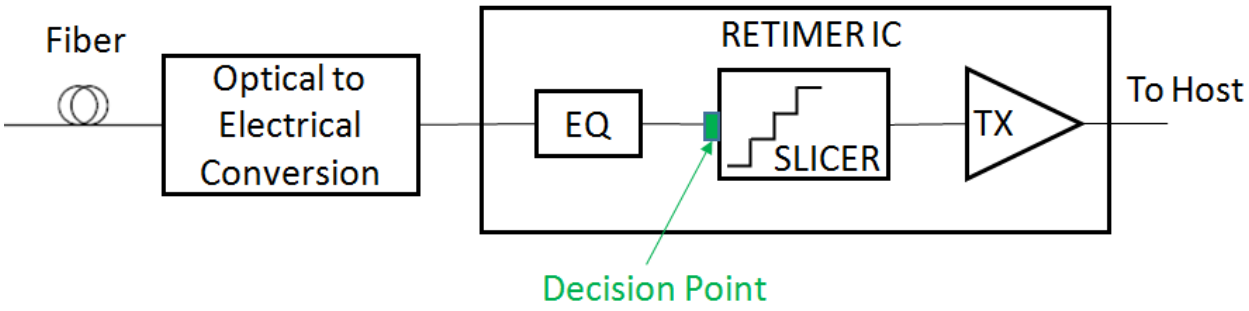

Figure 6-1 Optical ingress path of Module

Figure 6-2 is a view of the aggregate PAM4 data expressed as a histogram measured at a vertical slice in the center of the eye, showing the measurement method for SNR and level transition parameters.

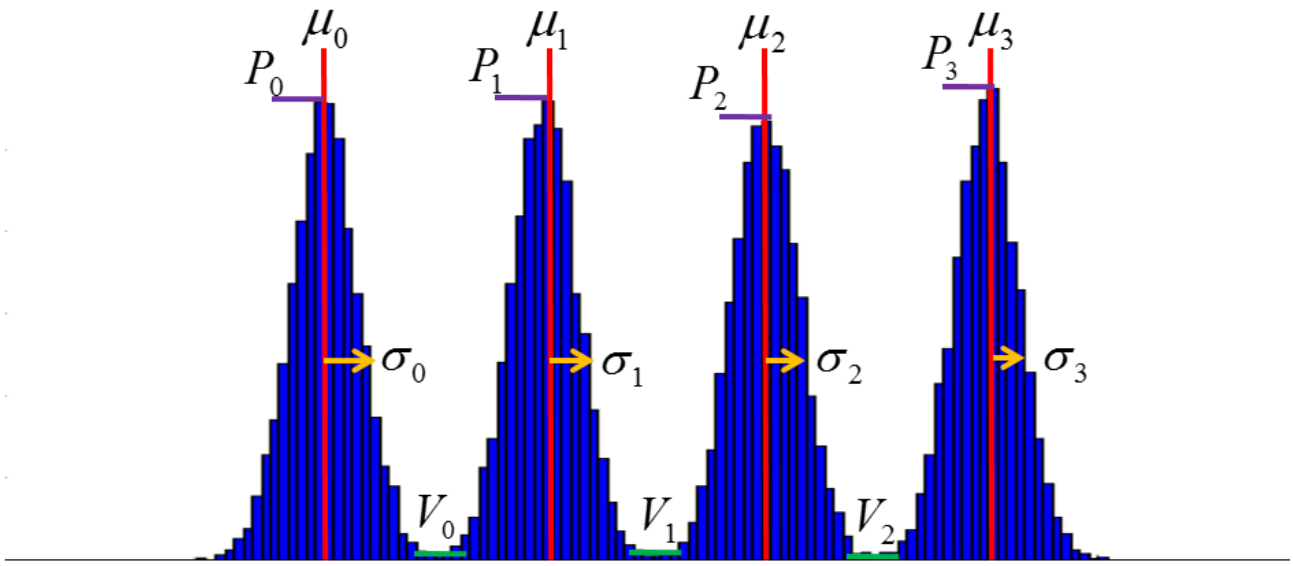

Figure 6-2 PAM4 vertical slice histogram

The histogram x-axis is in bins and the y-axis is in number of bin hits. The number of bins and the hit count magnitude is vendor specific. The histogram is taken at the point in the time domain where data is converted from analog to digital. The PAM4 slicer determines the best points to split the data between values of 0, 1, 2 or 3. The peak is the bin with the largest number of counts between any two valleys (or below valley 1/above valley 3 for the first and last peaks). The valley location is determined by the slicer, and is the bin number where data below is considered to be i and data above is considered to be i+1.

The calculations for the reported eye parameters are:

SNR = $10^* \log_{10}(\min\{SNR_0, SNR_1, SNR_2\})$ where $SNR_i = (\mu_{i+1} - \mu_i)/(\sigma_{i+1} + \sigma_i)$, expressed in 1/256 dB units

LTP = $10^* \log_{10}(\min\{LTP_0, LTP_1, LTP_2\})$ where $LTP_i = (P_{i+1} + P_i)/(2V_i)$, expressed in 1/256 dB units

Where,

μ_i: level of ith peak, optionally averaged over neighboring bins
σ_i: std dev of ith peak, optionally averaged over neighboring bins
P_i: height of ith peak, optionally averaged over neighboring bins
V_i: height of ith valley, optionally averaged over neighboring bins

For the vendor specified wavelength, the accuracy of the reported SNR and LTP parameters shall be better than +/-3 dB over specified temperature and voltage.

6.7.4 Detailed Description of Additional Monitored Parameters for PAM4

6.7.4.1 SNR

This feature measures the electrical signal-to-noise ratio on the ingress optical channel, as defined in Figure 6-2. It is the minimum of the individual eye SNR values, where the SNRi for each of the three eyes is defined as the ratio of the difference of the mean voltage between neighboring levels divided by the sum of the standard deviations of the two neighboring levels.

SNR is encoded as a 16-bit unsigned integer in units of 1/256 dB. For example a value of 1380h is interpreted as an SNR of 19.5 dB.

6.7.4.2 Residual ISI/Dispersion:

Chromatic dispersion is monitored at TP3 and will report the same value as an external dispersion meter (e.g., an optical vector analyzer) would report. The units are 0.1 ps/nm. For the vendor specified wavelength and line width, the accuracy of the reported Residual ISI/Dispersion parameter shall be better than +/-100 ps/nm over specified temperature and voltage.

6.7.4.3 PAM Level Transition Parameter

This feature measures the electrical level slicer noise, as defined in Figure 6-2. It is the minimum of the individual PAM level LTP values, where the LTP for each PAM level is defined as the average of the peak histogram intensity of neighboring PAM levels divided by the minimum histogram intensity between them. Both the SNR and LTP parameters measure signal-to-noise but the LTP parameter is more sensitive to a noise floor.

PAM Level Transition Parameter is encoded as a 16-bit unsigned integer in units of 1/256 dB. For example a value of 3080h is interpreted as an LTP of 48.5 dB. It is possible that the minimum histogram intensity between PAM levels is actually zero in which case this parameter would be infinite. In this case the special value of FFFFh is used. If the parameter measures a value of greater than 255.996 dB but is not infinite, then FFFEh is used.

6.7.4.4 Error Figures

Frame error rate is reported in RS(544,514) FEC equivalent frames (see IEEE 802.3 Clause 91.5). If the actual FEC is not RS(544,514) then the measured frame error rate is converted. So for example, if the FEC frame size is 10% larger than the RS(544,514) FEC frame, then the reported frame error rate will be 10% higher than the measured frame error rate. This is done so as to be able to compare frame error rates regardless of the FEC encoding employed.

Two different error figures may be supported:

- RS(544,514) Frame Error Rate (FER): This parameter measures the uncorrected/errored RS(544,514) equivalent frames per second.
- Pre-FEC Bit Error Ratio (BER): This is the total number of errored bits that were corrected by the FEC during

an interval divided by the total number of bits received in the interval. Note that different FEC schemes have different maximum pre-FEC BER requirements for a specific corrected BER maximum target.

Both the BER and the FER are monitored using the following technique:

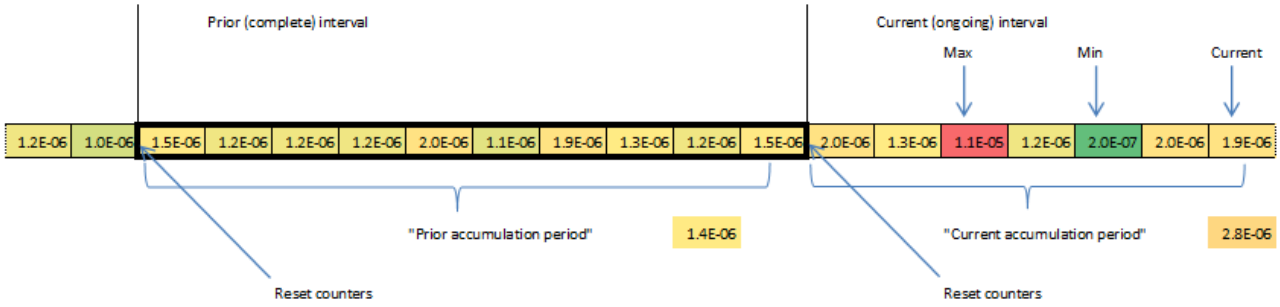

Figure 6-3 Error rate accumulation intervals

The module shall collect BER/FER data over a vendor-specific fine time slice, defined by the module (for example, 1 ms). The host may read the data at a slower rate.

The module calculates a BER/FER at each fine interval (light borders). The Host may have performance monitoring intervals (dark borders). Figure 6-3 shows a series (in time) of fine intervals punctuated by counter reset events that demark the host monitoring interval. If supported by the module, the host can read various calculated values. The selection of the which value(s) is/are available depends on the parameter type identifier (see Table 6-43).

Current:

If supported, the module shall keep a recent reading for the host to read at any time. This is referred to as the "instantaneous" value. For this value, a parameter type (See Table 6-43) of 12 for BER or 15 for FER is used.

Average:

If supported by the module, the average value shall be determined by using the counters reset function to program the averaging time interval. The module shall report a continuously averaged reading over the entire averaging interval. For this value, a parameter type of 4 for BER or 5 for FER is used. This value provides a glimpse as to how the current monitoring interval is performing. The module shall reset the counters for this purpose upon a write of 1b to register 250, bit 7 on page 20h.

Prior Period:

This value is the total averaged in the last monitoring interval as defined by the two most recent counter reset events. This is provided to assure that an interval can be calculated regardless of how quickly the host is reading the data.

If supported, the module shall allow the host to continue to read the BER/FER that was averaged between the last two counter reset events (i.e. between the two dark lines in Figure 6-3). For this value, a parameter type of 12 for BER and 16 for FER is used. The module shall reset the counters for this purpose upon a write of 1b to register 250, bit 7 on page 20h.

Latched Maximum/Maximum:

This is the largest/smallest fine-interval calculation since the last time the host read the data. The host can then

keep track of the maximum of these readings to report as an overall maximum/minimum within its performance monitoring interval.

If supported, the module shall latch the lowest and highest (respectively) measurements it has calculated over any fine interval since the last time the host read each value. The module shall clear the corresponding latch when the host reads the value. These values are not cleared with the counters reset feature. For these values, a parameter type of 9 for BER minimum, 10 for BER maximum, 13 for FER minimum, and 15 for FER maximum is used.

Note that the thresholds system is maintained for BER and FER, but the low thresholds should be 0, and the high threshold for FER should also be 0 unless other error correcting schemes are present.

The error parameters are interpreted as an unsigned 16-bit floating point number with 5 bits for base-10 exponent, offset by -24, and 11 bits for mantissa. Thus the format is:

$$m * 10^{s+o}$$

Where m ranges from 0 to 2047 (11 bits), s ranges from 0 to 31 (5 bits) and o is fixed at -24. The smallest non-zero number is m=1 and s=0 or 1*10^(-24). The largest number supported is m=2047 and s=31, or 2.047*10^10. Within the 2 bytes of the value (stored lowest byte first), m and s are encoded as follows:

Table 6-48 Encoding for BER/FER

Byte	Bits	Description
1	7:3	Exponent (s)
1	2:0	Mantissa (m), bits 10:8
2	7:0	Mantissa (m), bits 7:0

6.7.5 Detailed Description of Additional Monitored Parameters for DWDM

6.7.5.1 TC Current

If supported, this parameter monitors the amount of current flowing to the TC of a cooled laser.

It is a 16-bit signed 2s complement value in increments of 0.1 mA. Thus the total range is from -3.2768 A to +3.2767 A.

6.7.5.2 Laser Frequency

If supported, this parameter monitors the difference (in frequency units) between the target center frequency and the actual current center frequency. It is a similar measurement to the Laser Temperature except expressed as a frequency difference instead of a temperature difference, and vendors may support one or the other measurement, or both.

It is a 16-bit signed 2s complement value in increments of 10 MHz. Thus the total range is from -327.68 GHz to 327.67 GHz.

6.7.5.3 Laser Temperature

If supported, this parameter monitors the laser temperature difference between the target laser temperature for a cooled laser, and the actual current temperature. It is a similar measurement to the Frequency Error except expressed as a temperature difference instead of a frequency difference, and vendors may support one or the other measurement, or both.

It is a 16-bit signed 2s complement value in increments of 1/256 °C. Thus the total range is from -128 °C to +128 °C.

7 Address A2h Page 22h High Accuracy Timing

Page 22h has been defined for parameters used for enhanced calibration for high accuracy timing. There are two formats depending on the format identifier at the start of the page. The two formats are

- Calibration format for Optical Modules. See Table 7-1 and section 7.4
- Calibration format for Loopback Modules. See Table 7-2 and section 7.5

This specification describes a multi-lane memory map where Lane N is defined to be within (1-8). In SFF-8636 Lanes 1-4 (N=4) applies.

Format ID (Bytes 128-129)

Format ID determines if page 22h contains a valid entry. One of the following valid values determines the format of the definition. The following formats are defined:

- CA1Bh => 'CALB' Calibration format for Optical Modules (see section 7.4)
- 100Bh => 'LOOB' Calibration format for Loopback Modules (see section 7.5)

CC_CALIB (Byte 255)

This check code is a one-byte code that can be used to verify that the 127 bytes of calibration configuration data are correct. It uses byte 128 to 254 inclusive to calculate the check codes. This method is the same as the CC_* check code computation in other tables in the document.

In the discovery of this page the host shall read and validate the format ID bytes 128-129 as well as a checksum CC_CALIB to be as expected before the data of this page is used.

Table 7-1 Register Summary Page 22h – Calibration format for Optical Modules

A2h	Size Bytes	Name	Description
128-129	2	Format ID	CA1Bh – Indicates page 22h has the calibration format for Optical Modules
130-149	20	Common Header	Common Header, see section 7.3
150	1	Nb_Lanes	Number of lanes for which delays are specified in the module. For SFF-8636 this value is 4.
151	1	Op_Mode_Id	ID of the "Operational mode" associated with the values of the page. For SFF-8636 this value is 0.
152-154	3	Rx_Pwr_Dly(0)	Curve coefficient for RX optical power dependent delay
155-157	3	Rx_Pwr_Dly(1)	Curve coefficient for RX optical power dependent delay
158-160	3	Rx_Pwr_Dly(2)	Curve coefficient for RX optical power dependent delay
161-163	3	Rx_Pwr_Dly(3)	Curve coefficient for RX optical power dependent delay
164-166	3	Rx_Pwr_Dly(4)	Curve coefficient for RX optical power dependent delay
167-168	2	T_Detune_Offset	Temperature dependent laser wavelength de-tuning offset
169-170	2	T_Detune_Slope	Temperature dependent laser wavelength de-tuning slope
171-174	4	Delta_Rx_Max	Largest value of the 3-sigma standard deviations of all (four for SFF-8636) reported Average Receiving delays, in ns
175-178	4	Delta_Tx_Max	Largest value of the 3-sigma standard deviations of all (four for SFF-8636) reported Average Transmitting delays, in ns
179-182	4	Avg_Rx_Lane	Average Receiving delay on Lane 1, in ns
183-186	4	Avg_Tx_Lane	Average Transmitting delay on Lane 1, in ns
187-190	4	Avg_Rx_Lane	Average Receiving delay on Lane 2, in ns
191-194	4	Avg_Tx_Lane	Average Transmitting delay on Lane 2, in ns
195-198	4	Avg_Rx_Lane	Average Receiving delay on Lane 3, in ns
199-202	4	Avg_Tx_Lane	Average Transmitting delay on Lane 3, in ns
203-206	4	Avg_Rx_Lane	Average Receiving delay on Lane 4, in ns
207-210	4	Avg_Tx_Lane	Average Transmitting delay on Lane 4, in ns
211-254	44	Reserved 00h	All bytes 00h
255	1	CC_CALIB	Checkcode over bytes 128-254

See 7.4 Calibration format for Optical Modules.

Table 7-2 Register Summary Page 22h – Calibration format for Loopback Modules

A2h	Size Bytes	Name	Description
128-129	2	Format ID	100Bh – Indicates page 22h has the calibration format for Loopback Modules
130-149	20	Common Header	Common Header, see section 7.3
150-153	4	Calibration Inaccuracy	Largest value of the 3-sigma standard deviations of all reported delays.
154	1	Reserved 00h	Byte 00h
155-158	4	Tx1_to_Rx1 Delay	Delay from looped back Tx1 to Rx1 port
159	1	Reserved 00h	Byte 00h
160-163	4	Tx1_to_Mon1 Delay	Delay from Tx1 port to Mon1 monitoring connector
164	1	Reserved 00h	Byte 00h
165-168	4	Rx1_to_Mon1 Delay	Delay from Rx1 port to Mon1 monitoring connector
169	1	Reserved 00h	All bytes 00h
170-173	4	Tx2_to_Rx2 Delay	Delay from looped back Tx2 to Rx2 port
174-177	4	Tx2_to_Mon2 Delay	Delay from Tx2 port to Mon2 monitoring connector
178-181	4	Rx2_to_Mon2 Delay	Delay from Rx2 port to Mon2 monitoring connector
182-185	4	Tx3_to_Rx3 Delay	Delay from looped back Tx3 to Rx3 port
186-189	4	Tx3_to_Mon3 Delay	Delay from Tx3 port to Mon3 monitoring connector
190-193	4	Rx3_to_Mon3 Delay	Delay from Rx3 port to Mon3 monitoring connector
194-197	4	Tx4_to_Rx4 Delay	Delay from looped back Tx4 to Rx4 port
198-201	4	Tx4_to_Mon4 Delay	Delay from Tx4 port to Mon4 monitoring connector
202-205	4	Rx4_to_Mon4 Delay	Delay from Rx4 port to Mon4 monitoring connector
206-254	49	Reserved 00h	All bytes 00h
255	1	CC_CALIB	Checkcode over bytes 128-254

See 7.5 Calibration format for Loopback Modules.

This page 22h is read-only by the host application to avoid accidental erasures of the contents of the page. However, the module shall support a method to allow the content of this page to be written via the 2-wire interface. This allows outsourcing of high accuracy calibration to a specialized third party.

The method to write to this page is currently not defined here in this specification and is left to the manufacturer.

7.1 Definition of time reference planes and delays associated

The delay calibration parameters stored in page 22h apply to delays between electrical and optical time reference planes (also called phase planes). These reference planes are:

- **Electrical reference plane:** If connectors are used that specify their reference plane (like many RF connectors) then that reference plane shall be used. Otherwise the electrical reference plane shall be the landing spot of the contact finger.
- **Optical reference plane:** The fiber physical contact plane.

Manufacturers shall specify the reference planes that apply to the calibration of their modules.

7.1.1 Delays associated with Optical Modules

All Rx delays are from optical reference plane to electrical reference plane; all Tx delays are from electrical reference plane to optical reference plane.
The module is characterized (in each direction) by two types of delays:

- Avg_Rx/Tx_LaneN: an average delay, and
- Delta_Rx/Tx_Max: a 3 sigma deviation from the average delay to take into account variations that can

occur between different units of the same module type and over the lifetime of the device, and calibration inaccuracies.

IEEE Std 1588 allows for the compensation of known delays and their asymmetries in the ingress and egress paths. The average delay (Avg_Rx/Tx_LaneN) is used by the host of the module as input for this compensation. When a module has multiple lanes, the host will select one of the lanes for sending the PTP messages. Therefore the host needs the average delay value for each lane. The remaining unknown residual delay cannot be compensated for, but the value of Delta_Rx/Tx_Max can be used to estimate the remaining inaccuracy of the module after compensation of the average value. As the choice of the lane for PTP cannot be controlled outside the host, a single value (worst-case, i.e. maximum over all its lanes) is sufficient per module. More details about the role of the host can be found in IEEE 802.3cx-2023.
The actual Receiver delay of a lane "N" (Rx_delay_LaneN) of the module (in a given operational mode) is statistically bounded by the 3 sigma range;

7.1.1-(1) $Avg\_Rx\_LaneN - Delta\_Rx\_max \leq Rx\_Delay\_LaneN \leq Avg\_Rx\_LaneN + Delta\_Rx\_max$

Similarly, the actual Transmitter delay of a lane "N" (Tx_Delay_LaneN) of the module (in a given operational mode) is bounded by the 3 sigma range;

7.1.1-(2) $Avg\_Tx\_LaneN - Delta\_Tx\_max \leq Tx\_Delay\_LaneN \leq Avg\_Tx\_LaneN + Delta\_Tx\_max$

The number of lanes defined in SFF-8636 is 4.

7.1.2 Delays associated with Loopback Modules

A Calibration Loopback Module (Figure 7-1) provides calibrated access to the electrical reference plane (see 7.1) of the module's connector to enable electrical absolute calibration of equipment that use optical modules.

The module is characterized by:

- TxN_to_RxN, TxN_to_MonN and RxN_to_MonN: four (N=[1-4]) sets of average delays between the respective ports of the module, and
- Calibration Inaccuracy: largest value of the 3-sigma standard deviations of all reported delays.

Note: This method originates from H. Peek and P. Jansweijer, "White Rabbit Absolute Calibration."

7.2 Numeric Formats

The calibration parameters in this page use numeric fixed-point arithmetic formats described in sections 7.2.1 to 7.2.6. The fixed-point arithmetic format notation used is: q<Number of bits for integer part>.< Number of bits for fractional part >. The value in this format is obtained by multiplying the original value by $2^{<\text{ Number of bits for fractional part }>}$. For example, 2.5 ns is expressed in q48.16 format as 0000 0000 0002 8000h.

NOTE: These numeric formats used for time are similar to the IEEE Std 1588 Time Interval data type (q48.16), which is used to store ingress/ingress latencies, such that conversions and calculations are simple.

7.2.1 Description of the q16.16 format for time delay

Time in ns is represented by a fixed-point unsigned 32-bit integer in q16.16 format. The range of delays that can be represented is from 0 to 65 μs (2^{16} ns) with a granularity of 15 fs ($1/2^{16}$ ns).

7.2.2 Description of the q8.16 format for time correction

Time correction in ns is represented by a fixed-point signed two's complement 24-bit integer in q8.16 format. The range of delays that can be represented is [-128.0000 to +127.9999] ns with a granularity of 15 fs ($1/2^{16}$ ns).

7.2.3 Description of the q8.8 format for temperature

Temperature in ºC is represented by a fixed-point signed two's complement 16-bit integer in q8.8 format. The range of temperature that can be represented is [-128 to +127.996] ºC with a granularity of $1/2^8$ ºC.

7.2.4 Description of the q8.8 format for wavelength correction

Wavelength correction in $1/10^{th}$ of a nm (0.1 nm) is represented by a fixed point signed two's complement 16-bit integer in q8.8 format. The range of wavelength that can be represented is [-12.8 to +12.7996] nm with a granularity of 0.4 pm ($1/2^8$ * 0.1 nm).

7.2.5 Description of the q8.16 format time correction coefficient

Time correction in ns per dBm^n is represented by a fixed-point signed two's complement 24-bit integer in q8.16 format. The range of coefficient that can be represented is [-128.0000 to +127.9999] ns/dBm^n with a granularity of 15 fs/dBm^n ($1/2^{16}$ ns/dBm^n). The "n" is the order of the coefficient.

7.2.6 Description of the q8.8 format for wavelength correction rate (temperature change)

Wavelength correction in 1/100 of a nm (0.01 nm) per ºC is represented by a fixed point signed two's complement 16-bit integer in q8.8 format. The represented range is [-1.28 to +1.27996] nm/ºC with granularity of 0.04 pm/ºC ($1/2^8$ * 0.01 nm/ºC).

7.3 Common Header Section

Table 7-3 Register Groups for Page 22h

A2h	Size Bytes	Name	Description
130	1	Version	This version number shall be 01h
131-133	3	Calibration Date	
134-139	6	Cal Uniq ID	Calibration Unique Identifier (CUI). Calibration Responsible
140	1	Stratum	Calibration Stratum. 0 is the highest precision.
141-149	9	Reserved	Common header section. Reserved 00h.

7.3.1 Version (Byte 130)

This is the version number that describes this memory map format. It shall be set to 1.

7.3.2 Calibration Date (Bytes 131-133)

The 3 bytes define the "Calibration Date" which is the date at which the calibration for this module was validated.

Each field described below cannot be all "1"s. If any field is invalid because the field is set to all 1s bit value, then the Calibration Date is deemed invalid.

Table 7-4 Page 22h High Accuracy Timing Calibration Date Encoding

A2h	Bit	Name	Description
131	7-0	Year encoding	This byte conveys the Year encoding. YEAR = Byte131 + 2000. Byte131 = FFh means this year encoding is not valid/defined.
132	7-4	Month Encoding	These 4 bits define the Month encoding. MONTH = Byte132.7-4.
	3-0	Day Encoding	See Byte133.7. Day encoding is a 5-bit value. These 4 bits are the upper bits of the 5-bit value.
133	7	Day Encoding	This bit defines the least significant bit of the day encoding. DayByte = (Byte132.3-0)<<1) + Byte133.7 DAY = DayByte + 1.
	6-0	Number Encoding	Number in the range 0 to 126 is assigned such that multiple calibrations done in one day can be distinguished. The number value of 127 is considered not valid.

As an example, December 29, 2024 is encoded as follows:

- Byte 131 = 18h (24d). YEAR = 2000 + 24 = 2024.
- Byte 132 = CEh.
  - Month = Ch (12d).
  - Partial Date value = Eh. (see next line below)
- Byte 133 bit 7 = 0b
  - DATE = (Eh<<1) + 0h + 1 = 1Dh. (29d).

Note that one is added to DayByte ('DayByte+1') so that 31 calendar days can be encoded with the value range from 0 to 30 of DayByte. The value 31 of DayByte (all 1s bit value) is reserved to mean invalid.

7.3.3 Calibration Unique Identifier (CUI) (Bytes 134-139)

The CUI consists of a 48-bit, 6 byte value, representing:

- OUI/CID (Organizational Unique Identifier, assigned by IEEE or Company Identifier). This field identifies the organization that is responsible for the calibration (the Calibration Responsible).
- OSI (Organizational Specific Identifier) assigned by the Calibration Responsible for internal identification (device, version, etc.).

The Calibration Responsible is the organization that performs the calibration which is not necessarily the vendor.

Table 7-5 Page 22h Calibrated Unique ID format

A2h	Size Bytes	Name	Description
134-136	3	OUI/CID	Organization Unique Identifier Company ID (Identifier) - As assigned by IEEE.
137-139	3	OSI	Organization Specific Identifier.

7.3.4 Stratum (Byte 140)

This byte provides stratum value which indicates the length of the calibration chain, i.e. calibrator generation.

Calibration accuracy decreases with each calibrator generation. For example, a QSFP calibration performed using proper equipment would render stratum n=0, such QSFP can become a calibrator. A QSFP calibration performed using a calibrator QSFP with stratum n=0 would render QSFP with stratum = 1 (next calibrator generation), such QSFP can become a calibrator again, and so forth. The n-th generation has Stratum-n (0 being the highest accuracy). When Stratum is unused or undefined this byte should be set to FFh.

NOTE: This value is informative, the inaccuracy of the provided calibration values is provided by calibration inaccuracy bytes (see 7.1.1 and 7.1.2).

7.4 Calibration format for Optical Modules (Bytes 150-254)

Table 7-1 shows the summary of the register definitions when the Format ID is equal to CA1Bh (i.e., the "Calibration format for Optical Modules" is used). The details of the registers are described in this section.

7.4.1 Nb_Lanes (Byte 150)

This unsigned integer value of 1 Byte indicates the number of lanes supported by the module. SFF-8636 supports four lanes so this value is 4. This field is introduced for compatibility of Page 22h with multi-lane modules.

7.4.2 Op_Mode_Id (Byte 151)

This unsigned integer value of 1 Byte indicates the operational mode for which the set of delay values of page 22h are valid.
An operational mode is a given combination of interface speed, DSP algorithms (e.g., FEC schemes), etc… Different operational modes can lead to different delay values. The intention of this field is to identify the operational mode for which the delay values in the page apply. The Id is an arbitrary number set by the module manufacturer. The host is aware of the current operational mode of the module and needs to know the association to the corresponding Id, via configuration. Note that the assumption is that all lanes operate in the same mode, so a single Op_Mode_Id reflects the mode of all lanes.
The module shall support at least one mode and contain at least one page. The default value is 0, which indicates that the module has only a single operational mode it can work in. This is the scope of this document. Modules with multiple operational modes would have one Op_Mode_Id value (different from 0) per mode and one associated page per mode. This is out of scope of this document.

7.4.3 RX Power Dependent Delay (Bytes 152-166)

These bytes provide Rx_Pwr_Dly(4-0) coefficients (see Table 7-1) in q8.16 format (see 7.2.5) of an RX power dependent delay curve that is described by a 4th order polynomial (equation 7.4.3-(1)).

$$\begin{aligned} \text{7.4.3-(1) } Rx\_Pwr\_Dly\_CorN\ (ns) = {} & Rx\_Pwr\_Dly(4) * RxN\_PWR\_dBm^4 + \\ & Rx\_Pwr\_Dly(3) * RxN\_PWR\_dBm^3 + \\ & Rx\_Pwr\_Dly(2) * RxN\_PWR\_dBm^2 + \\ & Rx\_Pwr\_Dly(1) * RxN\_PWR\_dBm + \\ & Rx\_Pwr\_Dly(0) \end{aligned}$$

Where (see Table 7-1)

- Rx_Pwr_Dly(0) is located in bytes 152-154 in format q8.16 (in ns/dBm^0)
- Rx_Pwr_Dly(1) is located in bytes 155-157 in format q8.16 (in ns/dBm^1)
- Rx_Pwr_Dly(2) is located in bytes 158-160 in format q8.16 (in ns/dBm^2)
- Rx_Pwr_Dly(3) is located in bytes 161-163 in format q8.16 (in ns/dBm^3)
- Rx_Pwr_Dly(4) is located in bytes 164-166 in format q8.16 (in ns/dBm^4)

For each of the four lanes (N=[1-4]), the resulting Rx_Pwr_Dly_CorN values shall be converted to the q8.16 format (in ns, see 7.2.2). If the result of the equation 7.4.3-(1) yields a value outside the q8.16 range then the result of Rx_Pwr_Dly_CorN shall be bounded to the respective min or max of the q8.16 format.

The input variable RxN_PWR_dBm in equation 7.4.3-(1) is calculated using 7.4.3-(2).

```
7.4.3-(2) RxN_PWR_dBm = 10 * log10( RxN_Power )
```

The input variable in equation 7.4.3-(2) is RxN_Power (see section 6.2.5). It is read in 0.1 microwatt units and shall be converted into dBm units, RxN_PWR_dBm as per the 7.4.3-(2) equation, before being used in equation 7.4.3-(1) to calculate the output delay correction (Rx_Pwr_Dly_CorN) for Average Receiving delay (Avg_Rx_LaneN, see section 7.1.1) in ns using q16.16 format (see section 7.2.2). The correction shall be applied as follows:

```
7.4.3-(3)      Avg_Rx_LaneN_Corrected = Avg_Rx_LaneN + Rx_Pwr_Dly_CorN
```

Where
- Avg_Rx_LaneN is located in bytes (179-182)+(N-1)*8 (see 7.4.6), in unsigned q16.16 (in ns, see 7.2.1)
- Rx_Pwr_Dly_CorN is the result of 7.4.3-(1) in signed q8.16 (in ns, see 7.2.2)

And the resulting Avg_Rx_LaneN_Corrected is in format q16.16 (in ns, see 7.2.1), it is the average delay, corrected for received power, for the module in the receiver direction of lane N.
The result of equation 7.4.3-(3) should be limited within the range of unsigned q16.16 (see 7.2.1) even if it can yield a value outside of this range.

When the Rx_Pwr_Dly(4-0) fields are not used then the bytes 152-166 shall be set to zero.

7.4.4 T_Detune_Offset (Bytes 167-168), T_Detune_Slope (Bytes 169-170)

These bytes provide T_Detune_Offset and T_Detune_Slope coefficients (see Table 7-1) in equation 7.4.4-(1) that defines temperature-dependent wavelength de-tuning with respect to the specified laser wavelength. When a module has multiple lanes, it is expected that the lasers will have similar thermal behavior. Therefore the characterization of a single laser is sufficient per module.

The input variable in equation 7.4.4-(1) is the temperature in fixed point q8.8 format (see section 7.2.3 and section 6.2.4). The output of the equation is the correction to the specified wavelength, expressed as a fixed point q8.8 value (see section 7.2.4). This means that de-tuning can range from -12.8 nm up to +12.7996 nm, from the specified laser wavelength.

```
7.4.4-(1)     T_Detune (0.1 nm) = T_Detune_Slope * T(C) + T_Detune_Offset
```

Where:
- T_Detune_Offset is in q8.8 (in 0.1 nm, see 7.2.4)
- T_Detune_Slope is in q8.8 (in 0.01 nm/ ºC, see 7.2.6)

When the T_Detune_Slope and T_Detune_Offset fields are not used then the bytes 167-170 shall be set to zero.

The resulting T_Detune value shall be converted to the q8.8 format (see 7.2.4). If the result of the equation yields a value outside the q8.8 range then the result T_Detune shall be bounded to the respective min or max of the q8.8 format.

7.4.5 Delta_Rx_max (Bytes 171-174), Delta_Tx_Max (Bytes 175-178)

The residual delay is indicated in unsigned q16.16 format (see 7.2.1) in ns units. It represents the maximum over all lanes (for SFF-8636 the number of lanes is 4) of the 3-sigma deviations from the average delays in the respective

direction (receiving or transmitting). It is an unknown delay introduced by the device and holds for all reported delays. When related to the average values in section 7.4.6 and 7.4.7, it can be used to classify the synchronization inaccuracy performance of the device.

NOTE: The reported values shall take account of the inaccuracy of the calibration process and calibration generation chain that is indicated by the stratum value, see 7.3.4.

7.4.6 Avg_Rx_LaneN with N=[1-4] for SFF-8636 (Bytes (179-182)+(N-1)*8)

The delay is indicated in unsigned q16.16 format (see 7.2.1) in ns units. It represents the average delay characterized for the module in the Receiver direction of lane N. It is the known delay added by the device, and can be compensated for by the host, e.g., for the purpose of synchronization using IEEE Std 1588.
The register of unused or non-existing lanes is filled with 00h Bytes.

7.4.7 Avg_Tx_LaneN with N=[1-4] for SFF-8636 (Bytes (183-186)+(N-1)*8)

The delay is indicated in unsigned q16.16 format (see 7.2.1) in ns units. It represents the average delay characterized for the module in the Transmitter direction of lane N. It is the known delay added by the device, and can be compensated for by the host, e.g., for the purpose of synchronization using IEEE Std 1588.
The register of unused or non-existing lanes is filled with 00h Bytes.

7.5 Calibration format for Loopback Modules (Bytes 150-254)

Table 7-2 shows the summary of the register definitions when the Format ID (see Section 7) is equal to 100Bh (i.e., the "Calibration format for Loopback Modules" is used). The details of the registers are described in this section.

The Calibration Loopback module connects the TxN and RxN ports on the electrical QSFP connector and probes this electrical loopback connection while forwarding the probed signals with fixed and calibrated delay to the monitoring connector (i.e., MonN, see Figure 7-1). This allows for calibrated access of the electric time reference plane of QSFP/QSFP+ sockets of network devices. The calibrated delays between TxN, RxN and MonN are provided in the bytes defined below.

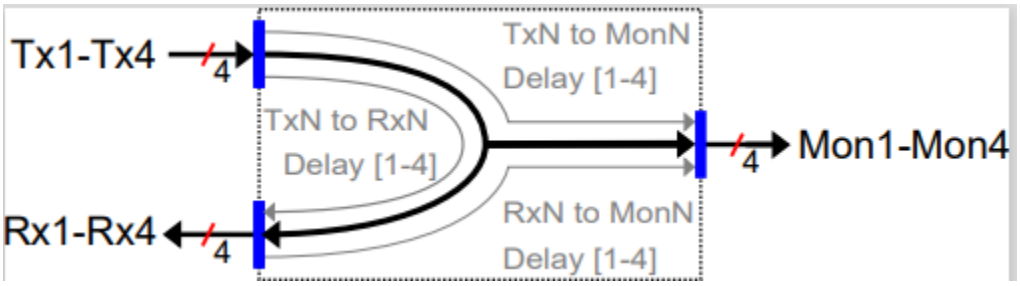

Figure 7-1 Calibration Loopback Module

7.5.1 Calibration Inaccuracy (Bytes 150-153)

The value represents the calibration inaccuracy of the reported delays. It is a 4 byte value in unsigned q16.16 format (see section 7.2.1) in ns units.

NOTE: The reported values shall take account of the inaccuracy of the calibration process and calibration generation chain that is indicated by the stratum value, see 7.3.4.

7.5.2 TxN to RxN Delay with N=[1-4] for SFF-8636 ((Bytes 155-158 for N=1; Bytes 170-173+(N-2)*12 for N[2-4])

TxN-to-RxN Delay is the fixed delay from TxN to RxN port for lane "N" in ns using q16.16 format (see section 7.2.1).

7.5.3 TxN to MonN Delay with N=[1-4] for SFF-8636 ((Bytes 160-163 for N=1; Bytes 174-177 +(N-2)*12 for N[2-4])

TxN-to-MonN Delay is the fixed delay from TxN to the MonN output connector for lane "N" in ns using q16.16 format (see section 7.2.1).

7.5.4 RxN to MonN Delay with N=[1-4] for SFF-8636 ((Bytes 165-168 for N=1; Bytes 178-181 +(N-2)*12 for N[2-4])

RxN-to-MonN Delay is the fixed delay from RxN to the MonN output connector for lane "N" in ns using q16.16 format (see section 7.2.1).

Appendix A. Rate Select and Configuration for Multi-rate Modules (Informative)

The host system (fixed-side) can use the management interface to reconfigure modules (free-side) to operate at different rates or to comply with different specifications. One method of reconfiguration is for the host to write directly, one at a time, to the various controls provided by the module. Alternatively the module may offer optional rate select controls whereby the host writes to a single location and the module firmware makes all necessary adjustments to change operation from one rate to another.

When rate select controls are provided, the module may automatically make changes to the Tx and Rx datapath components, including the ability to:

- Enable/Disable (bypass) Tx and Rx CDRs
- Enable/Disable/Adjust Tx input equalizers and set fixed or adaptive modes of operation
- Enable/Disable/Adjust Rx output emphasis and Rx output amplitude
- Adjust the bandwidth and/or gain of internal components

Various advertising bits state which optional features are implemented by a module. Key bits for this discussion are:

CDR options
Page 00h, byte 129, bits 3-2: CDRs implemented
Page 00h, byte 194, bits 7-6: CDR On/Off Control implemented

Tx Input Equalizer options
Page 00h, byte 193, bit 3: Tx Input Equalizer Auto Adaptive Capable
Page 00h, byte 193, bit 2: Tx Input Equalizer Fixed Programmable Settings
Page 03h, byte 224, bits 7-4: Tx Input Equalizer Maximum Magnitude Supported

Rx Output Emphasis options
Page 00h, byte 193, bit 1: Rx Output Emphasis Control implemented
Page 03h, byte 224, bits 3-0: Rx Output Emphasis Maximum Magnitude Supported
Page 03h, byte 225, bits 5-4: Rx Output Emphasis Type

Rx Output Amplitude options
Page 00h, byte 193, bit 0: Rx Output Amplitude Control implemented
Page 03h, byte 225, bits 3-0: Rx Output Amplitude Codes Supported

Rate Select options
Page 00h, byte 195, bit 5: Rate Select implemented
Page 00h, byte 221, bits 3-2: Rate Selection Type Declaration
Page 00h, byte 141, bits 1-0: Extended Rate Selection Compliance Tags

A.1. Direct Control Configuration

The host system can directly control the CDRs, Tx Input Equalizers, Rx Output Emphasis and Rx Output Amplitude if those options are implemented by the module. After checking the various advertising bits, the host can control these features using the control bits at:

Page 00h, byte 98: Tx and Rx CDR control bits
Page 03h, bytes 234-235: Tx Input Equalizer settings
Page 03h, byte 241, bits 3-0: Tx Input Adaptive Equalizer enable bits
Page 03h, bytes 236-237: Rx Output Emphasis settings

Page 03h, bytes 238-239: Rx Output Amplitude settings

Note that CDRs and Tx input equalizers are designed for operation at the maximum rate specified for the module. For module operation at low rates, the host may need to disable Tx and Rx CDRs and set the Tx input equalizers for 0 dB of equalization.

A.2. Rate Select

If rate select is supported by a module, the host can set up the module for a desired rate using the Tx and Rx rate select control bits (bytes 87-88). There are several advertising bits that tell the host whether the module supports rate select, and which types of rate select are available.

Table A-1 summarizes the advertising bits related to Rate Select support.

Table A-1 Rate Select Advertising Bits

Field	RS supported	RS Type		Ext RS Compliance		
Page	**00h**					
Byte	**195**	**221**		**141**		
Bit	**5**	**3**	**2**	**1**	**0**	**Meaning**
Value	0	X	X	X	X	Rate select not supported. Use manual controls if available.
	1	0	0	X	X	Reserved
		1	1	X	X	Reserved
		1	0	0	0	Reserved
				1	1	Reserved
				0	1	Extended Rate Select Version 1 supported.
				1	0	Extended Rate Select Version 2 supported.
		0	1	X	X	Reserved. Previously used to indicate Application Select Table support.

If the module supports rate select the host can change configuration by using the rate select controls at:

Page 00h, bytes 87-88: Tx and Rx Rate Select control bits

The module is responsible for making all necessary adjustments for operation at the selected rate. These adjustments may include changes to Tx and Rx bandwidths, changes in CDR operation, and adjustments to equalizer, emphasis and amplitude settings, without requiring the host to write those control bits.

If the module makes adjustments to these settings there is no requirement for the module firmware to change the related control bits. For example, if the module bypasses the Tx or Rx CDRs in order to operate at a reduced rate, byte 98 may still be set to show the CDRs enabled.

A.3. Extended Rate Selection

If one of the extended rate select versions is supported, as listed in Table A-2, then the host can use bytes 87-88 to optimize the Tx and Rx data paths for particular signaling rates. Two bits are assigned to each receiver in Byte 87 (Rxn_Rate_Select) and two bits for each transmitter in Byte 88 (Txn_Rate_Select) to specify up to four signaling rates.

Table A-2 XN_Rate_Select with Extended Rate Selection

xN_Rate_Select		Description
MSB	**LSB**	
Version 1 - Page 00h Byte 141 Bit 0 = 1		
0	0	Optimized for signaling rates less than 2.2 GBd
0	1	Optimized for signaling rates from 2.2 up to 6.6 GBd
1	0	Optimized for 6.6 GBd signaling rates and above
1	1	Reserved
Version 2 - Page 00h Byte 141 Bit 1 = 1		
0	0	Optimized for signaling rates less than 12 GBd
0	1	Optimized for signaling rates from 12 up to 24 GBd
1	0	Optimized for signaling rates from 24 up to 26 GBd
1	1	Optimized for 26 GBd signaling rates and above

----------END OF DOCUMENT----------