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SFF-8449

Specification for

Management Interface for SAS Shielded Cables

Rev 2.1a June 15, 2018

Secretariat: SFF TA TWG

Abstract: This specification defines a common management interface for shielded cable assemblies. Physical layer and mechanical details of the connector interface are outside the scope of this document.

This specification provides a common reference for systems manufacturers, system integrators, and suppliers.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

The description of a connector in this specification does not assure that the specific component is actually available from connector suppliers. If such a connector is supplied it must comply with this specification to achieve interoperability between suppliers.

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Change History

Rev 1.7 - Initial release
Rev 1.8 - Table 5-2 editorial changes
- Tables 5-2 and 5-9 changed due to recognition of industry practices
Rev 1.9 - Increased maximum Iman in Table 5-2 from 8mA to 30 mA to enable use of a microcontroller instead of a segmented NVRAM.
Rev 2.0 - Added industry document reference to SFF-8636 and SFF-8644
Rev 2.1 - Updated to SNIA template
- Added tolerance to pull-up resistor value in Table 4-2

Rev 2.1a (June 15,2018)
- Removed watermark

Foreword

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, the membership has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors. The SFF Committee provided a forum for system integrators and vendors to define the form factor of disk drives.

During their definition, other activities were suggested because participants in SFF faced more challenges than the form factors. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

In July 2016, the SFF Committee transitioned to SNIA (Storage Networking Industry Association), as a TA (Technology Affiliate) TWG (Technical Work Group).

Industry consensus is not a requirement to publish a specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF meets during the T10 (see www.t10.org) and T11 (see www.t11.org) weeks, and SSWGs (Specific Subject Working Groups) are held at the convenience of the participants. Material presented to SFF becomes public domain, and there are no restrictions on the open mailing of the presented material by Members.

Many of the specifications developed by SFF have either been incorporated into standards or adopted as standards by ANSI, EIA, JEDEC and SAE.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at:
http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:
http://www.snia.org/sff/specifications/SFF-8000.TXT

If you wish to know more about the SFF TWG, the principles which guide the activities can be found at:
http://www.snia.org/sff/specifications/SFF-8032.PDF

Suggestions for improvement of this specification will be welcome, they should be submitted to:
http://www.snia.org/feedback

CONTENTS

FIGURES

TABLES

1. Scope

This specification defines a management interface for SFF-8644 external cable assembly implementations. The detailed mechanical design is documented in SFF-8644. The interface memory map and protocol operation are also outside the scope of this specification but can be found in SFF-8636. This document provides a detailed description of the electrical interface characteristics.

This approach facilitates a common memory map and management interface for applications with different mechanical, physical layer and otherwise different implementations. For example, SFF-8449 defines a four channel solution which documents the management interface physical layer, references SFF-8636 to ensure compatibility with the common memory map and protocol. See Figure 1-1.

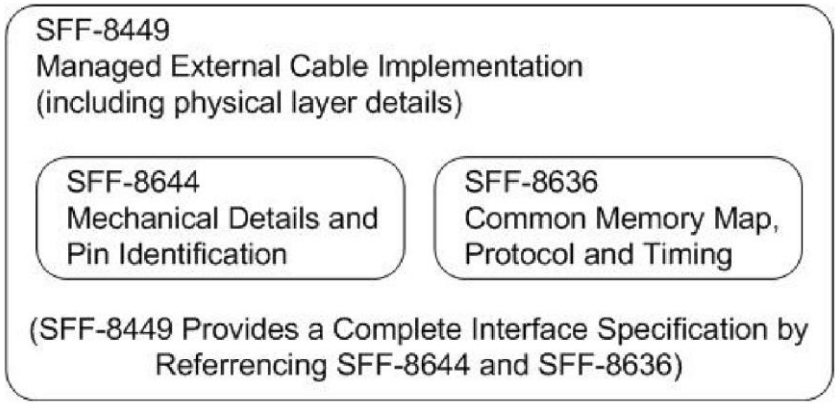

FIGURE 1-1 HIERARCHY OF INTERFACE SPECIFICATIONS (EXAMPLE)

Note that the SFF-8636 memory map is shared amongst multiple standards. SFF-8636 may include signals beyond the scope of the SFF-8449 interface.

1.1 Copyright

receipt. Any denial of permission for the Exception shall include an explanation of such refusal.

1.2 Disclaimer

The information contained in this publication is subject to change without notice. The SNIA makes no warranty of any kind with regard to this specification, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The SNIA shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this specification.

Suggestions for revisions should be directed to http://www.snia.org/feedback/

2. References

2.1 Industry Documents

The following interface standards and specifications are relevant to this specification.

- SFF-8636 Common Management Interface
- SFF-8644 Mini Multilane 12 Gbs 8/4X Shielded Connector

2.2 Sources

There are several projects active within the SFF TWG. The complete list of specifications which have been completed or are still being worked on are listed in http://www.snia.org/sff/specifications/SFF-8000.TXT

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://www.techstreet.com/incitsgate.tmpl).

2.3 Conventions

The dimensioning conventions are described in ANSI-Y14.5M, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

2.4 Definitions

For the purpose of SFF Specifications, the following definitions apply:

Active Cable: In this standard, an active cable requires power for circuitry that is integral to any of the TX/RX high speed serial channels supported by the cable. In addition, the active cable requires power to operate the management interface.

Fixed: Used to describe the gender of the mating side of the connector that accepts its mate upon mating. This gender is frequently, but not always, associated with the common terminology "receptacle". Other terms commonly used are "female" and "socket connector". The term "fixed" is adopted from EIA standard terminology as the gender that most commonly exists on the fixed end of a connection, for example, on the board or bulkhead side. In this specification "fixed" is specifically used to describe the mating side gender illustrated in Figure 2-1.

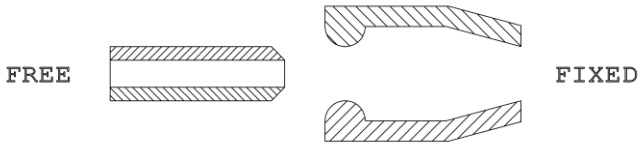

FIGURE 2-1 MATING SIDE GENDER DEFINTION

Free: Used to describe the gender of the mating side of the connector that penetrates its mate upon mating. This gender is frequently, but not always, associated with the common terminology "plug". Other terms commonly used are "male" and "pin connector". The term "free" is adopted from EIA standard terminology as the gender that most commonly exists on the free end of a connection, for example, on the cable side. In this specification "free" is specifically used to describe the mating side gender illustrated in Figure 2-1.

Passive Cable: In this standard, a passive cable only requires power to operate the management interface circuitry.

Reserved: Where this term is used for defining the signal on a connector contact its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields and code values; the bits, bytes, fields and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

3. General Description

The external cable management interface provides a method for the fixed side to determine the characteristics and status of the free side. In some implementations, the interface also provides a mechanism to control the operation of the free side circuitry. For the case where the free side is a cable, the fixed side can determine if the cable is passive, active copper, or active optical. Parameters such as supplier, part number, propagation delay and loss (for passive cables) can also be determined.

3.1 Fixed-to-Free Side Block Diagram

Figure 4-1 depicts the fixed-to-free side management interface. Note the limitations in scope of SFF-8449.

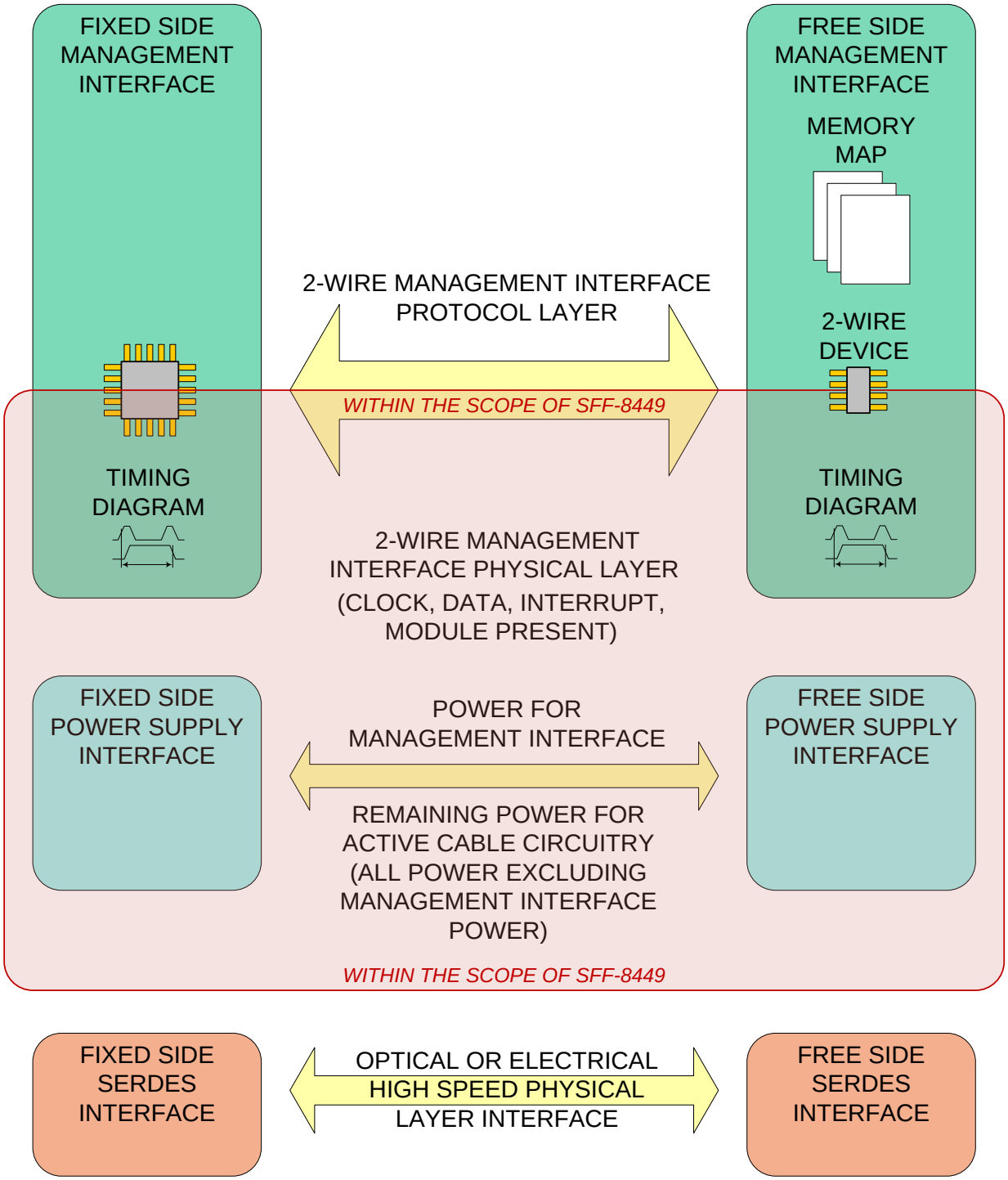

FIGURE 3-1 EXTERNAL CABLE MANAGEMENT INTERFACE BLOCK DIAGRAM

3.2 Physical Cable Assembly Implementation

3.2.1 Direct Attach

Figure 4-2 depicts a direct attach passive, active copper or optical cable interconnect implementation.

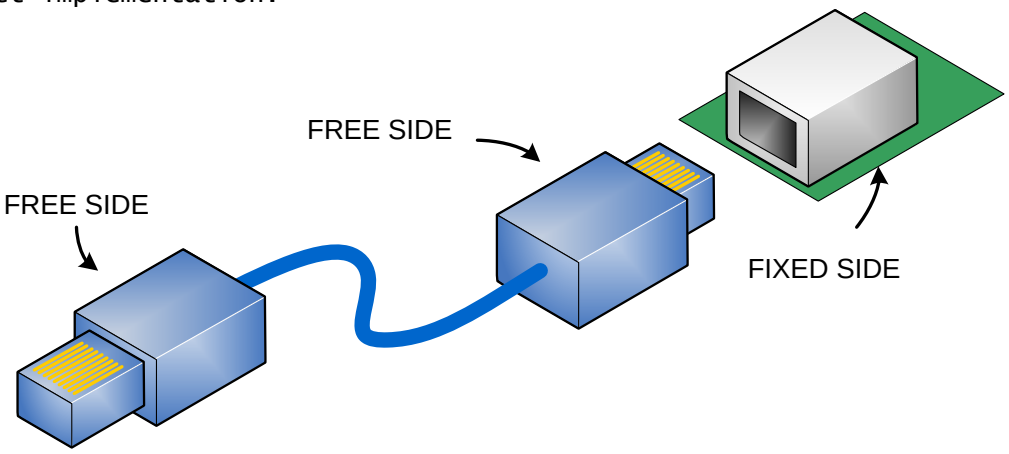

FIGURE 3-2 DIRECT ATTACH CABLE ASSEMBLY IMPLEMENTATION

3.2.2 Management Interface Scope

Figure 4-3 depicts the limited scope of the management and active cable power interfaces. Note that management and power interfaces do not extend from one free side end of the cable to the other.

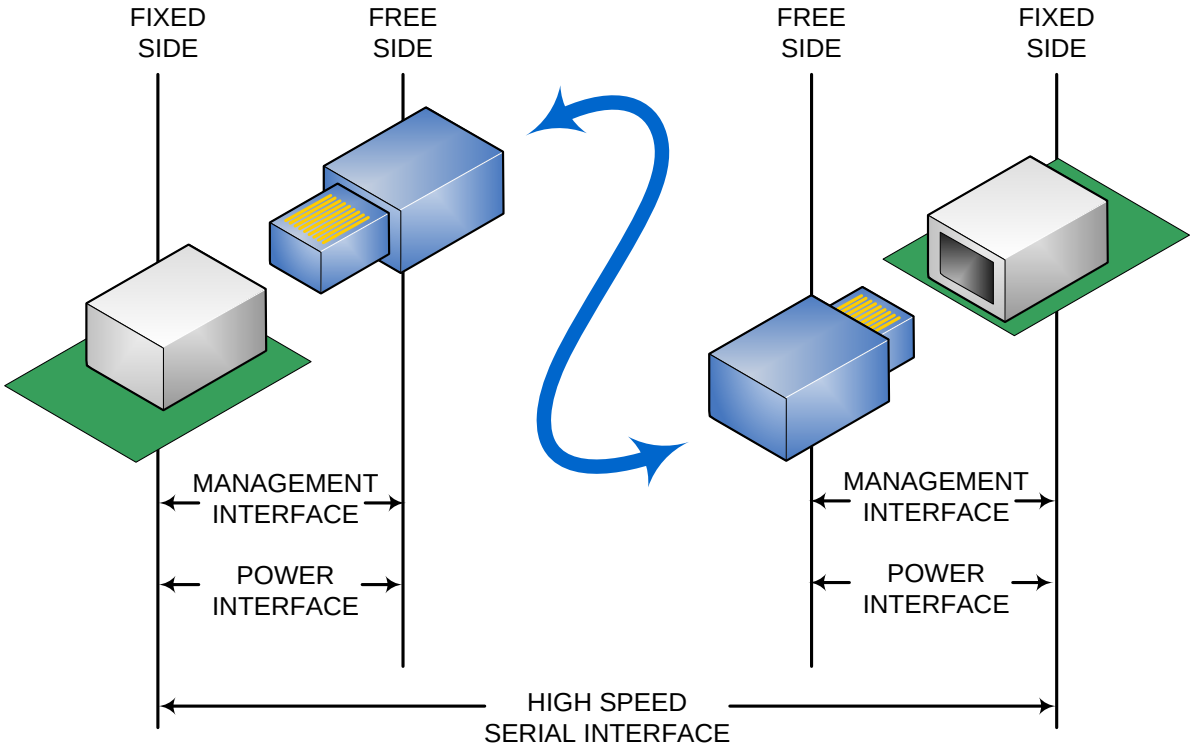

FIGURE 3-3 MANAGEMENT INTERFACE SCOPE

4. High Density (HD) Connector Physical Layer Interface

4.1 Signal Assignment

The fixed and free-side HD connector interface supports four bi-directional high speed differential serial links and a management interface. Table 4-1 identifies all signals of the connector interface.

TABLE 4-1 HD CONNECTOR PHYSICAL LAYER INTERFACE

Signal	Pin	Mating Level	Definition
Reserved	A1	Second	Reserved for future use
IntL	A2	Second	Management interface interrupt signal
GND	A3	First	Signal ground
RX1+	A4	Third	Fixed side receiver channel 1 non-inverting input
RX1-	A5	Third	Fixed side receiver channel 1 inverting input
GND	A6	First	Signal ground
RX3+	A7	Third	Fixed side receiver channel 3 non-inverting input
RX3-	A8	Third	Fixed side receiver channel 3 inverting input
GND	A9	First	Signal ground
Vact	B1	Second	Free side power input for non-management interface circuitry
ModPrsL	B2	Second	Free side active low present output
GND	B3	First	Signal ground
RX0+	B4	Third	Fixed side receiver channel 0 non-inverting input
RX0-	B5	Third	Fixed side receiver channel 0 inverting input
GND	B6	First	Signal ground
RX2+	B7	Third	Fixed side receiver channel 2 non-inverting input
RX2-	B8	Third	Fixed side receiver channel 2 inverting input
GND	B9	First	Signal ground
SCL	C1	Second	Management interface serial clock
SDA	C2	Second	Management interface serial data output
GND	C3	First	Signal ground
TX1+	C4	Third	Fixed side transmitter channel 1 non-inverting output
TX1-	C5	Third	Fixed side transmitter channel 1 inverting output
GND	C6	First	Signal ground
TX3+	C7	Third	Fixed side transmitter channel 3 non-inverting output
TX3-	C8	Third	Fixed side transmitter channel 3 inverting output
GND	C9	First	Signal ground
Vact	D1	Second	Free side power input for non-management interface circuitry
Vman	D2	Second	Free side power input for management interface circuitry
GND	D3	First	Signal ground
TX0+	D4	Third	Fixed side transmitter channel 0 non-inverting output
TX0-	D5	Third	Fixed side transmitter channel 0 inverting output
GND	D6	First	Signal ground
TX2+	D7	Third	Fixed side transmitter channel 2 non-inverting output
TX2-	D8	Third	Fixed side transmitter channel 2 inverting output
GND	D9	First	Signal ground

4.2 High Speed Serial Interface

Electrical characteristics of signals on pins A4, A5, A7, A8, B4, B5, B7, B8, C4, C5, C7, C8, D4, D5, D7 and D8 are outside the scope of this document.

4.3 Management Interface

Pins A1, A2, B1, B2, C1, C2, D1 and D2 comprise the management interface. Note that GND pins A3, A6, A9, B3, B6, B9, C3, C6, C9, D3, D6 and D9 are required for reliable management interface operation although they are not classified as part of the management interface.

4.3.1 Signal Definition

4.3.1.1 Vman

The fixed-side shall provide power for the free-side device management interface circuitry on the Vman signal. Removal of power from the Vman signal shall disable the free-side management circuitry. Upon restoration of power to the Vman signal, the management interface shall perform all necessary power up tasks. The SFF-8449 management interface does not include a dedicated reset signal. To reset the free-side management interface circuitry, the fixed side may cycle power off and on. See table 5-5 for Initialization Time requirements, signal levels and other reset circuitry parameters.

4.3.1.2 Vact

To support active cable designs, the fixed side shall provide power to both Vact pins in addition to the Vman pin. See section 5.4 for electrical requirements. All Vact pins shall be not connected on passive free side designs. Since Vman provides reset functionality for the management interface, no power sequencing requirements for Vman with respect to Vact shall be placed on the fixed side other than those specified in section 5.5.

4.3.1.3 ModPrsL

The fixed-side shall de-assert the active-low ModPrsL signal. When mated with the fixed side, the free-side device shall assert ModPrsL low. During power up initialization, the free-side device shall assert ModPrsL prior to assertion of IntL. ModPrsL shall remain asserted until the free-side device is no longer mated to the fixed side. See section 5.4 for electrical characteristics of the signal, fixed-side and free-side termination characteristics.

4.3.1.4 IntL

The fixed-side shall de-assert the active-low IntL signal. The free-side device shall assert IntL low to indicate that an event has occurred that requires interrupt service. The free-side device shall de-assert IntL after the fixed side has cleared the appropriate interrupt flag bits within the free-side device memory map. In addition, the free-side device indicates completion of reset, including power up initialization by asserting the IntL signal with the Data_Not_Ready (See SFF-8636) bit negated. IntL can be cleared as detailed in SFF-8636. See section 5.4 for electrical characteristics of the signal, fixed-side and free-side termination characteristics. Timing requirements are specified in section 5.5.

4.3.1.5 SCL

Two-wire interface clock.

4.3.1.6 SDA

Two-wire interface data.

4.3.2 Free Side Device Addressing

The SFF-8449 management interface does not provide a mechanism to address individual free-side devices. The fixed-side shall provide an independent physical layer interface for each free-side device. Multiple free-side devices shall not share the same clock and data signals.

4.3.3 DC Electrical Characteristics

TABLE 4-2 DC ELECTRICAL CHARACTERISTICS

Signal	Symbol	Min	Max	Unit	Condition
SCL, SDA (see note 1)	Vol	0	0.4	V	Iol=3.0mA
	Voh	Vman-0.5	Vman+0.3	V	
	Vil	-0.3	Vman*0.3	V	
	Vih	Vman*0.7	Vman+0.5	V	
ModPrsL, IntL (see note 2)	Vol	0	0.4	V	Iol=2.0mA
	Voh	Vman-0.5	Vman+0.3	V	
	Vil	-0.3	Vman*0.3	V	
	Vih	Vman*0.7	Vman+0.5	V	
Management Interface Power Supply Voltage	Vman	3.0	3.6	V	
Management Interface Power Supply Current	Iman	-	30	mA	
Active Circuitry Power Supply Voltage	Vact	-	3.6	V	See section 5.6 for reduced voltage support
Note 1. Fixed side termination impedance to Vman determined by total bus capacitance and the input rise time (outside the scope of this document).					
Note 2. Fixed side termination impedance with a nominal value of 10 kOhm or less and a tolerance no greater than 5%.					

4.3.4 AC Electrical Characteristics

TABLE 4-3 AC ELECTRICAL CHARACTERISTICS

Signal	Max	Unit	Condition
Initialization Time Window	500	ms	
Current Inrush Window Duration	150	us	
Power Supply Noise including ripple	50	mV	1kHz to frequency of operation measured at Vcc host.
Current Inrush Limit with LPMode enabled	600	mA	Occurs within initialization time window. Pulse width less than 50 micro-seconds.
Sustained Initialization Time Current Limit with LPMode enabled	500	mA	Maximum current within initialization time window excluding 50 micro-second current inrush pulse window.
Current Inrush Limit with LPMode disabled	2500	mA	Occurs within initialization time window. Pulse width less than 50 micro-seconds.
Sustained initialization time current with LPMode disabled	750	mA	Maximum current within initialization time window excluding 50 micro-second current inrush pulse window.
Note the Post Initialization Window Current Limit is described in section 5.6.			

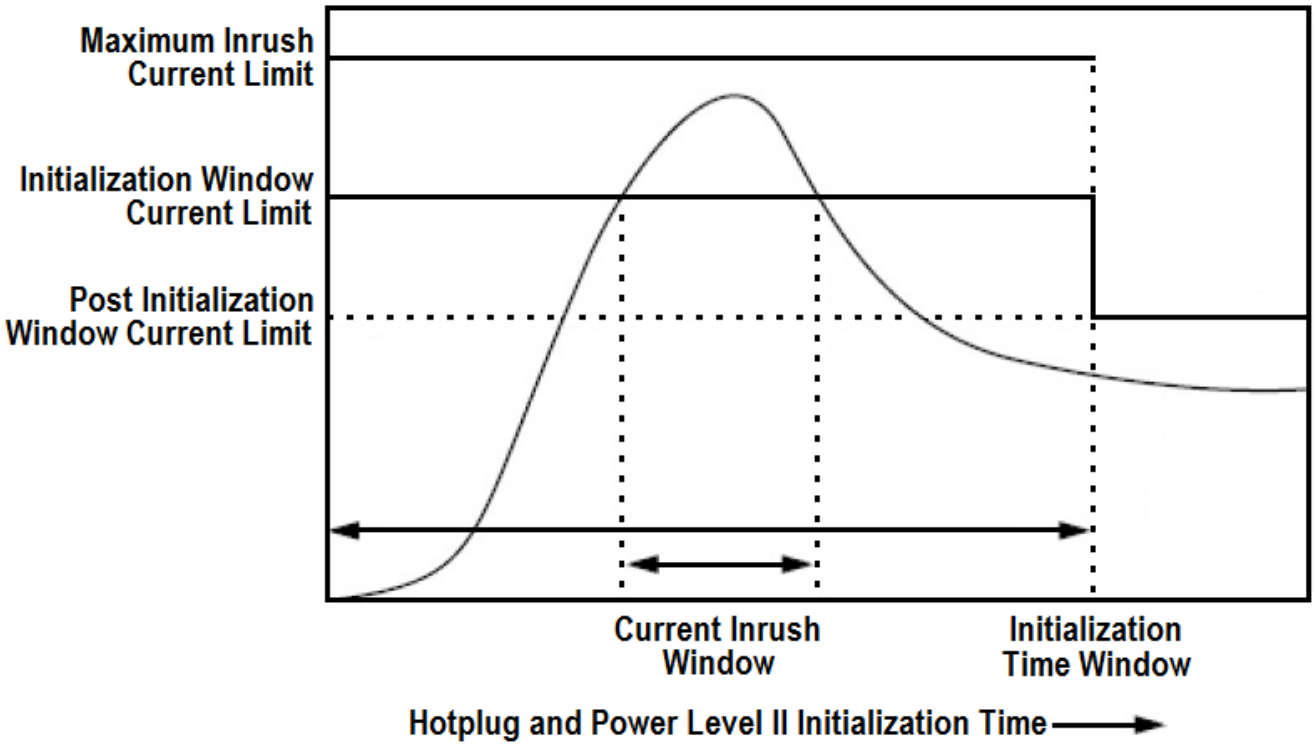

FIGURE 4-1 INRUSH CURRENT (VACT PINS)

4.3.5 Absolute Maximum/ Minimum Ratings

TABLE 4-4 ABSOLUTE MAXIMUM/MINIMUM RATINGS

Signal	Min	Max	Unit	Condition
Vman	-0.3	3.6	V	
Vact	-0.3	3.6	V	
SCL, SDA, ModPrsL, IntL	-0.3	Vman+1.0	V	With respect to GND
Free-side device Vact input capacitance	-	22	uF	Both pins combined. This value includes all variations due to process, voltage and temperature.
Free-side device Vman input capacitance	-	1	uF	This value includes all variations due to process, voltage and temperature.
Free-side device input capacitance for SCL and SDA	-	14	pF	
Note the differential high speed serial receiver input voltage rating is outside the scope of this document.				

4.4 Timing Requirements

The free side device software control and status function timing specifications are described in Table 4-5.

TABLE 4-5 TIMING FOR SOFT CONTROL AND STATUS FUNCTIONS

Parameter	Symbol	Max	Unit	Conditions
Free Side Active Device Initialization Time	t_init	2000	ms	Time from power on[2] or hot plug event until the free side active device is fully functional[3]. Does not include delay due to device interrogation.
Management Interface Initialization Time	t_man_init	2000	ms	Time from application of Vman or hot plug event until the free side device management interface is fully functional. This requirement applies to both passive and active free side designs.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[2] until the free side responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[2] to data not ready, IntL asserted and bit 0 of Byte 2, deasserted. See SFF-8636.
LPMode Assert Time	ton_LPMode	100	us	Delay from low power mode enable until the free side device power consumption does not exceed Power Level 1. See SFF-8636.
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL	500	us	Time from clear on read[4] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits. See SFF-8636.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted. See SFF-8636.
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted. See SFF-8636.
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and IntL asserted. See SFF-8636.
Mask Assert Time	ton_mask	100	ms	Time from mask bit set (value = 1b)[1] until associated IntL assertion is inhibited . See SFF-8636.
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared (value = 0b)[1] until associated IntL operation resumes. See SFF-8636.
Application or Rate Select Change Time	t_ratesel	100	ms	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification. See SFF-8636.
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set (value = 1b)[1] until module power consumption reaches Power Level 1. See SFF-8636.
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared (value = 0b)[1] until the module is fully functional[3] See SFF-8636.
Note 1. Measured from falling clock edge after stop bit of write transaction				
Note 2. Active free side device power on is defined as the instant when all supply voltages reach and remain at or above the minimum level specified in Table 5-2				
Note 3. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2, deasserted. The module should also meet optical and electrical specifications.				
Note 4. Measured from falling clock edge after stop bit of read transaction				

Timing requirements for TX and RX disable controls are defined in Table 4-6.

TABLE 4-6 DISABLE CONTROL TIMING

Parameter	Symbol	Max	Unit	Conditions
Tx Disable Assert Time	ton_txdis	100	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal. See SFF-8636.
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal. See SFF-8636.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal. See SFF-8636.
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal. See SFF-8636.
Note 1: Measured from falling clock edge after stop bit of write transaction				

4.5 Power Consumption Modes

The management interface provides a mechanism to limit free side device power consumption by the Vact power inputs.

If the Power Override read/write bit (See SFF-8636, page 00h, byte 93, bit 0) is low, then the free-side device power is in the low power mode and power consumption shall be 1.5W or less. If the Power Override bit is in the high state and the Power Set read/write bit (see SFF-8636, page 00h, byte 93, bit 1) is low, then the free-side device power consumption may be greater than 1.5W. For the latter case, the Extended Identifier read-only bits (see SFF-8636, page 00h, byte 129, bits 6-7) indicate the maximum consumption for the specific free-side device.

If the Extended Identifier bits indicate power consumption greater than 1.5W and the free side device is in low power mode, then the free side device shall reduce power consumption to 1.5W or less. The exact method of reducing power consumption is not specified. However, it is likely that either the Tx or Rx or both will not be operational in this state.

If both Extended Identifier bits are in the low state, then the free side device power consumption shall be 1.5W or less. In this case, the free side device shall be fully functional regardless of the power mode.

A truth table for the relevant configurations of the Power Override, Power Set and Extended Identifier bits is shown in Table 4-7.

TABLE 4-7 POWER CONSUMPTION CONTROL FUNCTIONALITY

Power Override	Power Set	Byte 129, bits 7-6	Module Power Allowed
0	X	X	Low Power (1.5W)
1	0	00	High Power (1.5W)
1	0	01	High Power (2.0W)
1	0	10	High Power (2.5W)
1	0	11	High Power (3.5W)
1	1	X	Low Power (1.5W)
Note: The symbol 'X' in a column indicates any entry satisfies the condition.			

The free side device may declare maximum power consumption levels less than 1.5W by using the using read-only 'Advanced Low Power Mode' parameter shown in Table 4-8. For example, if the fixed side does not support free side devices consuming more than 1W, this parameter will allow the fixed side to determine if it has adequate power allocated prior to application of power to the Vact pins. All states not listed in Table 4-8 are reserved.

TABLE 4-8 REDUCED POWER CONSUMPTION LEVELS

Advanced Low Power Mode (Byte 110, bits 7-4)	Declared Maximum Power Consumption
0000	Advanced Low Power Mode Not supported
0001	1W
0010	0.75W
0011	0.5W
Note: Free-side power levels specified for 3.3V level on both Vact inputs.	

Additional power savings can be obtained by reducing the Vact input voltage level. The read only minimum operating voltage parameter is specified by bits 2-0 of byte 110. All states not listed in Table 4-9 are reserved.

TABLE 4-9 MINIMUM OPERATING VOLTAGE

Minimum Operating Voltage (Byte 110, bits 2-0)	Declared Minimum Operating Voltage
000	Not Supported (Default is nominal 3.3V). See section 5,4.
001	2.3V
010	1.7V
011	Reserved

4.6 Power Supply Filtering Network

The following fixed side power supply filtering network is recommended for the Vman and Vact output pins. The network isolates the fixed side Vsrc power rail from transients induced on the Vact and Vman power rails during hotplug events.

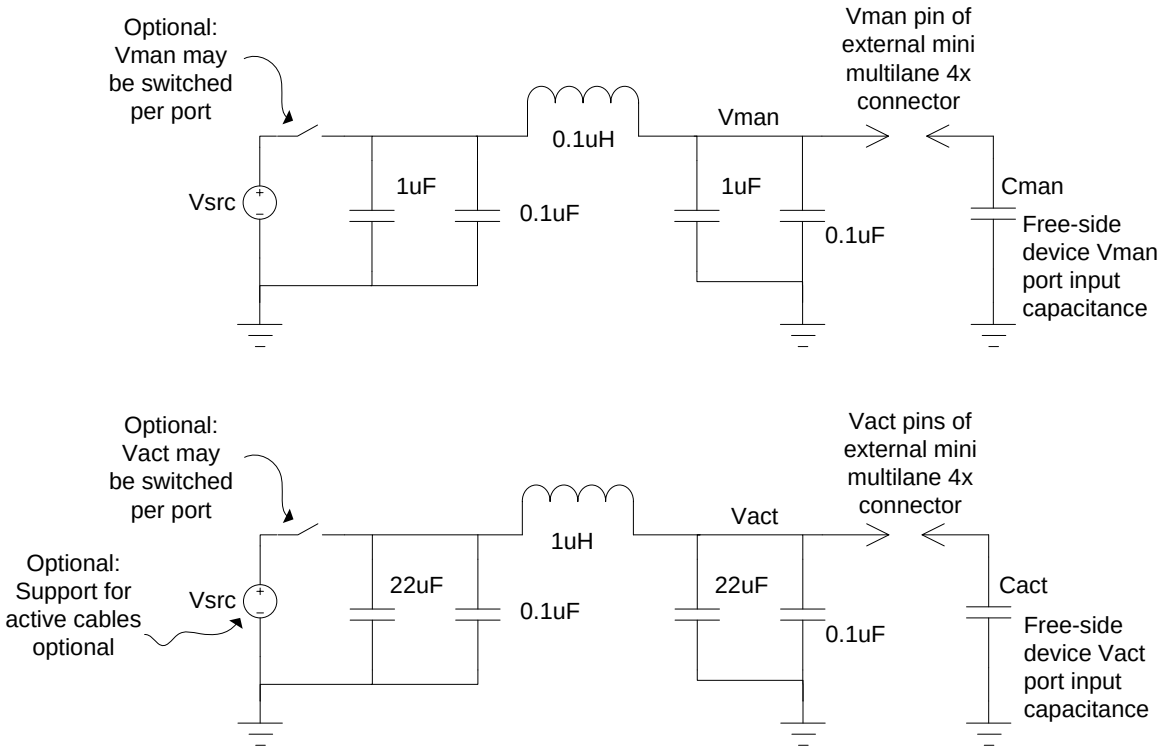

FIGURE 4-2 RECOMMNEDED FIXED SIDE POWER SUPPLY FILTERING NETWORK

For proper operation of the filtering networks with multi-bay receptacles, one instance of both networks (Vman and Vact) is required for each 4X mini multilane bay. See Figure 4-3.

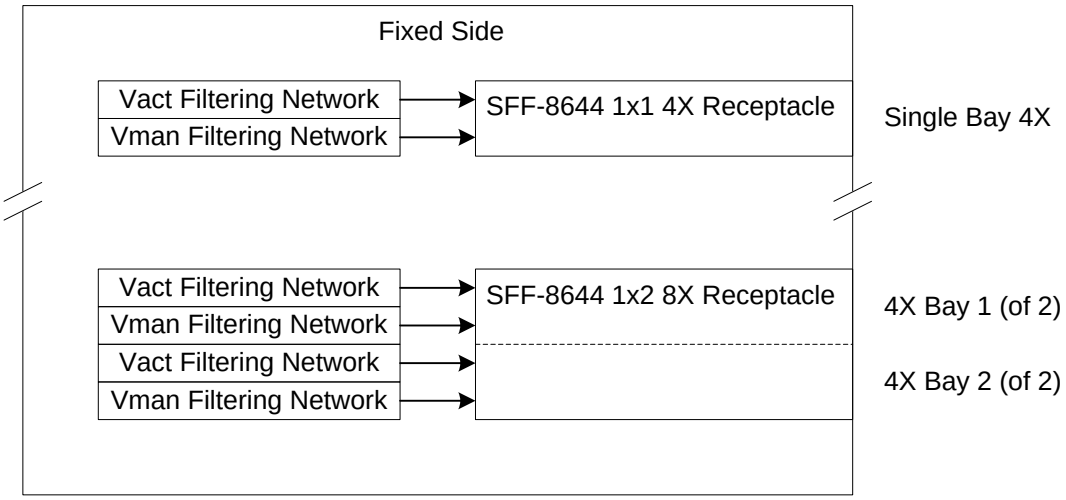

FIGURE 4-3 FILTERING NETWORKS WITH MULI-BAY RECEPTACLE DESIGNS

4.7 Squelch (Active Cable Implementations)

SFF-8449 compliant cable assemblies are non-separable. Functionality of circuitry within the active cable assembly integral to the TX/RX channel such as squelch control is outside the scope of this standard.