

SFF-9402

Reference Guide for

Multi-Protocol Internal Cable Pinouts for SAS and/or PCIe

Rev 1.1.1 November 20, 2026

SECRETARIAT: SFF ~~TA~~ TWG

This specification is made available for public review at https://www.snia.org/sff/specifications. Comments may be submitted at https://www.snia.org/feedback. Comments received ~~will be~~are considered for inclusion in future revisions of this specification.

ABSTRACT: Industry storage solutions are now implementing both PCIe and SAS within the same or similar enclosures. As there are multiple standard connectors available for creating internal cable solutions, numerous custom cables solutions have appeared. This reference guide incorporates pinouts that provide multiprotocol and/ or reversible cable solutions that reduce development/ design time and the resulting increasing number of custom cables.

The confusion between the CPU centric (PCIe) specification solutions and the drive centric (SAS) specification solutions was eliminated by creating and employing a common naming convention. The result being that TX is always the input to the cable and RX is always the output from the cable. The signal direction was also appropriately added to the tables. Table 8-7 has been added illustrating why SAS-2.1 and SAS-3 cables are not reversible in SAS-4 applications. The pinout solutions begin in Section 6.

This document provides an implementation guide for systems manufacturers, system integrators, and suppliers. ~~This is an internal working document of the SFF Committee, an industry ad hoc group.~~

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Foreword

The development work on this specification was done by the SNIA ~~SFF~~ TWG, an industry group. Since its formation as the SFF Committee in August 1990, as well as since SFF's transition to SNIA in 2016, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/sff/join.

Revision History

Rev 0.2 *March 1, 2016:*
- Introduced as a Reference Guide

Rev 0.5 *April 25, 2016:*
- Informal work group approved new Sideband assignments for MiniLink and Ultraport SlimSAS™
- Sideband naming revised – removed references to Sidebands 8 and 9, added in the alternate (A Sidebands for 0 and 1)
- Added SClock to Sideband 0 and SLoad to Sideband 1
- Sideband 2 replaced Sideband 8//VSP8 was renamed VSP2
- Sideband 3 replaced Sideband 9//VSP9 was renamed VSP3

Rev 0.6 *August 8, 2016:*
- Content completely restructured to clarify the presentation of the solutions
- Pinouts did not change from previous revision
- Additional tables provided to separate applications
- Added alternate pinout for legacy PCI Express® REFCLK implementation

Rev 0.7 "(prior to comments)" *September 12, 2016:*
- There are "NO" changes to any signal/ pin assignments with this revision
- Section 4 item 6 include SFF-8485 next to SGPIO
- Section 4 item 11 spelled out Vendor Specific Pins to identify the VSP abbreviation
- Section 4 item 12 changed 2-Wire types names from 2-Wire S-Type to Standard 2-Wire Type, 2-Wire A-Type to Other 2-Wire Type and added definition about signal logic level for the sidebands
- In section 4 item 13 changed Backplane Type to Backplane_Type (BP_Type) to match SFF-8448
- Updated tables (All) signal naming conventions associated with PCIe and SAS
- Updated PCIe only tables to show their naming convention only
- Updated SAS only tables to show their naming convention only
- Changed references from SFF-8612 to SFF-8611
- Renamed Nano-Pitch I/O™ to OCuLink or MiniLink where applicable throughout the document
- Renamed iPass+™ HD to Mini SAS HD or SFF-8643 where applicable throughout the document
- Updated section 6 alternate sideband assignment to include improved board layout
- Added additional description about the use of color coding plus italics to show the difference between the two protocols
- Added definition of NC as "no connect"
- Added SFF-9639 Multifunction 6X Unshielded Connector Pinouts to the reference section

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Rev 0.7J "(Includes Rev 0.7H plus comment resolutions to create Rev 0.7J (green text))" *December 12, 2016:*

- Updated document header information
- Change document to show SNIA format
- Updated Title description
- Changed the word "specification" to "Reference Guide or "document" where applicable throughout to indicate this is a reference document and not a specification
- Updated Points of Contact
- Added dates to the different Change history rev level
- Updated Forward to reflect SNIA format
- Changes incorporated are editorial clarifications plus the removal of proposed mini-SAS HD Alternate for PCIe cable solutions per user comment
- Reworded the abstract to clarify the purpose of this Reference Guide
- Removed the Note: Content completely restructured to clarify the presentation of the solutions
- Updated the Rev 0.7 revision section to correct typos
- Section 1 Replaced Purpose with Scope and updated the statement
- Added Section 1.1 Copyright for SNIA format
- Added Section 1.2 Disclaimer for SNIA format
- Section 2.1 Industry Documents, Added SFF-8485, SAS-3, SAS-4, SES-2 and SES-3
- Section 2.2 replaced with sources per SNIA format
- Added Section 2.3 Conventions per SNIA format
- Added Section 2.4 Definitions per SNIA format
- Throughout document changed SFF-8611 to SFF-8621 to include both the fixed (SFF-8612) and free (SFF-8611) interfaces
- Throughout document changed Slimline SAS to SFF-8654
- All the tables and document headings in this document were updated to just show the SFF associated with the connector and removed the connector names to eliminate any issues with abbreviated trademark names
- Section 4 updated opening sentence
- Section 4 Item 1 defined what is considered Other Protocol (O/P)
- Section 4 Item 2 replaced PCI Express® with Other Protocol implementations
- Section 4 Item 3 defined what connectors are considered Legacy
- Section 4 Item 4 added the word signals after (HCSL)
- Section 4 Item 7 removed must be "SFF-9402 AWARE" and reworded sentence to "implementations must be aware"
- Section 4 Item 10 "New Item/ Definition" now defines signals and convention follow OCuLink specification (Prev. item 10 now 12)
- Section 4 Item 11 "New Item/ Definition" for device connections in tables (Prev. item 11 now 13)
- Section 4 Item 13 (Prev. Item 11) removed PCI Express® and indicated sidebands based on OCuLink and SFF-8448
- Section 4 Item 14 (Prev. Item 12) changed PCIe x8 to Other Protocol (x8) implementations
- Section 4 Item 15 (Prev. Item 13) removed PCI Express® and replaced with OCuLink and Other Protocol
- Section 4 Item 15b (Prev. Item 13b) removed PCI Express® replaced with SFF-8448 to indicate common 2-Wire signals
- Section 4 Item 16 (Prev. Item 14) improved the wording for full crossover cables and replaced specification with reference guide
- Section 4 Item 17 "New item/ Definition" Added definition/ description about 3.3 Vact TX and RX usage
- Section 4 Item 18 "New item/ Definition" Added definition/ description about Power 5V#1/ #2.
- Section 4 Item 19 was Item 15 in the previous level

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- Section 4 Previous Item 16 about REFCLK optimization was removed
- Section 4 Item 19 (Prev. Item 15) reworded the first part of the sentence
- Section 4 Item 20 (Prev. Item 17) changed legacy to SFF-8087/ SFF-8643 and Slimline SAS to SFF-8654
- Section 4 Item 21 combined old Item 18 and 19 define the use of OCuLink signal naming convention
- Section 4 Added Item 22 about CWAKE# / OBFF implementation
- Section 4 Added Item 23 about CPERST# implementation
- Section 5 Updated opening sentence such that references to x8 SFF-8621 or SFF-8654 are considered Other Protocol
- Section 5 Second paragraph grammar correction added associated prior to (PERST[A,B]#/ CPRSNT[A,B]#)
- Section 5 Third paragraph removed PCI Express® and replaced with OCuLink/ Other Protocol
- Section 5 Third paragraph changed state about reserve pins as no connects to "NO WIRE" Power pins being "NO WIRE"
- Section 5 Item 1 replaced PCI Express® with OCuLink and Other Protocol where applicable
- Section 5 Item 2 replaced PCI Express® (x8) with Other Protocol (x8)
- Section 5 Item 2a replaced "It is still recommended that pins associated with" with "must be" for the diff pairs
- Section 5 Item 3 replaced PCI Express® (x8) with Other Protocol
- Table 5-1 Removed references to x8 PCIe, PCI Express® with the exception of the U.2 device
- Table 5-1 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module and MultiLink
- Table 5-1 Changed the endpoint high speed naming convention to match the OCuLink specification
- Table 5-1 Changed NC to NO WIRE and changed the reserve pins for OCuLink to the Power pins called out in OCuLink specification external only
- Table 5-1 Arrows cover SAS, OCuLink and Other Protocol. Dots were changed to dashes.
- Table 5-1 VSP+/- must be updated in OCuLink Specification
- Table 5-1 CWAKE#/OBFF (VSP) must be reflected in OCuLink
- Table 5-2 Removed references to x8 PCIe, PCI Express® with the exception of the U.2 device
- Table 5-2 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module and MultiLink
- Table 5-2 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
- Table 5-2 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only
- Table 5-2 Removed double ground assignments A19 and B19 in tables
- Table 5-2 Arrows cover SAS, and Other Protocol. Dots were changed to dashes
- Table 5-2 VSP+/- must be reflected in Other Protocol
- Table 5-2 CWAKE#/OBFF (VSP) must be reflected in OCuLink Specification
- Table 5-3 Removed references to x8 PCIe, PCI Express® with the exception of the U.2 device
- Table 5-3 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module and MultiLink
- Table 5-3 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
- Table 5-3 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only
- Table 5-3 Double ground assignments A19 and B19 still required for Y-cables
- Table 5-3 Arrows cover SAS, and Other Protocol. Dots were changed to dashes
- Table 5-3 VSP+/- must be reflected in Other Protocol
- Section 6 Heading - removed PCI Express® replaced with OCuLink and added Other Protocol (O/P)
- Section 6 Opening sentence removed PCI Express® added (O/P)
- Section 6 First paragraph (Prev. version), about the alternate sideband pin assignments was removed
- Section 6 First paragraph (Second in Prev. version) removed PCI Express® and reworded the description about the highlighted

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diff pairs in the table including the x8
- Section 6 Second paragraph (Third in Prev. version) removed PCI Express® and replaced with OCuLink, Other Protocol
- Added new statement about pins designated as "POWER"
- Section 6 Item 1 Removed PCI Express® defined connectors that were not OCuLink x4 as Other Protocol x4/ x8 SFF-8621, SFF-8654 and SFF-8643
- Section 6 Item 2 Replaced PCI Express® with Other Protocol (x8) updated to SFF-8654
- Section 6 Item 2 Updated description about pins associated with REFCLK must be wired as differential pairs
- Section 6 Item 3 Replaced PCI Express® with Other Protocol
- Section 6 Item 3 Replaced "It is still recommended that pins associated with" with "must be"
- Table 6-1 Heading changed PCI Express® to OCuLink and added Other Protocol
- Table 6-1 Changed SFF-8643/ SFF-8654 from PCI Express® to Other Protocol (O/P)
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- Table 6-1 Changed Dots to dashes for the grounds
- Table 6-2 Heading changed PCI Express® to OCuLink and added Other
- Table 6-2 Changed SFF-8643, SFF-8654 (x8) and MiniLink (x8) from PCI Express® to Other Protocol (O/P)
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- Table 6-2 Changed Dots to dashes for the grounds
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- Table 6-3 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external only
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- Table 6-4 Removed columns for mini-SAS HD (SFF-8643) Alternate
- Table 6-4 Changed Dots to dashes for the grounds
- Table 6-4 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol

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- Table 6-4 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module
- Table 6-4 Changed NC to NO WIRE and changed the reserve pins for Other Protocol to the Power names for external
- Table 6-4 CWAKE#/OBFF (VSP) [A, B] and must be reflected in Other Protocol to line up with OCuLink
- Table 6-4 VSP+/- [A, B] must be updated in Other Protocol to line up with OCuLink specification
- Table 6-5 Heading - Removed PCI Express® added Other Protocol
- Table 6-5 All x8 connectors, SFF-8654 and SFF-8643 defined as Other Protocol
- Table 6-5 Removed columns for mini-SAS HD (SFF-8643) Alternate
- Table 6-5 Changed Dots to dashes for the grounds
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- Table 6-5 Changed the endpoint high speed naming convention to match OCuLink/ Other Protocol
- Table 6-5 Changed Device columns to SFF-8639/ U.2 connector versus SFF-8639 Module
- Section 7 Updated heading
- Section 7 Updated opening sentence
- Section 7 Changed SFF-8611 to SFF-8621
- Section 7 Items 1-4 changed SFF-8611 to SFF-8621
- Section 7 Item 5 Added (SFF-8621/SFF-8654) after SAS-4 and (SFF-8643/ SFF-8087) after Legacy
- Section 7 Item 5 added second sentence inserted Sideband in front of signals are "highlighted"
- Tables 7-1 through 7-6 headings changed SFF-8611 to SFF-8621
- Tables 7-1 through 7-6 Changed dots to dashes for the grounds
- Tables 7-1 through 7-6 Changed Device column to SFF-8639/ U.2 connector versus Multilink
- Tables 7-7 Added connector name above their associated SFF designations and changed dots to dashes for the grounds

Rev 1.0 *July 6, 2018:*

- Replaced "Reference Guide" with "Published" in header
- Added "Reference" watermark

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Rev 1.1 *October 16, 2019:*

- Upgraded to new document template
  - Updated front matter and added Section 3
  - Note: all sections, figures, and tables after Section 3 were incremented by 1
- Changed "Device" column header to "Device on Backplane" in all existing tables
- Minor editorial edits throughout (e.g. grammar, clarification, emphasis, etc.)
- Removed all references to U.3
- Cleaned up references to PCIe SFF-8639 Module Specification/ U.2
- Updated the Abstract and Scope
- Updated the Industry Documents in Section 2.1
  - Added SFF-TA-1001, SFF-TA-1005 (UBM), SFF-8639 PCI Express SFF-8639 Module Specification
  - Removed SFF-8613 and SFF-8673
- Updated General Description (Section 4) and header descriptions (Sections 5, 6, & 7)
- Updated Figure 4-1~~Figure 4-1~~
- Added information to Section 5 on UBM/ SFF-TA-1001
- In Section 5, replaced SFF-8639 with U.2/ SFF-TA-1001 where appropriate (multiple instances)
- Sections 6 and 7:
  - Added additional text and notes to better describe content
  - Corrected table references
  - Split bullets, for clarity
- Added notes about sideband signal assignments to Sections 6, 7, and 8
- Table 6-1 through Table 6-5 and Table 7-1 through Table 7-5:
  - Added column for SFF-TA-1001
  - Added U.2 to identify the lane assignments
  - Added VSP to some OCuLink assigned sidebands to be in alignment with SFF-8448 (Other 2-Wire Type interface)
- Added Table 6-6, Table 7-6, and Table 8-7 to summarize all possible sideband implementations for all other tables in each respective section
- Table 8-7 was updated to include symbols illustrating that cables are not reversible; additional text was added to explain added symbols

Rev 1.1.1 *November 20, 2026:*

- Upgraded to new document template
- Added CopprLink, OCP, SAS-5, SFF-TA-1016 Industry Document References
- Section 5: Added Note 24 in the Implementation Notes
- Section 5: Added "Additional Notes" for notes that pertain to changes made after Revision 1.1
- Added Section 9 specifically to show how existing pin assignments map to various SFF-TA-1016 connector implementations.

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1. Scope

This reference guide enables the PCIe and SAS storage industry to reduce the design time and limit the number of cables required for both single and multiple protocol SAS/PCIe solutions within the same and like enclosures. It introduces pinout solutions that include both current and legacy connector applications.

2. References and Conventions

2.1 Industry Documents

The following documents are relevant to this reference guide:

- PCI Express® Card Electromechanical (CEM) Specification Revision 3.0
- PCI Express® OCuLink Specification Revision 1.0
- PCI Express® SFF-8639 Module Specification (see note)
- PCI Express® CopprLink Internal Cable Specification for PCI Express 5.0 and 6.0 Version 1.0
- Open Compute Project Modular - Extensible IO (M-XIO) Base Specification Version 1.04
- SAS-3 Serial Attached SCSI – 3 T10/2212
- SAS-4 Serial Attached SCSI – 4 T10/BSR INCITS 534
- SAS-5 Serial Attached SCSI – 5 SCSI/INCITS 561
- SES-2 SCSI Enclosure Services – 2 T10/1559
- SES-3 SCSI Enclosure Services – 3 T10/2149
- SFF-8087 Mini Multilane 4X Unshielded Connector Shell and Plug
- SFF-8448 SAS Sideband Signal Assignments
- SFF-8485 Specification for Serial GPIO (SGPIO) Bus
- SFF-8621 MiniLink 4/8X I/O Connector and Cable Assemblies
- SFF-8639 Multifunction 6x Unshielded Connector
- SFF-8643 Mini Multilane 4/8X 12 Gb/s Unshielded Connector (HD12un)
- SFF-8654 0.6mm 4/8X Unshielded I/O Connector
- SFF-9400 Universal 4/8X Pinout
- SFF-9639 Multifunction 6X Unshielded Connector Pinouts
- SFF-TA-1001 Universal x4 Link Definition for SFF-8639
- SFF-TA-1005 Universal Backplane Management (UBM)
- SFF-TA-1016 Internal Unshielded High Speed Connector System

NOTE: This specification is frequently referred to as "U.2".

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee ~~can be~~ is found at https://www.snia.org/sff/specifications. Suggestions for improvement of this ~~specification will be~~document are welcome and~~,~~ ~~they~~ should be submitted to https://www.snia.org/feedback.

REFERENCE

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Copies of PCIe standards may be obtained from PCI-SIG (https://pcisig.com).

Copies of SAS and other ANSI standards may be obtained from the International Committee for Information Technology Standards (INCITS) (https://www.incits.org).

Copies of Open Compute Project standards may be obtained from (https://www.opencompute.org)

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS:
Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they~~y~~ text first appears.

ORDER OF PRECEDENCE:
If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS:
Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a. red (i.e., one of the following colors):
    A. crimson; or
    B. pink;
b. blue; or
c. green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1. top;
2. middle; and
3. bottom.

Lists are associated with an introductory paragraph or phrase, and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

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3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, the feature shall be implemented as defined by the specification. Describing a feature as optional in the text is an informational callout to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Where the term is used for a signal on a connector contact, the signal or connector contact is set aside for future standardization. The feature is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies to the restricted designation, then the restricted bit, byte, word, or field shall be treated as a value whose definition is not in scope of this document and is not interpreted by this specification.

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

~~**May/ may not:** Indicates flexibility of choice with no implied preference.~~

~~**Optional:** Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be done in the same way as defined by the specification. Describing a feature as optional in the text is done to assist the reader.~~

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~~**Reserved:** Defines the signal on a connector contact [when] its actual function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.~~

~~**Shall:** Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.~~

~~**Should:** Indicates flexibility of choice with a strongly preferred alternative.~~

~~**Vendor specific:** Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.~~

3.2 Acronyms and Abbreviations

There are no acronyms or abbreviations defined for this reference guide.

3.3 Definitions

There are no definitions defined for this reference guide.

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4. General Description

This reference guide reduces the design time and the proliferation of internal cable designs that enable multiprotocol and/or reversible pinouts for single and multiprotocol PCIe/SAS cable solutions.

The connector figures below are shown for reference only to show how the pinouts shown in the tables ~~relates~~relate to the physical locations within each of the connector styles addressed in this guide. These signal assignments comply with the SAS-4/ SFF-8448 and PCIe OCuLink Rev 1.0 pinouts. All are based on the fixed end definitions of the pin assignments.

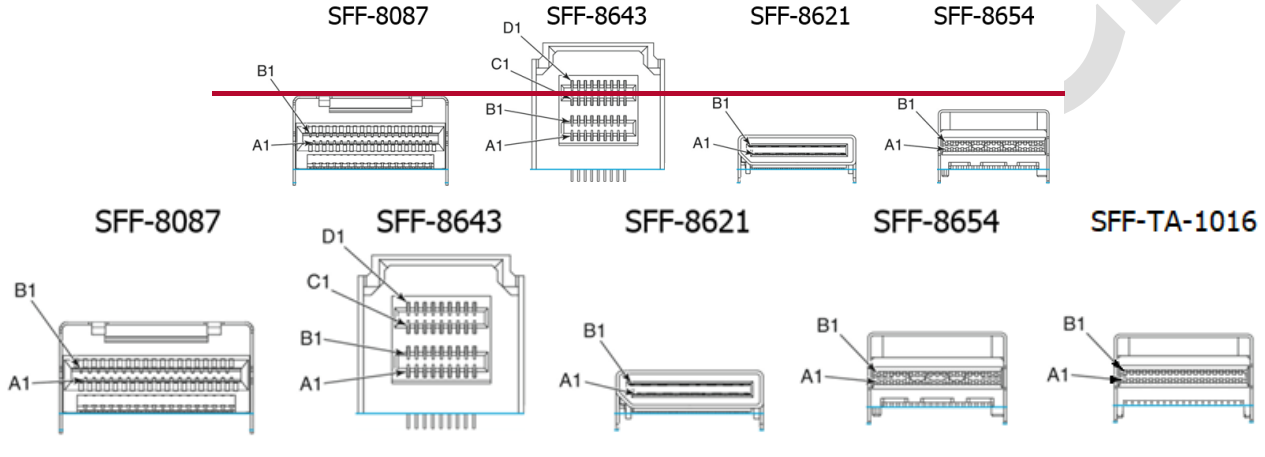


Figure 4-1 Connector Views

5. Implementation Notes for System Compatibility Issues

The following notes provide background information required to implement universal multiprotocol cables for SAS-4 (Controller/ Backplane/ Device) and OCuLink (Root/ Endpoint/ Device).

System Compatibility Issues

1. Caution - Present PCI Express® internal implementations using SFF-8643/8673/8654 connectors are vendor specific (Not standardized) and are defined in this document as Other Protocol (O/P). They do not align with SAS/SATA legacy SFF-8643/8673 implementations (Some range from 85 to 100 ohms; some have a white ring on fixed ends). As a result, PCIe cables utilizing SFF-8643/8673 connectors used for SFF-9402 can currently be plugged into legacy SAS/SATA implementations resulting in signal incompatibilities.
2. Multiple implementations exist for Other Protocol implementations based on SFF-8643/8673 connectors. SFF-9402 was created based on an industry survey to enable a common pin assignment and a cable across multiple interfaces; therefore, the previous protocol specific pinouts may not apply.
3. SAS/SATA SFF-8643/ SFF-8087 are defined as Legacy in this document and their internal connector pin assignments are based on SAS 2.1/ SAS-3 T-10 standards and SFF-8448.

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4. SFF-9402 was based on, and now supersedes SFF-9401 to provide a common industry two cable solution. SAS-4 reassigned the four SAS sidebands 2, 3, 4, 5 and eliminated designations 8 and 9 for only the MiniLink and Ultraport SlimSAS™ SAS connectors. Moving forward, this provided better optimization of a common cable for SAS/ PCI Express® operation by eliminating the multiple grounds (two pins were freed up) so that SAS single-ended signals ~~where~~were not shared with PCIe High Speed Current Steering Logic (HCSL) signals. Refer to tables included in SAS-4 and SFF-9402 for their new locations.

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5. Changing the pin assignments for SAS-4 impacted cable solutions when migrating from the legacy mini SAS (SFF-8087) / Mini SAS HD (SFF-8643) to MiniLink (SFF-8621) / Ultraport SlimSAS™ (SFF-8654) hybrid cables as follows.
   a. SAS and OCuLink legacy hybrid solutions currently require independent cables for each specific protocol.
   b. In addition, SAS hybrid only cables ~~only~~ are no longer reversible such that they cannot be flipped between controller and backplane. Example: A SAS cable designed such that the controller end is Mini SAS HD and the backplane end is MiniLink cannot be used where the controller has MiniLink and the backplane with Mini SAS HD.
6. SAS standards can incorporate SGPIO (SFF-8485) or Storage Enclosure Services (SES) depending on the physical sideband protocol utilized. SES provides a method to bridge the multiprotocol environment via 2-Wire interface to discover what backplane/end point is present prior to any in-band communication/operation.
7. Controller and Backplane implementations must be aware of incompatibility issues with signal levels when migrating from legacy connectors such as SFF-8087/ SFF-8643 to SFF-8621/ SFF-8654 with PCIe and SAS.
8. SFF-9402 signal assignments are controlled by the "Fixed" side initiator and "Fixed" side backplane only.
9. OCuLink defines the signals based on the "Fixed" ends of the interface. SFF-8448 defines them for SAS and also for the common signals shared with OCuLink.
10. The signal name assignments follow the OCuLink signal conventions~~s~~ such that the TX pairs are inputs to the cable and RX pairs are outputs from the cable.
11. Device~~s~~ connections are defined as SFF-8639 connector base PCIe/ SFF-TA-1001 with pin numbers for PCI Express© and MultiLink SAS™ to eliminate confusion with signal directions between the cable and backplane receptacle connectors.
12. SFF-9400 defines the basic locations of undefined High Speed and Vendor Specific signals for the SFF-8621 and SFF-8654 connectors.
13. SFF-8643 Vendor Specific Pins (VSP)/ sideband assignments are based on the OCuLink and SFF-8448 definitions for consistency.
14. SFF-9402 (like the previous SFF-9401) aligns both OCuLink and SAS sideband assignments via SFF-8448 (SB0-7, SB+/-) where applicable. The addition of "Other 2-Wire Type" to SFF-8448 Rev 1.2 facilitates a common 2-Wire interface and Backplane_Type (BP_Type) for SAS, OCuLink (x4), SFF-TA-1005 (UBM) and Other Protocol (x8) implementations for determining bus type operation. Note - because the use of sideband signals differs between protocols, each sideband signal should be isolated i.e. NOT COMMONED in the cable.
   a. Sidebands 0-7 and VSP pins are defined as single ended, 3.3V logic and use open drain when sourcing the signals.
   b. Sidebands SB+/- and VSP+/- ~~utilizes~~utilize High Speed Current Steering Logic (HCSL) signal levels only.
15. The sidebands' signal names shown provide recommended uses for SAS, OCuLink and Other Protocol applications.
   a. The SAS cable implementation also includes an associated sideband number as defined in SFF-8448.
   b. SFF-8448 indicates the common signals between the Standard 2-Wire Type and Other 2-Wire Type. The remaining sidebands are labeled VSP and must refer to the OCuLink 1.0 or later specification.
   c. SFF-TA-1005 (UBM) can be implemented as another alternative sideband interface for both the Standard 2-Wire Type or Other 2-Wire Type as defined in SFF-8448 with no changes to the physical pin assignments.

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Implementation Notes:

16. The pinouts in this reference guide define full crossover cables (The A row on one end crosses over to the B row on the other end) unless otherwise noted. This enables the use of ribbon cable construction solutions.
    a. Based on a full crossover the TX (inputs to the cable at one end) crossover to RX (outputs from the cable at the other end).
    b. The sideband signals also implement a full crossover such that the Root/ Controller and Endpoint/ Backplane have different fixed end pin assignments.
17. The signals defined as POWER 3.3 Vact TX and POWER 3.3 Vact RX are associated with Active cable applications only.
    a. These power connections are used for active components within the free ends only and do not propagate down the cable.
    b. The Root and Endpoint must supply independent voltage sources for their associated fixed end.
    c. They use the same pin assignments at both ends of the cable.
    d. They may be commoned at each fixed end.
18. The signals defined as POWER 5 V #1 and POWER 5 V #2 sourced by the Root are specified for **"External"** applications only.
    a. These power connections "**Do Not"** follow the full crossover (A side to B side) used by the signals.
    b. They use the same pin assignments at both ends of the cable.
    c. They may be commoned at each fixed end.
19. SAS cables built to this SFF-9402 pinout will still work on old initiators and backplanes based on legacy (SFF-8087 and SFF-8643) SAS pinouts.
20. SAS cables based on SFF-8087/ SFF-8643 and ~~the new~~ SAS-4 SFF-8621/ SFF-8654 which are considered "Hybrid" assemblies, but they are no longer reversible. Example: A SAS cable designed such that the controller end is Mini SAS HD and the backplane end is MiniLink cannot be used where the controller has MiniLink and the backplane with Mini SAS HD.
21. These SFF-9402 tables define the lane and polarity of the highspeed pairs.
    a. Utilizes the OCuLink/ Other Protocol signal naming convention
    b. Lane reversal is not mandatory for end point devices (See the PCI Express® CEM Spec).
22. Sideband signal CWAKE#/ OBFF which is optional, may be used as a VSP or go through some interim control logic between the root and PCIe/ SFF-TA-1001 device itself such that it is not directly connected to the cable interface.
23. Sideband signal PERST# may go through some interim control logic between the root and SFF-8639 device itself such that is not directly connected to the cable interface.
~~23.~~24. For cables that split from a wider interface into two smaller interfaces (I.e. Y-Cables and 1-to-4 Cables) there may be situations where a ground shared by adjacent differential pairs in the wider interface must go to separate grounds to each leg of the cable. This is indicated by duplicating the signal row on the wider interface and coloring the pin number RED.

Additional Notes with the addition of SAS-5 SFF-TA-1016, CopprLink & M-XIO pinouts

25. With the addition of the PCI Express ® CopprLink and OCP M-XIO standards, PCIe now officially has a specified connector and a specified pinout. -
26. CopprLink & M-XIO pinouts use the SFF-TA-1016 connector specification.
27. SAS-5 has adopted SFF-TA-1016 as an additional SAS connector, with the connector named the same as the SFF mechanical specification SFF-TA-1016.
28. CopprLink specifies the 38-pin (x4), 74-pin (x8), 148-pin (x16), and 124-pin (x16 w/ limited sidebands) versions of the SFF-TA-1016 connector.
29. CopprLink does not specify Y-cable types. SFF-9402 however does extrapolate the use of CopprLink's extended sidebands into a duplicate usage of the baseline sidebands onto the extended sidebands for purposes of continuing the use of Y-cable types.

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30. M-XIO specifies the 38-pin (x4), 74-pin (x8), and 148-pin (x16) versions of the SFF-TA-1016 connector.
31. M-XIO specifies x16 to x8 Y-cables. It specifically does NOT allow x8 to x4 Y-cables. M-XIO labeling is removed from such tables when the situation occurs.
32. SAS-5 SFF-TA-1016 specifies the 38-pin (4i), 74-pin (8i), and 148-pin (16i) versions of the SFF-TA-1016 connector.
33. SAS-5 SFF-TA-1016 specifies 4 instances of the sidebands signals for the 16i version, allowing for x8 and x4 breakout cables with full sideband assignment.
34. x4 and x8 versions of CopprLink, ~~&~~ M-XIO, & SAS-5 SFF-TA-1016 pin counts and signal definitions are identical to the SFF-8654 ~~pin count~~connector versions.

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35. CopprLink & MXIO high speed signal locations and direction are identical to the SFF-8654 signal usage.
36. CopprLink & MXIO sideband assignments to pin numbers are nearly identical to the SFF-8654 listing in this specification. The most common signals (REFCLK, 2Wire, PERST#, and CPRSNT#) are identical in usage. The other sideband assignments are closely matched to the FlexIO assignments that are defined in the new connectors.
37. To preserve legacy documentation, the addition of the CopprLink & MXIO pinouts are limited to new Section 9 tables, with the existing SFF-8654 signals as the reference baseline to any conversions between these new additions and previously documented connectors.

6. SAS-4 / OCuLink / Other Protocol Multiprotocol/ Reversible Cables

The following six (6) tables provide multiprotocol signal assignments based on OCuLink, SAS-4/ SFF-8448 and Other Protocol SFF-8621 (x8), SFF-8654 (x4, x8) applications. In addition, cable signal direction and target/ endpoint device connections are also shown.

In this section:

1. Cables with the same mechanical connector at both ends are electrically and physically reversible.
2. Cables with different connectors on its ends will work regardless of the mechanical location of the fixed side connectors.
3. Table that only defines the sideband assignments based on OCuLink, SFF-8448, and SFF-TA-1005 (UBM).
4. Standard 2-Wire Type and UBM was not added to Table 6-1 through Table 6-5 to minimize the number of columns required.

The high speed differential pairs including the sidebands for REFCLK (VSP+/-) and their reversible path (PERST#/ CPRSNT#) respectively are highlighted/ shaded in the x4 along with (VSP[A,B]+/-) and their associated (PERST[A,B]#/ CPRSNT[A,B]#) x8 connections. They shall be wired as differential pairs to enable the cable being flipped between Root and Endpoint.

The highspeed differential and sideband signals are color coded (SAS=Blue and OCuLink / Other Protocol=Green/ Italic) to indicate their associated naming convention and protocol. The arrows provide the signal flow direction between the Root/ Controller and Endpoint/ Backplane. In addition, brown was used to identify double ground assignments where applicable between different connector types and Y-cables. The Reserved and Power pin connections between the Root/ Controller and Endpoint/ Backplane are defined as "NO WIRE".

1. SAS-4/ OCuLink (x4) Multiprotocol Cables
   Table 6-1 defines multiprotocol cable interface for SAS-4 (SFF-8621, SFF-8654)/ OCuLink (SFF-8621)/ Other Protocol (SFF-8654) x4 connections only. These cables are fully reversible such that they can be flipped end to end between Controller/ Root and Backplane/ Endpoint
2. SAS-4/ Other Protocol (x8) Multiprotocol Cables
   Table 6-2and Table 6-3 defines multiprotocol cable interface for SAS/ Other Protocol for SFF-8621/ SFF-8654 x8 connections only. These cables are fully reversible such that they can be flipped end to end between Controller/ Root and Backplane/ Endpoint
   a. Note: In the x8 configuration the sidebands designated with an "A" suffix are considered the primary path when only a single set of sidebands are required to manage the bus. The sideband bus with a "B" suffix is also shown with VSP indicating possible vendor specification. The pins associated with REFCLKB+/- (VSPB+/-) and PERSTB#/ CPRSNTB#) shall be wired as differential pairs. Note: VSP[A,B]+/- are defined as High Speed Current Steering Logic (HSCL).
3. SAS-4/ Other Protocol (SFF-8621, SFF8654) (x8) to OCuLink/ MiniLink (SFF-8621) and Other Protocol (SFF-8654) Y-Cables ~~_____~~and~~_____~~ define multiprotocol the cable interface for SAS/ Other Protocol for SFF-8621 / SFF-8654 x8 to a pair of x4 OCuLink or Other Protocol connections only.

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a. Note: Both sets of sidebands (A and B) are required to support a Y-cable configuration where two independent x4 interfaces are connected to a single x8 interface as described in the previous table.

4. Sideband Signal Assignments
   Table 6-6 defines the sideband assignments only. Although Table 6-1 through Table 6-5 define OCuLink and SFF-8448 SGPIO, this table includes the SFF-8448 Standards 2-Wire Type and SFF-TA-1005 (UBM). Note: UBM can be considered the Other 2-Wire Type that can support both SAS and PCIe protocols.

REFERENCE

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Table 6-1 Multiprotocol SAS-4/ OCuLink/ Other Protocol (x4) Cables (1 of 1)

	Root / Controller				CABLE	*Endpoint*/ Backplane				*Devices on Backplane*		
SFF-9400	SFF-8654 (38-circuit)	SFF-8621 (42-circuit)	9402 Multi-Protocol (OCuLink, Other Protocol (O/P), SAS-4)) x4 Cable Interface			9402 Multi-Protocol (OCuLink, Other Protocol (O/P), SAS-4)) x4 Cable Interface		SFF-8621 (42-circuit)	SFF-8654 (38-circuit)	SFF-8639 Connector		
Type 1 4X	*O/P* SAS-4	*OCuLink* / SAS-4	OCuLink and SAS-4/ SFF-8448 Signal Names			OCuLink and SAS-4/ SFF-8448 Signal Names		*OCuLink* / SAS-4	*O/P* SAS-4	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
	PIN	PIN	*ROOT*	Controller	DIR	*Endpoint*	Backplane	PIN	PIN	PIN	PIN	PIN
RSV		*A1*	POWER 3.3 Vact RX	RESERVED	NO WIRE	POWER 5 V #1	RESERVED	B1				
GND	A1	A2	GROUND	GROUND	—	GROUND	GROUND	B2	B1			
HS	A2	A3	*PERp0*	RX0+	←	*PETp0*	TX0+	B3	B2	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
HS	A3	A4	*PERn0*	RX0-	←	*PETn0*	TX0-	B4	B3	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
GND	A4	A5	GROUND	GROUND	—	GROUND	GROUND	B5	B4			
HS	A5	A6	*PERp1*	RX1+	←	PETp1	TX1+	B6	B5	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
HS	A6	A7	*PERn1*	RX1-	←	PETn1	TX1-	B7	B6	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
GND	A7	A8	GROUND	GROUND	—	GROUND	GROUND	B8	B7			
SB	A8	A9	*BP_TYPE (VSP)*	BP_TYPE (SB7)	↔	BP_TYPE(VSP)	BP_TYPE (SB7)	B9	B8			
SB	A9	A10	*CWAKE#,OBFF (VSP)*	RESET, SDataOut (SB4)	↔	CWAKE#,OBFF/(VSP)	RESET, SDataOut (SB4)	B10	B9	P1 (WAKE#)	P1 (WAKE#)	
SB	A10	A11	*GND*	GND (SB3)	—	GND	GND (SB3)	B11	B10			
SB	A11	A12	*REFCLK+(VSP+)*	(SB+)	→	*REFCLK+(VSP+)*	(SB+)	B12	B11	E7 (REFCLK+)	E7 (REFCLK+)	
SB	A12	A13	*REFCLK-(VSP-)*	(SB-)	→	*REFCLK-(VSP-)*	(SB-)	B13	B12	E8 (REFCLK-)	E8 (REFCLK-)	
GND	A13	A14	GROUND	GROUND	—	GROUND	GROUND	B14	B13			
HS	A14	A15	*PERp2*	RX2+	←	*PETp2*	TX2+	B15	B14	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
HS	A15	A16	*PERn2*	RX2-	←	*PETn2*	TX2-	B16	B15	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
GND	A16	A17	GROUND	GROUND	—	GROUND	GROUND	B17	B16			
HS	A17	A18	*PERp3*	RX3+	←	*PETp3*	TX3+	B18	B17	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
HS	A18	A19	*PERn3*	RX3-	←	*PETn3*	TX3-	B19	B18	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
GND	A19	A20	GROUND	GROUND	—	GROUND	GROUND	B20	B19			
RSV		A21	POWER 5 V #2	RESERVED	NO WIRE	POWER 3.3 Vact TX	RESERVED	B21				
RSV		B1	POWER 5 V #1	RESERVED	NO WIRE	POWER 3.3 Vact RX	RESERVED	A1				
GND	B1	B2	GROUND	GROUND	—	GROUND	GROUND	A2	A1			
HS	B2	B3	*PETp0*	TX0+	→	*PERp0*	RX0+	A3	A2	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
HS	B3	B4	*PETn0*	TX0-	→	*PERn0*	RX0-	A4	A3	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
GND	B4	B5	GROUND	GROUND	—	GROUND	GROUND	A5	A4			
HS	B5	B6	*PETp1*	TX1+	→	*PERp1*	RX1+	A6	A5	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
HS	B6	B7	*PETn1*	TX1-	→	*PERn1*	RX1-	A7	A6	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
GND	B7	B8	GROUND	GROUND	—	GROUND	GROUND	A8	A7			
SB	B8	B9	*2W-CLK*	2W-CLK, Sclock (SB0)	↔	*2W-CLK*	2W-CLK, SClock (SB0)	A9	A8			
SB	B9	B10	*2W-DATA*	2W-DATA, Sload (SB1)	↔	*2W-DATA*	2W-DATA, SLoad(SB1)	A10	A9			
SB	B10	B11	*GND*	GND (SB2)	—	*GND*	GND(SB2)	A11	A10			
SB	B11	B12	*PERST# (VSP)*	ADD, SDataIn (SB5)	↔	*PERST# (VSP)*	ADD, SDataIn (SB5)	A12	A11	E5 (PERST#)	E5 (PERST#)	
SB	B12	B13	*CPRSNT# (VSP)*	CNTRLR_TYPE (SB6)	↔	*CPRSNT#(VSP)*	CNTRLR_TYPE (SB6)	A13	A12			
GND	B13	B14	GROUND	GROUND	—	GROUND	GROUND	A14	A13			
HS	B14	B15	*PETp2*	TX2+	→	*PERp2*	RX2+	A15	A14	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
HS	B15	B16	*PETn2*	TX2-	→	*PERn2*	RX2-	A16	A15	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
GND	B16	B17	GROUND	GROUND	—	GROUND	GROUND	A17	A16			
HS	B17	B18	*PETp3*	TX3+	→	*PERp3*	RX3+	A18	A17	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
HS	B18	B19	*PETn3*	TX3-	→	*PERn3*	RX3-	A19	A18	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
GND	B19	B20	GROUND	GROUND	—	GROUND	GROUND	A20	A19			
RSV		B21	POWER 3.3 Vact TX	RESERVED	NO WIRE	POWER 5 V #2	RESERVED	A21				

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Table 6-2 Multiprotocol SAS-4/ Other Protocol (x8) Cables (1 of 2)

	Root / Controller				CABLE	Endpoint / Backplane				Devices on Backplane		
SFF-9400	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 Multi-Protocol (Other Protocol (O/P), SAS-4)) x8 Cable Interface			9402 Multi-Protocol (Other Protocol (O/P), SAS-4)) x8 Cable Interface		SFF-8621 (80-circuit)	SFF-8654 (74-circuit)	SFF-8639 Connector		
Type 1 8X	O/P SAS-4	O/P SAS-4	Other Protocol and SAS-4/ SFF-8448 Signal Names			Other Protocol and SAS-4/ SFF-8448 Signal Names		O/P SAS-4	O/P SAS-4	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
	PIN	PIN	ROOT	Controller	DIR	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
GND	A1	A1	GROUND	GROUND	–	GROUND	GROUND	B1	B1			
HS	A2	A2	PERp0	RX0+	←	PETp0	TX0+	B2	B2	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
HS	A3	A3	PERn0	RX0-	←	PETn0	TX0-	B3	B3	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
GND	A4	A4	GROUND	GROUND	–	GROUND	GROUND	B4	B4			
HS	A5	A5	PERp1	RX1+	←	PETp1	TX1+	B5	B5	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
HS	A6	A6	PERn1	RX1-	←	PETn1	TX1-	B6	B6	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
GND	A7	A7	GROUND	GROUND	–	GROUND	GROUND	B7	B7			
SB	A8	A8	BP_TYPEA(VSPA)	BP_TYPEA (SB7A)	↔	BP_TYPEA(VSPA)	BP_TYPEA(SB7A)	B8	B8			
SB	A9	A9	CWAKEA#,OBFFA (VSPA)	RESETA, SDataOutA (SB4A)	↔	CWAKEA#,OBFFA)(VSPA)	RESETA, SDataOutA(SB4A)	B9	B9	P1 (WAKE#)	P1 (WAKE#)	
SB	A10	A10	GND	GND (SB3A)	–	GND	GND(SB3A)	B10	B10			
SB	A11	A11	REFCLKA+(VSPA+)	(SBA+)	→	REFCLKA+(VSPA+)	(SBA+)	B11	B11	E7 (REFCLK+)	E7 (REFCLK+)	
SB	A12	A12	REFCLKA-(VSPA-)	(SBA-)	→	REFCLKA-(VSPA-)	(SBA-)	B12	B12	E8 (REFCLK-)	E8 (REFCLK-)	
GND	A13	A13	GROUND	GROUND	–	GROUND	GROUND	B13	B13			
HS	A14	A14	PERp2	RX2+	←	PETp2	TX2+	B14	B14	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
HS	A15	A15	PERn2	RX2-	←	PETn2	TX2-	B15	B15	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
GND	A16	A16	GROUND	GROUND	–	GROUND	GROUND	B16	B16			
HS	A17	A17	PERp3	RX3+	←	PETp3	TX3+	B17	B17	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
HS	A18	A18	PERn3	RX3-	←	PETn3	TX3-	B18	B18	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
GND	A19	A19	GROUND	GROUND	–	GROUND	GROUND	B19	B19			
RSV		A20	POWER 3.3 Vact RX	RESERVED	NO WIRE	POWER 5V #1	RESERVED	B20				
RSV		A21	POWER 3.3 Vact TX	RESERVED	NO WIRE	POWER 5V #2	RESERVED	B21				
GND		A22	GROUND	GROUND	–	GROUND	GROUND	B22				
HS	A20	A23	PERp4	RX4+	←	PETp4	TX4+	B23	B20	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
HS	A21	A24	PERn4	RX4-	←	PETn4	TX4-	B24	B21	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
GND	A22	A25	GROUND	GROUND	–	GROUND	GROUND	B25	B22			
HS	A23	A26	PERp5	RX5+	←	PETp5	TX5+	B26	B23	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
HS	A24	A27	PERn5	RX5-	←	PETn5	X5-	B27	B24	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
GND	A25	A28	GROUND	GROUND	–	GROUND	GROUND	B28	B25			
SB	A26	A29	BP_TYPEB (VSPB)	BP_TYPEB (SB7B)	↔	BP_TYPEB (VSPB)	BP_TYPEB(SB7B)	B29	B26			
SB	A27	A30	CWAKEB#,OBFFB (VSPB)	RESETB, SDataOutB (SB4B)	↔	CWAKEB#,OBFFB (VSPB)	RESETB, SDataOutB (SB4B)	B30	B27	P1 (WAKE#)	P1 (WAKE#)	
SB	A28	A31	GND	GND(SB3B)	–	GND	GND(SB3B)	B31	B28			
SB	A29	A32	REFCLKB+ (VSPB+)	(SBB+)	→	REFCLKB+(VSPB+)	(SBB+)	B32	B29	E7 (REFCLK+)	E7 (REFCLK+)	
SB	A30	A33	REFCLKB- (VSPB-)	(SBB-)	→	REFCLKB- (VSPB-)	(SBB-)	B33	B30	E8 (REFCLK-)	E8 (REFCLK-)	
GND	A31	A34	GROUND	GROUND	–	GROUND	GROUND	B34	B31			
HS	A32	A35	PERp6	RX6+	←	PETp6	TX6+	B35	B32	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
HS	A33	A36	PERn6	RX6-	←	PETn6	TX6-	B36	B33	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
GND	A34	A37	GROUND	GROUND	–	GROUND	GROUND	B37	B34			
HS	A35	A38	PERp7	RX7+	←	PETp7	TX7+	B38	B35	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
HS	A36	A39	PERn7	RX7-	←	PETn	TX7-	B39	B36	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
GND	A37	A40	GROUND	GROUND	–	GROUND	GROUND	B40	B37			

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Table 6-3 Multiprotocol SAS-4/ Other Protocol (x8) Cables (2 of 2)

	Root / Controller				CABLE	*Endpoint* / Backplane				*Devices on Backplane*		
SFF-9400	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 Multi-Protocol (Other Protocol (O/P), SAS-4)) x8 Cable Interface			9402 Multi-Protocol (Other Protocol (O/P), SAS-4)) x8 Cable Interface		SFF-8621 (80-circuit)	SFF-8654 (74-circuit)	SFF-8639 Connector		
Type 1 8X	*O/P* SAS-4	*O/P* SAS-4	Other Protocol and SAS-4/ SFF-8448 Signal Names			Other Protocol and SAS-4/ SFF-8448 Signal Names		*O/P SAS-4*	*O/P SAS-4*	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
	PIN	PIN	*ROOT*	Controller	DIR	*Endpoint*	Backplane	PIN	PIN	PIN	PIN	PIN
GND	B1	B1	GROUND	GROUND	–	*GROUND*	*GROUND*	A1	A1			
HS	B2	B2	*PETp0*	TX0+	→	*PERp0*	RX0+	A2	A2	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
HS	B3	B3	*PETn0*	TX0-	→	*PERn0*	RX0-	A3	A3	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
GND	B4	B4	GROUND	GROUND	–	GROUND	GROUND	A4	A4			
HS	B5	B5	*PETp1*	TX1+	→	*PERp1*	RX1+	A5	A5	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
HS	B6	B6	*PETn1*	TX1-	→	*PERn1*	RX1-	A6	A6	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
GND	B7	B7	GROUND	GROUND	–	GROUND	GROUND	A7	A7			
SB	B8	B8	*2W-CLKA*	2W-CLKA, SClockA (SB0A)	↔	*2W-CLKA*	2W-CLKA, SClockA (SB0A)	A8	A8			
SB	B9	B9	*2W-DATAA*	2W-DATAA, SLoadA (SB1A)	↔	*2W-DATAA*	2W-DATAA, SLoadA (SB1A)	A9	A9			
SB	B10	B10	*GND*	GND (SB2A)	–	*GND*	GND (SB2A)	A10	A10			
SB	B11	B11	*PERSTA# (VSPA)*	ADDA, SDataInA (SB5A)	↔	*PERSTA# (VSPA)*	ADDA, SDataInA (SB5A)	A11	A11	E5 (PERST#)	E5 (PERST#)	
SB	B12	B12	*CPRSNTA# (VSPA)*	CNTRLR_TYPEA (SB6A)	↔	*CPRSNTA# (VSPA)*	CNTRLR_TYPEA (SB6A)	A12	A12			
GND	B13	B13	GROUND	GROUND	–	GROUND	GROUND	A13	A13			
HS	B14	B14	*PETp2*	TX2+	→	*PERp2*	RX2+	A14	A14	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
HS	B15	B15	*PETn2*	TX2-	→	*PERn2*	RX2-	A15	A15	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
GND	B16	B16	GROUND	GROUND	–	GROUND	GROUND	A16	A16			
HS	B17	B17	*PETp3*	TX3+	→	*PERp3*	RX3+	A17	A17	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
HS	B18	B18	*PETn3*	TX3-	→	*PERn3*	RX3-	A18	A18	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
GND	B19	B19	GROUND	GROUND	–	GROUND	GROUND	A19	A19			
RSV		B20	POWER 5V #1	RESERVED	NO WIRE	POWER 3.3 Vact RX	RESERVED	A20				
RSV		B21	POWER 5V #2	RESERVED	NO WIRE	POWER 3.3 Vact TX	RESERVED	A21				
GND		B22	GROUND	GROUND	–	GROUND	GROUND	A22				
HS	B20	B23	*PETp4*	TX4+	→	*PERp4*	RX4+	A23	A20	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
HS	B21	B24	*PETn4*	TX4-	→	*PERn4*	RX4-	A24	A21	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
GND	B22	B25	GROUND	GROUND	–	GROUND	GROUND	A25	A22			
HS	B23	B26	*PETp5*	TX5+	→	*PERp5*	RX5+	A26	A23	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
HS	B24	B27	*PETn5*	TX5-	→	*PERn5*	RX5-	A27	A24	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
GND	B25	B28	GROUND	GROUND	–	GROUND	GROUND	A28	A25			
SB	B26	B29	*2W-CLKB (VSPB)*	2W-CLKB, SClockB (SB0B)	↔	*2W-CLKB (VSPB)*	2W-CLKB, SClockB (SB0B)	A29	A26			
SB	B27	B30	*2W-DATAB (VSPB)*	2W-DATAB, SLoadB (SB1B)	↔	*2W-DATAB (VSPB)*	2W-DATAB, SLoadB (SB1B)	A30	A27			
SB	B28	B31	*GND*	GND (SB2B)	–	*GND*	GND (SB2B)	A31	A28			
SB	B29	B32	*PERSTB# (VSPB)*	ADDB, SDataInB (SB5B)	↔	*PERSTB# (VSPB)*	ADDB, SDataIn (SB5B)	A32	A29	E5 (PERST#)	E5 (PERST#)	
SB	B30	B33	*CPRSNTB# (VSPB)*	CNTRLR_TYPEB (SB6B)	↔	*CPRSNTB# (VSPB)*	CNTRLR_TYPEB (SB6B)	A33	A30			
GND	B31	B34	GROUND	GROUND	–	GROUND	GROUND	A34	A31			
HS	B32	B35	*PETp6*	TX6+	→	*PERp6*	RX6+	A35	A32	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
HS	B33	B36	*PETn6*	TX6-	→	*PERn6*	RX6-	A36	A33	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
GND	B34	B37	GROUND	GROUND	–	GROUND	GROUND	A37	A34			
HS	B35	B38	*PETp7*	TX7+	→	*PERp*	RX7+	A38	A35	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
HS	B36	B39	*PETn7*	TX7-	→	*PERn7*	RX7-	A39	A36	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
GND	B37	B40	GROUND	GROUND	–	GROUND	GROUND	A40	A37			

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Table 6-4 Multiprotocol SAS-4/ Other Protocol (x8) to SAS-4/ OCuLink/ Other Protocol (x4) Y-Cables (1 of 2)

	Root / Controller				CABLE	*Endpoint* / Backplane				*Devices on Backplane*		
SFF-9400	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 Multi-Protocol (Other Protocol (O/P), SAS-4)) x8 Cable Interface			9402 Multi-Protocol (OCuLink, Other Protocol (O/P), SAS-4)) Pair of x4 Cable Interfaces		SFF-8621 (42-circuit)	SFF-8654 (38-circuit)	SFF-8639 Connector		
Type 1 8X	*O/P* SAS-4	*O/P* SAS-4	Other Protocol and SAS-4 / SFF-8448 Signal Names			OCuLink, Other Protocol and SAS-4 / SFF-8448 Signal Names		*OCuLink/* SAS-4	*O/P* SAS-4	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
	PIN	PIN	*ROOT*	Controller	DIR	*Endpoint*	Backplane	PIN	*PIN*	PIN	PIN	PIN
					NO WIRE	POWER_5V		B1				
GND	A1	A1	GROUND	GROUND	–	GROUND	GROUND	B2	B1			
HS	A2	A2	*PERp0*	RX0+	←	*PETp0*	TX0+	B3	B2	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
HS	A3	A3	*PERn0*	RX0-	←	*PETn0*	TX0-	B4	B3	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
GND	A4	A4	GROUND	GROUND	–	GROUND	GROUND	B5	B4			
HS	A5	A5	*PERp1*	RX1+	←	*PETp1*	TX1+	B6	B5	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
HS	A6	A6	*PERn1*	RX1-	←	*PETn1*	TX1-	B7	B6	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
GND	A7	A7	GROUND	GROUND	–	GROUND	GROUND	B8	B7			
SB	A8	A8	*BP_TYPEA(VSPA)*	BP_TYPEA (SB7A)	↔	*BP_TYPEA(VSPA)*	BP_TYPEA (SB7A)	B9	B8			
SB	A9	A9	*CWAKEA#,OBFFA (VSPA)*	RESETA, SDataOutA (SB4A)	↔	*CWAKEA#, OBFFA)(VSPA)*	RESETA, SDataOutA (SB4A)	B10	B9	P1 (WAKE#)	P1 (WAKE#)	
SB	A10	A10	*GND*	GND (SB3A)	–	*GND*	GND (SB3A)	B11	B10			
SB	A11	A11	*REFCLKA+ (VSPA+)*	(SBA+)	→	*REFCLKA+(VSPA+)*	(SBA+)	B12	B11	E7 (REFCLK+)	E7 (REFCLK+)	
SB	A12	A12	*REFCLKA- (VSPA-)*	(SBA-)	→	*REFCLKA-(VSPA-)*	(SBA-)	B13	B12	E8 (REFCLK-)	E8 (REFCLK-)	
GND	A13	A13	GROUND	GROUND	–	GROUND	GROUND	B14	B13			
HS	A14	A14	*PERp2*	RX2+	←	*PETp2*	TX2+	B15	B14	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
HS	A15	A15	*PERn2*	RX2-	←	*PETn2*	TX2-	B16	B15	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
GND	A16	A16	GROUND	GROUND	–	GROUND	GROUND	B17	B16			
HS	A17	A17	*PERp3*	RX3+	←	*PETp3*	TX3+	B18	B17	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
HS	A18	A18	*PERn3*	RX3-	←	*PETn3*	TX3-	B19	B18	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
GND	A19	A19	GROUND	GROUND	–	GROUND	GROUND	B20	B19			
RSV		A20	POWER 3.3 Vact RX	RESERVED	NC	POWER 3.3 Vact TX	RESERVED	B21				
RSV		A21	POWER 3.3 Vact TX	RESERVED	NC	POWER_5V #1	RESERVED	B1				
GND	A19	A22	GROUND	GROUND	–	GROUND	GROUND	B2	B1			
HS	A20	A23	*PERp4*	RX4+	←	*PETp4*	TX4+	B3	B2	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
HS	A21	A24	*PERn4*	RX4-	←	*PETn4*	TX4-	B4	B3	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
GND	A22	A25	GROUND	GROUND	–	GROUND	GROUND	B5	B4			
HS	A23	A26	*PERp5*	RX5+	←	*PETp5*	TX5+	B6	B5	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
HS	A24	A27	*PERn5*	RX5-	←	*PETn5*	TX5-	B7	B6	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
GND	A25	A28	GROUND	GROUND	–	GROUND	GROUND	B8	B7			
SB	A26	A29	*BP_TYPEB (VSPB)*	BP_TYPEB (SB7B)	↔	*BP_TYPEB (VSPB)*	BP_TYPEB (SB7B)	B9	B8			
SB	A27	A30	*CWAKEB#,OBFFB (VSPB)*	RESETB, SDataOutB (SB4B)	↔	*CWAKEB#,OBFFB (VSPB)*	RESETB, SDataOutB (SB4B)	B10	B9	P1 (WAKE#)	P1 (WAKE#)	
SB	A28	A31	*GND*	GND (SB3B)	–	*GND*	GND (SB3B)	B11	B10			
SB	A29	A32	*REFCLKB+ (VSPB+)*	(SBB+)	→	*REFCLKB+ (VSPB+)*	(SBB+)	B12	B11	E7 (REFCLK+)	E7 (REFCLK+)	
SB	A30	A33	*REFCLKB- (VSPB-)*	(SBB-)	→	*REFCLKB- (VSPB-)*	(SBB-)	B13	B12	E8 (REFCLK-)	E8 (REFCLK-)	
GND	A31	A34	GROUND	GROUND	–	GROUND	GROUND	B14	B13			
HS	A32	A35	*PERp6*	RX6+	←	*PETp6*	TX6+	B15	B14	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
HS	A33	A36	*PERn6*	RX6-	←	*PETn6*	TX6-	B16	B15	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
GND	A34	A37	GROUND	GROUND	–	GROUND	GROUND	B17	B16			
HS	A35	A38	*PERp7*	RX7+	←	*PETp7*	TX7+	B18	B17	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
HS	A36	A39	*PERn7*	RX7-	←	*PETn7*	TX7-	B19	B18	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
GND	A37	A40	GROUND	GROUND	–	GROUND	GROUND	B20	B19			
					NO WIRE	POWER 3.3 Vact TX		B21				

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Table 6-5 Multiprotocol SAS-4/ Other Protocol (x8) to SAS-4/ OCuLink/ Other Protocol (x4) Y-Cables (2 of 2)

	Root / Controller				CABLE	*Endpoint* / Backplane				*Devices on Backplane*		
SFF-9400	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 Multi-Protocol (Other Protocol (O/P), SAS-4)) x8 Cable Interface			9402 Multi-Protocol (OCuLink, Other Protocol (O/P), SAS-4)) Pair of x4 Cable Interfaces		SFF-8621 (42-circuit)	SFF-8654 (38-circuit)	SFF-8639 Connector		
Type 1 8X	*O/P* SAS-4	*O/P* SAS-4	Other Protocol and SAS-4/ SFF-8448 Signal Names			OCuLink and SAS-4/ SFF-8448 Signal Names		*OCuLink/* SAS-4	*O/P* SAS-4	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
	PIN	PIN	*ROOT*	Controller	DIR	*Endpoint*	Backplane	PIN	PIN	PIN	PIN	PIN
				RESERVED	NO WIRE	POWER 3.3 Vact RX	RESERVED	A1				
GND	B1	B1	*GROUND*	*GROUND*	—	*GROUND*	*GROUND*	A2	A1			
HS	B2	B2	*PETp0*	TX0+	→	*PERp0*	RX0+	A3	A2	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
HS	B3	B3	*PETn0*	TX0-	→	*PERn0*	RX0-	A4	A3	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
GND	B4	B4	GROUND	GROUND	—	GROUND	GROUND	A5	A4			
HS	B5	B5	*PETp1*	TX1+	→	*PERp1*	RX1+	A6	A5	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
HS	B6	B6	*PETn1*	TX1-	→	*PERn1*	RX1-	A7	A6	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
GND	B7	B7	*GROUND*	*GROUND*	—	*GROUND*	*GROUND*	A8	A7			
SB	B8	B8	*2W-CLKA*	2W-CLKA, SClockA (SB0A)	↔	*2W-CLKA*	2W-CLKA, SClockA (SB0A)	A9	A8			
SB	B9	B9	*2W-DATAA*	2W-DATAA, SLoadA (SB1A)	↔	*2W-DATAA*	2W-DATAA, SLoadA (SB1A)	A10	A9			
SB	B10	B10	*GND*	GND(SB2A)	—	*GND*	GND(SB2A)	A11	A10			
SB	B11	B11	*PERSTA# (VSPA)*	ADDA, SDataInA (SB5A)	↔	*PERSTA# (VSPA)*	ADDA, SDataInA (SB5A)	A12	A11	E5 (PERST#)	E5 (PERST#)	
SB	B12	B12	*CPRSNTA# (VSPA)*	CNTRLR_TYPEA (SB6A)	↔	*CPRSNTA# (VSPA)*	CNTRLR_TYPEA (SB6A)	A13	A12			
GND	B13	B13	*GROUND*	*GROUND*	—	*GROUND*	*GROUND*	A14	A13			
HS	B14	B14	*PETp2*	TX2+	→	*PERp2*	RX2+	A15	A14	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
HS	B15	B15	*PETn2*	TX2-	→	*PERn2*	RX2-	A16	A15	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
GND	B16	B16	GROUND	GROUND	—	GROUND	GROUND	A17	A16			
HS	B17	B17	*PETp3*	TX3+	→	*PERp3*	RX3+	A18	A17	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
HS	B18	B18	*PETn3*	TX3-	→	*PERn3*	RX3-	A19	A18	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
GND	B19	B19	*GROUND*	*GROUND*	—	*GROUND*	*GROUND*	A20	A19			
RSV		B20	POWER 5V #1	RESERVED	NO WIRE	POWER 5 V #2	RESERVED	A21				
RSV		B21	POWER 5V #2	RESERVED	NO WIRE	POWER 3.3 Vact RX	RESERVED	A1				
GND	B19	B22	*GROUND*	*GROUND*	—	*GROUND*	*GROUND*	A2	A1			
HS	B20	B23	*PETp4*	TX4+	→	*PERp4*	RX4+	A3	A2	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
HS	B21	B24	*PETn4*	TX4-	→	*PERn4*	RX4-	A4	A3	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
GND	B22	B25	GROUND	GROUND	—	GROUND	GROUND	A5	A4			
HS	B23	B26	*PETp5*	TX5+	→	*PERp5*	RX5+	A6	A5	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
HS	B24	B27	*PETn5*	TX5-	→	*PERn5*	RX5-	A7	A6	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
GND	B25	B28	*GROUND*	*GROUND*	—	*GROUND*	*GROUND*	A8	A7			
SB	B26	B29	*2W-CLKB*	2W-CLKB, SClockB (SB0B)	↔	*2W-CLKB*	2W-CLKB, SClockB (SB0B)	A9	A8			
SB	B27	B30	*2W-DATAB*	2W-DATAB, SLoadB (SB1B)	↔	*2W-DATAB*	2W-DATAB, SLoadB (SB1B)	A10	A9			
SB	B28	B31	*GND*	GND(SB2B)	—	*GND*	(SB2B)GND	A11	A10			
SB	B29	B32	*PERSTB# (VSPB)*	ADDB, SDataInB (SB5B)	↔	*PERSTB# (VSPB)*	ADDB, SDataIn (SB5B)	A12	A11	E5 (PERST#)	E5 (PERST#)	
SB	B30	B33	*CPRSNTB# (VSPB)*	CNTRLR_TYPEB (SB6B)	↔	*CPRSNTB (VSPB)*	CNTRLR_TYPEB (SB6B)	A13	A12			
GND	B31	B34	*GROUND*	*GROUND*	—	*GROUND*	*GROUND*	A14	A13			
HS	B32	B35	*PETp6*	TX6+	→	*PERp6*	RX6+	A15	A14	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
HS	B33	B36	*PETn6*	TX6-	→	*PERn6*	RX6-	A16	A15	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
GND	B34	B37	GROUND	GROUND	—	GROUND	GROUND	A17	A16			
HS	B35	B38	*PETp7*	TX7+	→	*PERp7*	RX7+	A18	A17	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
HS	B36	B39	*PETn7*	TX7-	→	*PERn7*	RX7-	A19	A18	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
GND	B37	B40	*GROUND*	*GROUND*	—	*GROUND*	*GROUND*	A20	A19			
					NO WIRE	POWER 5 V #2	RESERVED	A21				

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Table 6-6 Multiprotocol SAS-4/ OCuLink/ Standard and Other 2-Wire Type/ UBM Sideband Table (1 of 1)

	Multiprotocol Sideband Signal Assignments					Root/ Controller		CABLE	Endpoint/ Backplane	
	SFF-9402 Inerface for Multiprotocol (SAS/ PCIe OCuLink / Other Protocol) Root/ Contoller (x4) to Endpoint/ Backplane (x4) Cables					SFF-8654 (38-circuit)	SFF-8621 (42-circuit)		SFF-8621 (42-circuit)	SFF-8654 (38-circuit)
SIDE BANDS	SGPIO (SFF-8485) SFF-8448	Standard 2-Wire Type SFF-8448	PCIe OCuLink	Other 2-Wire Type SFF-8448	UBM SFF-TA-1005	SAS-4	SAS-4		SAS-4	SAS-4
NAME	*Signal Name*	*Signal Name*	*Signal Name*	*Signal Name*	*Signal Name*	PIN	PIN	DIR	PIN	PIN
SB7	BP_TYPE	BP_TYPE	BP_TYPE/ VSP	BP_TYPE/ VSP	BP_TYPE	A8	A9	←	B9	B8
SB4	SDataOut	RESET	*CWAKE#/ OBFF*	VSP	2W_RST#	A9	A10	→	B10	B9
SB3	GND	GND	GND	VSP	GND	A10	A11	—	B11	B10
SB+	(SB+)	(SB+)	VSP(+)	VSP+	(SB+)	A11	A12	→	B12	B11
SB-	(SB-)	(SB-)	VSP(-)	VSP-	(SB-)	A12	A13	→	B13	B12
SB0	SClock	2W-CLK	2W-CLK	2W-CLK	2W-CLK	B8	B9	↔	A9	A8
SB1	SLoad	2W-DATA	2W-DATA	2W-DATA	2W-DATA	B9	B10	↔	A10	A9
SB2	GND	GND	GND	GND	GND	B10	B11	—	A11	A10
SB5	SDataIn	ADD	PERST#	VSP	PERST#	B11	B12	↔	A12	A11
SB6	CNTRLR_TYPE	CNTRLR_TYPE	CPRSNT#	VSP	CHG_DETECT#/ CPRSNT#	B12	B13	↔	A13	A12

In Table 6-6above, the five (5) possible sideband connection types shown support SGPIO/ Standard 2-Wire Type (normally associated with SAS)/ PCIe OCuLink and Other 2-Wire Type/ SFF-TA-1005 UBM. UBM supports both SAS and PCIe management. It also fits within the Other 2-Wire Type defined in SFF-8448.

Note: All the highspeed connections shown in Table 6-1 through Table 6-5 are common and independent of the sideband interface implemented.

REFERENCE

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7. SFF-8621, SFF-8654, SFF-8643, OCuLink (x4)/ Other Protocol (x4/x8) Legacy Cables

The following five (5) tables provide signal assignments for OCuLink x4 and Other Protocol x4/ x8 applications based on SFF-8621, SFF-8654 and SFF-8643. This section addresses Root and Endpoint devices that may have different physical connectors.

In this section:

1. Cables with the same mechanical connector at both ends are electrically and physically reversible.
2. Cables with different connectors on its ends will work regardless of the mechanical location of the fixed side ends but are not mechanically reversible.
3. Table that only defines the sideband assignments based on OCuLink, SFF-8448 Other 2-Wire Type and SFF-TA-1005 (UBM).UBM was not added to Table 7-1 through Table 7-5 to minimize the number of columns required.

The high speed differential pairs including the sidebands for REFCLK (VSP+/-) and their reversible path (PERST#/ CPRSNT#) respectively are highlighted/ shaded in the x4 along with (VSP[A,B]+/-) as well as their (PERST[A,B]#/ CPRSNT[A,B]#) x8 connections. They must be wired as differential pairs to cover the cable being flipped between Root and Endpoint.

The highspeed differential and sideband signals are color coded (OCuLink, Other Protocol=Green/ Italic) to indicate their associated naming convention/ protocol. The arrows provide the signal flow direction between Root and Endpoint. In addition, brown was used to identify double ground pin assignments where applicable between different connector types and Y-cables.

The pins designated "POWER" that are shown in these tables as "NO WIRE". Refer to Section 5 for more details.

1. OCuLink SFF-8621 / Other Protocol SFF-8654/ SFF-8643 Other Protocol x4 Cables
   Table 7-1 defines the cable interface between SFF-8621/ SFF-8654/ SFF-8643 connections only. These cables are fully reversible such that they can be flipped end to end between Root and Endpoint
2. Other Protocol SFF-8621 / SFF-8654 / SFF-8643 x8 Cables
   Table 7-2 and Table 7-3 define the cable interface for SFF-8621/ SFF-8654 to SFF-8643 connections only. These cables are fully reversible such that they can be flipped end to end between Root and Endpoint
   a. Note: In the x8 configuration the sidebands designated with an "A" suffix are considered the primary path when only a single set of sidebands are required to manage the bus. The sideband bus with a "B" suffix is also shown with VSP indicating possible vendor specific specification. The pins associated with associated with REFCLKB+/- (VSPB+/-) and PERSTB#/ CPRSNTB#) must be implemented in the cable as differential pairs.
3. Other Protocol SFF-8621, SFF-8654, SFF-8643 x8 to SFF-8621, SFF-8654, SFF-8643 Y-Cables
   Table 7-4 and Table 7-5 defines the cable interface for Other Protocol x8 SFF-8621/ SFF-8654/ SFF-8643 to OCuLink (SFF-8621)/ Other Protocol SFF-8654/ SFF-8643 x4 "Y-Cable" connections only. These cables are fully reversible such that they can be flipped end to end between Root and Endpoint
   a. Note: Both sets of sidebands are required to support a Y-cable configuration where two independent x4 interfaces are connected to a single x8 interface as described in the previous table.
4. Sideband Signal Assignments
   Table 7-6 defines the sideband assignments only. Although Table 7-1 through Table 7-5 define OCuLink and SFF-8448 Other 2-Wire Type, this table includes SFF-TA-1005 (UBM). Note: UBM can be considered the Other 2-Wire Type that can support PCIe and Other protocol.

REFERENCE

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Table 7-1 OCuLink and Other Protocol (x4) Legacy Cables (1 of 1)

	Root				Cable	End Point				Devcies on Backplane	
SFF-9400	SFF-8643	SFF-8654 (38-circuit)	SFF-8621 (42-circuit)	9402 Multi-Protocol *OCuLink, Other Protocol (O/P)* x4 Cable Interface		9402 Multi-Protocol *OCuLink, Other Protocol (O/P)* x4 Cable Interface	SFF-8621 (42 Circuit)	SFF-8654 (38 Circuit)	SFF-8643	SFF-8639 Connector	
Type 1 4X	*O/P*	*O/P*	*OCuLink*	*OCuLink* Signal Names		*OCuLink* Signal Names	*OCuLink*	*O/P*	*O/P*	Quad PCI Express® (x4)	SFF-TA-1001 (x4)
	PIN	PIN	PIN	*ROOT*	DIR	*END Point*	PIN	PIN	PIN	PIN	PIN
RSV			A1	POWER 3.3 Vact RX	NO WIRE	POWER 5 V #1	B1				
GND	B3	A1	A2	GROUND	—	GROUND	B2	B1	D3		
HS	B4	A2	A3	*PERp0*	←	*PETp0*	B3	B2	D4	E14 (PERp0)	S6 (PERp0)
HS	B5	A3	A4	*PERn0*	←	*PETn0*	B4	B3	D5	E13 (PERn0)	S5 (PERn0)
GND	A3	A4	A5	GROUND	—	GROUND	B5	B4	C3		
HS	A4	A5	A6	*PERp1*	←	*PETp1*	B6	B5	C4	S21 (PERp1)	S13 (PERp1)
HS	A5	A6	A7	*PERn1*	←	*PETn1*	B7	B6	C5	S20 (PERn1)	S12 (PERn1)
GND	A6	A7	A8	GROUND	—	GROUND	B8	B7	C6		
SB	A1	A8	A9	*BP_TYPE (VSP)*	↔	*BP_TYPE (VSP)*	B9	B8	A2		
SB	B1	A9	A10	*CWAKE#, OBFF (VSP)*	↔	*CWAKE#, OBFF (VSP)*	B10	B9	B2	P1 (WAKE#)	P1 (WAKE#)
SB		A10	A11	*GND*	—	*GND*	B11	B10			
SB	C1	A11	A12	*REFCLK+ (VSP+)*	→	*REFCLK+ (VSP+)*	B12	B11	C2	E7 (REFCLK+)	E7 (REFCLK+)
SB	D1	A12	A13	*REFCLK- (VSP-)*	→	*REFCLK- (VSP-)*	B13	B12	D2	E8 (REFCLK-)	E8 (REFCLK-)
GND	B6	A13	A14	GROUND	—	GROUND	B14	B13	D6		
HS	B7	A14	A15	*PERp2*	←	*PETp2*	B15	B14	D7	S27 (PERp2)	S21(PERp2)
HS	B8	A15	A16	*PERn2*	←	*PETn2*	B16	B15	D8	S26 (PERn2)	S20 (PERn2)
GND	B9	A16	A17	GROUND	—	GROUND	B17	B16	D9		
HS	A7	A17	A18	*PERp3*	←	*PETp3*	B18	B17	C7	E21 (PERp3)	S27 (PERp3)
HS	A8	A18	A19	*PERn3*	←	*PETn3*	B19	B18	C8	E20 (PERn3)	S26 (PERn3)
GND	A9	A19	A20	GROUND	—	GROUND	B20	B19	C9		
RSV			A21	POWER 5 V #2	NO WIRE	POWER 3.3 Vact TX	B21				
RSV			B1	POWER 5 V #1	NO WIRE	POWER 3.3 Vact RX	A1				
GND	D3	B1	B2	GROUND	—	GROUND	A2	A1	B3		
HS	D4	B2	B3	*PETp0*	→	*PERp0*	A3	A2	B4	E10 (PETp0)	S2 (PETp0)
HS	D5	B3	B4	*PETn0*	→	*PERn0*	A4	A3	B5	E11 (PETn0)	S3 (PETn0)
GND	C3	B4	B5	GROUND	—	GROUND	A5	A4	A3		
HS	C4	B5	B6	*PETp1*	→	*PERp1*	A6	A5	A4	S17 (PETp1)	S9 (PETp1)
HS	C5	B6	B7	*PETn1*	→	*PERn1*	A7	A6	A5	S18 (PETn1)	S10 (PETn1)
GND	C6	B7	B8	GROUND	—	GROUND	A8	A7	A6		
SB	A2	B8	B9	*2W-CLK*	↔	*2W-CLK*	A9	A8	A1		
SB	B2	B9	B10	*2W-DATA*	↔	*2W-DATA*	A10	A9	B1		
SB		B10	B11	*GND*	—	*GND*	A11	A10			
SB	C2	B11	B12	*PERST# (VSP)*	→	*PERST# (VSP)*	A12	A11	C1	E5 (PERST#)	E5 (PERST#)
SB	D2	B12	B13	*CPRSNT# (VSP)*	←	*CPRSNT# (VSP)*	A13	A12	D1		
GND	D6	B13	B14	GROUND	—	GROUND	A14	A13	B6		
HS	D7	B14	B15	*PETp2*	→	*PERp2*	A15	A14	B7	S23 (PETp2)	S17 (PETp2)
HS	D8	B15	B16	*PETn2*	→	*PERn2*	A16	A15	B8	S24 (PETn2)	S18 (PETn2)
GND	D9	B16	B17	GROUND	—	GROUND	A17	A16	B9		
HS	C7	B17	B18	*PETp3*	→	*PERp3*	A18	A17	A7	E17 (PETp3)	S23 (PETp3)
HS	C8	B18	B19	*PETn3*	→	*PERn3*	A19	A18	A8	E18 (PETn3)	E18 (PETn3)
GND	C9	B19	B20	GROUND	—	GROUND	A20	A19	A9		
RSV			B21	POWER 3.3 Vact TX	NO WIRE	POWER 5 V #2	A21				

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Table 7-2 Other Protocol (x8) Cables Based on SFF-8621/ SFF-8654/ SFF-8643 (1 of 2)

	Root					Endpoint				Devices on Backplane	
SFF-9400	SFF-8643	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface	CABLE	9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface	SFF-8621 (80-circuit)	SFF-8654 (74-circuit)	SFF-8643	SFF-8639 Connector	
Type 1 8X	O/P x4	O/P x8	O/P x8	Other Protocol Signal Names		Other Protocol Signal Names	O/P x8	O/P x8	O/P x4	Quad PCI Express® (x4)	SFF-TA-1001 (x4)
	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN	PIN
GND	B3	A1	A1	GROUND	–	GROUND	B1	B1	D3		
HS	B4	A2	A2	PERp0	←	PETp0	B2	B2	D4	E14 (PERp0)	S6 (PERp0)
HS	B5	A3	A3	PERn0	←	PETn0	B3	B3	D5	E13 (PERn0)	S5 (PERn0)
GND	A3	A4	A4	GROUND	–	GROUND	B4	B4	C3		
HS	A4	A5	A5	PERp1	←	PETp1	B5	B5	C4	S21 (PERp1)	S13 (PERp1)
HS	A5	A6	A6	PERn1	←	PETn1	B6	B6	C5	S20 (PERn1)	S12 (PERn1)
GND	A6	A7	A7	GROUND	–	GROUND	B7	B7	C6		
SB	A1	A8	A8	BP_TYPEA(VSPA)	↔	BP_TYPEA(VSPA)	B8	B8	A2		
SB	B1	A9	A9	CWAKEA#,OBFFA,(VSPA)	↔	CWAKEA#,OBFFA(VSPA)	B9	B9	B2	P1 (WAKE#)	P1 (WAKE#)
SB		A10	A10	GND	–	GND	B10	B10			
SB	C1	A11	A11	REFCLKA+ (VSPA+)	→	REFCLKA+ (VSPA+)	B11	B11	C2	E7 (REFCLK+)	E7 (REFCLK+)
SB	D1	A12	A12	REFCLKA- (VSPA-)	→	REFCLKA- (VSPA-)	B12	B12	D2	E8 (REFCLK-)	E8 (REFCLK-)
GND	B6	A13	A13	GROUND	–	GROUND	B13	B13	D6		
HS	B7	A14	A14	PERp2	←	PETp2	B14	B14	D7	S27 (PERp2)	S21(PERp2)
HS	B8	A15	A15	PERn2	←	PETn2	B15	B15	D8	S26 (PERn2)	S20 (PERn2)
GND	B9	A16	A16	GROUND	–	GROUND	B16	B16	D9		
HS	A7	A17	A17	PERp3	←	PETp3	B17	B17	C7	E21 (PERp3)	S27 (PERp3)
HS	A8	A18	A18	PERn3	←	PETn3	B18	B18	C8	E20 (PERn3)	S26 (PERn3)
GND	A9	A19	A19	GROUND	–	GROUND	B19	B19	C9		
RSV			A20	POWER 3.3 Vact RX	NO WIRE	POWER 5V#1	B20				
RSV			A21	POWER 3.3 Vact TX	NO WIRE	POWER 5V#2	B21				
GND	B3		A22	GROUND	–	GROUND	B22		D3		
HS	B4	A20	A23	PERp4	←	PETp4	B23	B20	D4	E14 (PERp0)	S6 (PERp0)
HS	B5	A21	A24	PERn4	←	PETn4	B24	B21	D5	E13 (PERn0)	S5 (PERn0)
GND	A3	A22	A25	GROUND	–	GROUND	B25	B22	C3		
HS	A4	A23	A26	PERp5	←	PETp5	B26	B23	C4	S21 (PERp1)	S13 (PERp1)
HS	A5	A24	A27	PERn5 /	←	PETn5	B27	B24	C5	S20 (PERn1)	S12 (PERn1)
GND	A6	A25	A28	GROUND	–	GROUND	B28	B25	C6		
SB	A1	A26	A29	BP_TYPEB (VSPB)	↔	BP_TYPEB (VSPB)	B29	B26	A2		
SB	B1	A27	A30	CWAKEB#,OBFFB (VSPB)	↔	CWAKEB#,OBFFB (VSPB)	B30	B27	B2	P1 (WAKE#)	P1 (WAKE#)
SB		A28	A31	GND	–	GND	B31	B28			
SB	C1	A29	A32	REFCLKB+ (VSPB+)	→	REFCLKB+ (VSPB+)	B32	B29	C2	E7 (REFCLK+)	E7 (REFCLK+)
SB	D1	A30	A33	REFCLKB- (VSPB-)	→	REFCLKB- (VSPB-)	B33	B30	D2	E8 (REFCLK-)	E8 (REFCLK-)
GND	B6	A31	A34	GROUND	–	GROUND	B34	B31	D6		
HS	B7	A32	A35	PERp6	←	PETp6	B35	B32	D7	S27 (PERp2)	S21(PERp2)
HS	B8	A33	A36	PERn6	←	PETn6	B36	B33	D8	S26 (PERn2)	S20 (PERn2)
GND	B9	A34	A37	GROUND	–	GROUND	B37	B34	D9		
HS	A7	A35	A38	PERp7	←	PETp7	B38	B35	C7	E21 (PERp3)	S27 (PERp3)
HS	A8	A36	A39	PERn7	←	PETn7	B39	B36	C8	E20 (PERn3)	S26 (PERn3)
GND	A9	A37	A40	GROUND	–	GROUND	B40	B37	C9		

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Table 7-3 Other Protocol (x8) Cables Based on SFF-8621/ SFF-8654/ SFF-8643 (2 of 2)

	Root					Endpoint				Devices on Backplane	
SFF-9400	SFF-8643	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 Multi-Protocol *(Other Protocol (O/P))* x8 Cable Interface	CABLE	9402 Multi-Protocol *(Other Protocol (O/P))* x8 Cable Interface	SFF-8621 (80-circuit)	SFF-8654 (74-circuit)	SFF-8643	SFF-8639 Connector	
Type 1 8X	*O/P x4*	*O/P x8*	*O/P x8*	*Other Protocol* Signal Names		*Other Protocol* Signal Names	*O/P x8*	*O/P x8*	*O/P x4*	Quad PCI Express® (x4)	SFF-TA-1001 (x4)
	PIN	PIN	PIN	*ROOT*	DIR	*END Point*	PIN	PIN	PIN	PIN	PIN
GND	D3	B1	B1	*GROUND*	–	*GROUND*	A1	A1	B3		
HS	D4	B2	B2	*PETp0*	→	*PERp0*	A2	A2	B4	E10 (PETp0)	S2 (PETp0)
HS	D5	B3	B3	*PETn0*	→	*PERn0*	A3	A3	B5	E11 (PETn0)	S3 (PETn0)
GND	C3	B4	B4	GROUND	–	*GROUND*	A4	A4	A3		
HS	C4	B5	B5	*PETp1*	→	*PERp1*	A5	A5	A4	S17 (PETp1)	S9 (PETp1)
HS	C5	B6	B6	*PETn1*	→	*PERn1*	A6	A6	A5	S18 (PETn1)	S10 (PETn1)
GND	C6	B7	B7	*GROUND*	–	*GROUND*	A7	A7	A6		
SB	A2	B8	B8	*2W-CLKA*	↔	*2W-CLKA*	A8	A8	A1		
SB	B2	B9	B9	*2W-DATAA*	↔	*2W-DATAA*	A9	A9	B1		
SB		B10	B10	*GND*	–	*GND*	A10	A10			
SB	C2	B11	B11	*PERSTA# (VSPA)*	→	*PERSTA# (VSPA)*	A11	A11	C1	E5 (PERST#)	E5 (PERST#)
SB	D2	B12	B12	*CPRSNTA# (VSPA)*	←	*CPRSNT# (VSPA)*	A12	A12	D1		
GND	D6	B13	B13	*GROUND*	–	*GROUND*	A13	A13	B6		
HS	D7	B14	B14	*PETp2*	→	*PERp2*	A14	A14	B7	S23 (PETp2)	S17 (PETp2)
HS	D8	B15	B15	*PETn2*	→	*PERn2*	A15	A15	B8	S24 (PETn2)	S18 (PETn2)
GND	D9	B16	B16	GROUND	–	GROUND	A16	A16	B9		
HS	C7	B17	B17	*PETp3*	→	*PERp3*	A17	A17	A7	E17 (PETp3)	S23 (PETp3)
HS	C8	B18	B18	*PETn3*	→	*PERn3*	A18	A18	A8	E18 (PETn3)	S24 (PETn3)
GND	*C9*	B19	B19	*GROUND*	–	*GROUND*	A19	A19	A9		
RSV			B20	POWER 5V #1	NO WIRE	POWER 3.3 Vact RX	A20				
RSV			B21	POWER 5V #2	NO WIRE	POWER 3.3 Vact TX	A21				
GND	D3		B22	*GROUND*	–	*GROUND*	A22		B3		
HS	D4	B20	B23	*PETp4*	→	*PERp4*	A23	A20	B4	E10 (PETp0)	S2 (PETp0)
HS	D5	B21	B24	*PETn4*	→	*PERn4*	A24	A21	B5	E11 (PETn0)	S3 (PETn0)
GND	C3	B22	B25	GROUND	–	GROUND	A25	A22	A3		
HS	C4	B23	B26	*PETp5*	→	*PERp5*	A26	A23	A4	S17 (PETp1)	S9 (PETp1)
HS	C5	B24	B27	*PETn5*	→	*PERn5*	A27	A24	A5	S18 (PETn1)	S10 (PETn1)
GND	C6	B25	B28	*GROUND*	–	*GROUND*	A28	A25	A6		
SB	A2	B26	B29	*2W-CLKB (VSPB)*	↔	*2W-CLKB (VSPB)*	A29	A26	A1		
SB	B2	B27	B30	*2W-DATAB (VSPB)*	↔	*2W-DATAB (VSPB)*	A30	A27	B1		
SB		B28	B31	*GND*	–	*GND*	A31	A28			
SB	C2	B29	B32	*PERSTB# (VSPB)*	→	*PERSTB# (VSPB)*	A32	A29	C1	E5 (PERST#)	E5 (PERST#)
SB	D2	B30	B33	*CPRSNTB# (VSPB)*	←	*CPRSNTB# (VSPB)*	A33	A30	D1		
GND	D6	B31	B34	*GROUND*	–	*GROUND*	A34	A31	B6		
HS	D7	B32	B35	*PETp6/*	→	*PERp6*	A35	A32	B7	S23 (PETp2)	S17 (PETp2)
HS	D8	B33	B36	*PETn6*	→	*PERn6*	A36	A33	B8	S24 (PETn2)	S18 (PETn2)
GND	D9	B34	B37	GROUND	–	GROUND	A37	A34	B9		
HS	C7	B35	B38	*PETp7*	→	*PERp7*	A38	A35	A7	E17 (PETp3)	S23 (PETp3)
HS	C8	B36	B39	*PETn7*	→	*PERn7*	A39	A36	A8	E18 (PETn3)	S24 (PETn3)
GND	C9	B37	B40	*GROUND*	–	*GROUND*	A40	A37	A9		

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Table 7-4 Other Protocol (x8) to OCuLink/ Other Protocol (x4) Y-Cables (1 of 2)

	Root				CABLE	Endpoint				Devices on Backplane	
SFF-9400	SFF-8643	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface		9402 Multi-Protocol (OCuLink, Other Protocol (O/P)) Pair of x4 Cable Interfaces	SFF-8621 (42-circuit)	SFF-8654 (38-circuit)	SFF-8643	SFF-8639 Connector	
Type 1 8X	O/P	O/P	O/P	Other Protocol Signal Names		Other Protocol Signal Names	OCuLink x4	O/P x4	O/P x4	Quad PCI Express® (x4)	SFF-TA-1001 (x4)
	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN	PIN
					NO WIRE	POWER 5 V #1	B1				
GND	B3	A1	A1	GROUND	—	GROUND	B2	B1	D3		
HS	B4	A2	A2	PERp0	←	PETp0	B3	B2	D4	E14 (PERp0)	S6 (PERp0)
HS	B5	A3	A3	PERn0	←	PETn0	B4	B3	D5	E13 (PERn0)	S5 (PERn0)
GND	A3	A4	A4	GROUND	—	GROUND	B5	B4	C3		
HS	A4	A5	A5	PERp1	←	PETp1	B6	B5	C4	S21 (PERp1)	S13 (PERp1)
HS	A5	A6	A6	PERn1	←	PETn1	B7	B6	C5	S20 (PERn1)	S12 (PERn1)
GND	A6	A7	A7	GROUND	—	GROUND	B8	B7	C6		
SB	A1	A8	A8	BP_TYPEA (VSPA)	↔	BP_TYPEA (VSPA)	B9	B8	A2		
SB	B1	A9	A9	CWAKEA#, OBFFA (VSPA)	↔	CWAKEA#, OBFFA (VSPA)	B10	B9	B2	P1 (WAKE#)	P1 (WAKE#)
SB		A10	A10	GND	—	GND	B11	B10			
SB	C1	A11	A11	REFCLKA+ (VSPA+)	→	REFCLKA+ (VSPA+)	B12	B11	C2	E7 (REFCLK+)	E7 (REFCLK+)
SB	D1	A12	A12	REFCLKA- (VSPA-)	→	REFCLKA- (VSPA-)	B13	B12	D2	E8 (REFCLK-)	E8 (REFCLK-)
GND	B6	A13	A13	GROUND	—	GROUND	B14	B13	D6		
HS	B7	A14	A14	PERp2	←	PETp2	B15	B14	D7	S27 (PERp2)	S21(PERp2)
HS	B8	A15	A15	PERn2	←	PETn2	B16	B15	D8	S26 (PERn2)	S20 (PERn2)
GND	B9	A16	A16	GROUND	—	GROUND	B17	B16	D9		
HS	A7	A17	A17	PERp3	←	PETp3	B18	B17	C7	E21 (PERp3)	S27 (PERp3)
HS	A8	A18	A18	PERn3	←	PETn3	B19	B18	C8	E20 (PERn3)	S26 (PERn3)
GND	A9	A19	A19	GROUND	—	GROUND	B20	B19	C9		
RSV			A20	POWER 3.3 Vact RX	NO WIRE	POWER 3.3 Vact TX	B21				
RSV			A21	POWER 3.3 Vact TX	NO WIRE	POWER_5V #1	B1				
GND	B3	A19	A22	GROUND	—	GROUND	B2	B1	D3		
HS	B4	A20	A23	PERp4	←	PETp4	B3	B2	D4	E14 (PERp0)	S6 (PERp0)
HS	B5	A21	A24	PERn4	←	PETn4	B4	B3	D5	E13 (PERn0)	S5 (PERn0)
GND	A3	A22	A25	GROUND	—	GROUND	B5	B4	C3		
HS	A4	A23	A26	PERp5	←	PETp5	B6	B5	C4	S21 (PERp1)	S13 (PERp1)
HS	A5	A24	A27	PERn5	←	PETn5	B7	B6	C5	S20 (PERn1)	S12 (PERn1)
GND	A6	A25	A28	GROUND	—	GROUND	B8	B7	C6		
SB	A1	A26	A29	BP_TYPEB (VSPB)	↔	BP_TYPEB (VSPB)	B9	B8	A2		
SB	B1	A27	A30	CWAKEB#, OBFFB (VSPB)	↔	CWAKEB#, OBFFB (VSPB)	B10	B9	B2	P1 (WAKE#)	P1 (WAKE#)
SB		A28	A31	GND	—	GND	B11	B10			
SB	C1	A29	A32	REFCLKB+ (VSPB+)	→	REFCLKB+ (VSPB+)	B12	B11	C2	E7 (REFCLK+)	E7 (REFCLK+)
SB	D1	A30	A33	REFCLKB- (VSPB-)	→	REFCLKB- (VSPB-)	B13	B12	D2	E8 (REFCLK-)	E8 (REFCLK-)
GND	B6	A31	A34	GROUND	—	GROUND	B14	B13	D6		
HS	B7	A32	A35	PERp6	←	PETp6	B15	B14	D7	S27 (PERp2)	S21(PERp2)
HS	B8	A33	A36	PERn6	←	PETn6	B16	B15	D8	S26 (PERn2)	S20 (PERn2)
GND	B9	A34	A37	GROUND	—	GROUND	B17	B16	D9		
HS	A7	A35	A38	PERp7	←	PETp7	B18	B17	C7	E21 (PERp3)	S27 (PERp3)
HS	A8	A36	A39	PERn7	←	PETn7	B19	B18	C8	E20 (PERn3)	S26 (PERn3)
GND	A9	A37	A40	GROUND	—	GROUND	B20	B19	C9		
					NO WIRE	POWER 3.3 Vact TX	B21				

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Table 7-5 Other Protocol (x8) to OCuLink/ Other Protocol Y-Cables (2 of 2)

	Root				CABLE	Endpoint				DEVICES	
SFF-9400	SFF-8643	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 Multi-Protocol (Other Protocol (O/P)) x8 Cable Interface		9402 Multi-Protocol (OCuLink, Other Protocol (O/P)) Pair of x4 Cable Interfaces	SFF-8621 (42-circuit)	SFF-8654 (38-circuit)	SFF-8643	SFF-8639 Connector	
Type 1 8X	O/P	O/P	O/P	Other Protocol Signal Names		Other Protocol Signal Names	OCuLink 1.0 x4	O/P x4	O/P x4	Quad PCI Express® (x4)	SFF-TA-1001 (x4)
	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN	PIN
					NO WIRE	POWER	A1				
GND	D3	B1	B1	GROUND	—	GROUND	A2	A1	B3		
HS	D4	B2	B2	PETp0	→	PERp0	A3	A2	B4	E10 (PETp0)	S2 (PETp0)
HS	D5	B3	B3	PETn0	→	PERn0	A4	A3	B5	E11 (PETn0)	S3 (PETn0)
GND	C3	B4	B4	GROUND	—	GROUND	A5	A4	A3		
HS	C4	B5	B5	PETp1	→	PERp1	A6	A5	A4	S17 (PETp1)	S9 (PETp1)
HS	C5	B6	B6	PETn1	→	PERn1	A7	A6	A5	S18 (PETn1)	S10 (PETn1)
GND	C6	B7	B7	GROUND	—	GROUND	A8	A7	A6		
SB	A2	B8	B8	2W-CLKA	↔	2W-CLKA	A9	A8	A1		
SB	B2	B9	B9	2W-DATAA	↔	2W-DATAA	A10	A9	B1		
SB		B10	B10	GND	—	GND	A11	A10			
SB	C2	B11	B11	PERSTA# (VSPA)	→	PERSTA# (VSPA)	A12	A11	C1	E5 (PERST#)	E5 (PERST#)
SB	D2	B12	B12	CPRSNTA# (VSPA)	←	CPRSNT# (VSPA)	A13	A12	D1		
GND	D6	B13	B13	GROUND	—	GROUND	A14	A13	B6		
HS	D7	B14	B14	PETp2	→	PERp2	A15	A14	B7	S23 (PETp2)	S17 (PETp2)
HS	D8	B15	B15	PETn2	→	PERn2	A16	A15	B8	S24 (PETn2)	S18 (PETn2)
GND	D9	B16	B16	GROUND	—	GROUND	A17	A16	B9		
HS	C7	B17	B17	PETp3	→	PERp3	A18	A17	A7	E17 (PETp3)	S23 (PETp3)
HS	C8	B18	B18	PETn3	→	PERn3	A19	A18	A8	E18 (PETn3)	S24 (PETn3)
GND	C9	B19	B19	GROUND	—	GROUND	A20	A19	A9		
RSV			B20	POWER 5V #1	NO WIRE	POWER 5V #2	A21				
RSV			B21	POWER 5V #2	NO WIRE	POWER 3.3 Vact RX	A1				
GND	D3	B19	B22	GROUND	—	GROUND	A2	A1	B3		
HS	D4	B20	B23	PETp4	→	PERp4	A3	A2	B4	E10 (PETp0)	S2 (PETp0)
HS	D5	B21	B24	PETn4	→	PERn4	A4	A3	B5	E11 (PETn0)	S3 (PETn0)
GND	C3	B22	B25	GROUND	—	GROUND	A5	A4	A3		
HS	C4	B23	B26	PETp5	→	PERp5	A6	A5	A4	S17 (PETp1)	S9 (PETp1)
HS	C5	B24	B27	PETn5	→	PERn5	A7	A6	A5	S18 (PETn1)	S10 (PETn1)
GND	C6	B25	B28	GROUND	—	GROUND	A8	A7	A6		
SB	A2	B26	B29	2W-CLKB (VSPB)	↔	2W-CLKB (VSPB)	A9	A8	A1		
SB	B2	B27	B30	2W-DATAB (VSPB)	↔	2W-DATAB (VSPB)	A10	A9	B1		
SB		B28	B31	GND	—	GND	A11	A10			
SB	C2	B29	B32	PERSTB# (VSPB)	→	PERSTB# (VSPB)	A12	A11	C1	E5 (PERST#)	E5 (PERST#)
SB	D2	B30	B33	CPRSNTB# (VSPB)	←	CPRSNTB# (VSPB)	A13	A12	D1		
GND	D6	B31	B34	GROUND	—	GROUND	A14	A13	B6		
HS	D7	B32	B35	PETp6/	→	PERp6	A15	A14	B7	S23 (PETp2)	S17 (PETp2)
HS	D8	B33	B36	PETn6	→	PERn6	A16	A15	B8	S24 (PETn2)	S18 (PETn2)
GND	D9	B34	B37	GROUND	—	GROUND	A17	A16	B9		
HS	C7	B35	B38	PETp7	→	PERp7	A18	A17	A7	E17 (PETp3)	S23 (PETp3)
HS	C8	B36	B39	PETn7	→	PERn7	A19	A18	A8	E18 (PETn3)	S24 (PETn3)
GND	C9	B37	B40	GROUND	—	GROUND	A20	A19	A9		
					NO WIRE	POWER 5V #2	A21				

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Table 7-6 PCIe OCuLink/ Other 2-Wire Type/ UBM Sideband Table (1 of 1)

Sideband Signal Assignments			Root			CABLE	Endpoint/ Backplane		
SFF-9402 Signal / Pin Assigments for PCIe / Other Protocol Cables			SFF-8643 (36-circuit)	SFF-8654 (38-circuit)	SFF-8621 (42-circuit)		SFF-8621 (42-circuit)	SFF-8654 (38-circuit)	SFF-8643 (36-circuit)
PCIe OCuLink	Other 2-Wire Type SFF-8448	UBM SFF-TA-1005	O/P	O/P	OCuLink		OCuLink	O/P	O/P
Signal Name	*Signal Name*	*Signal Name*	PIN	PIN	PIN	DIR	PIN	PIN	PIN
BP_TYPE/ VSP	BP_TYPE/ VSP	BP_TYPE (SB7)	A1	A8	A9	←	B9	B8	A2
CWAKE#/ OBFF	VSP	2W_RST# (SB4)	B1	A9	A10	→	B10	B9	B2
GND	VSP	GND (SB3)	—	A10	A11	—	B11	B10	—
VSP(+)	VSP+	REFCLK+ (SB+)	C1	A11	A12	→	B12	B11	C2
VSP(-)	VSP-	REFCLK- (SB-)	D1	A12	A13	→	B13	B12	D2
2W-CLK	2W-CLK	2W-CLK (SB0)	A2	B8	B9	↔	A9	A8	A1
2W-DATA	2W-DATA	2W-DATA (SB1)	B2	B9	B10	↔	A10	A9	B1
GND	GND	GND (SB2)	—	B10	B11	—	A11	A10	—
PERST#	VSP	PERST# (SB5)	C2	B11	B12	→	A12	A11	C1
CPRSNT#	VSP	CHG_DETECT#/ CPRSNT# (SB6)	D2	B12	B13	←	A13	A12	D1

In Table 7-6 above, three (3) possible sideband connection types are shown that support PCIe OCuLink, SFF-8448 Other 2-Wire Type, and SFF-TA-1005 UBM. UBM supports both SAS and PCIe software management. It also fits within the Other 2-Wire Type defined in SFF-8448. Therefore, implementing one of the UBM hardware/ pinouts above enables a common PCIe/ SAS-4 reversible cable.

Note: All the highspeed connections shown in Table 7-1 through Table 7-5 are common and independent of the sideband interface implemented.

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8. SAS-4 (SFF-8621/ SFF-8654), MiniSAS HD (SFF-8643), MiniSAS (SFF-8087) (Legacy) Not Reversible Cables

The following seven (7) tables provide recommended signal assignments for SAS-4 (SFF-8621/ SFF-8654) and SAS-2.1/ SAS-3 (SFF-8087/ SFF-8643) only applications.

These cables are "NOT" reversible meaning that they cannot be flipped end to end between controller and a backplane. The SAS-4 specification moved SB4 and SB5 to allow SB+/- to be placed on dedicated pins to better optimize the SFF-8621/ SFF-8654 interfaces for multiprotocol operation. This indirectly impacted physical pin assignments for SB1/ SB2 and SB3/ SB4 on the x4 and SB[A,B]1, SB[A,B]2, SB[A,B]3 and SB[A,B]4 on the x8 configurations.

1. SAS (x4) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane
   Table 8-1 defines a cable solution between a controller with SFF-8087/ SFF-8643 to a backplane with SFF-8621/ SFF-8654
2. SAS (x4) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane
   Table 8-2 defines a cable solution between a controller with SFF-8621/ SFF-8654 to a backplane with legacy SFF-8087/ SFF-8643.
3. SAS (x8) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane
   Table 8-3 and Table 8-4 defines a cable solution between a controller with SFF-8087/ SFF-8654 to a backplane with SAS-4 SFF-8621/ SFF-8654.
   a. Note: This configuration could be considered as a Y-Cable for a pair of legacy x4 on a controller to backplane with x8 SAS-4 connections.
4. SAS (x8) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane
   Table 8-5 and Table 8-6 defines a cable solution between a controller with SAS-4 SFF-8621/ SFF-8654 and a backplane with legacy SFF-8087/ SFF-8654 x8.
   a. Note: This configuration could be considered as a Y-Cable with a SAS-4 x8 on the controller and a pair of legacy x4s on a backplane connection.
5. SFF-9402 SAS Sidebands SAS-4 (SFF-8621/ SFF-8654) and SAS-2.1/ SAS 3 Legacy(SFF-8643/ SFF-8087)
   Table 8-7 was provided to show NON-REVERSIBLE SAS sideband physical pin assignments for cables that utilize SFF-8087 / SFF-8643 (Legacy) and SFF-8621/ SFF-8654 (SAS-4). The sideband signals are "highlighted" to indicate why these assemblies cannot be flipped between controller and backplane (This condition was due to changes in the SAS-4 specification that moved SB4 and SB5 to allow SB+/- to be placed on dedicated pins to better optimize the SFF-8621/ SFF-8654 interfaces for multiprotocol operations. This indirectly impacted physical pin assignments for SB1/ SB2 and SB3/ SB4 on the x4 and SB[A,B]1, SB[A,B]2, SB[A,B]3 and SB[A,B]4 on the x8 configurations).
   a. Note: SAS sideband management consists of SFF-8448 SGPIO, Standard 2-Wire Type, and Other 2-Wire Type/ SFF-TA-1001 UBM.

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Table 8-1 SAS(x4) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane (1 of 1)

	Controller			CABLE	Backplane			Device on Backplane
SFF-9400	SFF-8087	SFF-8643	9402 SAS Non-Symetrical Legacy (SFF-8087, SFF-8643) to SAS-4 (x4) Cable Interface		9402 SAS Non-Symetrical SAS-4 to Legacy (SFF-8087, SFF-8643) (x4) Cable Interface	SFF-8621 (42-circuit)	SFF-8654 (38-circuit)	SFF-8639 Connector
Type 1 4X	SAS-2.1	SAS-2.1, 3	SAS Only Cable SFF-8448		SAS Only Cable SFF-8448	SAS-4	SAS-4	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
RSV			RESERVED	NO WIRE	RESERVED	B1		
GND	A1	B3	GROUND	—	GROUND	B2	B1	
HS	A2	B4	RX0+	←	TX0+	B3	B2	S6 (TX0+)
HS	A3	B5	RX0-	←	TX0-	B4	B3	S5 (TX0-)
GND	A4	A3	GROUND	—	GROUND	B5	B4	
HS	A5	A4	RX1+	←	TX1+	B6	B5	S13 (TX1+)
HS	A6	A5	RX1-	←	TX1-	B7	B6	S12 (TX1-)
GND	A7	A6	GROUND	—	GROUND	B8	B7	
SB	A8	A1	BP_TYPE(SB7)	←	BP_TYPE (SB7)	B9	B8	
SB	A10	C1	RESET, SDataOut (SB4)	→	RESET, SDataOut (SB4)	B10	B9	
SB	A9	B1	GND(SB3)	—	GND (SB3)	B11	B10	
SB			(SB+)	→	(SB+)	B12	B11	
SB			(SB-)	→	(SB-)	B13	B12	
GND	A12	B6	GROUND	—	GROUND	B14	B13	
HS	A13	B7	RX2+	←	TX2+	B15	B14	S21 (TX2+)
HS	A14	B8	RX2-	←	TX2-	B16	B15	S20 (TX2-)
GND	A15	B9	GROUND	—	GROUND	B17	B16	
HS	A16	A7	RX3+	←	TX3+	B18	B17	S27 (TX3+)
HS	A17	A8	RX3-	←	TX3-	B19	B18	S26 (TX3-)
GND	A18	A9	GROUND	—	GROUND	B20	B19	
RSV			RESERVED	NO WIRE	RESERVED	B21		
RSV			RESERVED	NO WIRE	RESERVED	A1		
GND	B1	D3	GROUND	—	GROUND	A2	A1	
HS	B2	D4	TX0+	→	RX0+	A3	A2	S2 (RX0+)
HS	B3	D5	TX0-	→	RX0-	A4	A3	S3 (RX0-)
GND	B4	C3	GROUND	—	GROUND	A5	A4	
HS	B5	C4	TX1+	→	RX1+	A6	A5	S9 (RX1+)
HS	B6	C5	TX1-	→	RX1-	A7	A6	S10 (RX1-)
GND	B7	C6	GROUND	—	GROUND	A8	A7	
SB	B8	A2	2W-CLK, Sclock (SB0)	↔	2W-CLK, SClock (SB0)	A9	A8	
SB	B9	B2	2W-DATA, Sload (SB1)	↔	2W-DATA, Sload (SB1)	A10	A9	
SB	B10	C2	GND (SB2)	—	(SB2)GND (SB2)	A11	A10	
SB	A11	D1	ADD, SDatain (SB5)	↔	ADD, SDatain (SB5)	A12	A11	
SB	B11	D2	CNTRLR_TYPE (SB6)	→	CNTRLR_TYPE (SB6)	A13	A12	
GND	B12	D6	GROUND	—	GROUND	A14	A13	
HS	B13	D7	TX2+	→	RX2+	A15	A14	S17 (RX2+)
HS	B14	D8	TX2-	→	RX2-	A16	A15	S18 (RX2-)
GND	B15	D9	GROUND	—	GROUND	A17	A16	
HS	B16	C7	TX3+	→	RX3+	A18	A17	S23 (RX3+)
HS	B17	C8	TX3-	→	RX3-	A19	A18	S24 (RX3-)
GND	B18	C9	GROUND	—	GROUND	A20	A19	
RSV			RESERVED	NO WIRE	RESERVED	A21		

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Table 8-2 SAS (x4) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane (1 of 1)

					Backplane			Device on Backplane
SFF-9400	SFF-8654 (38-circuit)	SFF-8621 (42-circuit)	9402 SAS Non-Symetrical SAS-4 to Legacy (SFF-8087, SFF-8643) (x4) Cable Interface	CABLE	9402 SAS Non-Symetrical Legacy (SFF-8087, SFF-8643) to SAS-4 (x4) Cable Interface	SFF-8643	SFF-8087	SFF-8639 Connector
Type 1 4X	SAS-4	SAS-4	SAS Only Cable SFF-8448		SAS Only Cable SFF-8448	SAS-2.1, 3	SAS-2.1	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
RSV		A1	RESERVED	NO WIRE	RESERVED			
GND	A1	A2	GROUND	—	GROUND	D3	B1	
HS	A2	A3	RX0+	←	TX0+	D4	B2	S6 (TX0+)
HS	A3	A4	RX0-	←	TX0-	D5	B3	S5 (TX0-)
GND	A4	A5	GROUND	—	GROUND	C3	B4	
HS	A5	A6	RX1+	←	TX1+	C4	B5	S13 (TX1+)
HS	A6	A7	RX1-	←	TX1-	C5	B6	S12 (TX1-)
GND	A7	A8	GROUND	—	GROUND	C6	B7	
SB	A8	A9	BP_TYPE (SB7)	←	BP_TYPE (SB7)	A2	B8	
SB	A9	A10	RESET, SDataOut (SB4)	↔	RESET, SDataOut (SB4)	C2	B10	
SB	A10	A11	GND (SB3)	—	GND (SB3)	B2	B9	
SB	A11	A12	(SB+)	→	(SB+)			
SB	A12	A13	(SB-)	→	(SB-)			
GND	A13	A14	GROUND	—	GROUND	D6	B12	
HS	A14	A15	RX2+	←	TX2+	D7	B13	S21 (TX2+)
HS	A15	A16	RX2-	←	TX2-	D8	B14	S20 (TX2-)
GND	A16	A17	GROUND	—	GROUND	D9	B15	
HS	A17	A18	RX3+	←	TX3+	C7	B16	S27 (TX3+)
HS	A18	A19	RX3-	←	TX3-	C8	B17	S26 (TX3-)
GND	A19	A20	GROUND	—	GROUND	C9	B18	
RSV		A21	RESERVED	NC	RESERVED			
RSV		B1	RESERVED	NC	RESERVED			
GND	B1	B2	GROUND	—	GROUND	B3	A1	
HS	B2	B3	TX0+	→	RX0+	B4	A2	S2 (RX0+)
HS	B3	B4	TX0-	→	RX0-	B5	A3	S3 (RX0-)
GND	B4	B5	GROUND	—	GROUND	A3	A4	
HS	B5	B6	TX1+	→	RX1+	A4	A5	S9 (RX1+)
HS	B6	B7	TX1-	→	RX1-	A5	A6	S10 (RX1-)
GND	B7	B8	GROUND	—	GROUND	A6	A7	
SB	B8	B9	2W-CLK, Sclock (SB0)	↔	2W-CLK, SClock (SB0)	A1	A8	
SB	B9	B10	2W-DATA, Sload (SB1)	↔	2W-DATA, Sload (SB1)	B1	A9	
SB	B10	B11	GND (SB2)	—	(SB2)GND (SB2)	C1	A10	
SB	B11	B12	ADD, SDatain (SB5)	↔	ADD, SDatain (SB5)	D2	B11	
SB	B12	B13	CNTRLR_TYPE (SB6)	→	CNTRLR_TYPE (SB6)	D1	A11	
GND	B13	B14	GROUND	—	GROUND	B6	A12	
HS	B14	B15	TX2+	→	RX2+	B7	A13	S17 (RX2+)
HS	B15	B16	TX2-	→	RX2-	B8	A14	S18 (RX2-)
GND	B16	B17	GROUND	—	GROUND	B9	A15	
HS	B17	B18	TX3+	→	RX3+	A7	A16	S23 (RX3+)
HS	B18	B19	TX3-	→	RX3-	A8	A17	S24 (RX3-)
GND	B19	B20	GROUND	—	GROUND	A9	A18	
RSV		B21	RESERVED	NO WIRE	RESERVED			

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Table 8-3 SAS (x8) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane (1 of 2)

	Controller			CABLE	Backplane			Devices on Backplane
SFF-9400	SFF-8087	SFF-8643	9402 SAS Non-Symetrical Legacy (SFF-8087, SFF-8643) (x4) Pair to SAS-4 (x8) Cable Interface		9402 SAS Non-Symetrical SAS-4 (x8) to Legacy (SFF-8087, SFF-8643) (x4) Pair Cable Interface	SFF-8621 (80-circuit)	SFF-8654(74-circuit)	SFF-8639 Connector (Pair of x4)
Type 1 8X	SAS-2.1 x4	SAS-2.1, 3 x4	Pair of (x4) SAS Legacy/ SFF-8448 Cables		8x SAS-4/ SFF-8448 Cable	SAS-4 x8	SAS-4 x8	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
GND	A1	B3	GROUND	–	GROUND	B1	B1	
HS	A2	B4	RX0+	←	TX0+	B2	B2	S6 (TX0+)
HS	A3	B5	RX0-	←	TX0-	B3	B3	S5 (TX0-)
GND	A4	A3	GROUND	–	GROUND	B4	B4	
HS	A5	A4	RX1+	←	TX1+	B5	B5	S13 (TX1+)
HS	A6	A5	RX1-	←	TX1-	B6	B6	S12 (TX1-)
GND	A7	A6	GROUND	–	GROUND	B7	B7	
SB	A8	A1	BP_TYPEA(SB7A)	←	BP_TYPEA (SB7A)	B8	B8	
SB	A10	C1	RESETA, SDataOutA(SB4A)	↔	RESETA, SDataOutA (SB4A)	B8	B9	
SB	A9	B1	GND(SB3A)	–	GND (SB3A)	B10	B10	
SB			SBA+)	→	(SBA+)	B11	B11	
SB			(SBA-)	→	(SBA-)	B12	B12	
GND	A12	B6	GROUND	–	GROUND	B13	B13	
HS	A13	B7	RX2+	←	TX2+	B14	B14	S21 (TX2+)
HS	A14	B8	RX2-	←	TX2-	B15	B15	S20 (TX2-)
GND	A15	B9	GROUND	–	GROUND	B16	B16	
HS	A16	A7	RX3+	←	TX3+	B17	B17	S27 (TX3+)
HS	A17	A8	RX3-	←	TX3-	B18	B18	S26 (TX3-)
GND	A18	A9	GROUND	–	GROUND	B19	B19	
RSV			RESERVED	NO WIRE	RESERVED	B20		
RSV			RESERVED	NO WIRE	RESERVED	B21		
GND	A1	B3	GROUND	–	GROUND	B22	B19	
HS	A2	B4	RX4+	←	TX4+	B23	B20	S6 (TX0+)
HS	A3	B5	RX4-	←	TX4-	B24	B21	S5 (TX0-)
GND	A4	A3	GROUND	–	GROUND	B25	B22	
HS	A5	A4	RX5+	←	TX5+	B26	B23	S13 (TX1+)
HS	A6	A5	RX5-	←	TX5-	B27	B24	S12 (TX1-)
GND	A7	A6	GROUND	–	GROUND	B28	B25	
SB	A8	A	BP_TYPEB(SB7B)	←	BP_TYPEB (SB7B)	B29	B26	
SB	A10	C1	RESETB, SDataOutB(SB4B)	→	RESETB, SDataOutB (SB4B)	B30	B27	
SB	A9	B1	GND(SB3B)	–	GND (SB3B)	B31	B28	
SB			(SBB+)	→	(SBB+)	B32	B29	
SB			(SBB-)	→	(SBB-)	B33	B30	
GND	A12	B6	GROUND	–	GROUND	B34	B31	
HS	A13	B7	RX6+	←	TX6+	B35	B32	S21 (TX2+)
HS	A14	B8	RX6-	←	TX6-	B36	B33	S20 (TX2-)
GND	A15	B9	GROUND	–	GROUND	B37	B34	
HS	A16	A7	RX7+	←	TX7+	B38	B35	S27 (TX3+)
HS	A17	A8	RX7-	←	TX7-	B39	B36	S26 (TX3-)
GND	A18	A9	GROUND	–	GROUND	B40	B37	

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Table 8-4 SAS (x8) SFF-8087/ SFF-8643 Controller to SFF-8621/ SFF-8654 Backplane (2 of 2)

	Controller			CABLE	Backplane			DEVICE
SFF-9400	SFF-8087	SFF-8643	9402 SAS Non-Symetrical Legacy (SFF-8087, SFF-8643) (x4) Pair to SAS-4 (x8) Cable Interface		9402 SAS Non-Symetrical SAS-4 (x8) to Legacy (SFF-8087, SFF-8643) (x4) Pair Cable Interface	SFF-8621 (80-circuit)	SFF-8654 (74-circuit)	SFF-8639 Connector (Pair of x4)
Type 1 8X	SAS-2.1 x4	SAS-2.1, 3 x4	Pair of (x4) SAS Legacy/ SFF-8448 Cables		8x SAS-4/ SFF-8448 Cables	SAS-4 x8	SAS-4 x8	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
GND	B1	D3	GROUND	–	GROUND	A1	A1	
HS	B2	D4	TX0+	→	RX0+	A2	A2	S2 (RX0+)
HS	B3	D5	TX0-	→	RX0-	A3	A3	S3 (RX0-)
GND	B4	C3	GROUND	–	GROUND	A4	A4	
HS	B5	C4	TX1+	→	RX1+	A5	A5	S9 (RX1+)
HS	B6	C5	TX1-	→	RX1-	A6	A6	S10 (RX1-)
GND	B7	C6	GROUND	–	GROUND	A7	A7	
SB	B8	A2	2W-CLKA, SClockA (SB0A)	↔	2W-CLKA, SClockA (SB0A)	A8	A8	
SB	B9	B2	2W-DATAA, SLoadA (SB1A)	↔	2W-DATAA, SLoadA (SB1A)	A9	A9	
SB	B10	C2	GND (SB2A)	–	GND (SB2A)	A10	A10	
SB	A11	D1	ADDA, SDataInA (SB5A)	↔	ADDA, SDataInA (SB5A)	A11	A11	
SB	B11	D2	CNTRLR_TYPEA (SB6A)	→	CNTRLR_TYPEA (SB6)	A12	A12	
GND	B12	D6	GROUND	–	GROUND	A13	A13	
HS	B13	D7	TX2+	→	RX2+	A14	A14	S17 (RX2+)
HS	B14	D8	TX2-	→	RX2-	A15	A15	S18 (RX2-)
GND	B15	D9	GROUND	–	GROUND	A16	A16	
HS	B16	C7	TX3+	→	RX3+	A17	A17	S23 (RX3+)
HS	B17	C8	TX3-	→	RX3-	A18	A18	S24 (RX3-)
GND	B18	C9	GROUND	–	GROUND	A19	A19	
RSV			RESERVED	NO WIRE	RESERVED	A20		
RSV			RESERVED	NO WIRE	RESERVED	A21		
GND	B1	D3	GROUND	–	GROUND	A22	A19	
HS	B2	D4	TX4+	→	RX4+	A23	A20	S2 (RX0+)
HS	B3	D5	TX4-	→	RX4-	A24	A21	S3 (RX0-)
GND	B4	C3	GROUND	–	GROUND	A25	A22	
HS	B5	C4	TX5+	→	RX5+	A26	A23	S9 (RX1+)
HS	B6	C5	TX5-	→	RX5-	A27	A24	S10 (RX1-)
GND	B7	C6	GROUND	–	GROUND	A28	A25	
SB	B8	A2	2W-CLKB, SClockB (SB0B)	↔	2W-CLKB, SClockB (SB0B)	A29	A26	
SB	B9	B2	2W-DATAB, SLoadB (SB1B)	↔	2W-DATAB, SLoadB (SB1B)	A30	A27	
SB	B10	C2	GND (SB2B)	–	GND (SB2B)	A31	A28	
SB	A11	D1	ADDB, SDataInB (SB5B)	↔	ADDB, SDataIn (SB5B)	A32	A29	
SB	B11	D2	CNTRLR_TYPEB (SB6B)	→	CNTRLR_TYPEB (SB6B)	A33	A30	
GND	B12	D6	GROUND	–	GROUND	A34	A31	
HS	B13	D7	TX6+	→	RX6+	A35	A32	S17 (RX2+)
HS	B14	D8	TX6-	→	RX6-	A36	A33	S18 (RX2-)
GND	B15	D9	GROUND	–	GROUND	A37	A34	
HS	B16	C7	TX7+	→	RX7+	A38	A35	S23 (RX3+)
HS	B17	C8	TX7-	→	RX7-	A39	A36	S24 (RX3-)
GND	B18	C9	GROUND	–	GROUND	A40	A37	

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Table 8-5 SAS (x8) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane (1 of 2)

	Controller			CABLE	Backplane			Devices on Backplane
SFF-9400	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 SAS Non-Symetrical SAS-4 (x8) to Legacy (SFF-8087, SFF-8643) (x4) Pair Cable Interface		9402 SAS Non-Symetrical Legacy (SFF-8087, SFF-8643) (x4) Pair to SAS-4 (x8) Cable Interface	SFF-8643	SFF-8087	SFF-8639 Connector (Pair of x4)
Type 1 8X	SAS-4 x8	SAS-4 x8	8X SAS Cables SFF-8448		8X SAS Cables SFF-8448	SAS-2.1, 3 x4	SAS-2.1 x4	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
GND	A1	A1	GROUND	–	GROUND	D3	B1	
HS	A2	A2	RX0+	←	TX0+	D4	B2	S6 (TX0+)
HS	A3	A3	RX0-	←	TX0-	D5	B3	S5 (TX0-)
GND	A4	A4	GROUND	–	GROUND	C3	B4	
HS	A5	A5	RX1+	←	TX1+	C4	B5	S13 (TX1+)
HS	A6	A6	RX1-	←	TX1-	C5	B6	S12 (TX1-)
GND	A7	A7	GROUND	–	GROUND	C6	B7	
SB	A8	A8	BP_TYPEA(SB7A)	←	BP_TYPEA (SB7A)	A2	B8	
SB	A9	A9	RESETA, SDataOutA(SB4A)	↔	RESETA, SDataOutA (SB4A)	C2	B10	
SB	A10	A10	GND(SB3A)	–	GND (SB3A)	B2	B9	
SB	A11	A11	(SBA+)	→	(SBA+)			
SB	A12	A12	(SBA-)	→	(SBA-)			
GND	A13	A13	GROUND	–	GROUND	D6	B12	
HS	A14	A14	RX2+	←	TX2+	D7	B13	S21 (TX2+)
HS	A15	A15	RX2-	←	TX2-	D8	B14	S20 (TX2-)
GND	A16	A16	GROUND	–	GROUND	D9	B15	
HS	A17	A17	RX3+	←	TX3+	C7	B16	S27 (TX3+)
HS	A18	A18	RX3-	←	TX3-	C8	B17	S26 (TX3-)
GND	A19	A19	GROUND	–	GROUND	C9	B18	
RSV		A20	RESERVED	NO WIRE	RESERVED			
RSV		A21	RESERVED	NO WIRE	RESERVED			
GND	A19	A22	GROUND	–	GROUND	D3	B1	
HS	A20	A23	RX4+	←	TX4+	D4	B2	S6 (TX0+)
HS	A21	A24	RX4-	←	TX4-	D5	B3	S5 (TX0-)
GND	A22	A25	GROUND	–	GROUND	C3	B4	
HS	A23	A26	RX5+	←	TX5+	C4	B5	S13 (TX1+)
HS	A24	A27	RX5-	←	TX5-	C5	B6	S12 (TX1-)
GND	A25	A28	GROUND	–	GROUND	C6	B7	
SB	A26	A29	BP_TYPEB(SB7B)	←	BP_TYPEB (SB7B)	A2	B8	
SB	A27	A30	RESETB, SDataOutB(SB4B)	↔	RESETB, SDataOutB (SB4B)	C2	B10	
SB	A28	A31	GND(SB3B)	–	GND (SB3B)	B2	B9	
SB	A29	A32	(SBB+)	→	(SBB+)			
SB	A30	A33	(SBB-)	→	(SBB-)			
GND	A31	A34	GROUND	–	GROUND	D6	B12	
HS	A32	A35	RX6+	←	TX6+	D7	B13	S21 (TX2+)
HS	A33	A36	RX6-	←	TX6-	D8	B14	S20 (TX2-)
GND	A34	A37	GROUND	–	GROUND	D9	B15	
HS	A35	A38	RX7+	←	TX7+	C7	B16	S27 (TX3+)
HS	A36	A39	RX7-	←	TX7-	C8	B17	S26 (TX3-)
GND	A37	A40	GROUND	–	GROUND	C9	B18	

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Table 8-6 SAS (x8) SFF-8621/ SFF-8654 Controller to SFF-8087/ SFF-8643 Backplane (2 of 2)

	Controller			CABLE	Backplane			Devices on Backplane
SFF-9400	SFF-8654 (74-circuit)	SFF-8621 (80-circuit)	9402 SAS Non-Symetrical SAS-4 (x8) to Legacy (SFF-8087, SFF-8643) (x4) Pair Cable Interface		9402 SAS Non-Symetrical Legacy (SFF-8087, SFF-8643) (x4) Pair to SAS-4 (x8) Cable Interface	SFF-8643	SFF-8087	SFF-8639 Connector (Pair of x4)
Type 1 8X	SAS-4 x8	SAS-4 x8	8X SAS Cables SFF-8448		8X SAS Cables SFF-8448	SAS-2.1, 3 x4	SAS-2.1 x4	MultiLink SAS™
	PIN	PIN	Controller	DIR	Backplane	PIN	PIN	PIN
GND	B1	B1	GROUND	–	GROUND	B3	A1	
HS	B2	B2	TX0+	→	RX0+	B4	A2	S2 (RX0+)
HS	B3	B3	TX0-	→	RX0-	B5	A3	S3 (RX0-)
GND	B4	B4	GROUND	–	GROUND	A3	A4	
HS	B5	B5	TX1+	→	RX1+	A4	A5	S9 (RX1+)
HS	B6	B6	TX1-	→	RX1-	A5	A6	S10 (RX1-)
GND	B7	B7	GROUND	–	GROUND	A6	A7	
SB	B8	B8	2W-CLKA, SClockA (SB0A)	↔	2W-CLKA, SClockA (SB0A)	A1	A8	
SB	B9	B9	2W-DATAA, SLoadA (SB1A)	↔	2W-DATAA, SloadA (SB1A)	B1	A9	
SB	B10	B10	GND (SB2A)	–	GND (SB2A)	C1	A10	
SB	B11	B11	ADDA, SDataInA (SB5A)	↔	ADDA, SDataInA (SB5A)	D2	B11	
SB	B12	B12	CNTRLR_TYPEA (SB6A)	→	CNTRLR_TYPEA (SB6)	D1	A11	
GND	B13	B13	GROUND	–	GROUND	B6	A12	
HS	B14	B14	TX2+	→	RX2+	B7	A13	S17 (RX2+)
HS	B15	B15	TX2-	→	RX2-	B8	A14	S18 (RX2-)
GND	B16	B16	GROUND	–	GROUND	B9	A15	
HS	B17	B17	TX3+	→	RX3+	A7	A16	S23 (RX3+)
HS	B18	B18	TX3-	→	RX3-	A8	A17	S24 (RX3-)
GND	B19	B19	GROUND	–	GROUND	A9	A18	
RSV		B20	RESERVED	NO WIRE	RESERVED			
RSV		B21	RESERVED	NO WIRE	RESERVED			
GND	B19	B22	GROUND	–	GROUND	B3	A1	
HS	B20	B23	TX4+	→	RX4+	B4	A2	S2 (RX0+)
HS	B21	B24	TX4-	→	RX4-	B5	A3	S3 (RX0-)
GND	B22	B25	GROUND	–	GROUND	A3	A4	
HS	B23	B26	TX5+	→	RX5+	A4	A5	S9 (RX1+)
HS	B24	B27	TX5-	→	RX5-	A5	A6	S10 (RX1-)
GND	B25	B28	GROUND	–	GROUND	A6	A7	
SB	B26	B29	2W-CLKB, SClockB (SB0B)	↔	2W-CLKB, SClockB (SB0B)	A1	A8	
SB	B27	B30	2W-DATAB, SLoadB (SB1B)	↔	2W-DATAB, SLoadB (SB1B)	B1	A9	
SB	B28	B31	GND (SB2B)	–	GND (SB2B)	C1	A10	
SB	B29	B32	ADDB, SDataInB (SB5B)	↔	ADDB, SDataIn (SB5B)	D2	B11	
SB	B30	B33	CNTRLR_TYPEB (SB6B)	→	CNTRLR_TYPEB (SB6B)	D1	A11	
GND	B31	B34	GROUND	–	GROUND	B6	A12	
HS	B32	B35	TX6+	→	RX6+	B7	A13	S17 (RX2+)
HS	B33	B36	TX6-	→	RX6-	B8	A14	S18 (RX2-)
GND	B34	B37	GROUND	–	GROUND	B9	A15	
HS	B35	B38	TX7+	→	RX7+	A7	A16	S23 (RX3+)
HS	B36	B39	TX7-	→	RX7-	A8	A17	S24 (RX3-)
GND	B37	B40	GROUND	–	GROUND	A9	A18	

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Table 8-7 SAS-4 and SAS-2.1/ SAS-3 Sidebands Only (1 of 1)

	Sideband Signal Assignments				Controller				CABLE	Backplane			
	SFF-9402 Signal/ Pin Assignments for Contoller SAS-4/ Legacy to BackplaneSAS-4/ Legacy Interface Only				SFF-8087 (36-circuit)	SFF-8643 (36-circuit)	SFF-8654 (38-circuit)	SFF-8621 (42-circuit)		SFF-8621 (42-circuit)	SFF-8654 (38-circuit)	SFF-8643 (36-circuit)	SFF-8087 (36-circuit)
SIDE BANDS	SGPIO (SFF-8485) SFF-8448	Standard 2-Wire Type SFF-8448	Other 2-Wire Type SFF-8448	UBM SFF-TA-1005	SAS-2.1	SAS-2.1, 3	SAS-4	SAS-4		SAS-4	SAS-4	SAS-2.1, 3	SAS-2.1
NAME	*Signal Name*	*Signal Name*	*Signal Name*	*Signal Name*	PIN	PIN	PIN	PIN	DIR	PIN	PIN	PIN	PIN
SB7	BP_TYPE	BP_TYPE	BP_TYPE/ VSP	BP_TYPE	A8	A1	A8	A9	←	B9	B8	A2	B8
SB4	SDataOut	RESET	VSP	2W_RST#	A10	C1	A9	A10	→	B10	B9	C2	B10
SB3	GND	GND	VSP	GND	A9	B1	A10	A11	—	B11	B10	B2	B9
SB+	(SB+)	(SB+)	VSP+	(SB+)	na	na	A11	A12	→	B12	B11	na	na
SB-	(SB-)	(SB-)	VSP-	(SB-)	na	na	A12	A13	→	B13	B12	na	na
SB0	SClock	2W-CLK	2W-CLK	2W-CLK	B8	A2	B8	B9	↔	A9	A8	A1	A8
SB1	SLoad	2W-DATA	2W-DATA	2W-DATA	B9	B2	B9	B10	↔	A10	A9	B1	A9
SB2	GND	GND	GND	GND	B10	C2	B10	B11	—	A11	A10	C1	A10
SB5	SDataIn	ADD	VSP	PERST# (na)	A11	D1	B11	B12	↔	A12	A11	D2	B11
SB6	CNTRLR_TYPE	CNTRLR_TYPE	VSP	CHG_DETECT#/ CPRSNT#	B11	D2	B12	B13	↔	A13	A12	D1	A11

Example: In Table 8-7 above, SFF-8643 Controller B2 connects to SFF-8621 Backplane A10 (RED) while SFF-8643 Backplane B2 connectors to SFF-8621 Controller A11 (GREEN). As the table shows, both directions do not match; therefore, the cables are not reversible. This holds true for any sideband connections between SFF-8087/ SFF-8643 and SFF-8621/ SFF-8654.

Table 8-7 above also defines the four (4) possible sideband connection types SFF-8448 SGPIO, Standard/ Other 2-Wire Type, and SFF-TA-1005 UBM. UBM supports SAS and PCIe management. It also fits within the Other 2-Wire Type defined in SFF-8448. Note: All the highspeed connections shown in Table 8-1 through Table 8-6 are common and independent of the sideband interface implemented.

REFERENCE

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9. SFF-8654 / CopprLink / M-XIO / SAS-5 SFF-TA-1016 Reversible Cables

The following eighteen (18) tables extend the tables provided in previous sections to newer standards from PCI Express ® and OCP using the SFF-8654 connector as a base reference. Cable signal direction and target/endpoint device connections continue to be shown.

In this section:

1. All cables are electrically and physically reversible.
2. Cables with different connectors on each end will work regardless of the mechanical location of the fixed side connectors.
3. Reference column SFF-9400 has been removed for space considerations and given it is now a de-facto standard application.
4. Other Protocol signal names continue to be listed for the x4 and x8 tables.
5. For convenience, the EDSFF pinout specified in SFF-TA-1009 has been added.
6. The 124 circuit version of the CopprLink x16 connector is included in the x16 Cables tables. Note that the 124-circuit version does not include a secondary set of sidebands.
7. CopprLink and M-XIO define a baseline group of 10 sidebands for the x4, add an extended set of 10 sidebands for x8, and duplicate a second sideband and extended set for the x16. The enumeration of designators B are assigned to the additional ~~8 lanes~~set.
8. SAS SFF-TA-1016 enumerates its 4 times replicated 10 sidebands as A for the first x4, B for the additional sidebands in x8, and continues with sidebands C and D for the additional sidebands in X16 148 pin.
9. A logical extension of the existing SFF-9402 grouping of sidebands, originally derived from OCuLink's Other Protocol designation, would extend the X8 method of duplicating the original X4 designations for a port B to a X16 designation of continuing the X4 sideband designations to a port C and D. Note this usage may conflict with CopprLink and M-XIO's usage as Extended Sidebands and Group B sidebands.
10. Given the conflict in naming that occurs when CopprLink and M-XIO's quad B sidebands align in pin assignment with SAS and classic SFF-9402's quad C sidebands, x16 tables will now change from OCuLinks' Other Protocol sideband assignments to SFF-9402 Quad naming, with sidebands now enumerated as Q0, Q1, Q2, & Q3; replacing the A, B, C, & D designations.

The highspeed differential and sideband signals are color coded (SAS=Blue and PCIe / M-XIO=Green/ Italic) to indicate their associated naming convention and protocol. All other coding in the tables match the format started in Section 6.

Sideband Signal Assignments

Table 9-18 defines the sideband assignments only. Although Table 9-1 through Table 9-17 define CopprLink/M-XIO and SFF-8448 SGPIO, this table includes the SFF-8448 Standards 2-Wire Type and SFF-TA-1005 (UBM). (Note: UBM can be considered the Other 2-Wire Type that can support both SAS and PCIe protocols.) This table also extends the pin assignments to a full x16 map. In order to keep the tables readable, the other tables in this section will adopt the new SFF-9402 naming convention for sideband signals.

Note:- Implementers may make specific design adjustments to accommodate any dual usage requirements for some conflicting sideband usages (such as the additional RefClks that are used in the Extended Sideband section will conflict with USB 2.0 signal assignments). Detection of signal usage can be done either over the 2-Wire interface or over the PESTI interface described in M-XIO. Both interfaces share common signal assignments across all sideband definitions.

REFERENCE

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Table 9-1 Multiprotocol SAS~~-4~~/ CopprLink/ M-XIO (x4) Cables (1 of 1)

Multiprotocol SAS/ CopprLink / M-XIO x4 Cables (Sheet 1 of 1)											
Root / Controller				CABLE	*Endpoint* / Backplane				*Devices on Backplane*			
SFF-8654, CopprLink/M-XIO SFF-TA-1016 (38-circuit)	9402 Multi-Protocol (PCIe, SAS-4) x4 Cable Interface				9402 Multi-Protocol (PCIe, SAS) x4 Cable Interface			SFF-8654, CopprLink/M-XIO SFF-TA-1016 (38-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P, PCIe/ SAS	*O/P (OCuLink Assigned)*	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			*O/P (OCuLink Assigned)*	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		*O/P, PCIe/ SAS-4*	SFF-TA-1009 (x4)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	*ROOT*	ROOT	Controller	DIR	*Endpoint*	NON-ROOT	Backplane	PIN	PIN	PIN	PIN	PIN
A1	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**B1**				
A2	*PERp0*	PERp0	RX0+	←	*PETp0*	PETp0	TX0+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A3	*PERn0*	PERn0	RX0-	←	*PETn0*	PETn0	TX0-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A4	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**B4**				
A5	*PERp1*	PERp1	RX1+	←	*PETp1*	PETp1	TX1+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A6	*PERn1*	PERn1	RX1-	←	*PETn1*	PETn1	TX1-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A7	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**B7**				
A8	*BP_TYPE (VSP)*	FLEXIO9_A, (3p3AUX_MGMT)	BP_TYPE (SB7)	↔	*BP_TYPE(VSP)*	FLEXIO9_A, (3p3AUX_MGMT)	BP_TYPE (SB7)	B8				
A9	*CWAKE#,OBFF (VSP)*	FLEXIO0_A	RESET, SDataOut (SB4)	↔	*CWAKE#,OBFF/(VSP)*	FLEXIO0_A	RESET, SDataOut (SB4)	B9		P1 (WAKE#)	P1 (WAKE#)	
A10	*GND*	GND	GND (SB3)	–	*GND*	GND	GND (SB3)	B10				
A11	*REFCLK+(VSP+)*	RCLK_Ap,REFCLK_A_Dp	(SB+)	→	*REFCLK+(VSP+)*	RCLK_Ap,REFCLK_A_Dp	(SB+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A12	*REFCLK-(VSP-)*	RCLK_An,REFCLK_A_Dn	(SB-)	→	*REFCLK-(VSP-)*	RCLK_An,REFCLK_A_Dn	(SB-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A13	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**B13**				
A14	*PERp2*	PERp2	RX2+	←	*PETp2*	PETp2	TX2+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A15	*PERn2*	PERn2	RX2-	←	*PETn2*	PETn2	TX2-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A16	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**B16**				
A17	*PERp3*	PERp3	RX3+	←	*PETp3*	PETp3	TX3+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A18	*PERn3*	PERn3	RX3-	←	*PETn3*	PETn3	TX3-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A19	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**B19**				
B1	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**A1**				
B2	*PETp0*	PETp0	TX0+	→	*PERp0*	PERp0	RX0+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B3	*PETn0*	PETn0	TX0-	→	*PERn0*	PERn0	RX0-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B4	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**A4**				
B5	*PETp1*	PETp1	TX1+	→	*PERp1*	PERp1	RX1+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B6	*PETn1*	PETn1	TX1-	→	*PERn1*	PERn1	RX1-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B7	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**A7**				
B8	*2W-CLK*	2WCL_A,SMSCL_A	2W-CLK, Sclock (SB0)	↔	*2W-CLK*	2WCL_A,SMSCL_A	2W-CLK, SClock (SB0)	A8				
B9	*2W-DATA*	2WDA_A,SMSDA_A	2W-DATA, Sload (SB1)	↔	*2W-DATA*	2WDA_A,SMSDA_A	2W-DATA, SLoad(SB1)	A9				
B10	*GND*	GND	GND (SB2)	–	*GND*	GND	GND(SB2)	A10				
B11	*PERST# (VSP)*	PERST#_A,PERST_A_N	ADD, SDataIn (SB5)	↔	*PERST# (VSP)*	PERST#_A,PERST_A_N	ADD, SDataIn (SB5)	A11	B10 (PERSTO#)	E5 (PERST#)	E5 (PERST#)	
B12	*CPRSNT# (VSP)*	PRPE_A,CBL_PRES_A_PESTI_A_N	CNTRLR_TYPE (SB6)	↔	*CPRSNT#(VSP)*	PRPE_A,CBL_PRES_A_PESTI_A_N	CNTRLR_TYPE (SB6)	A12				
B13	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**A13**				
B14	*PETp2*	PETp2	TX2+	→	*PERp2*	PERp2	RX2+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B15	*PETn2*	PETn2	TX2-	→	*PERn2*	PERn2	RX2-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B16	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**A16**				
B17	*PETp3*	PETp3	TX3+	→	*PERp3*	PERp3	RX3+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B18	*PETn3*	PETn3	TX3-	→	*PERn3*	PERn3	RX3-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B19	**GROUND**	**GND**	**GROUND**	–	**GROUND**	**GND**	**GROUND**	**A19**				

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Table 9-2 Multiprotocol SAS-4/ CopprLink/ M-XIO (x8) Cables (1 of 2)

Multiprotocol SAS/ CopprLink / M-XIO x8 Cables (Sheet 1 of 2)

Root / Controller				CABLE	Endpoint / Backplane				Devices on Backplane			
SFF-8654, CopprLink/M-XIO SFF-TA-1016 (74-circuit)	9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface				9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface			SFF-8654, CopprLink/M-XIO SFF-TA-1016 (74-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P, PCIe/ SAS	O/P (OCuLink Assigned)	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			O/P (OCuLink Assigned)	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		O/P SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	ROOT	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
A1	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B1**				
A2	PERp0	PERp0	RX0+	←	PETp0	PETp0	TX0+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A3	PERn0	PERn0	RX0-	←	PETn0	PETn0	TX0-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A4	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B4**				
A5	PERp1	PERp1	RX1+	←	PETp1	PETp1	TX1+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A6	PERn1	PERn1	RX1-	←	PETn1	PETn1	TX1-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A7	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B7**				
A8	BP_TYPEA(VSPA)	FLEXIO9_A, (3p3AUX_MGMT)	BP_TYPE (SB7)	↔	BP_TYPEA(VSPA)	FLEXIO9_A, (3p3AUX_MGMT)	BP_TYPE (SB7)	B8				
A9	CWAKEA#,OBFFA (VSPA)	FLEXIO0_A	RESET, SDataOut (SB4)	↔	CWAKEA#,OBFFA)(VSPA)	FLEXIO0_A	RESET, SDataOut (SB4)	B9		P1 (WAKE#)	P1 (WAKE#)	
A10	GND	GND	GND (SB3)	–	GND	GND	GND (SB3)	B10				
A11	REFCLKA+(VSPA+)	RCLK_Ap,REFCLK_A_Dp	(SB+)	→	REFCLKA+(VSPA+)	RCLK_Ap,REFCLK_A_Dp	(SB+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A12	REFCLKA-(VSPA-)	RCLK_An,REFCLK_A_Dn	(SB-)	→	REFCLKA-(VSPA-)	RCLK_An,REFCLK_A_Dn	(SB-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A13	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B13**				
A14	PERp2	PERp2	RX2+	←	PETp2	PETp2	TX2+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A15	PERn2	PERn2	RX2-	←	PETn2	PETn2	TX2-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A16	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B16**				
A17	PERp3	PERp3	RX3+	←	PETp3	PETp3	TX3+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A18	PERn3	PERn3	RX3-	←	PETn3	PETn3	TX3-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A19	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B19**				
A20	PERp4	PERp4	RX4+	←	PETp4	PETp4	TX4+	B20	A31 (PERp4)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A21	PERn4	PERn4	RX4-	←	PETn4	PETn4	TX4-	B21	A30 (PERn4)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A22	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B22**				
A23	PERp5	PERp5	RX5+	←	PETp5	PETp5	TX5+	B23	A34 (PERp5)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A24	PERn5	PERn5	RX5-	←	PETn5	PETn5	X5-	B24	A33 (PERn5)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A25	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B25**				
A26	BP_TYPEB (VSPB)	FLEXIO5_A (PCIe x1 RXp)	BP_TYPEB (SB7B)	↔	BP_TYPEB (VSPB)	FLEXIO5_A (PCIe x1 TXp)	BP_TYPEB(SB7B)	B26				
A27	CWAKEB#,OBFFB (VSPB)	FLEXIO6_A (PCIe x1 RXn)	RESETB, SDataOutB (SB4B)	↔	CWAKEB#,OBFFB (VSPB)	FLEXIO6_A (PCIe x1 TXn)	RESETB, SDataOutB (SB4B)	B27		P1 (WAKE#)	P1 (WAKE#)	
A28	GND	GND	GND(SB3B)	–	GND	GND	GND(SB3B)	B28				
A29	REFCLKB+ (VSPB+)	FLEXIO7_A (USB2p), USB2_Dp	(SBB+)	→	REFCLKB+(VSPB+)	FLEXIO7_A (USB2p), USB2_Dp	(SBB+)	B29		E7 (REFCLK+)	E7 (REFCLK+)	
A30	REFCLKB- (VSPB-)	FLEXIO8_A (USB2n), USB2_Dn	(SBB-)	→	REFCLKB- (VSPB-)	FLEXIO8_A (USB2n), USB2_Dn	(SBB-)	B30		E8 (REFCLK-)	E8 (REFCLK-)	
A31	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B31**				
A32	PERp6	PERp6	RX6+	←	PETp6	PETp6	TX6+	B32	A37 (PERp6)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A33	PERn6	PERn6	RX6-	←	PETn6	PETn6	TX6-	B33	A36 (PERn6)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A34	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B34**				
A35	PERp7	PERp7	RX7+	←	PETp7	PETp7	TX7+	B35	A40 (PERp7)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A36	PERn7	PERn7	RX7-	←	PETn	PETn	TX7-	B36	A39 (PERn7)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A37	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B37**				

REFERENCE

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Table 9-3 Multiprotocol SAS-4/ CopprLink/ M-XIO (x8) Cables (2 of 2)

Multiprotocol SAS/ CopprLink / M-XIO x8 Cables (Sheet 2 of 2)

SFF-8654, CopprLink/M-XIO SFF-TA-1016 (74-circuit)	9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface			CABLE	Endpoint / Backplane			SFF-8654 (74-circuit)	Devices on Backplane			
					9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface				EDSFF Connector	SFF-8639 Connector		
O/P SAS	O/P (OCuLink Assigned)	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			O/P (OCuLink Assigned)	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		O/P SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	ROOT	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
B1	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**				
B2	PETp0	PETp0	TX0+	→	PERp0	PERp0	RX0+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B3	PETn0	PETn0	TX0-	→	PERn0	PERn0	RX0-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B4	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**				
B5	PETp1	PETp1	TX1+	→	PERp1	PERp1	RX1+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B6	PETn1	PETn1	TX1-	→	PERn1	PERn1	RX1-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B7	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**				
B8	2W-CLK	2WCL_A,SMSCL	2W-CLK, Sclock (SB0)	↔	2W-CLKA	2WCL_A,SMSCL	2W-CLK, SClock (SB0)	A8				
B9	2W-DATA	2WDA_A,SMSDA	2W-DATA, Sload (SB1)	↔	2W-DATAA	2WDA_A,SMSDA	2W-DATA, SLoad(SB1)	A9				
B10	GND	GND	GND (SB2)	—	GND	GND	GND(SB2)	A10				
B11	PERST# (VSP)	PERST#_A,PERST_N	ADD, SDataIn (SB5)	↔	PERSTA# (VSPA)	PERST#_A,PERST_N	ADD, SDataIn (SB5)	A11	B10 (PERST0#)	E5 (PERST#)	E5 (PERST#)	
B12	CPRSNT# (VSP)	PRPE_A,CBL_PRES_A_PESTI_N	CNTRLR_TYPE (SB6)	↔	CPRSNTA# (VSPA)	PRPE_A,CBL_PRES_A_PESTI_N	CNTRLR_TYPE (SB6)	A12				
B13	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**				
B14	PETp2	PETp2	TX2+	→	PERp2	PERp2	RX2+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B15	PETn2	PETn2	TX2-	→	PERn2	PERn2	RX2-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B16	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**				
B17	PETp3	PETp3	TX3+	→	PERp3	PERp3	RX3+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B18	PETn3	PETn3	TX3-	→	PERn3	PERn3	RX3-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B19	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**				
B20	PETp4	PETp4	TX4+	→	PERp4	PERp4	RX4+	A20	B31 (PETp4)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B21	PETn4	PETn4	TX4-	→	PERn4	PERn4	RX4-	A21	B30 (PETn4)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B22	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A22**				
B23	PETp5	PETp5	TX5+	→	PERp5	PERp5	RX5+	A23	B34 (PETp5)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B24	PETn5	PETn5	TX5-	→	PERn5	PERn5	RX5-	A24	B33 (PETn5)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B25	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A25**				
B26	2W-CLKB (VSPB)	FLEXIO3_A(PCIe x1 TXp)	2W-CLKB, SClockB (SB0B)	↔	2W-CLKB (VSPB)	FLEXIO3_A(PCIe x1 RXp)	2W-CLKB, SClockB (SB0B)	A26				
B27	2W-DATAB (VSPB)	FLEXIO4_A(PCIe x1 TXn)	2W-DATAB, SLoadB (SB1B)	↔	2W-DATAB (VSPB)	FLEXIO4_A(PCIe x1 RXn)	2W-DATAB, SLoadB (SB1B)	A27				
B28	GND	GND	GND (SB2B)	—	GND	GND	GND (SB2B)	A28				
B29	PERSTB# (VSPB)	FLEXIO1_A	ADDB, SDataInB (SB5B)	↔	PERSTB# (VSPB)	FLEXIO1_A	ADDB, SDataIn (SB5B)	A29		E5 (PERST#)	E5 (PERST#)	
B30	CPRSNTB# (VSPB)	FLEXIO2_A	CNTRLR_TYPEB (SB6B)	↔	CPRSNTB# (VSPB)	FLEXIO2_A	CNTRLR_TYPEB (SB6B)	A30				
B31	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A31**				
B32	PETp6	PETp6	TX6+	→	PERp6	PERp6	RX6+	A32	B37 (PETp6)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B33	PETn6	PETn6	TX6-	→	PERn6	PERn6	RX6-	A33	B36 (PETn6)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B34	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A34**				
B35	PETp7	PETp7	TX7+	→	PERp	PERp	RX7+	A35	B40 (PETp7)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B36	PETn7	PETn7	TX7-	→	PERn7	PERn7	RX7-	A36	B39 (PETn7)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B37	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A37**				

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Table 9-4 Multiprotocol SAS-4/ CopprLink (x8) to SAS-4/ CopprLink (x4) Y-Cables (1 of 2)

Multiprotocol SAS/ CopprLink x8) to SAS / CopprLink (x4) Y-Cables (Sheet 1 of 2)

Root / Controller				CABLE	Endpoint / Backplane				Devices on Backplane			
SFF-8654, CopprLink SFF-TA-1016 (74-circuit)	9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface				9402 Multi-Protocol (PCIe, SAS) Pair of x4 Cable Interfaces			SFF-8654, CopprLink SFF-TA-1016 (38-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P, PCIe/ SAS	O/P (OCuLink Assigned)	CopprLink and SAS/ SFF-8448 Signal Names			O/P (OCuLink Assigned)	CopprLink and SAS/ SFF-8448 Signal Names		O/P SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	ROOT	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
A1	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B1**				
A2	PERp0	PERp0	RX0+	←	PETp0	PETp0	TX0+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A3	PERn0	PERn0	RX0-	←	PETn0	PETn0	TX0-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A4	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B4**				
A5	PERp1	PERp1	RX1+	←	PETp1	PETp1	TX1+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A6	PERn1	PERn1	RX1-	←	PETn1	PETn1	TX1-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A7	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B7**				
A8	BP_TYPEA(VSPA)	FLEXIO9_A	BP_TYPE (SB7)	↔	BP_TYPEA(VSPA)	FLEXIO9_A	BP_TYPE (SB7)	B8				
A9	CWAKEA#,OBFFA (VSPA)	FLEXIO0_A	RESET, SDataOut (SB4)	↔	CWAKEA#,OBFFA)(VSPA)	FLEXIO0_A	RESET, SDataOut (SB4)	B9		P1 (WAKE#)	P1 (WAKE#)	
A10	GND	GND	GND (SB3)	–	GND	GND	GND (SB3)	B10				
A11	REFCLKA+(VSPA+)	RCLK_Ap	(SB+)	→	REFCLKA+(VSPA+)	RCLK_Ap	(SB+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A12	REFCLKA-(VSPA-)	RCLK_An	(SB-)	→	REFCLKA-(VSPA-)	RCLK_An	(SB-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A13	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B13**				
A14	PERp2	PERp2	RX2+	←	PETp2	PETp2	TX2+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A15	PERn2	PERn2	RX2-	←	PETn2	PETn2	TX2-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A16	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B16**				
A17	PERp3	PERp3	RX3+	←	PETp3	PETp3	TX3+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A18	PERn3	PERn3	RX3-	←	PETn3	PETn3	TX3-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A19	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B19**				
A19	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B1**				
A20	PERp4	PERp4	RX4+	←	PETp0	PETp0	TX4+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A21	PERn4	PERn4	RX4-	←	PETn0	PETn0	TX4-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A22	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B4**				
A23	PERp5	PERp5	RX5+	←	PETp1	PETp1	TX5+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A24	PERn5	PERn5	RX5-	←	PETn1	PETn1	X5-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A25	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B7**				
A26	BP_TYPEB (VSPB)	FLEXIO5_A (PCIe x1 RXp)	BP_TYPEB (SB7B)	↔	BP_TYPEB (VSPB)	FLEXIO5_A (PCIe x1 TXp)	BP_TYPEB(SB7B)	B8				
A27	CWAKEB#,OBFFB (VSPB)	FLEXIO6_A (PCIe x1 RXn)	RESETB, SDataOutB (SB4B)	↔	CWAKEB#,OBFFB (VSPB)	FLEXIO6_A (PCIe x1 TXn)	RESETB, SDataOutB (SB4B)	B9		P1 (WAKE#)	P1 (WAKE#)	
A28	GND	GND	GND(SB3B)	–	GND	GND	GND(SB3B)	B10				
A29	REFCLKB+ (VSPB+)	FLEXIO7_A (USB2p)	(SBB+)	→	REFCLKB+(VSPB+)	FLEXIO7_A (USB2p)	(SBB+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A30	REFCLKB- (VSPB-)	FLEXIO8_A (USB2n)	(SBB-)	→	REFCLKB- (VSPB-)	FLEXIO8_A (USB2n)	(SBB-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A31	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B13**				
A32	PERp6	PERp6	RX6+	←	PETp2	PETp2	TX6+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A33	PERn6	PERn6	RX6-	←	PETn2	PETn2	TX6-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A34	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B16**				
A35	PERp7	PERp7	RX7+	←	PETp3	PETp3	TX7+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A36	PERn7	PERn7	RX7-	←	PETn3	PETn3	TX7-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A37	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B19**				

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Table 9-5 Multiprotocol SAS-4/ CopprLink (x8) to SAS-4/ CopprLink (x4) Y-Cables (2 of 2)

Multiprotocol SAS/ CopprLink x8) to SAS / CopprLink (x4) Y-Cables (Sheet 2 of 2)

Root / Controller				CABLE	Endpoint / Backplane				Devices on Backplane			
SFF-8654, CopprLink SFF-TA-1016 (74-circuit)	9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface				9402 Multi-Protocol (PCIe, SAS) Pair of x4 Cable Interfaces			SFF-8654, CopprLink SFF-TA-1016 (38-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P SAS	O/P (OCuLink Assigned)	CopprLink/M-XIO and SAS-4/ SFF-8448 Signal Names			O/P (OCuLink Assigned)	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		O/P SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	ROOT	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
B1	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**				
B2	PETp0	PETp0	TX0+	→	PERp0	PERp0	RX0+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B3	PETn0	PETn0	TX0-	→	PERn0	PERn0	RX0-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B4	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**				
B5	PETp1	PETp1	TX1+	→	PERp1	PERp1	RX1+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B6	PETn1	PETn1	TX1-	→	PERn1	PERn1	RX1-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B7	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**				
B8	2W-CLK	2WCL_A	2W-CLK, Sclock (SB0)	↔	2W-CLKA	2WCL_A	2W-CLK, SClock (SB0)	A8				
B9	2W-DATA	2WDA_A	2W-DATA, Sload (SB1)	↔	2W-DATAA	2WDA_A	2W-DATA, SLoad(SB1)	A9				
B10	GND	GND	GND (SB2)	—	GND	GND	GND(SB2)	A10				
B11	PERST# (VSP)	PERST#_A	ADD, SDataIn (SB5)	↔	PERSTA# (VSPA)	PERST#_A	ADD, SDataIn (SB5)	A11	B10 (PERST0#)	E5 (PERST#)	E5 (PERST#)	
B12	CPRSNT# (VSP)	PRPE_A	CNTRLR_TYPE (SB6)	↔	CPRSNTA# (VSPA)	PRPE_A	CNTRLR_TYPE (SB6)	A12				
B13	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**				
B14	PETp2	PETp2	TX2+	→	PERp2	PERp2	RX2+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B15	PETn2	PETn2	TX2-	→	PERn2	PERn2	RX2-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B16	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**				
B17	PETp3	PETp3	TX3+	→	PERp3	PERp3	RX3+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B18	PETn3	PETn3	TX3-	→	PERn3	PERn3	RX3-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B19	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**				
B19	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**				
B20	PETp4	PETp4	TX4+	→	PERp0	PERp0	RX4+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B21	PETn4	PETn4	TX4-	→	PERn0	PERn0	RX4-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B22	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**				
B23	PETp5	PETp5	TX5+	→	PERp1	PERp1	RX5+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B24	PETn5	PETn5	TX5-	→	PERn1	PERn1	RX5-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B25	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**				
B26	2W-CLKB (VSPB)	FLEXIO3_A(PCIe x1 TXp)	2W-CLKB, SClockB (SB0B)	↔	2W-CLKB (VSPB)	FLEXIO3_A(PCIe x1 RXp)	2W-CLKB, SClockB (SB0B)	A8				
B27	2W-DATAB (VSPB)	FLEXIO4_A(PCIe x1 TXn)	2W-DATAB, SLoadB (SB1B)	↔	2W-DATAB (VSPB)	FLEXIO4_A(PCIe x1 RXn)	2W-DATAB, SLoadB (SB1B)	A9				
B28	GND	GND	GND (SB2B)	—	GND	GND	GND (SB2B)	A10				
B29	PERSTB# (VSPB)	FLEXIO1_A	ADDB, SDataInB (SB5B)	↔	PERSTB# (VSPB)	FLEXIO1_A	ADDB, SDataIn (SB5B)	A11	B10 (PERST0#)	E5 (PERST#)	E5 (PERST#)	
B30	CPRSNTB# (VSPB)	FLEXIO2_A	CNTRLR_TYPEB (SB6B)	↔	CPRSNTB# (VSPB)	FLEXIO2_A	CNTRLR_TYPEB (SB6B)	A12				
B31	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**				
B32	PETp6	PETp6	TX6+	→	PERp2	PERp2	RX6+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B33	PETn6	PETn6	TX6-	→	PERn2	PERn2	RX6-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B34	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**				
B35	PETp7	PETp7	TX7+	→	PERp3	PERp3	RX7+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B36	PETn7	PETn7	TX7-	→	PERn3	PERn3	RX7-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B37	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**				

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Table 9-~~66~~5 Multiprotocol SAS/ CopprLink/ M-XIO (x16) to SAS/ CopprLink/ M-XIO (x16) Cables (1 of 4)

Multiprotocol SAS/ CopprLink / M-XIO x16 Cables (Sheet 1 of 4)														
Root / Controller					CABLE	*Endpoint* / Backplane					*Devices on Backplane*			
CopprLink/M-XIO SFF-TA-1016 (148-circuit)	CopprLink SFF-TA-1016 (124-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface			9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		CopprLink SFF-TA-1016 (124-circuit)	CopprLink/M-XIO SFF-TA-1016 (148-circuit)	EDSFF Connector	SFF-8639 Connector		
PCIe/ SAS	*PCIe*	*PCIe/ SAS*	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			*PCIe/ SAS*	*PCIe*	SAS	*PCIe*	*PCIe/ SAS*	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	PIN	*Endpoint*	*ROOT*	Controller	DIR	*Endpoint*	*Endpoint*	Backplane	PIN	PIN	PIN	PIN	PIN	PIN
A1	**A1**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B1**	**B1**				
A2	A2	RX0+	*PERp0*	RX0+	←	TX0+	*PETp0*	TX0+	B2	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A3	A3	RX0-	*PERn0*	RX0-	←	TX0-	*PETn0*	TX0-	B3	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A4	**A4**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B4**	**B4**				
A5	A5	RX1+	*PERp1*	RX1+	←	TX1+	PETp1	TX1+	B5	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A6	A6	RX1-	*PERn1*	RX1-	←	TX1-	PETn1	TX1-	B6	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A7	**A7**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B7**	**B7**				
A8	A8	BP_TYPE_Q0	*FLEXIO9_A, (3p3AUX_MGMT)*	BP_TYPE (SB7A)	↔	BP_TYPE_Q0	FLEXIO9_A, (3p3AUX_MGMT)	BP_TYPE (SB7A)	B8	B8				
A9	A9	FLEXIO0_Q0	*FLEXIO0_A*	RESET, SDataOut (SB4A)	↔	FLEXIO0_Q0	FLEXIO0_A	RESET, SDataOut (SB4A)	B9	B9		P1 (WAKE#)	P1 (WAKE#)	
A10	A10	GND	*GND*	GND (SB3A)	–	GND	GND	GND (SB3A)	B10	B10				
A11	A11	RCLK_Q0p	*RCLK_Ap,REFCLK_A_Dp*	(SBA+)	→	RCLK_Q0p	RCLK_Ap,REFCLK_A_Dp	(SBA+)	B11	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A12	A12	RCLK_Q0n	*RCLK_An,REFCLK_A_Dn*	(SBA-)	→	RCLK_Q0n	RCLK_An,REFCLK_A_Dn	(SBA-)	B12	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A13	**A13**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B13**	**B13**				
A14	A14	RX2+	*PERp2*	RX2+	←	TX2+	*PETp2*	TX2+	B14	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A15	A15	RX2-	*PERn2*	RX2-	←	TX2-	*PETn2*	TX2-	B15	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A16	**A16**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B16**	**B16**				
A17	A17	RX3+	*PERp3*	RX3+	←	TX3+	*PETp3*	TX3+	B17	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A18	A18	RX3-	*PERn3*	RX3-	←	TX3-	*PETn3*	TX3-	B18	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A19	**A19**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B19**	**B19**				
A20	A20	RX4+	*PERp4*	RX4+	←	TX4+	*PETp4*	TX4+	B20	B20	A31 (PERp4)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A21	A21	RX4-	*PERn4*	RX4-	←	TX4-	*PETn4*	TX4-	B21	B21	A30 (PERn4)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A22	**A22**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B22**	**B22**				
A23	A23	RX5+	*PERp5*	RX5+	←	TX5+	*PETp5*	TX5+	B23	B23	A34 (PERp5)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A24	A24	RX5-	*PERn5*	RX5-	←	TX5-	*PETn5*	TX5-	B24	B24	A33 (PERn5)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A25	**A25**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B25**	**B25**				
A26	A26	BP_TYPE_Q1	*FLEXIO5_A (PCIe x1 RXp)*	BP_TYPEB (SB7B)	↔	BP_TYPE_Q1	*FLEXIO5_A (PCIe x1 TXp)*	BP_TYPEB(SB7B)	B26	B26				
A27	A27	FLEXIO0_Q1	*FLEXIO6_A (PCIe x1 RXn)*	RESETB, SDataOutB (SB4B)	↔	FLEXIO0_Q1	*FLEXIO6_A (PCIe x1 TXn)*	RESETB, SDataOutB (SB4B)	B27	B27		P1 (WAKE#)	P1 (WAKE#)	
A28	A28	GND	*GND*	GND(SB3B)	–	GND	*GND*	GND(SB3B)	B28	B28				
A29	A29	RCLK_Q1p	FLEXIO7_A (USB2p), USB2_Dp	(SBB+)	→	RCLK_Q1p	*FLEXIO7_A (USB2p), USB2_Dp*	(SBB+)	B29	B29		E7 (REFCLK+)	E7 (REFCLK+)	
A30	A30	RCLK_Q1n	FLEXIO8_A (USB2n), USB2_Dn	(SBB-)	→	RCLK_Q1n	*FLEXIO8_A (USB2n), USB2_Dn*	(SBB-)	B30	B30		E8 (REFCLK-)	E8 (REFCLK-)	
A31	**A31**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B31**	**B31**				
A32	A32	RX6+	*PERp6*	RX6+	←	TX6+	*PETp6*	TX6+	B32	B32	A37 (PERp6)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A33	A33	RX6-	*PERn6*	RX6-	←	TX6-	*PETn6*	TX6-	B33	B33	A36 (PERn6)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A34	**A34**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B34**	**B34**				
A35	A35	RX7+	*PERp7*	RX7+	←	TX7+	*PETp7*	TX7+	B35	B35	A40 (PERp7)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A36	A36	RX7-	*PERn7*	RX7-	←	TX7-	*PETn*	TX7-	B36	B36	A39 (PERn7)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A37	**A37**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B37**	**B37**				

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Table 9-~~7~~6 Multiprotocol SAS/ CopprLink/ M-XIO (x16) to SAS/ CopprLink/ M-XIO (x16) Cables (2 of 4)

Multiprotocol SAS/ CopprLink / M-XIO x16 Cables (Sheet 2 of 4)														
Root / Controller					CABLE	*Endpoint* / Backplane					*Devices on Backplane*			
CopprLink/M-XIO SFF-TA-1016 (148-circuit)	CopprLink SFF-TA-1016 (124-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface			9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		CopprLink SFF-TA-1016 (124-circuit)	CopprLink/M-XIO SFF-TA-1016 (148-circuit)	EDSFF Connector	SFF-8639 Connector		
PCIe/ SAS	*PCIe*	*PCIe/ SAS*	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			*PCIe/ SAS*	*PCIe*	SAS	*PCIe*	*PCIe/ SAS*	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	PIN	*Endpoint*	*ROOT*	Controller	DIR	*Endpoint*	*Endpoint*	Backplane	PIN	PIN	PIN	PIN	PIN	PIN
A38	**A38**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B38**	**B38**				
A39	A39	RX8+	*PERp8*	RX8+	←	TX8+	*PETp8*	TX8+	B39	B39	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A40	A40	RX8-	*PERn8*	RX8-	←	TX8-	*PETn8*	TX8-	B40	B40	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A41	**A41**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B41**	**B41**				
A42	A42	RX9+	*PERp9*	RX9+	←	TX9+	PETp9	TX9+	B42	B42	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A43	A43	RX9-	*PERn9*	RX9-	←	TX9-	PETn9	TX9-	B43	B43	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A44	**A44**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B44**	**B44**				
A45		BP_TYPE_Q2	*FLEXIO9_B, (3p3AUX_MGMT)*	BP_TYPE (SB7C)	↔	BP_TYPE_Q2	FLEXIO9_B, (3p3AUX_MGMT)	BP_TYPE (SB7C)		B45				
A46		FLEXIO0_Q2	*FLEXIO0_B*	RESET, SDataOut (SB4C)	↔	FLEXIO0_Q2	FLEXIO0_B	RESET, SDataOut (SB4C)		B46		P1 (WAKE#)	P1 (WAKE#)	
A47		GND	*GND*	GND (SBC3)	–	GND	GND	GND (SB3C)		**B47**				
A48		RCLK_Q2p	*RCLK_Bp,REFCLK_B_Dp*	(SBC+)	→	RCLK_Q2p	RCLK_Bp,REFCLK_B_Dp	(SBC+)		B48	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A49		RCLK_Q2n	*RCLK_Bn,REFCLK_B_Dn*	(SBC-)	→	RCLK_Q2n	RCLK_Bn,REFCLK_B_Dn	(SBC-)		B49	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A50		**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**		**B50**				
A51	A45	RX10+	*PERp10*	RX10+	←	TX10+	*PETp10*	TX10+	B45	B51	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A52	A46	RX10-	*PERn10*	RX10-	←	TX10-	*PETn10*	TX10-	B46	B52	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A53	**A47**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B47**	**B53**				
A54	A48	RX11+	*PERp11*	RX11+	←	TX11+	*PETp11*	TX11+	B48	B54	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A55	A49	RX11-	*PERn11*	RX11-	←	TX11-	*PETn11*	TX11-	B49	B55	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A56	**A50**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B50**	**B56**				
A57	A51	RX12+	*PERp12*	RX12+	←	TX12+	*PETp12*	TX12+	B51	B57	A31 (PERp4)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A58	A52	RX12-	*PERn12*	RX12-	←	TX12-	*PETn12*	TX12-	B52	B58	A30 (PERn4)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A59	**A53**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B53**	**B59**				
A60	A54	RX13+	*PERp13*	RX13+	←	TX13+	*PETp13*	TX13+	B54	B60	A34 (PERp5)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A61	A55	RX13-	*PERn13*	RX13-	←	TX13-	*PETn13*	TX13-	B55	B61	A33 (PERn5)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A62	**A56**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B56**	**B62**				
A63		BP_TYPE_Q3	*FLEXIO5_B (PCIe x1 RXp)*	BP_TYPEB (SB7D)	↔	BP_TYPE_Q3	*FLEXIO5_B (PCIe x1 TXp)*	BP_TYPEB(SB7D)		B63				
A64		FLEXIO0_Q3	*FLEXIO6_B (PCIe x1 RXn)*	RESETB, SDataOutB (SB4D)	↔	FLEXIO0_Q3	*FLEXIO6_B (PCIe x1 TXn)*	RESETB, SDataOutB (SB4D)		B64		P1 (WAKE#)	P1 (WAKE#)	
A65		GND	*GND*	GND(SB3D)	–	GND	*GND*	GND(SB3D)		**B65**				
A66		RCLK_Q3p	FLEXIO7_B (USB2p), USB2_Dp	(SBD+)	→	RCLK_Q3p	*FLEXIO7_B (USB2p), USB2_Dp*	(SBD+)		B66		E7 (REFCLK+)	E7 (REFCLK+)	
A67		RCLK_Q3n	FLEXIO8_B (USB2n), USB2_Dn	(SBD-)	→	RCLK_Q3n	*FLEXIO8_B (USB2n), USB2_Dn*	(SBD-)		B67		E8 (REFCLK-)	E8 (REFCLK-)	
A68		**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**		**B68**				
A69	A57	RX14+	*PERp14*	RX14+	←	TX14+	*PETp14*	TX14+	B57	B69	A37 (PERp6)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A70	A58	RX14-	*PERn14*	RX14-	←	TX14-	*PETn14*	TX14-	B58	B70	A36 (PERn6)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A71	**A59**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B59**	**B71**				
A72	A60	RX15+	*PERp15*	RX15+	←	TX15+	*PETp15*	TX15+	B60	B72	A40 (PERp7)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A73	A61	RX15-	*PERn15*	RX15-	←	TX15-	*PETn15*	TX15-	B61	B73	A39 (PERn7)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A74	**A62**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B62**	**B74**				

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Table 9-~~88~~6 Multiprotocol SAS/ CopprLink/ M-XIO (x16) to SAS/ CopprLink/ M-XIO (x16) Cables (3 of 4)

Multiprotocol SAS/ CopprLink / M-XIO x16 Cables (Sheet 3 of 4)

Root / Controller					CABLE	*Endpoint* / Backplane					*Devices on Backplane*			
CopprLink/M-XIO SFF-TA-1016 (148-circuit)	CopprLink SFF-TA-1016 (124-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface			9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		CopprLink SFF-TA-1016 (124-circuit)	SFF-8654 (148-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P SAS	*PCIe*	*PCIe*/ SAS	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			*PCIe*/ SAS	*PCIe*	SAS	*PCIe*	*PCIe*/ SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	PIN	*Endpoint*	*ROOT*	Controller	DIR	*Endpoint*	*Endpoint*	Backplane	PIN	PIN	PIN	PIN	PIN	PIN
B1	**B1**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**	**A1**				
B2	B2	TX0+	*PETp0*	TX0+	→	RX0+	*PERp0*	RX0+	A2	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B3	B3	TX0-	*PETn0*	TX0-	→	RX0-	*PERn0*	RX0-	A3	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B4	**B4**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**	**A4**				
B5	B5	TX1+	*PETp1*	TX1+	→	RX1+	*PERp1*	RX1+	A5	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B6	B6	TX1-	*PETn1*	TX1-	→	RX1-	*PERn1*	RX1-	A6	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B7	**B7**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**	**A7**				
B8	B8	2WCLK_Q0	*2WCL_A,SMSCL*	2W-CLK, Sclock (SB0A)	↔	2WCLK_Q0	*2WCL_A,SMSCL*	2W-CLK, SClock (SB0A)	A8	A8				
B9	B9	2WDA_Q0	*2WDA_A,SMSDA*	2W-DATA, Sload (SB1A)	↔	2WDA_Q0	*2WDA_A,SMSDA*	2W-DATA, SLoad(SB1A)	A9	A9				
B10	B10	GND	*GND*	GND (SB2A)	—	GND	*GND*	GND(SB2A)	A10	A10				
B11	B11	PERST#_Q0	*PERST#_A,PERST_N*	ADD, SDataIn (SB5A)	↔	PERST#_Q0	*PERST#_A,PERST_N*	ADD, SDataIn (SB5A)	A11	A11	B10 (PERSTO#)	E5 (PERST#)	E5 (PERST#)	
B12	B12	CPRESNT#_Q0	*PRPE_A,CBL_PRES_A_PESTI_N*	CNTRLR_TYPE (SB6A)	↔	CPRESNT#_Q0	*PRPE_A,CBL_PRES_A_PESTI_N*	CNTRLR_TYPE (SB6A)	A12	A12				
B13	**B13**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**	**A13**				
B14	B14	TX2+	*PETp2*	TX2+	→	RX2+	*PERp2*	RX2+	A14	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B15	B15	TX2-	*PETn2*	TX2-	→	RX2-	*PERn2*	RX2-	A15	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B16	**B16**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**	**A16**				
B17	B17	TX3+	*PETp3*	TX3+	→	RX3+	*PERp3*	RX3+	A17	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B18	B18	TX3-	*PETn3*	TX3-	→	RX3-	*PERn3*	RX3-	A18	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B19	**B19**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**	**A19**				
B20	B20	TX4+	*PETp4*	TX4+	→	RX4+	*PERp4*	RX4+	A20	A20	B31 (PETp4)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B21	B21	TX4-	*PETn4*	TX4-	→	RX4-	*PERn4*	RX4-	A21	A21	B30 (PETn4)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B22	**B22**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A22**	**A22**				
B23	B23	TX5+	*PETp5*	TX5+	→	RX5+	*PERp5*	RX5+	A23	A23	B34 (PETp5)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B24	B24	TX5-	*PETn5*	TX5-	→	RX5-	*PERn5*	RX5-	A24	A24	B33 (PETn5)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B25	**B25**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A25**	**A25**				
B26	B26	2WCLK_Q1	*FLEXIO3_A(PCIe x1 TXp)*	2W-CLKB, SClockB (SB0B)	↔	2WCLK_Q1	*FLEXIO3_A(PCIe x1 RXp)*	2W-CLKB, SClockB (SB0B)	A26	A26				
B27	B27	2WDA_Q1	*FLEXIO4_A(PCIe x1 TXn)*	2W-DATAB, SLoadB (SB1B)	↔	2WDA_Q1	*FLEXIO4_A(PCIe x1 RXn)*	2W-DATAB, SLoadB (SB1B)	A27	A27				
B28	B28	GND	*GND*	GND (SB2B)	—	GND	*GND*	GND (SB2B)	A28	A28				
B29	B29	PERST#_Q1	*FLEXIO1_A*	ADDB, SDataInB (SB5B)	↔	PERST#_Q1	*FLEXIO1_A*	ADDB, SDataIn (SB5B)	A29	A29		E5 (PERST#)	E5 (PERST#)	
B30	B30	CPRESNT#_Q1	*FLEXIO2_A*	CNTRLR_TYPEB (SB6B)	↔	CPRESNT#_Q1	*FLEXIO2_A*	CNTRLR_TYPEB (SB6B)	A30	A30				
B31	**B31**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A31**	**A31**				
B32	B32	TX6+	*PETp6*	TX6+	→	RX6+	*PERp6*	RX6+	A32	A32	B37 (PETp6)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B33	B33	TX6-	*PETn6*	TX6-	→	RX6-	*PERn6*	RX6-	A33	A33	B36 (PETn6)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B34	**B34**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A34**	**A34**				
B35	B35	TX7+	*PETp7*	TX7+	→	RX7+	*PERp*	RX7+	A35	A35	B40 (PETp7)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B36	B36	TX7-	*PETn7*	TX7-	→	RX7-	*PERn7*	RX7-	A36	A36	B39 (PETn7)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B37	**B37**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A37**	**A37**				

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Table 9-~~6~~-9 Multiprotocol SAS/ CopprLink/ M-XIO (x16) to SAS/ CopprLink/ M-XIO (x16) Cables (4 of 4)

Multiprotocol SAS/ CopprLink / M-XIO x16 Cables (Sheet 4 of 4)

Root / Controller					CABLE	Endpoint / Backplane					Devices on Backplane			
CopprLink/M-XIO SFF-TA-1016 (148-circuit)	CopprLink SFF-TA-1016 (124-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface			9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		CopprLink SFF-TA-1016 (124-circuit)	CopprLink/M-XIO SFF-TA-1016 (148-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P SAS	PCIe	PCIe/ SAS	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			PCIe/ SAS	PCIe	SAS	PCIe	PCIe/ SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	PIN	Endpoint	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN	PIN
B38	**B38**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A38**	**A38**				
B39	B39	TX8+	*PETp8*	TX8+	→	RX8+	*PERp8*	RX8+	A39	A39	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B40	B40	TX8-	*PETn8*	TX8-	→	RX8-	*PERn8*	RX8-	A40	A40	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B41	**B41**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A41**	**A41**				
B42	B42	TX9+	*PETp9*	TX9+	→	RX9+	*PERp9*	RX9+	A42	A42	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B43	B43	TX9-	*PETn9*	TX9-	→	RX9-	*PERn9*	RX9-	A43	A43	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B44	**B44**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A44**	**A44**				
B45		2WCLK_Q2	*2WCL_B,SMSCL*	2W-CLK, Sclock (SBC)	↔	2WCLK_Q2	*2WCL_B,SMSCL*	2W-CLK, SClock (SBC0)		A45				
B46		2WDA_Q2	*2WDA_B,SMSDA*	2W-DATA, Sload (SBC)	↔	2WDA_Q2	*2WDA_B,SMSDA*	2W-DATA, SLoad(SBC1)		A46				
B47		GND	*GND*	GND (SB2C)	—	GND	*GND*	GND(SBC2)		**A47**				
B48		PERST#_Q2	*PERST#_B,PERST_N*	ADD, SDataIn (SB5C)	↔	PERST#_Q2	*PERST#_B,PERST_N*	ADD, SDataIn (SBC5)		A48	B10 (PERST0#)	E5 (PERST#)	E5 (PERST#)	
B49		CPRESNT#_Q2	*PRPE_B,CBL_PRES_B_PESTI_N*	CNTRLR_TYPE (SB6C)	↔	CPRESNT#_Q2	*PRPE_B,CBL_PRES_B_PESTI_N*	CNTRLR_TYPE (SBC6)		A49				
B50		**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**		**A50**				
B51	B45	TX10+	*PETp10*	TX10+	→	RX10+	*PERp10*	RX10+	A45	A51	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B52	B46	TX10-	*PETn10*	TX10-	→	RX10-	*PERn10*	RX10-	A46	A52	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B53	**B47**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A47**	**A53**				
B54	B48	TX11+	*PETp11*	TX11+	→	RX11+	*PERp11*	RX11+	A48	A54	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B55	B49	TX11-	*PETn11*	TX11-	→	RX11-	*PERn11*	RX11-	A49	A55	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B56	**B50**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A50**	**A56**				
B57	B51	TX12+	*PETp12*	TX12+	→	RX12+	*PERp12*	RX12+	A51	A57	B31 (PETp4)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B58	B52	TX12-	*PETn12*	TX12-	→	RX12-	*PERn12*	RX12-	A52	A58	B30 (PETn4)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B59	**B53**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A53**	**A59**				
B60	B54	TX13+	*PETp13*	TX13+	→	RX13+	*PERp13*	RX13+	A54	A60	B34 (PETp5)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B61	B55	TX13-	*PETn13*	TX13-	→	RX13-	*PERn13*	RX13-	A55	A61	B33 (PETn5)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B62	**B56**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A56**	**A62**				
B63		2WCLK_Q3	*FLEXIO3_B(PCIe x1 TXp)*	2W-CLKB, SClockB (SB0D)	↔	2WCLK_Q3	*FLEXIO3_B(PCIe x1 RXp)*	2W-CLKB, SClockB (SB0D)		A63				
B64		2WDA_Q3	*FLEXIO4_B(PCIe x1 TXn)*	2W-DATAB, SLoadB (SB1D)	↔	2WDA_Q3	*FLEXIO4_B(PCIe x1 RXn)*	2W-DATAB, SLoadB (SB1D)		A64				
B65		GND	*GND*	GND (SB2D)	—	GND	*GND*	GND (SB2D)		**A65**				
B66		PERST#_Q3	*FLEXIO1_B*	ADDB, SDataInB (SB5D)	↔	PERST#_Q3	*FLEXIO1_B*	ADDB, SDataIn (SB5D)		A66		E5 (PERST#)	E5 (PERST#)	
B67		CPRESNT#_Q3	*FLEXIO2_B*	CNTRLR_TYPEB (SB6D)	↔	CPRESNT#_Q3	*FLEXIO2_B*	CNTRLR_TYPEB (SB6D)		A67				
B68		**GROUND**	**GROUND**	**GROUND**	—		**GROUND**	**GROUND**		**A68**				
B69	B57	TX14+	*PETp14*	TX14+	→	RX14+	*PERp14*	RX14+	A57	A69	B37 (PETp6)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B70	B58	TX14-	*PETn14*	TX14-	→	RX14-	*PERn14*	RX14-	A58	A70	B36 (PETn6)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B71	**B59**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A59**	**A71**				
B72	B60	TX15+	*PETp15*	TX15+	→	RX15+	*PERp 15*	RX15+	A60	A72	B40 (PETp7)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B73	B61	TX15-	*PETn15*	TX15-	→	RX15-	*PERn15*	RX15-	A61	A73	B39 (PETn7)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B74	**B62**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A62**	**A74**				

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Table 9-~~10~~10 Multiprotocol SAS-~~4~~/ CopprLink/ M-XIO (x16) to SAS-~~4~~/ CopprLink/ M-XIO (x8) Y-Cables (1 of 4)

Multiprotocol SAS/ CopprLink / M-XIO x16 Y-Cables (Sheet 1 of 4)														
Root / Controller					CABLE	Endpoint / Backplane				Devices on Backplane				
CopprLink/M-XIO SFF-TA-1016 (148-circuit)	CopprLink SFF-TA-1016 (124-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface			9402 Multi-Protocol (PCIe, SAS) Pair of x8 Cable Interfaces	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		CopprLink/M-XIO SFF-TA-1016 (74-circuit)	EDSFF Connector	SFF-8639 Connector			
PCIe/ SAS	PCIe	PCIe/ SAS	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			PCIe/ SAS	PCIe	SAS	PCIe/ SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™	
PIN	PIN	Endpoint	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN	
A1	**A1**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B1**					
A2	A2	RX0+	*PERp0*	RX0+	←	TX0+	*PETp0*	TX0+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)	
A3	A3	RX0-	*PERn0*	RX0-	←	TX0-	*PETn0*	TX0-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)	
A4	**A4**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B4**					
A5	A5	RX1+	*PERp1*	RX1+	←	TX1+	PETp1	TX1+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)	
A6	A6	RX1-	*PERn1*	RX1-	←	TX1-	PETn1	TX1-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)	
A7	**A7**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B7**					
A8	A8	BP_TYPE_Q0	*FLEXIO9_A, (3p3AUX_MGMT)*	BP_TYPE (SB7A)	↔	BP_TYPE_Q0	FLEXIO9_A, (3p3AUX_MGMT)	BP_TYPE (SB7A)	B8					
A9	A9	FLEXIO0_Q0	*FLEXIO0_A*	RESET, SDataOut (SB4A)	↔	FLEXIO0_Q0	FLEXIO0_A	RESET, SDataOut (SB4A)	B9		P1 (WAKE#)	P1 (WAKE#)		
A10	A10	GND	*GND*	GND (SB3A)	—	GND	GND	GND (SB3A)	B10					
A11	A11	RCLK_Q0p	*RCLK_Ap,REFCLK_A_Dp*	(SBA+)	→	RCLK_Q0p	RCLK_Ap,REFCLK_A_Dp	(SBA+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)		
A12	A12	RCLK_Q0n	*RCLK_An,REFCLK_A_Dn*	(SBA-)	→	RCLK_Q0n	RCLK_An,REFCLK_A_Dn	(SBA-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)		
A13	**A13**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B13**					
A14	A14	RX2+	*PERp2*	RX2+	←	TX2+	*PETp2*	TX2+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)	
A15	A15	RX2-	*PERn2*	RX2-	←	TX2-	*PETn2*	TX2-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)	
A16	**A16**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B16**					
A17	A17	RX3+	*PERp3*	RX3+	←	TX3+	*PETp3*	TX3+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)	
A18	A18	RX3-	*PERn3*	RX3-	←	TX3-	*PETn3*	TX3-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)	
A19	**A19**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B19**					
A20	A20	RX4+	*PERp4*	RX4+	←	TX4+	*PETp4*	TX4+	B20	A31 (PERp4)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)	
A21	A21	RX4-	*PERn4*	RX4-	←	TX4-	*PETn4*	TX4-	B21	A30 (PERn4)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)	
A22	**A22**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B22**					
A23	A23	RX5+	*PERp5*	RX5+	←	TX5+	*PETp5*	TX5+	B23	A34 (PERp5)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)	
A24	A24	RX5-	*PERn5*	RX5-	←	TX5-	*PETn5*	TX5-	B24	A33 (PERn5)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)	
A25	**A25**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B25**					
A26	A26	BP_TYPE_Q1	*FLEXIO5_A (PCIe x1 RXp)*	BP_TYPEB (SB7B)	↔	BP_TYPE_Q1	*FLEXIO5_A (PCIe x1 TXp)*	BP_TYPEB(SB7B)	B26					
A27	A27	FLEXIO0_Q1	*FLEXIO6_A (PCIe x1 RXn)*	RESETB, SDataOutB (SB4B)	↔	FLEXIO0_Q1	*FLEXIO6_A (PCIe x1 TXn)*	RESETB, SDataOutB (SB4B)	B27		P1 (WAKE#)	P1 (WAKE#)		
A28	A28	GND	*GND*	GND(SB3B)	—	GND	*GND*	GND(SB3B)	B28					
A29	A29	RCLK_Q1p	FLEXIO7_A (USB2p), USB2_Dp	(SBB+)	→	RCLK_Q1p	*FLEXIO7_A (USB2p), USB2_Dp*	(SBB+)	B29		E7 (REFCLK+)	E7 (REFCLK+)		
A30	A30	RCLK_Q1n	FLEXIO8_A (USB2n), USB2_Dn	(SBB-)	→	RCLK_Q1n	*FLEXIO8_A (USB2n), USB2_Dn*	(SBB-)	B30		E8 (REFCLK-)	E8 (REFCLK-)		
A31	**A31**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B31**					
A32	A32	RX6+	*PERp6*	RX6+	←	TX6+	*PETp6*	TX6+	B32	A37 (PERp6)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)	
A33	A33	RX6-	*PERn6*	RX6-	←	TX6-	*PETn6*	TX6-	B33	A36 (PERn6)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)	
A34	**A34**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B34**					
A35	A35	RX7+	*PERp7*	RX7+	←	TX7+	*PETp7*	TX7+	B35	A40 (PERp7)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)	
A36	A36	RX7-	*PERn7*	RX7-	←	TX7-	*PETn*	TX7-	B36	A39 (PERn7)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)	
A37	**A37**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B37**					

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Table 9-11~~16~~ Multiprotocol SAS/ CopprLink/ M-XIO (x16) to SAS/ CopprLink/ M-XIO (x8) Y-Cables (2 of 4)

Multiprotocol SAS/ CopprLink / M-XIO x16 Y-Cables (Sheet 2 of 4)														
Root / Controller					CABLE	*Endpoint* / Backplane				*Devices on Backplane*				
CopprLink/M-XIO SFF-TA-1016 (148-circuit)	CopprLink SFF-TA-1016 (124-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface			9402 Multi-Protocol (PCIe, SAS) Pair of x8 Cable Interfaces	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		CopprLink/M-XIO SFF-TA-1016 (74-circuit)	EDSFF Connector	SFF-8639 Connector			
PCIe/ SAS	*PCIe*	*PCIe/ SAS*	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			*PCIe/ SAS*	*PCIe*	SAS	*PCIe/ SAS*	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™	
PIN	PIN	*Endpoint*	*ROOT*	Controller	DIR	*Endpoint*	*Endpoint*	Backplane	PIN	PIN	PIN	PIN	PIN	
A38	**A38**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B1**					
A39	A39	RX8+	*PERp8*	RX8+	←	TX0+	*PETp0*	TX0+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)	
A40	A40	RX8-	*PERn8*	RX8-	←	TX0-	*PETn0*	TX0-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)	
A41	**A41**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B4**					
A42	A42	RX9+	*PERp9*	RX9+	←	TX1+	PETp1	TX1+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)	
A43	A43	RX9-	*PERn9*	RX9-	←	TX1-	PETn1	TX1-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)	
A44	**A44**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B7**					
A45		BP_TYPE_Q2	*FLEXIO9_B, (3p3AUX_MGMT)*	BP_TYPE (SB7C)	↔	BP_TYPE_Q0	*FLEXIO9_A, (3p3AUX_MGMT)*	BP_TYPE (SB7A)	B8					
A46		FLEXIO0_Q2	*FLEXIO0_B*	RESET, SDataOut (SB4C)	↔	FLEXIO0_Q0	*FLEXIO0_A*	RESET, SDataOut (SB4A)	B9		P1 (WAKE#)	P1 (WAKE#)		
A47		GND	*GND*	GND (SBC3)	–	GND	GND	GND (SB3A)	B10					
A48		RCLK_Q2p	*RCLK_Bp,REFCLK_B_Dp*	(SBC+)	→	RCLK_Q0p	*RCLK_Ap,REFCLK_A_Dp*	(SBA+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)		
A49		RCLK_Q2n	*RCLK_Bn,REFCLK_B_Dn*	(SBC-)	→	RCLK_Q0n	*RCLK_An,REFCLK_A_Dn*	(SBA-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)		
A50		**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B13**					
A51	A45	RX10+	*PERp10*	RX10+	←	TX2+	*PETp2*	TX2+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)	
A52	A46	RX10-	*PERn10*	RX10-	←	TX2-	*PETn2*	TX2-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)	
A53	**A47**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B16**					
A54	A48	RX11+	*PERp11*	RX11+	←	TX3+	*PETp3*	TX3+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)	
A55	A49	RX11-	*PERn11*	RX11-	←	TX3-	*PETn3*	TX3-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)	
A56	**A50**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B19**					
A57	A51	RX12+	*PERp12*	RX12+	←	TX4+	*PETp4*	TX4+	B20	A31 (PERp4)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)	
A58	A52	RX12-	*PERn12*	RX12-	←	TX4-	*PETn4*	TX4-	B21	A30 (PERn4)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)	
A59	**A53**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B22**					
A60	A54	RX13+	*PERp13*	RX13+	←	TX5+	*PETp5*	TX5+	B23	A34 (PERp5)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)	
A61	A55	RX13-	*PERn13*	RX13-	←	TX5-	*PETn5*	TX5-	B24	A33 (PERn5)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)	
A62	**A56**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B25**					
A63		BP_TYPE_Q3	*FLEXIO5_B (PCIe x1 RXp)*	BP_TYPEB (SB7D)	↔	BP_TYPE_Q1	*FLEXIO5_A (PCIe x1 TXp)*	BP_TYPEB(SB7B)	B26					
A64		FLEXIO0_Q3	*FLEXIO6_B (PCIe x1 RXn)*	RESETB, SDataOutB (SB4D)	↔	FLEXIO0_Q1	*FLEXIO6_A (PCIe x1 TXn)*	RESETB, SDataOutB (SB4B)	B27		P1 (WAKE#)	P1 (WAKE#)		
A65		GND	*GND*	GND(SB3D)	–	GND	*GND*	GND(SB3B)	B28					
A66		RCLK_Q3p	FLEXIO7_B (USB2p), USB2_Dp	(SBD+)	→	RCLK_Q1p	FLEXIO7_A (USB2p), USB2_Dp	(SBB+)	B29		E7 (REFCLK+)	E7 (REFCLK+)		
A67		RCLK_Q3n	FLEXIO8_B (USB2n), USB2_Dn	(SBD-)	→	RCLK_Q1n	FLEXIO8_A (USB2n), USB2_Dn	(SBB-)	B30		E8 (REFCLK-)	E8 (REFCLK-)		
A68		**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B31**					
A69	A57	RX14+	*PERp14*	RX14+	←	TX6+	*PETp6*	TX6+	B32	A37 (PERp6)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)	
A70	A58	RX14-	*PERn14*	RX14-	←	TX6-	*PETn6*	TX6-	B33	A36 (PERn6)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)	
A71	**A59**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B34**					
A72	A60	RX15+	*PERp15*	RX15+	←	TX7+	*PETp7*	TX7+	B35	A40 (PERp7)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)	
A73	A61	RX15-	*PERn15*	RX15-	←	TX7-	*PETn*	TX7-	B36	A39 (PERn7)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)	
A74	**A62**	**GROUND**	**GROUND**	**GROUND**	–	**GROUND**	**GROUND**	**GROUND**	**B37**					

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Table 9-12~~12~~6 Multiprotocol SAS/ CopprLink/ M-XIO (x16) to SAS/ CopprLink/ M-XIO (x8) Y-Cables (3 of 4)

Multiprotocol SAS/ CopprLink / M-XIO x16 Y-Cables (Sheet 3 of 4)

Root / Controller					CABLE	Endpoint / Backplane				Devices on Backplane			
CopprLink/M-XIO SFF-TA-1016 (148-circuit)	CopprLink SFF-TA-1016 (124-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface			9402 Multi-Protocol (PCIe, SAS) Pair of x8 Cable Interfaces	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		CopprLink/M-XIO SFF-TA-1016 (74-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P SAS	PCIe	PCIe/ SAS	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			PCIe/ SAS	PCIe	SAS	PCIe/ SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	PIN	Endpoint	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
B1	**B1**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**				
B2	B2	TX0+	*PETp0*	TX0+	→	RX0+	*PERp0*	RX0+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B3	B3	TX0-	*PETn0*	TX0-	→	RX0-	*PERn0*	RX0-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B4	**B4**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**				
B5	B5	TX1+	*PETp1*	TX1+	→	RX1+	*PERp1*	RX1+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B6	B6	TX1-	*PETn1*	TX1-	→	RX1-	*PERn1*	RX1-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B7	**B7**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**				
B8	B8	2WCLK_Q0	*2WCL_A,SMSCL*	2W-CLK, SClock (SB0A)	↔	2WCLK_Q0	*2WCL_A,SMSCL*	2W-CLK, SClock (SB0A)	A8				
B9	B9	2WDA_Q0	*2WDA_A,SMSDA*	2W-DATA, SLoad (SB1A)	↔	2WDA_Q0	*2WDA_A,SMSDA*	2W-DATA, SLoad(SB1A)	A9				
B10	B10	GND	*GND*	GND (SB2A)	—	GND	*GND*	GND(SB2A)	A10				
B11	B11	PERST#_Q0	*PERST#_A,PERST_N*	ADD, SDataIn (SB5A)	↔	PERST#_Q0	*PERST#_A,PERST_N*	ADD, SDataIn (SB5A)	A11	B10 (PERST0#)	E5 (PERST#)	E5 (PERST#)	
B12	B12	CPRESNT#_Q0	*PRPE_A,CBL_PRES_A_PESTI_N*	CNTRLR_TYPE (SB6A)	↔	CPRESNT#_Q0	*PRPE_A,CBL_PRES_A_PESTI_N*	CNTRLR_TYPE (SB6A)	A12				
B13	**B13**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**				
B14	B14	TX2+	*PETp2*	TX2+	→	RX2+	*PERp2*	RX2+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B15	B15	TX2-	*PETn2*	TX2-	→	RX2-	*PERn2*	RX2-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B16	**B16**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**				
B17	B17	TX3+	*PETp3*	TX3+	→	RX3+	*PERp3*	RX3+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B18	B18	TX3-	*PETn3*	TX3-	→	RX3-	*PERn3*	RX3-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B19	**B19**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**				
B20	B20	TX4+	*PETp4*	TX4+	→	RX4+	*PERp4*	RX4+	A20	B31 (PETp4)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B21	B21	TX4-	*PETn4*	TX4-	→	RX4-	*PERn4*	RX4-	A21	B30 (PETn4)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B22	**B22**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A22**				
B23	B23	TX5+	*PETp5*	TX5+	→	RX5+	*PERp5*	RX5+	A23	B34 (PETp5)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B24	B24	TX5-	*PETn5*	TX5-	→	RX5-	*PERn5*	RX5-	A24	B33 (PETn5)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B25	**B25**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A25**				
B26	B26	2WCLK_Q1	*FLEXIO3_A(PCIe x1 TXp)*	2W-CLKB, SClockB (SB0B)	↔	2WCLK_Q1	*FLEXIO3_A(PCIe x1 RXp)*	2W-CLKB, SClockB (SB0B)	A26				
B27	B27	2WDA_Q1	*FLEXIO4_A(PCIe x1 TXn)*	2W-DATAB, SLoadB (SB1B)	↔	2WDA_Q1	*FLEXIO4_A(PCIe x1 RXn)*	2W-DATAB, SLoadB (SB1B)	A27				
B28	B28	GND	*GND*	GND (SB2B)	—	GND	*GND*	GND (SB2B)	A28				
B29	B29	PERST#_Q1	*FLEXIO1_A*	ADDB, SDataInB (SB5B)	↔	PERST#_Q1	*FLEXIO1_A*	ADDB, SDataIn (SB5B)	A29		E5 (PERST#)	E5 (PERST#)	
B30	B30	CPRESNT#_Q1	*FLEXIO2_A*	CNTRLR_TYPEB (SB6B)	↔	CPRESNT#_Q1	*FLEXIO2_A*	CNTRLR_TYPEB (SB6B)	A30				
B31	**B31**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A31**				
B32	B32	TX6+	*PETp6*	TX6+	→	RX6+	*PERp6*	RX6+	A32	B37 (PETp6)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B33	B33	TX6-	*PETn6*	TX6-	→	RX6-	*PERn6*	RX6-	A33	B36 (PETn6)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B34	**B34**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A34**				
B35	B35	TX7+	*PETp7*	TX7+	→	RX7+	*PERp*	RX7+	A35	B40 (PETp7)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B36	B36	TX7-	*PETn7*	TX7-	→	RX7-	*PERn7*	RX7-	A36	B39 (PETn7)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B37	**B37**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A37**				

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Table 9-~~131~~36 Multiprotocol SAS/ CopprLink/ M-XIO (x16) to SAS/ CopprLink/ M-XIO (x8) Y-Cables (4 of 4)

Multiprotocol SAS/ CopprLink / M-XIO x16 Y-Cables (Sheet 4 of 4)

Root / Controller					CABLE	Endpoint / Backplane				Devices on Backplane			
CopprLink/M-XIO SFF-TA-1016 (148-circuit)	CopprLink SFF-TA-1016 (124-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface			9402 Multi-Protocol (PCIe, SAS) Pair of x8 Cable Interfaces	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names		CopprLink/M-XIO SFF-TA-1016 (74-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P SAS	PCIe	PCIe/ SAS	CopprLink/M-XIO and SAS/ SFF-8448 Signal Names			PCIe/ SAS	PCIe	SAS	PCIe/ SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	PIN	Endpoint	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
B38	**B38**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**				
B39	B39	TX8+	*PETp8*	TX8+	→	RX0+	*PERp0*	RX0+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B40	B40	TX8-	*PETn8*	TX8-	→	RX0-	*PERn0*	RX0-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B41	**B41**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**				
B42	B42	TX9+	*PETp9*	TX9+	→	RX1+	*PERp1*	RX1+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B43	B43	TX9-	*PETn9*	TX9-	→	RX1-	*PERn1*	RX1-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B44	**B44**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**				
B45		2WCLK_Q2	*2WCL_B,SMSCL*	2W-CLK, Sclock (SBC)	↔	2WCLK_Q0	*2WCL_A,SMSCL*	2W-CLK, SClock (SB0A)	A8				
B46		2WDA_Q2	*2WDA_B,SMSDA*	2W-DATA, Sload (SBC)	↔	2WDA_Q0	*2WDA_A,SMSDA*	2W-DATA, SLoad(SB1A)	A9				
B47		GND	*GND*	GND (SB2C)	—	GND	*GND*	GND(SB2A)	A10				
B48		PERST#_Q2	*PERST#_B,PERST_N*	ADD, SDataIn (SB5C)	↔	PERST#_Q0	*PERST#_A,PERST_N*	ADD, SDataIn (SB5A)	A11	B10 (PERST0#)	E5 (PERST#)	E5 (PERST#)	
B49		CPRESNT#_Q2	*PRPE_B,CBL_PRES_B_PESTI_N*	CNTRLR_TYPE (SB6C)	↔	CPRESNT#_Q0	*PRPE_A,CBL_PRES_A_PESTI_N*	CNTRLR_TYPE (SB6A)	A12				
B50		**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**				
B51	B45	TX10+	*PETp10*	TX10+	→	RX2+	*PERp2*	RX2+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B52	B46	TX10-	*PETn10*	TX10-	→	RX2-	*PERn2*	RX2-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B53	**B47**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**				
B54	B48	TX11+	*PETp11*	TX11+	→	RX3+	*PERp3*	RX3+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B55	B49	TX11-	*PETn11*	TX11-	→	RX3-	*PERn3*	RX3-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B56	**B50**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**				
B57	B51	TX12+	*PETp12*	TX12+	→	RX4+	*PERp4*	RX4+	A20	B31 (PETp4)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B58	B52	TX12-	*PETn12*	TX12-	→	RX4-	*PERn4*	RX4-	A21	B30 (PETn4)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B59	**B53**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A22**				
B60	B54	TX13+	*PETp13*	TX13+	→	RX5+	*PERp5*	RX5+	A23	B34 (PETp5)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B61	B55	TX13-	*PETn13*	TX13-	→	RX5-	*PERn5*	RX5-	A24	B33 (PETn5)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B62	**B56**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A25**				
B63		2WCLK_Q3	*FLEXIO3_B(PCIe x1 TXp)*	2W-CLKB, SClockB (SB0D)	↔	2WCLK_Q1	*FLEXIO3_A(PCIe x1 RXp)*	2W-CLKB, SClockB (SB0B)	A26				
B64		2WDA_Q3	*FLEXIO4_B(PCIe x1 TXn)*	2W-DATAB, SLoadB (SB1D)	↔	2WDA_Q1	*FLEXIO4_A(PCIe x1 RXn)*	2W-DATAB, SLoadB (SB1B)	A27				
B65		GND	*GND*	GND (SB2D)	—	GND	*GND*	GND (SB2B)	A28				
B66		PERST#_Q3	*FLEXIO1_B*	ADDB, SDataInB (SB5D)	↔	PERST#_Q1	*FLEXIO1_A*	ADDB, SDataIn (SB5B)	A29		E5 (PERST#)	E5 (PERST#)	
B67		CPRESNT#_Q3	*FLEXIO2_B*	CNTRLR_TYPEB (SB6D)	↔	CPRESNT#_Q1	*FLEXIO2_A*	CNTRLR_TYPEB (SB6B)	A30				
B68		**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A31**				
B69	B57	TX14+	*PETp14*	TX14+	→	RX6+	*PERp6*	RX6+	A32	B37 (PETp6)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B70	B58	TX14-	*PETn14*	TX14-	→	RX6-	*PERn6*	RX6-	A33	B36 (PETn6)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B71	**B59**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A34**				
B72	B60	TX15+	*PETp15*	TX15+	→	RX7+	*PERp*	RX7+	A35	B40 (PETp7)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B73	B61	TX15-	*PETn15*	TX15-	→	RX7-	*PERn7*	RX7-	A36	B39 (PETn7)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B74	**B62**	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A37**				

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Table 9-1414 Multiprotocol SAS~~-4~~/ CopprLink (x16) to SAS~~-4~~/ CopprLink (x4) 1-to-4 Cables (1 of 4)

Multiprotocol SAS/ CopprLink x16 1-to-4 Cables (Sheet 1 of 4)

Root / Controller				CABLE	*Endpoint* / Backplane				*Devices on Backplane*			
CopprLink SFF-TA-1016 (148-circuit)	9402 Multi-Protocol (PCIe, SAS-4) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface			9402 Multi-Protocol (PCIe, SAS) Four of x4 Cable Interfaces	CopprLink and SAS/ SFF-8448 Signal Names		CopprLink/M-XIO SFF-TA-1016 (38-circuit)	EDSFF Connector	SFF-8639 Connector		
PCIe/ SAS	*PCIe/ SAS*	CopprLink and SAS/ SFF-8448 Signal Names			*PCIe/ SAS*	*PCIe*	SAS	*PCIe/ SAS*	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	*Endpoint*	*ROOT*	Controller	DIR	*Endpoint*	*Endpoint*	Backplane	PIN	PIN	PIN	PIN	PIN
A1	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B1**				
A2	RX0+	*PERp0*	RX0+	←	TX0+	*PETp0*	TX0+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A3	RX0-	*PERn0*	RX0-	←	TX0-	*PETn0*	TX0-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A4	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B4**				
A5	RX1+	*PERp1*	RX1+	←	TX1+	PETp1	TX1+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A6	RX1-	*PERn1*	RX1-	←	TX1-	PETn1	TX1-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A7	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B7**				
A8	BP_TYPE_Q0	*FLEXIO9_A, (3p3AUX_MGMT)*	BP_TYPE (SB7A)	↔	BP_TYPE	FLEXIO9_A, (3p3AUX_MGMT)	BP_TYPE (SB7)	B8				
A9	FLEXIO0_Q0	*FLEXIO0_A*	RESET, SDataOut (SB4A)	↔	FLEXIO0	FLEXIO0_A	RESET, SDataOut (SB4)	B9		P1 (WAKE#)	P1 (WAKE#)	
A10	GND	*GND*	GND (SB3A)	—	GND	GND	GND (SB3)	B10				
A11	RCLK_Q0p	*RCLK_Ap,REFCLK_A_Dp*	(SBA+)	→	RCLK_p	RCLK_Ap,REFCLK_A_Dp	(SBA+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A12	RCLK_Q0n	*RCLK_An,REFCLK_A_Dn*	(SBA-)	→	RCLK_n	RCLK_An,REFCLK_A_Dn	(SBA-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A13	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B13**				
A14	RX2+	*PERp2*	RX2+	←	TX2+	*PETp2*	TX2+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A15	RX2-	*PERn2*	RX2-	←	TX2-	*PETn2*	TX2-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A16	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B16**				
A17	RX3+	*PERp3*	RX3+	←	TX3+	*PETp3*	TX3+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A18	RX3-	*PERn3*	RX3-	←	TX3-	*PETn3*	TX3-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A19	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B19**				
A19	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B1**				
A20	RX4+	*PERp4*	RX4+	←	TX0+	*PETp4*	TX0+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A21	RX4-	*PERn4*	RX4-	←	TX0-	*PETn4*	TX0-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A22	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B4**				
A23	RX5+	*PERp5*	RX5+	←	TX1+	*PETp5*	TX1+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A24	RX5-	*PERn5*	RX5-	←	TX1-	*PETn5*	TX1-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A25	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B7**				
A26	BP_TYPE_Q1	*FLEXIO5_A (PCIe x1 RXp)*	BP_TYPEB (SB7B)	↔	BP_TYPE	*FLEXIO5_A (PCIe x1 TXp)*	BP_TYPE (SB7)	B8				
A27	FLEXIO0_Q1	*FLEXIO6_A (PCIe x1 RXn)*	RESETB, SDataOutB (SB4B)	↔	FLEXIO0	*FLEXIO6_A (PCIe x1 TXn)*	RESET, SDataOut (SB4)	B9		P1 (WAKE#)	P1 (WAKE#)	
A28	GND	*GND*	GND(SB3B)	—	GND	*GND*	GND (SB3)	B10				
A29	RCLK_Q1p	FLEXIO7_A (USB2p), USB2_Dp	(SBB+)	→	RCLK_p	*FLEXIO7_A (USB2p), USB2_Dp*	(SBA+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A30	RCLK_Q1n	FLEXIO8_A (USB2n), USB2_Dn	(SBB-)	→	RCLK_n	*FLEXIO8_A (USB2n), USB2_Dn*	(SBA-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A31	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B13**				
A32	RX6+	*PERp6*	RX6+	←	TX2+	*PETp6*	TX2+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A33	RX6-	*PERn6*	RX6-	←	TX2-	*PETn6*	TX2-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A34	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B16**				
A35	RX7+	*PERp7*	RX7+	←	TX3+	*PETp7*	TX3+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A36	RX7-	*PERn7*	RX7-	←	TX3-	*PETn*	TX3-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A37	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B19**				

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Table 9-~~151~~56 Multiprotocol SAS/ CopprLink (x16) to SAS/ CopprLink (x4) 1-to-4 Cables (2 of 4)

Multiprotocol SAS/ CopprLink x16 1-to-4 Cables (Sheet 2 of 4)

Root / Controller				CABLE	Endpoint / Backplane				Devices on Backplane			
CopprLink SFF-TA-1016 (148-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface			9402 Multi-Protocol (PCIe, SAS) Four of x4 Cable Interfaces	CopprLink and SAS/ SFF-8448 Signal Names		CopprLink/M-XIO SFF-TA-1016 (38-circuit)	EDSFF Connector	SFF-8639 Connector		
PCIe/ SAS	PCIe/ SAS	CopprLink and SAS/ SFF-8448 Signal Names			PCIe/ SAS	PCIe	SAS	PCIe/ SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	Endpoint	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
A38	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B1**				
A39	RX8+	*PERp8*	RX8+	←	TX0+	*PETp0*	TX0+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A40	RX8-	*PERn8*	RX8-	←	TX0-	*PETn0*	TX0-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A41	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B4**				
A42	RX9+	*PERp9*	RX9+	←	TX1+	PETp1	TX1+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A43	RX9-	*PERn9*	RX9-	←	TX1-	PETn1	TX1-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A44	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B7**				
A45	BP_TYPE_Q2	*FLEXIO9_B, (3p3AUX_MGMT)*	BP_TYPE (SB7C)	↔	BP_TYPE	*FLEXIO9_A, (3p3AUX_MGMT)*	BP_TYPE (SB7)	B8				
A46	FLEXIO0_Q2	*FLEXIO0_B*	RESET, SDataOut (SB4C)	↔	FLEXIO0	*FLEXIO0_A*	RESET, SDataOut (SB4)	B9		P1 (WAKE#)	P1 (WAKE#)	
A47	GND	*GND*	GND (SBC3)	—	GND	*GND*	GND (SB3)	B10				
A48	RCLK_Q2p	*RCLK_Bp,REFCLK_B_Dp*	(SBC+)	→	RCLK_p	*RCLK_Ap,REFCLK_A_Dp*	(SBA+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A49	RCLK_Q2n	*RCLK_Bn,REFCLK_B_Dn*	(SBC-)	→	RCLK_n	*RCLK_An,REFCLK_A_Dn*	(SBA-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A50	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B13**				
A51	RX10+	*PERp10*	RX10+	←	TX2+	*PETp2*	TX2+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A52	RX10-	*PERn10*	RX10-	←	TX2-	*PETn2*	TX2-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A53	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B16**				
A54	RX11+	*PERp11*	RX11+	←	TX3+	*PETp3*	TX3+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A55	RX11-	*PERn11*	RX11-	←	TX3-	*PETn3*	TX3-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A56	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B19**				
A56	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B1**				
A57	RX12+	*PERp12*	RX12+	←	TX0+	*PETp4*	TX0+	B2	A18 (PERp0)	E14 (PERp0)	S6 (PERp0)	S6 (TX0+)
A58	RX12-	*PERn12*	RX12-	←	TX0-	*PETn4*	TX0-	B3	A17 (PERn0)	E13 (PERn0)	S5 (PERn0)	S5 (TX0-)
A59	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B4**				
A60	RX13+	*PERp13*	RX13+	←	TX1+	*PETp5*	TX1+	B5	A21 (PERp1)	S21 (PERp1)	S13 (PERp1)	S13 (TX1+)
A61	RX13-	*PERn13*	RX13-	←	TX1-	*PETn5*	TX1-	B6	A20 (PERn1)	S20 (PERn1)	S12 (PERn1)	S12 (TX1-)
A62	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B7**				
A63	BP_TYPE_Q3	*FLEXIO5_B (PCIe x1 RXp)*	BP_TYPEB (SB7D)	↔	BP_TYPE	*FLEXIO5_A (PCIe x1 TXp)*	BP_TYPE (SB7)	B8				
A64	FLEXIO0_Q3	*FLEXIO6_B (PCIe x1 RXn)*	RESETB, SDataOutB (SB4D)	↔	FLEXIO0	*FLEXIO6_A (PCIe x1 TXn)*	RESET, SDataOut (SB4)	B9		P1 (WAKE#)	P1 (WAKE#)	
A65	GND	*GND*	GND(SB3D)	—	GND	*GND*	GND (SB3)	B10				
A66	RCLK_Q3p	FLEXIO7_B (USB2p), USB2_Dp	(SBD+)	→	RCLK_p	FLEXIO7_A (USB2p), USB2_Dp	(SBA+)	B11	B15 (REFCLKp0)	E7 (REFCLK+)	E7 (REFCLK+)	
A67	RCLK_Q3n	FLEXIO8_B (USB2n), USB2_Dn	(SBD-)	→	RCLK_n	FLEXIO8_A (USB2n), USB2_Dn	(SBA-)	B12	B14 (REFCLKn0)	E8 (REFCLK-)	E8 (REFCLK-)	
A68	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B13**				
A69	RX14+	*PERp14*	RX14+	←	TX2+	*PETp6*	TX2+	B14	A24 (PERp2)	S27 (PERp2)	S21(PERp2)	S21 (TX2+)
A70	RX14-	*PERn14*	RX14-	←	TX2-	*PETn6*	TX2-	B15	A23 (PERn2)	S26 (PERn2)	S20 (PERn2)	S20 (TX2-)
A71	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B16**				
A72	RX15+	*PERp15*	RX15+	←	TX3+	*PETp7*	TX3+	B17	A27 (PERp3)	E21 (PERp3)	S27 (PERp3)	S27 (TX3+)
A73	RX15-	*PERn15*	RX15-	←	TX3-	*PETn*	TX3-	B18	A26 (PERn3)	E20 (PERn3)	S26 (PERn3)	S26 (TX3-)
A74	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**B19**				

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Table 9-~~161~~66 Multiprotocol SAS/ CopprLink (x16) to SAS/ CopprLink (x4) 1-to-4 Cables (3 of 4)

Multiprotocol SAS/ CopprLink x16 1-to-4 Cables (Sheet 3 of 4)

Root / Controller				CABLE	Endpoint / Backplane				Devices on Backplane			
CopprLink SFF-TA-1016 (148-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface			9402 Multi-Protocol (PCIe, SAS) Four of x4 Cable Interfaces	CopprLink and SAS/ SFF-8448 Signal Names		CopprLink/M-XIO SFF-TA-1016 (38-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P SAS	PCIe/ SAS	CopprLink and SAS/ SFF-8448 Signal Names			PCIe/ SAS	PCIe	SAS	PCIe/ SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	Endpoint	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
B1	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**				
B2	TX0+	*PETp0*	TX0+	→	RX0+	*PERp0*	RX0+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B3	TX0-	*PETn0*	TX0-	→	RX0-	*PERn0*	RX0-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B4	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**				
B5	TX1+	*PETp1*	TX1+	→	RX1+	*PERp1*	RX1+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B6	TX1-	*PETn1*	TX1-	→	RX1-	*PERn1*	RX1-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B7	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**				
B8	2WCLK_Q0	*2WCL_A,SMSCL*	2W-CLK, Sclock (SB0A)	↔	2WCLK	*2WCL_A,SMSCL*	2W-CLK, SClock (SB0)	A8				
B9	2WDA_Q0	*2WDA_A,SMSDA*	2W-DATA, Sload (SB1A)	↔	2WDA	*2WDA_A,SMSDA*	2W-DATA, SLoad(SB1)	A9				
B10	GND	*GND*	GND (SB2A)	—	GND	*GND*	GND(SB2)	A10				
B11	PERST#_Q0	*PERST#_A,PERST_N*	ADD, SDataIn (SB5A)	↔	PERST#	*PERST#_A,PERST_N*	ADD, SDataIn (SB5)	A11	B10 (PERSTO#)	E5 (PERST#)	E5 (PERST#)	
B12	CPRESNT#_Q0	*PRPE_A,CBL_PRES_A_PESTI_N*	CNTRLR_TYPE (SB6A)	↔	CPRESNT#	*PRPE_A,CBL_PRES_A_PESTI_N*	CNTRLR_TYPE (SB6)	A12				
B13	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**				
B14	TX2+	*PETp2*	TX2+	→	RX2+	*PERp2*	RX2+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B15	TX2-	*PETn2*	TX2-	→	RX2-	*PERn2*	RX2-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B16	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**				
B17	TX3+	*PETp3*	TX3+	→	RX3+	*PERp3*	RX3+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B18	TX3-	*PETn3*	TX3-	→	RX3-	*PERn3*	RX3-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B19	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**				
B19	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**				
B20	TX4+	*PETp4*	TX4+	→	RX0+	*PERp4*	RX0+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B21	TX4-	*PETn4*	TX4-	→	RX0-	*PERn4*	RX0-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B22	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**				
B23	TX5+	*PETp5*	TX5+	→	RX1+	*PERp5*	RX1+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B24	TX5-	*PETn5*	TX5-	→	RX1-	*PERn5*	RX1-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B25	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**				
B26	2WCLK_Q1	*FLEXIO3_A(PCIe x1 TXp)*	2W-CLKB, SClockB (SB0B)	↔	2WCLK	*FLEXIO3_A(PCIe x1 RXp)*	2W-CLK, SClock (SB0)	A8				
B27	2WDA_Q1	*FLEXIO4_A(PCIe x1 TXn)*	2W-DATAB, SLoadB (SB1B)	↔	2WDA	*FLEXIO4_A(PCIe x1 RXn)*	2W-DATA, SLoad(SB1)	A9				
B28	GND	*GND*	GND (SB2B)	—	GND	*GND*	GND(SB2)	A10				
B29	PERST#_Q1	*FLEXIO1_A*	ADDB, SDataInB (SB5B)	↔	PERST#	*FLEXIO1_A*	ADD, SDataIn (SB5)	A11	B10 (PERSTO#)	E5 (PERST#)	E5 (PERST#)	
B30	CPRESNT#_Q1	*FLEXIO2_A*	CNTRLR_TYPEB (SB6B)	↔	CPRESNT#	*FLEXIO2_A*	CNTRLR_TYPE (SB6)	A12				
B31	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**				
B32	TX6+	*PETp6*	TX6+	→	RX2+	*PERp6*	RX2+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B33	TX6-	*PETn6*	TX6-	→	RX2-	*PERn6*	RX2-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B34	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**				
B35	TX7+	*PETp7*	TX7+	→	RX3+	*PERp*	RX3+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B36	TX7-	*PETn7*	TX7-	→	RX3-	*PERn7*	RX3-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B37	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**				

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Table 9-~~171~~176 Multiprotocol SAS/ CopprLink (x16) to SAS/ CopprLink (x4) 1-to-4 Cables (4 of 4)

Multiprotocol SAS/ CopprLink x16 1-to-4 Cables (Sheet 4 of 4)

Root / Controller				CABLE	Endpoint / Backplane				Devices on Backplane			
CopprLink SFF-TA-1016 (148-circuit)	9402 Multi-Protocol (PCIe, SAS) x16 Cable Interface	9402 Multi-Protocol (PCIe, SAS) x8 Cable Interface			9402 Multi-Protocol (PCIe, SAS) Four of x4 Cable Interfaces	CopprLink and SAS/ SFF-8448 Signal Names		CopprLink/M-XIO SFF-TA-1016 (38-circuit)	EDSFF Connector	SFF-8639 Connector		
O/P SAS	PCIe/ SAS	CopprLink and SAS/ SFF-8448 Signal Names			PCIe/ SAS	PCIe	SAS	PCIe/ SAS	SFF-TA-1009 (x8)	Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLink SAS™
PIN	Endpoint	ROOT	Controller	DIR	Endpoint	Endpoint	Backplane	PIN	PIN	PIN	PIN	PIN
B38	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**				
B39	TX8+	*PETp8*	TX8+	→	RX0+	*PERp0*	RX0+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B40	TX8-	*PETn8*	TX8-	→	RX0-	*PERn0*	RX0-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B41	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**				
B42	TX9+	*PETp9*	TX9+	→	RX1+	*PERp1*	RX1+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B43	TX9-	*PETn9*	TX9-	→	RX1-	*PERn1*	RX1-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B44	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**				
B45	2WCLK_Q2	*2WCL_B,SMSCL*	2W-CLK, Sclock (SBC)	↔	2WCLK	*2WCL_A,SMSCL*	2W-CLK, SClock (SB0)	A8				
B46	2WDA_Q2	*2WDA_B,SMSDA*	2W-DATA, Sload (SBC)	↔	2WDA	*2WDA_A,SMSDA*	2W-DATA, SLoad(SB1)	A9				
B47	GND	*GND*	GND (SB2C)	—	GND	*GND*	GND(SB2)	A10				
B48	PERST#_Q2	*PERST#_B,PERST_N*	ADD, SDataIn (SB5C)	↔	PERST#	*PERST#_A,PERST_N*	ADD, SDataIn (SB5)	A11	B10 (PERSTO#)	E5 (PERST#)	E5 (PERST#)	
B49	CPRESNT#_Q2	*PRPE_B,CBL_PRES_B_PESTI_N*	CNTRLR_TYPE (SB6C)	↔	CPRESNT#	*PRPE_A,CBL_PRES_A_PESTI_N*	CNTRLR_TYPE (SB6)	A12				
B50	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**				
B51	TX10+	*PETp10*	TX10+	→	RX2+	*PERp2*	RX2+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B52	TX10-	*PETn10*	TX10-	→	RX2-	*PERn2*	RX2-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B53	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**				
B54	TX11+	*PETp11*	TX11+	→	RX3+	*PERp3*	RX3+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B55	TX11-	*PETn11*	TX11-	→	RX3-	*PERn3*	RX3-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B56	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**				
B56	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A1**				
B57	TX12+	*PETp12*	TX12+	→	RX0+	*PERp4*	RX0+	A2	B18 (PETp0)	E10 (PETp0)	S2 (PETp0)	S2 (RX0+)
B58	TX12-	*PETn12*	TX12-	→	RX0-	*PERn4*	RX0-	A3	B17 (PETn0)	E11 (PETn0)	S3 (PETn0)	S3 (RX0-)
B59	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A4**				
B60	TX13+	*PETp13*	TX13+	→	RX1+	*PERp5*	RX1+	A5	B21 (PETp1)	S17 (PETp1)	S9 (PETp1)	S9 (RX1+)
B61	TX13-	*PETn13*	TX13-	→	RX1-	*PERn5*	RX1-	A6	B20 (PETn1)	S18 (PETn1)	S10 (PETn1)	S10 (RX1-)
B62	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A7**				
B63	2WCLK_Q3	*FLEXIO3_B(PCIe x1 TXp)*	2W-CLKB, SClockB (SB0D)	↔	2WCLK	*FLEXIO3_A(PCIe x1 RXp)*	2W-CLK, SClock (SB0)	A8				
B64	2WDA_Q3	*FLEXIO4_B(PCIe x1 TXn)*	2W-DATAB, SLoadB (SB1D)	↔	2WDA	*FLEXIO4_A(PCIe x1 RXn)*	2W-DATA, SLoad(SB1)	A9				
B65	GND	*GND*	GND (SB2D)	—	GND	*GND*	GND(SB2)	A10				
B66	PERST#_Q3	*FLEXIO1_B*	ADDB, SDataInB (SB5D)	↔	PERST#	*FLEXIO1_A*	ADD, SDataIn (SB5)	A11	B10 (PERSTO#)	E5 (PERST#)	E5 (PERST#)	
B67	CPRESNT#_Q3	*FLEXIO2_B*	CNTRLR_TYPEB (SB6D)	↔	CPRESNT#	*FLEXIO2_A*	CNTRLR_TYPE (SB6)	A12				
B68	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A13**				
B69	TX14+	*PETp14*	TX14+	→	RX2+	*PERp6*	RX2+	A14	B24 (PETp2)	S23 (PETp2)	S17 (PETp2)	S17 (RX2+)
B70	TX14-	*PETn14*	TX14-	→	RX2-	*PERn6*	RX2-	A15	B23 (PETn2)	S24 (PETn2)	S18 (PETn2)	S18 (RX2-)
B71	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A16**				
B72	TX15+	*PETp15*	TX15+	→	RX3+	*PERp*	RX3+	A17	B27 (PETp3)	E17 (PETp3)	S23 (PETp3)	S23 (RX3+)
B73	TX15-	*PETn15*	TX15-	→	RX3-	*PERn7*	RX3-	A18	B26 (PETn3)	E18 (PETn3)	S24 (PETn3)	S24 (RX3-)
B74	**GROUND**	**GROUND**	**GROUND**	—	**GROUND**	**GROUND**	**GROUND**	**A19**				

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Table 9-1815 Multiprotocol SAS-4/ CopprLink/ M-XIO and UBM Sideband Table (1 of 1)

SFF-9402 Sideband Name	SAS / PCIe Sideband Name	SFF-9402 Mutliprotocol Sideband Signal Assignments Only (Sheet 1 of 1)													
		Multiprotocol Sideband Signal Assignments								Root/ Controller			Endpoint/ Backplane		
		SFF- 9402 Interface for Multiprotocol (SAS/ PCIe OCuLink / Other Protocol) Root/ Controller (x4) to Endpoint/ Backplane (x4) Cables					SFF-TA-1016 for PCIe		SFF-9404 Generalized Name	SFF-8654 (74-circuit)	SFF-TA-1016 (148-circuit)	CABLE	SFF-8654 (74-circuit)	SFF-TA-1016 (148-circuit)
		SAS SIDE BANDS	SGPIO (SFF-8485) SFF-8448	Standard 2-Wire Type SFF-8448	PCIe OCuLink	Other 2-Wire Type SFF-8448	UBM SFF-TA-1005	CopprLink	M-XIO	SFF-9402	PCIe/SAS	PCIe/SAS		PCIe/SAS	PCIe/SAS
		NAME	*Signal Name*	*Signal Name*	*Signal Name*	*Signal Name*	*Signal Name*	*Signal Name*	*Signal Name*	*Signal Name*	PIN	PIN	DIR	PIN	PIN
Quad0	SAS Quad A / PCIe/M-XIO Baseline A	SB7	BP_TYPE	BP_TYPE	BP_TYPE/ VSP	BP_TYPE/ VSP	BP_TYPE	FLEXIO9_A	3p3AUX_MGMT	BP_TYPE_Q0	A8	A8	↔	B8	B8
		SB4	SDataOut	RESET	*CWAKE#/ OBFF*	VSP	2W_RST#	FLEXIO0_A	FLEXIO0_A	FLEXIO0_Q0	A9	A9	↔	B9	B9
		SB3	GND	GND	GND	VSP	GND	GND	GND	GND	A10	A10	—	B10	B10
		SB+	(SB+)	(SB+)	VSP(+)	VSP+	(SB+)	RCLK_Ap	REFCLK_A_Dp	RCLK_Q0p	A11	A11	→	B11	B11
		SB-	(SB-)	(SB-)	VSP(-)	VSP-	(SB-)	RCLK_An	REFCLK_A_Dn	RCLK_Q0n	A12	A12	→	B12	B12
		SB0	SClock	2W-CLK	2W-CLK	2W-CLK	2W-CLK	2WCLK_A	SMSCL_A	2WCLK_Q0	B8	B8	↔	A8	A8
		SB1	SLoad	2W-DATA	2W-DATA	2W-DATA	2W-DATA	2WDA_A	SMSDA_A	2WDA_Q0	B9	B9	↔	A9	A9
		SB2	GND	GND	GND	GND	GND	GND	GND	GND	B10	B10	—	A10	A10
		SB5	SDataIn	ADD	PERST#	VSP	PERST#	PERST#_A	PERST_A_N	PERST#_Q0	B11	B11	↔	A11	A11
		SB6	CNTRLR_TYPE	CNTRLR_TYPE	CPRSNT#	VSP	CHG_DETECT#/ CPRSNT#	PRPE_A	CBL_PRES_A_PESTI_A_N	CPRESNT#_Q0	B12	B12	↔	A12	A12
Quad1	SAS Quad B / PCIe/M-XIO Extended A	SB7	BP_TYPE	BP_TYPE	BP_TYPE/ VSP	BP_TYPE/ VSP	BP_TYPE	FLEXIO5_A (PCIe x1 RXp)	FLEXIO5_A	BP_TYPE_Q1	A26	A26	↔	B26	B26
		SB4	SDataOut	RESET	*CWAKE#/ OBFF*	VSP	2W_RST#	FLEXIO6_A (PCIe x1 RXn)	FLEXIO6_A	FLEXIO0_Q1	A27	A27	↔	B27	B27
		SB3	GND	GND	GND	VSP	GND	GND	GND	GND	A28	A28	—	B28	B28
		SB+	(SB+)	(SB+)	VSP(+)	VSP+	(SB+)	FLEXIO7_A (USB2p)	USB2_A_Dp	RCLK_Q1p	A29	A29	→	B29	B29
		SB-	(SB-)	(SB-)	VSP(-)	VSP-	(SB-)	FLEXIO8_A (USB2n)	USB2_A_Dn	RCLK_Q1n	A30	A30	→	B30	B30
		SB0	SClock	2W-CLK	2W-CLK	2W-CLK	2W-CLK	FLEXIO3_A (PCIe x1 TXp)	FLEXIO3_A	2WCLK_Q1	B26	B26	↔	A26	A26
		SB1	SLoad	2W-DATA	2W-DATA	2W-DATA	2W-DATA	FLEXIO4_A (PCIe x1 TXn)	FLEXIO4_A	2WDA_Q1	B27	B27	↔	A27	A27
		SB2	GND	GND	GND	GND	GND	GND	GND	GND	B28	B28	—	A28	A28
		SB5	SDataIn	ADD	PERST#	VSP	PERST#	FLEXIO1_A	FLEXIO1_A	PERST#_Q1	B29	B29	↔	A29	A29
		SB6	CNTRLR_TYPE	CNTRLR_TYPE	CPRSNT#	VSP	CHG_DETECT#/ CPRSNT#	FLEXIO2_A	FLEXIO2_A	CPRESNT#_Q1	B30	B30	↔	A30	A30
Quad2	SAS Quad C / PCIe/M-XIO Baseline B	SB7	BP_TYPE	BP_TYPE	BP_TYPE/ VSP	BP_TYPE/ VSP	BP_TYPE	FLEXIO9_B	3p3AUX_MGMT	BP_TYPE_Q2		A45	↔		B45
		SB4	SDataOut	RESET	*CWAKE#/ OBFF*	VSP	2W_RST#	FLEXIO0_B	FLEXIO0_B	FLEXIO0_Q2		A46	↔		B46
		SB3	GND	GND	GND	VSP	GND	GND	GND	GND		A47	—		B47
		SB+	(SB+)	(SB+)	VSP(+)	VSP+	(SB+)	RCLK_Bp	REFCLK_B_Dp	RCLK_Q2p		A48	→		B48
		SB-	(SB-)	(SB-)	VSP(-)	VSP-	(SB-)	RCLK_Bn	REFCLK_B_Dn	RCLK_Q2n		A49	→		B49
		SB0	SClock	2W-CLK	2W-CLK	2W-CLK	2W-CLK	2WCLK_B	SMSCL_B	2WCLK_Q2		B45	↔		A45
		SB1	SLoad	2W-DATA	2W-DATA	2W-DATA	2W-DATA	2WDA_B	SMSDA_B	2WDA_Q2		B46	↔		A46
		SB2	GND	GND	GND	GND	GND	GND	GND	GND		B47	—		A47
		SB5	SDataIn	ADD	PERST#	VSP	PERST#	PERST#_B	PERST_B_N	PERST#_Q2		B48	↔		A48
		SB6	CNTRLR_TYPE	CNTRLR_TYPE	CPRSNT#	VSP	CHG_DETECT#/ CPRSNT#	PRPE_B	CBL_PRES_B_PESTI_B_N	CPRESNT#_Q2		B49	↔		A49
Quad3	SAS Quad D / PCIe/M-XIO Extended B	SB7	BP_TYPE	BP_TYPE	BP_TYPE/ VSP	BP_TYPE/ VSP	BP_TYPE	FLEXIO5_B (PCIe x1 RXp)	FLEXIO5_B	BP_TYPE_Q3		A63	↔		B63
		SB4	SDataOut	RESET	*CWAKE#/ OBFF*	VSP	2W_RST#	FLEXIO6_B (PCIe x1 RXn)	FLEXIO6_B	FLEXIO0_Q3		A64	↔		B64
		SB3	GND	GND	GND	VSP	GND	GND	GND	GND		A65	—		B65
		SB+	(SB+)	(SB+)	VSP(+)	VSP+	(SB+)	FLEXIO7_B (USB2p)	USB2_B_Dp	RCLK_Q3p		A66	→		B66
		SB-	(SB-)	(SB-)	VSP(-)	VSP-	(SB-)	FLEXIO8_B (USB2n)	USB2_B_Dn	RCLK_Q3n		A67	→		B67
		SB0	SClock	2W-CLK	2W-CLK	2W-CLK	2W-CLK	FLEXIO3_B (PCIe x1 TXp)	FLEXIO3_B	2WCLK_Q3		B63	↔		A63
		SB1	SLoad	2W-DATA	2W-DATA	2W-DATA	2W-DATA	FLEXIO4_B (PCIe x1 TXn)	FLEXIO4_B	2WDA_Q3		B64	↔		A64
		SB2	GND	GND	GND	GND	GND	GND	GND	GND		B65	—		A65
		SB5	SDataIn	ADD	PERST#	VSP	PERST#	FLEXIO1_B	FLEXIO1_B	PERST#_Q3		B66	↔		A66
		SB6	CNTRLR_TYPE	CNTRLR_TYPE	CPRSNT#	VSP	CHG_DETECT#/ CPRSNT#	FLEXIO2_B	FLEXIO2_B	CPRESNT#_Q3		B67	↔		A67

Note: All the highspeed connections shown in Table 6-1~~Table 6-1~~Table 9-1 through Table 6-5~~Table 6-5~~Table 9-5 are common and independent

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10. CopprLink / ~~M-XIO~~ / SFF-TA-1045 Cables

Will be delayed until next release. .

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