SFF-9400

Specification for

Universal 4/8X Pinouts

Rev 1.1 January 19, 2026

SECRETARIAT: SFF TWG

This specification is made available for public review at https://www.snia.org/sff/specifications. Comments may be submitted at https://www.snia.org/feedback. Comments received will be considered for inclusion in future revisions of this specification.

This document has been released by SNIA. The SFF TWG believes that the ideas, methodologies, and technologies described in this document are technically accurate and are appropriate for widespread distribution.

The description in this specification does not assure that the specific component is available from suppliers. If such a component is supplied, it should comply with this specification to achieve interoperability between suppliers.

ABSTRACT: This specification outlines a set of connector pin signal definitions for an internal cable interface. The definitions are not functionally compatible but do prevent physical damage. Possible applications include, but are not limited to, SAS-3, SAS-4, and PCI Express® (PCIe®).

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FOREWORD

The development work on this specification was done by the SNIA SFF TWG, an industry group. Since its formation as the SFF Committee in August 1990, as well as since SFF's transition to SNIA in 2016, the membership has included a mix of companies which are leaders across the industry.

For those who wish to participate in the activities of the SFF TWG, the signup for membership can be found at https://www.snia.org/join.

REVISION HISTORY

Rev 0.2

-No change history information available before this release

Rev 1.0 *July 18, 2018*:

- Upgraded to SNIA template format
- Changed header from "Reference Guide" to "Published"
- Added "Reference" watermark
- Removed Section 1.1 Application Specific Criteria
- Added references
- Minor editorial changes

Rev 1.1 *January 19, 2026*:

- Converted document using the latest specification template
- Pulled out the Intellectual Property section since this is a reference document
- Fixed error reference in table of contents
- Added reference for PCI-SIG CopprLink internal and OCuLink specifications
- Fixed description in Sections 3.2, 3.3, 3.5, and 3.6 to align with their respective figures
- Other minor editorial

CONTENTS

FIGURES

1. Scope

This reference guide outlines a set of connector pin signal definitions for a two-row internal cable connector interface. The definitions are not functionally compatible but do prevent physical damage when two different pinout options are mated. Possible applications include, but are not limited to, SAS and PCIe. The intent is to facilitate greater flexibility and increased usage.

2. References and Conventions

2.1 Industry Documents

The following documents are relevant to this specification:

- INCITS 519 Serial Attached SCSI 3 (SAS-3)
- INCITS 534 Serial Attached SCSI 3 (SAS-4)
- PCI Express OCuLink Specification
- CopprLink Internal Cable Specification for PCI Express 5.0 and 6.0

2.2 Sources

The complete list of SFF documents which have been published, are currently being worked on, or that have been expired by the SFF Committee can be found at https://www.snia.org/sff/specifications. Suggestions for improvement of this specification are welcome and should be submitted to https://www.snia.org/feedback.

Other standards may be obtained from the organizations listed below:

Standard	Organization	Website
SAS and other ANSI standards	InterNational Committee for Information Technology Standards (INCITS)	https://www.incits.org
PCIe	PCI-SIG	https://www.pcisig.com/specifications

2.3 Conventions

The following conventions are used throughout this document:

DEFINITIONS: Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions or in the text where they first appear.

ORDER OF PRECEDENCE: If a conflict arises between text, tables, or figures, the order of precedence to resolve the conflicts is text; then tables; and finally figures. Not all tables or figures are fully described in the text. Tables show data format and values.

LISTS: Lists sequenced by lowercase or uppercase letters show no ordering relationship between the listed items.

EXAMPLE 1 - The following list shows no relationship between the named items:

a. red (i.e., one of the following colors):
    A. crimson; or
    B. pink;
b. blue; or
c. green.

Lists sequenced by numbers show an ordering relationship between the listed items.

EXAMPLE 2 -The following list shows an ordered relationship between the named items:

1. top;
2. middle; and
3. bottom.

Lists are associated with an introductory paragraph or phrase and are numbered relative to that paragraph or phrase (i.e., all lists begin with an a. or 1. entry).

DIMENSIONING CONVENTIONS: The dimensioning conventions are described in ASME-Y14.5, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

NUMBERING CONVENTIONS: The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point). This is equivalent to the English/American convention of a comma and a period.

American	**French**	**ISO**
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

3. Keywords, Acronyms, and Definitions

For the purposes of this document, the following keywords, acronyms, and definitions apply.

3.1 Keywords

May: Indicates flexibility of choice with no implied preference.

May or may not: Indicates flexibility of choice with no implied preference.

Obsolete: Indicates that an item was defined in prior specifications but has been removed from this specification.

Optional: Describes features which are not required by the SFF specification. However, if any feature defined by the SFF specification is implemented, it shall be implemented as defined by the specification. Describing a feature as optional in the text is an informational callout to assist the reader.

Prohibited: Describes a feature, function, or coded value that is defined in a referenced specification to which this SFF specification makes a reference, where the use of said feature, function, or coded value is not allowed for implementations of this specification.

Reserved: Where the term is used for a signal on a connector contact, the function is set aside for future standardization. It is not available for vendor specific use. Where this term is used for bits, bytes, fields, and code values; the bits, bytes, fields, and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

Restricted: Refers to features, bits, bytes, words, and fields that are set aside for other standardization purposes. If the context of the specification applies to the restricted designation, then the restricted bit, byte, word, or field shall be treated as a value whose definition is not in scope of this document, and is not interpreted by this specification.

Shall: Indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this specification.

Should: Indicates flexibility of choice with a strongly preferred alternative.

Vendor specific: Indicates something (e.g., a bit, field, code value) that is not defined by this specification. Specification of the referenced item is determined by the manufacturer and may be used differently in various implementations.

3.2 Acronyms and Abbreviations

GND: Signal return pin sometimes referred to as a ground
HS: High speed differential pair signal pin
SB: Sideband signal pin

3.3 Definitions

There are no unique definitions in this document.

4. General Description

Both 4X and 8X pinouts include a combination of high-speed differential pairs and vendor specific signals. Figure 4-1 and Figure 4-2 illustrate the location of vendor specific pins for 4X and 8X connector pinouts respectively. Each vendor specific block consists of ten pins.

Figure 4-1: Location of Vendor Specific Pins in a 4X Pinout

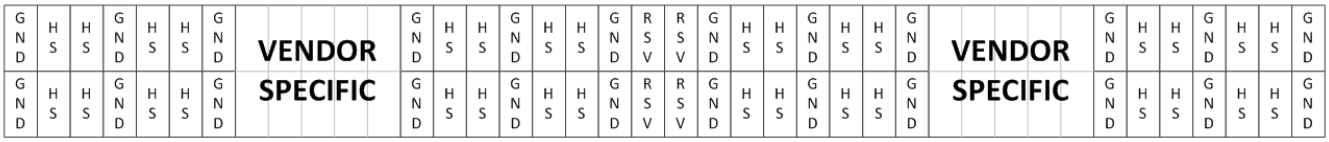

Figure 4-2: Location of Vendor Specific Pins in 8X Pinout

4.1 Type 1 4X pinout

The Type 1 4X Pinout assigns all vendor specific pins as discrete sideband signals as shown in Figure 4-3.

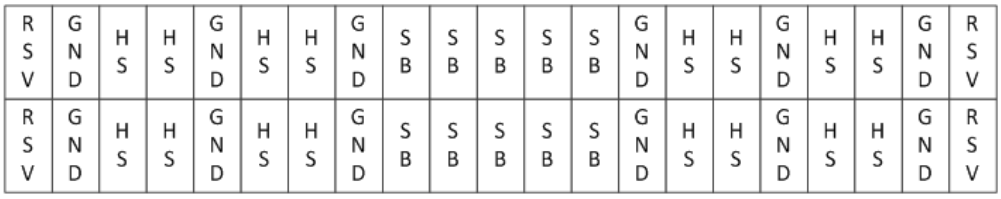

Figure 4-3: Type 1 4X pinout

4.2 Type 2 4X pinout

The Type 2 4X Pinout assigns four vendor specific pins as discrete sideband signals, two signals as grounds, and four signals for two additional high-speed differential pairs as shown in Figure 4-4.

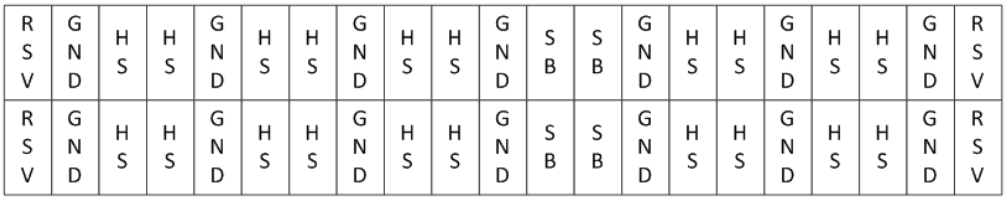

Figure 4-4: Type 2 4X Pinout

4.3 Type 3 4X Pinout

The Type 3 4X Pinout assigns all vendor specific pins for high-speed differential pairs and grounds as shown in Figure 4-5.

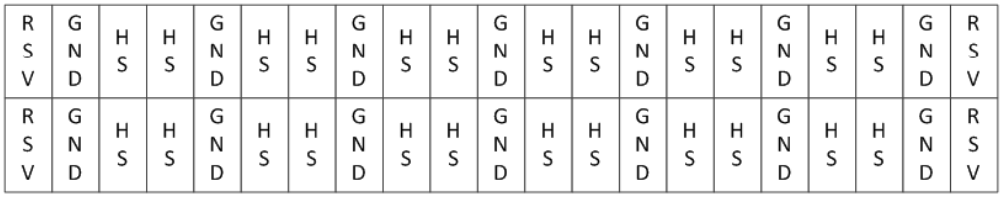

Figure 4-5: Type 3 4X Pinout

4.4 Type 1 8X Pinout

The Type 1 8X Pinout assigns all vendor specific pins as discrete sideband signals as shown in Figure 4-6.

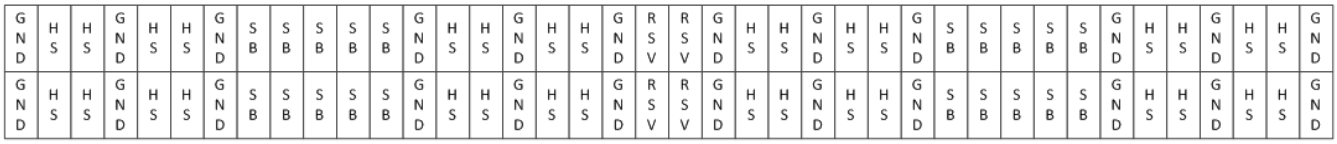

Figure 4-6: Type 1 8X Pinout

4.5 Type 2 8X Pinout

The Type 2 8X Pinout assigns eight vendor specific pins as discrete sideband signals, 4 grounds, and eight signals for four additional high-speed differential pairs as shown in Figure 4-7.

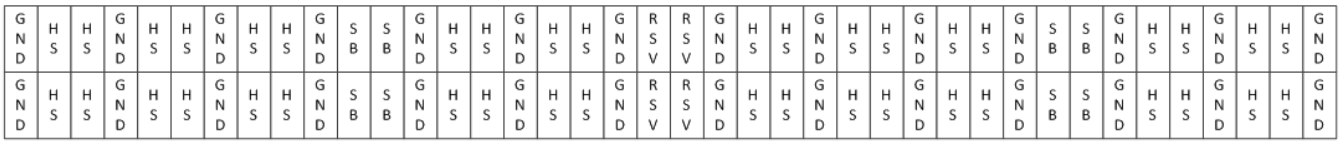

Figure 4-7: Type 2 8X Pinout

4.6 Type 3 8X Pinout

The Type 3 8X Pinout assigns all vendor specific pins for high-speed differential pairs and grounds as shown in Figure 4-8.

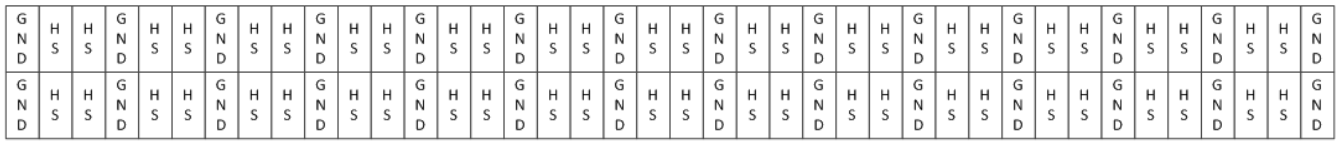

Figure 4-8: Type 3 8X Pinout