SFF specifications are available at http://www.snia.org/sff/specifications
or ftp://ftp.seagate.com/sff

This specification was developed by the SFF Committee prior to it becoming the SFF TA (Technology Affiliate) TWG (Technical Working Group) of SNIA (Storage Networking Industry Association).

The information below should be used instead of the equivalent herein.

POINTS OF CONTACT:

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If you are interested in participating in the activities of the SFF TWG, the membership application can be found at:
http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on can be found at:
http://www.snia.org/sff/specifications/SFF-8000.TXT

The operations which complement the SNIA's TWG Policies & Procedures to guide the SFF TWG can be found at:
http://www.snia.org/sff/specifications/SFF-8032.PDF

Suggestions for improvement of this specification will be welcome, they should be submitted to:
http://www.snia.org/feedback

SFF Committee documentation may be purchased in electronic form.
SFF specifications are available at ftp://ftp.seagate.com/sff.

SFF Committee

SFF-8485 Specification for Serial GPIO (SGPIO) Bus

Revision 0.7
1 February 2006

Secretariat: SFF Committee

Abstract: This document defines a Serial GPIO bus to be used in conjunction with Serial Attached SCSI (SAS) or Serial ATA (SATA).

This specification provides a common definition for systems manufacturers, system integrators, and suppliers. This is an internal working specification of the SFF Committee, an industry ad hoc group.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this document.

Support: This document is supported by the identified member companies of the SFF Committee.

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EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification:

Adaptec
Broadcom
Comax
EMC
ENDL
FCI
Foxconn
Fujitsu CPA
Hewlett Packard
Hitachi GST
LSI Logic
Molex
Sun Microsystems

The following SFF member companies voted no on the technical content of this industry specification:

Dell

The following member companies of the SFF Committee voted to abstain on this industry specification:

Amphenol
Emulex
Infineon
Intel
Seagate
Toshiba America
Tyco AMP
Unisys
Vitesse Semiconductor

REVISION HISTORY

R.1 Revision 0.1 (25 September 2003)

Initial version released to a few companies.

R.2 Revision 0.2 (2 October 2003)

Major cleanup to electricals and timing. Maximum frequency is 100 kHz. All signals are open-drain. Still need to decide where the interoperability point(s) is/are. The physical layer section is still very much subject to change. First release through SFF.

R.3 Revision 0.3 (25 January 2004)

Added a large minimum hold time so very slow receivers have a long time to sample the data. New: min 4400, max none, old: min 0, max 345.

Reduced the setup time from 250 ns to 200 ns.

Removed the minimum rise and fall times.

Reduced the minimum fall time from 300 ns to 20 ns. This is the actively driven edge. 20 ns should be plenty of time even with a 100 pF load.

Changed high level from 4700 ns to 4400 ns; low from 4000 ns to 4700 ns. The low period should be longer to allow more after the falling edge where a receiver can sample data.

Removed separate transmit and receive versions of the high and low levels. Assume everything is slow enough that the interconnect need not be treated as a transmission line.

Corrected text on active bit polarity. 1 = LED on, 0 = LED off. Whether 1 means active or inactive is not mandated (though the SAS READY LED convention is recommended).

Removed maximum hysteresis.

Removed “constant frequency” requirement.

Added advice about HBAs with more than 4 ports. Added brief discussion of backplane usage (where the bit stream from an expander is longer than 4).

Added notes about expected change to the port multiplier bit stream.

R.4 Revision 0.4 (25 May 2004)

Made SDataIn optional per request from John Lee at Intel (john.p.lee@intel.com).

Made the minimum bit stream length be four full drives, rather than 2 1/3 drives (the first bit position of the third drive). The target must still be prepared for a new SLoad at any time (the initiator might have been reset) but the usual dword stream should be a decent size.

Added advice to stop SClock low if the SGPIO initiator is still present, so targets can tell if the initiator is still present.

Reordered the chapters: 6) Physical, 7) Protocol, 8) Programming interface.

Added a SMP function programming interface. This could stand as its own SFF document; for now, it is proposed here.

R.5 Revision 0.5 (3 February 2005)

In the passive interconnect characteristics table, removed “Impedance R_B” with a range of 45 ohm to 55 ohm.

In the transmitter and receiver electrical characteristics table, changed “source impedance while driving low level R_S” with a range of 45 ohm to 55 ohm into “Output current while driving low level I_{OL}” with a range of 3 mA to 20 mA.

Reduced reset timeout for target detecting SClock, SLoad, and SDataOut set to 1 to 64 ms from 2 s. Removed SDataIn from the list (it only cares about signals from the SGPIO initiator when timing out the initiator).

Added a maximum period (minimum frequency) for SClock of 31.25 ms (32 Hz).

Changed recommended default for FORCE ACTIVITY OFF from 1/2 sec to 1/8 sec.

Changed recommended default for MAXIMUM ACTIVITY ON from 2 sec to 1/2 sec.

Changed recommended default for STRETCH ON to 1/64th.

Added more description of how MAXIMUM ACTIVITY ON, FORCE ACTIVITY OFF, and STRETCH OFF interact.

Added warning note about toggling LEDs in unison.

Corrected COUNT description in the GPIO_TX_GP_CFG register.

Added that during normal mode (in the register descriptions), the SLoad pattern is 0000b.

Updated PCI-E SIOM pin names and signal assignments to match those chosen SIOM revision 0.7 and 0.9.

Added “Suggested SGPIO usage model” chapter showing how the vendor-specific fields may be used.

Added these rules previously describing SClock to also describe SLoad: “When not using the SGPIO bus (e.g., during a reset), the initiator shall set SLoad to 1 (i.e., tristate it). When using the SGPIO bus but purposely not exchanging a bit stream, the initiator should set SLoad to 0. This lets the target know that the initiator is still present and has not been removed.”

Added this rule previously describing SClock to also describe SDataOut: “When not using the SGPIO bus (e.g., during a reset), the initiator shall set SDataOut to 1 (i.e., tristate it). support the corresponding drive number.”

R.6 Revision 0.6 (10 October 2005)

Made wording more consistent for the terms: “LED” vs. “indicator”, “assert” vs. “turn on” vs. “enable”.

Renamed STRETCH OFF field to STRETCH ACTIVITY OFF and STRETCH ON field to STRETCH ACTIVITY ON.

Based on Dell comment, deleted “(informative)” from chapter 9. The pin assignments for SGPIO on the various interfaces are normative. Added “(informative)” to chapter 10 to emphasize that the suggested SPIO usage is optional.

Changed SATA CABCON references to SATA 2.5 and updated the web site link to http://www.sata-io.org.

Changed PCI Express Server IO Module references to PCI Express ExpressModule (the final name chosen).

R.7 Revision 0.7 (1 February 2006)

Updated to reflect Published status.

FOREWORD

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see http://www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:

http://www.sffcommittee.com/ie/join.html

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:

ftp://ftp.seagate.com/sff/SFF-8032.TXT

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

1 Scope

This document defines a Serial General Purpose Input Output (SGPIO) bus used in conjunction with Serial Attached SCSI (SAS) and Serial ATA (SATA).

1.1 Description of Clauses

Clause 1 (Scope) contains the Scope.

Clause 2 (References) contains Referenced and Related Standards and SFF Specifications.

Clause 3 (General Description) contains a general description.

Clause 4 (Definitions and Conventions) contains definitions and conventions.

Clause 5 (Overview) contains the overview.

Clause 6 (Physical layer) defines the physical layer.

Clause 7 (Protocol layer) defines the protocol.

Clause 8 (Programming interface) defines the programming interface.

Clause 9 (Applications) defines applications where SGPIO is used (SAS, SATA, and PCI Express).

Clause 10 (Suggested SGPIO usage (informative)) defines a usage model for the vendor-specific SDataOut and SDataIn bits.

2 References

2.1 Industry Documents

The following interface standards are relevant to this specification:

EIA/JEDEC JESD8-B *Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits (LVTTL)*. See http://www.jedec.org.

IISO/IEC 14776-150 *Serial Attached SCSI (SAS) standard* (ANSI INCITS 376-2003). See http://www.iso.int, http://www.ansi.org, or http://www.incits.org (developed by T10 at http://www.t10.org).

ISO/IEC 14776-151 *Serial Attached SCSI 1.1 (SAS-1.1) standard* (ANSI INCITS 417-2006). See http://www.iso.int, http://www.ansi.org, or http://www.incits.org (developed by T10 at http://www.t10.org).

PCI Express ExpressModule Electromechanical Specification (PCI-EM) Revision 1.0. See http://www.pcisig.com.

Serial ATA (SATA) Revision 2.5. See http://www.sata-io.org.

2.2 SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at ftp://ftp.seagate.com/sff/SFF-8000.TXT.

2.3 Sources

Those who join the SFF Committee as an Observer or Member receive electronic copies of the minutes and SFF specifications (http://www.sffcommittee.com/ie/join.html).

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://tinyurl.com/c4psg).

Copies of SFF, ASC T10 (SCSI), T11 (Fibre Channel) and T13 (ATA) standards and standards still in development are available on the HPE version of CD_Access (http://tinyurl.com/85fts).

3 General Description

The environment for this SFF Specification includes any SAS or SATA disk cabinet.

4 Definitions and Conventions

4.1 Definitions

For the purpose of SFF Specifications, the following definitions apply:

4.1.1 optional: This term describes features which are not required by the SFF Specification. However, if any feature defined by the SFF Specification is implemented, it shall be done in the same way as defined by the Specification.

4.1.2 reserved: Where this term is used for bits, bytes, fields and code values; the bits, bytes, fields and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

4.1.3 vendor specific: This term is used to describe bits, bytes, fields, pins, signals, code values and features which are not described in this SFF Specification, and may be used in a way that varies between vendors.

4.2 Conventions

If there is a conflict between text and tables on a feature described as optional, the table shall be accepted as being correct.

A number of conditions, commands, sequence parameters, events, English text, states or similar terms are printed with the first letter of each word in uppercase and the rest lower-case; e.g., In, Out, Request Status. Any lower-case uses of these words have the normal American-English meaning.

The ISO convention of numbering is used (i.e., the thousands and higher multiples are separated by a space and a comma is used as the decimal point). Table 1 shows a comparison of the ISO and American numbering conventions.

Table 1 — ISO and American numbering conventions

ISO	American
0,6	0.6
3,141 592 65	3.14159265
1 000	1,000
1 323 462,95	1,323,462.95

5 Overview

Serial General Purpose Input Output (SGPIO) is a method to serialize general purpose IO signals. SGPIO defines the communication between an initiator (e.g. a host bus adapter) and a target (e.g. a backplane holding disk drives). The target typically converts the output signals into multiple parallel LED signals and provides the input signals from general purpose inputs.

Both the initiator and the target may be composed of one or multiple chips. If multiple chips are used, they shall coordinate driving the bus signals to maintain compliance with this standard.

Figure 1 depicts the SGPIO bus.

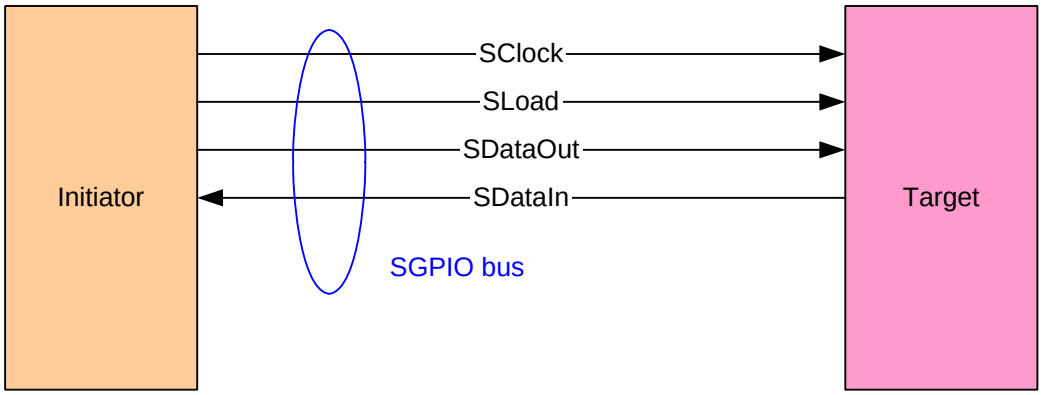


Figure 1 — SGPIO bus overview

Table 2 describes the signals used by SGPIO. All transmitters are open-drain.

Table 2 — SGPIO signals

Signal	Transmitter	Description
SClock	Initiator	Clock signal.
SLoad	Initiator	Last clock of a bit stream; begin a new bit stream on the next clock.
SDataOut	Initiator	Serial data output bit stream.
SDataIn	Target	Serial data input bit stream. SDataIn may not be supported by all SGPIO devices.

SGPIO typically accompanies a set of high-speed serial storage interfaces like SAS or SATA on a wide connector (e.g., an internal 4-wide connector). The data bits exchanged are related to drives supported by the target and are typically related to specific lanes of the high-speed serial storage interface.

Figure 2 shows SGPIO being used in conjunction with SAS or SATA, where each physical link is attached to a single disk drive.

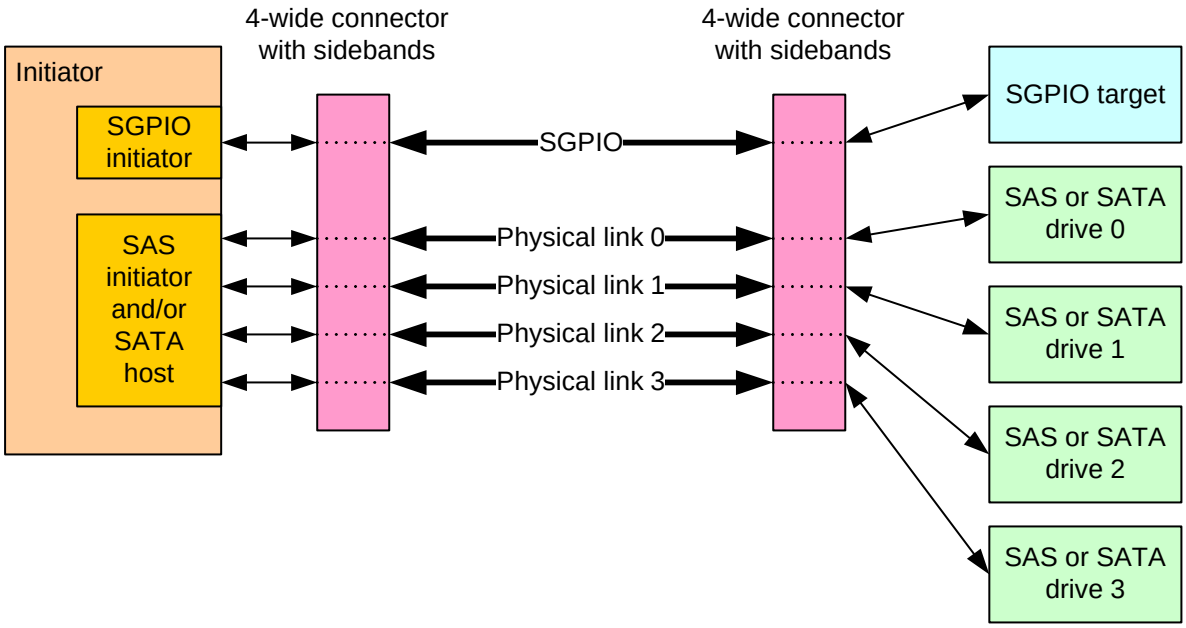


Figure 2 — SGPIO and SAS/SATA simple usage

Figure 3 shows SGPIO being used in conjunction with SAS or SATA, where some physical links are attached to SATA port multipliers, supporting multiple disk drives behind those physical links.

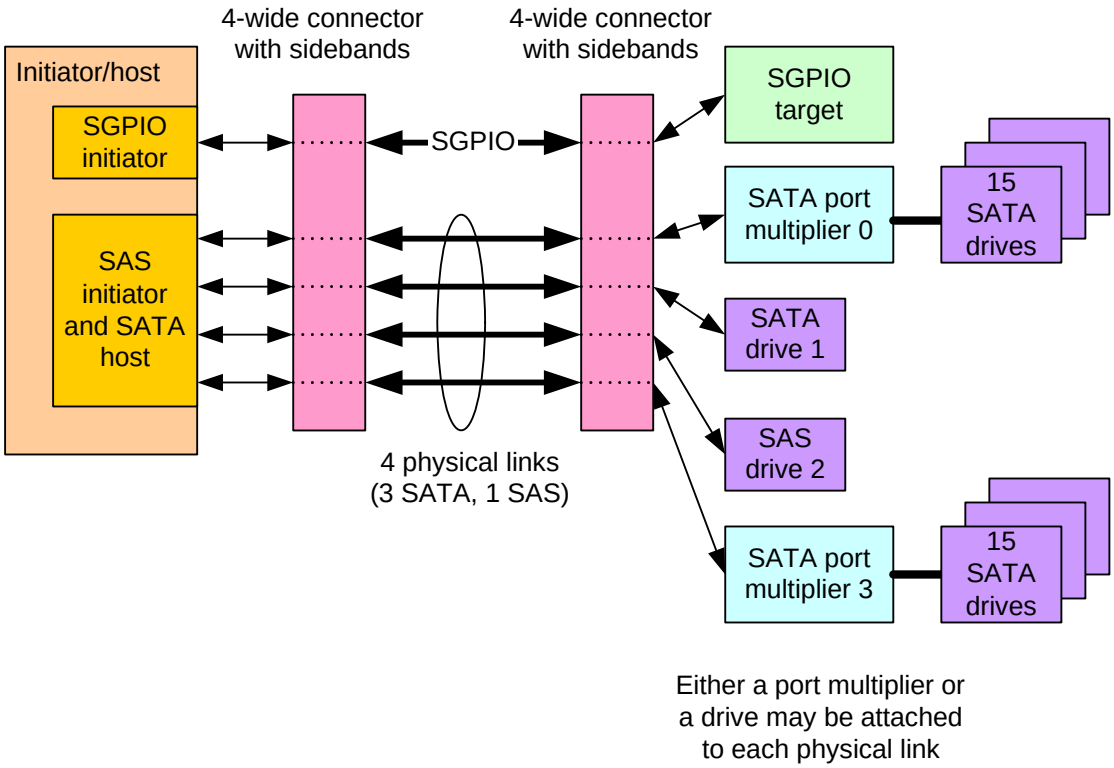


Figure 3 — SGPIO and SATA port multiplier usage

6 Physical layer

6.1 Passive interconnect

Table 3 describes characteristics of the passive interconnect (i.e., cables, connectors, and/or backplanes) carrying SGPIO.

Table 3 — SGPIO passive interconnect characteristics

Characteristic	Name	Minimum	Maximum
Skew between SClock and SLoad, SDataOut, and SDataIn signal lines	T_{SKEW}	-	10 ns
Wire delay [a]	T_{DELAY}	-	50 ns
Capacitance of the interconnect	C_B	10 pF	100 pF

[a] The target may transmit SDataIn based on the rising edge of SClock, so the wire delay affects the setup time of SDataIn to the falling edge of SClock.

6.2 Transmitter and receiver electrical characteristics

SGPIO signaling levels shall be compatible with 3.3V LVTTL technology (see LVTTL). Table 4 describes electrical characteristics of the SGPIO transmitters and receivers.

Table 4 — SGPIO transmitter and receiver electrical characteristics

Characteristic	Name	Minimum	Maximum
Low level (0) output voltage	V_{OL}	0,0 V	0,4 V
High level (1) output voltage	V_{OH}	2,4 V	3,3 V
Output current while driving low level (0)	I_{OL}	3 mA	20 mA
Low level (0) input voltage	V_{IL}	0,0 V	0,8 V
High level (1) input voltage	V_{IH}	2,0 V	3,3 V
Hysteresis of Schmitt trigger inputs	V_{HYS}	250 mV	-
Input current with an input voltage between 330 mV and 3,24 V	I_I	-10 µA	10 µA
Capacitance for initiator	C_I	-	50 pF
Capacitance for target	C_T	-	50 pF

SGPIO transmitters shall be open-drain (i.e., sink current) to transmit a low level (0) and be high-impedance (tristate) to transmit a high level (1)).

SGPIO receivers shall be Schmitt triggered.

All signals shall include a 2 Kohm pullup to Vcc on both the initiator and target boards (i.e., parallel 2 Kohm resistors).

All signals shall be tristated after power on.

6.3 Timing requirements

Figure 4 depicts the basic input voltages and their relationship to the rise and fall times.

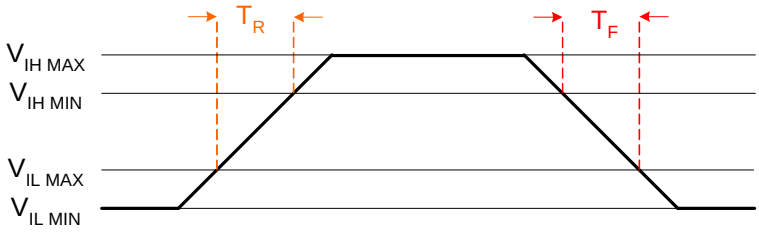


Figure 4 — Voltage and timing relationship

Figure 5 depicts the timing relationships between SClock and SLoad, SDataOut, and SDataIn at the transmitter and at the receiver.

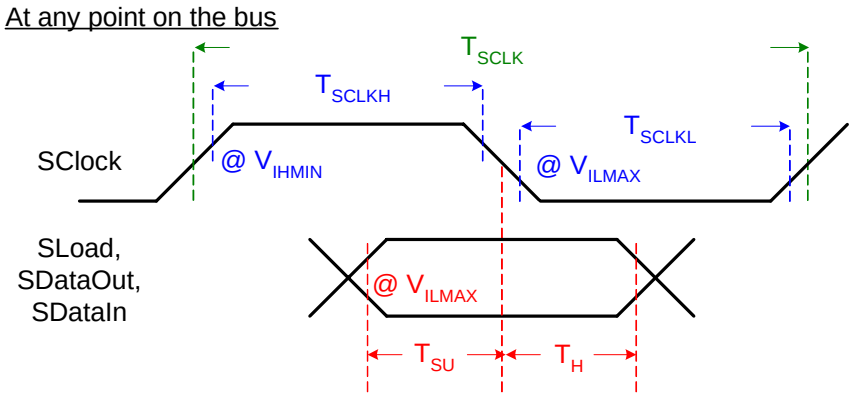


Figure 5 — Timing relationships

Table 5 describes SGPIO signal timing requirements.

Table 5 — SGPIO timing requirements

Characteristic	Name	Minimum	Maximum
SClock period (frequency)	T_{SCLK}	10 000 ns (i.e., 100 kHz)	31.25 ms (i.e., 32 Hz)
SClock high level time [c]	T_{SCLKH}	4 400 ns	none
SClock low level time [c]	T_{SCLKL}	4 700 ns	none
Rise time [c]	T_R	none	300 ns
Fall time [a] [c]	T_F	none	20 ns
Setup time to falling edge of SClock [b]	T_{SU}	200 ns	none [d]
Hold time from falling edge of SClock [b]	T_H	4 400 ns	none [e]

[a] The minimum fall time is not specified, but systems may require slope-controlled output stages, series resistors, or series ferrites.
[b] Transmitters may change SLoad, SDataOut, or SDataIn on the rising edge of SClock to meet setup and hold times on the falling edge of SClock.
[c] The high time, low time, rise time, and fall time must add up to the minimum requirement for T_{SCLK}.
[d] Although there is no maximum setup time specified, it must not interfere with the minimum hold time for the preceding falling edge.
[e] Although there is no maximum hold time specified, it must not interfere with the minimum setup time for the following falling edge.

7 Protocol layer

7.1 Signal overview

Figure 6 shows the signal relationships between SClock (see 7.2), SLoad (see 7.3), SDataOut (see 7.4), and SDataIn (see 7.5).

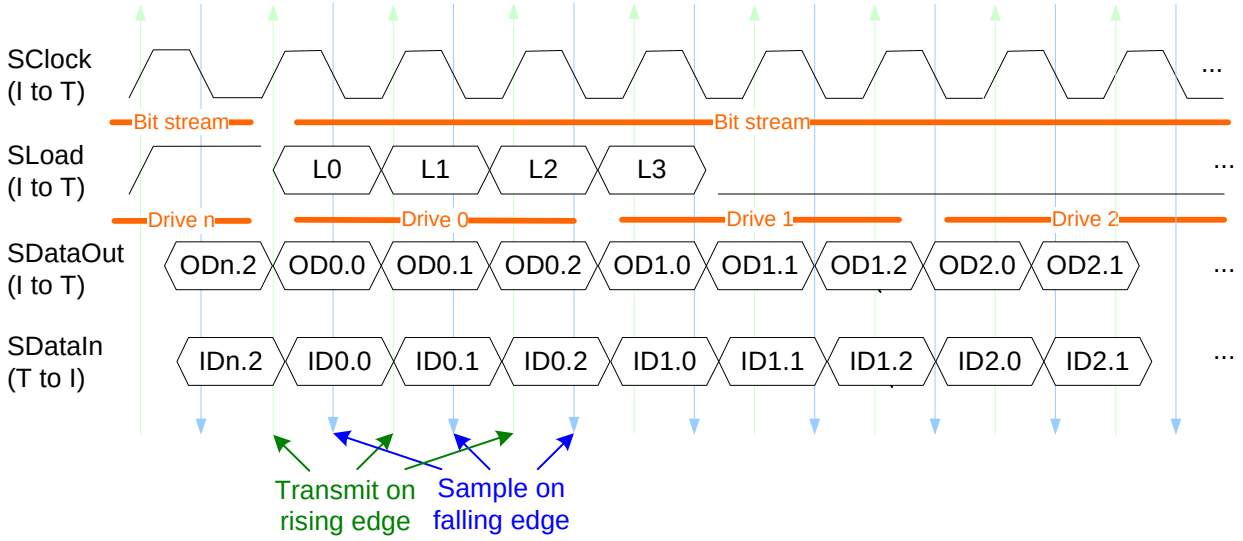


Figure 6 — Signal relationships

The bit stream on SLoad, SDataOut and SDataIn shall be restarted the clock after SLoad is set to 1. The bit stream shall contain at least 4 drives' worth of information. The bit stream need not be the same length every time and may end on any bit position starting with drive 3 bit 3.

Figure 7 shows the bit stream being restarted after 4 drives' worth of information has been communicated (the minimum bit stream length).

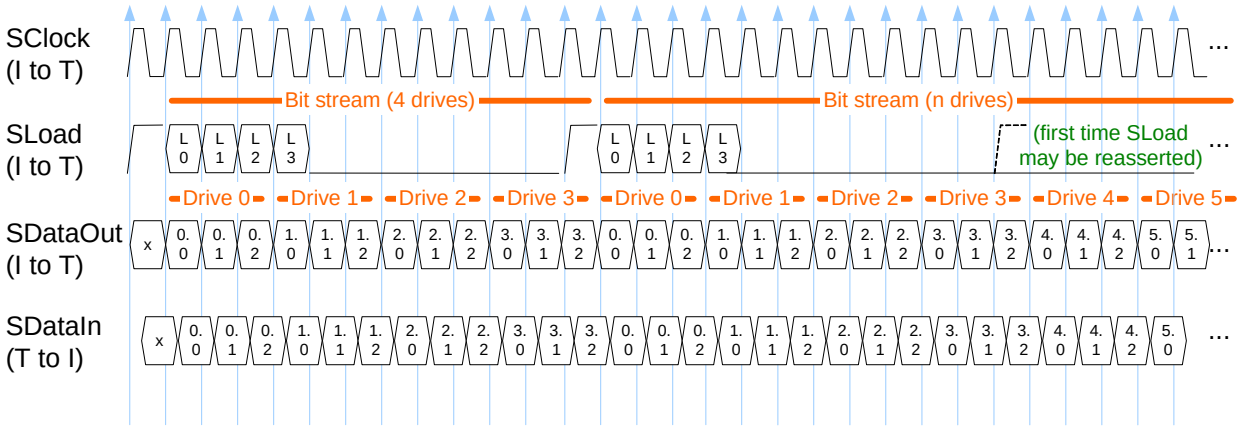


Figure 7 — Repeating bit stream

If the target detects SClock, SLoad, and SDataOut set to 1 for 64 ms (e.g., detects a reset), it shall disable (i.e., turn off) all indicators controlled by the SDataOut bit stream.

7.2 SClock

The initiator shall repeatedly toggle SClock at a frequency compliant with table 5.

The initiator should use the rising edge of SClock to transmit changes in SLoad and SDataOut. The target should use the rising edge of SClock to transmit changes in SDataIn.

The target shall use the falling edge of SClock to latch SLoad and SDataOut. The initiator shall use the falling edge of SClock to latch SDataIn.

When not using the SGPIO bus (e.g., during a reset), the initiator shall set SClock to 1 (i.e., tristate it).

When using the SGPIO bus but purposely not exchanging a bit stream, the initiator should set SClock to 0. This lets the target know that the initiator is still present and has not been removed.

7.3 SLoad

The SLoad signal indicates when the bit stream is ending and being restarted. The clock period during which SLoad is set to 1 is the last clock period of a bit stream.

After SLoad is set to 1, the initiator shall transmit a vendor-specific pattern in the next four bit positions on SLoad. Following that, the initiator shall set SLoad to 0 until it wants to restart the bit stream. The vendor-specific bits are intended to communicate drive-independent information to the target. The vendor-specific bits may change on each bit stream.

Figure 8 shows the SLoad signal.

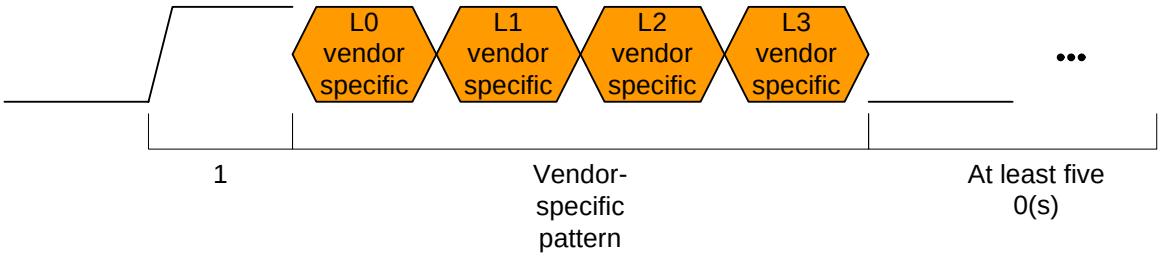


Figure 8 — SLoad signal

After power on, the initiator may set SLoad to 1 with the first rising edge of SClock. If SClock was already high and vendor-specific bit 0 is also set to 1, the target is not synchronized with the initiator during the first bit stream. Therefore, the initiator should not set vendor-specific bit 0 to 1 during the first bit stream.

The initiator shall not restart a bit stream until the third bit position of the fourth drive (i.e., drive 3). The initiator should only set SLoad to 1 to restart a bit stream during the third bit position for a drive.

At least 5 consecutive bits of 0 are needed to distinguish the first SLoad of 1 value from possible 1 values for L0 to L3. To identify the start of a bit stream, the target should detect SLoad set to 0 for 5 or more bits then detect it set to 1.

When not using the SGPIO bus (e.g., during a reset), the initiator shall set SLoad to 1 (i.e., tristate it).

When using the SGPIO bus but purposely not exchanging a bit stream, the initiator should set SLoad to 0. This lets the target know that the initiator is still present and has not been removed.

7.4 SDataOut

The SDataOut signal carries output bits associated with disk drives on the target backplane. It is intended to control indicators such as LEDs (e.g., activity, locate, and error indicators).

Figure 9 shows the SDataOut bits.

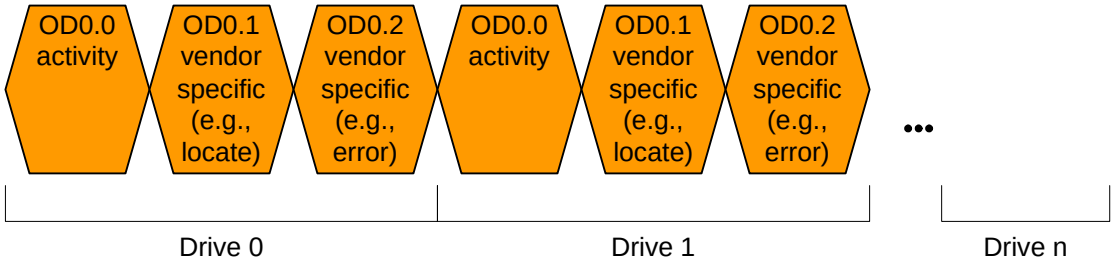


Figure 9 — SDataOut bits

There are 3 output data bits for each drive. Table 6 defines the meaning of the SDataOut bit values.

Table 6 — SDataOut bit meaning

Signal	Description
0	Disable (i.e., turn off) the indicator (e.g., an LED)
1	Enable (i.e., turn on) the indicator (e.g., an LED)

The first bit (i.e., ODn.0, the activity bit) is reserved for drive activity. An activity bit set to 1 specifies that the activity indicator shall be enabled (e.g., turn on an activity LED). An activity bit set to 0 specifies that the activity indicator shall be disabled (e.g., turn off an activity LED).

The activity bit should follow one of the patterns defined in SAS for the READY LED signal (see SAS-1.1):

a) Set to 0 while the drive is powered off or not present, 1 while powered on and idle, and toggles to 0 while processing a command; or
b) Set to 0 while the drive is powered off or not present, 0 while powered on and idle, and toggles to 1 while processing a command.

One way to report activity is to set the activity bit to 0 (for the a) pattern) whenever a frame is transmitted to or received from the drive.

The second (i.e., ODn.1) and third (i.e., ODn.2) bits are vendor-specific, and are intended for controlling indicators like error and locate indicators. A value of 1 specifies that the associated indicator should be enabled; a value of 0 specifies that the associated indicator should be disabled. In the suggested programming interface (see clause 8), bit 1 is used to control a locate indicator and bit 2 is used to control an error indicator.

The number of drives supported is dependent on the application (see clause 9). The initiator shall tristate SDataOut if it does not

When not using the SGPIO bus (e.g., during a reset), the initiator shall set SDataOut to 1 (i.e., tristate it). support the corresponding drive number.

7.5 SDataIn

The SDataIn signal carries input bits associated with disk drives on the target backplane. It is intended to report information such as drive presence detection (see SATA). SDataIn may not be supported by all initiators and targets.

Figure 10 shows the SDataIn bits.

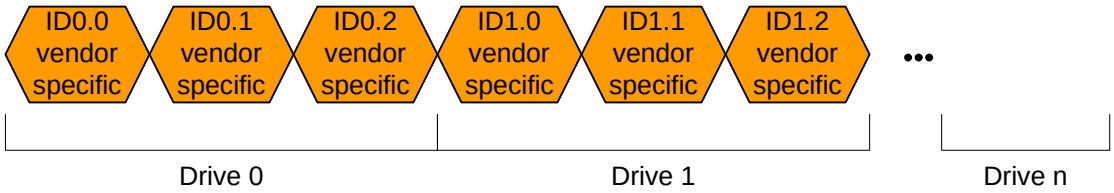


Figure 10 — SDataIn bits

There are 3 input data bits for each drive.

All input bits are vendor-specific. They are intended to carry information like presence-detect.

The number of drives supported is dependent on the application (see clause 9). The target shall tristate SDataIn if it does not support the corresponding drive number. The initiator shall ignore SDataIn for drives it does not support.

8 Programming interface

8.1 Introduction

Initiators should make available to software the ability to select the values to send values on:

a) Per-drive: OD0 (an optional override for the hardware-based activity tracker), OD1, and OD2
b) L0, L1, L2, and L3,

and to retrieve the values most recently received on:

a) Per-drive: ID0, ID1, and ID2.

Although the interface to control these is vendor specific, a recommended interface is defined in this clause.

8.2 SAS SMP GPIO interface

8.2.1 SAS SMP GPIO interface overview

For SAS devices implementing SGPIO initiator(s) (e.g., expanders or HBAs), this clause defines an SMP function interface that may be used to interface to the SGPIO initiator. These functions may also be used to control parallel GPIOs; whether serial or parallel GPIOs are used is outside the scope of this specification.

Figure 11 shows an example of how the SAS SMP function interface may be used with the SFF-8484 connector (see 9.2). When attached to a SAS expander device, the management application client uses the SAS SMP initiator port to send the SMP function over the SAS wide link to the SMP target port in the SAS expander device, controlling the SGPIO initiator in the expander device. When not attached to a SAS expander (e.g., when attached directly to disk drives), the management application sends the SMP functions to a virtual SMP target port inside the SAS initiator device, controlling the SGPIO initiator in the SAS initiator device.

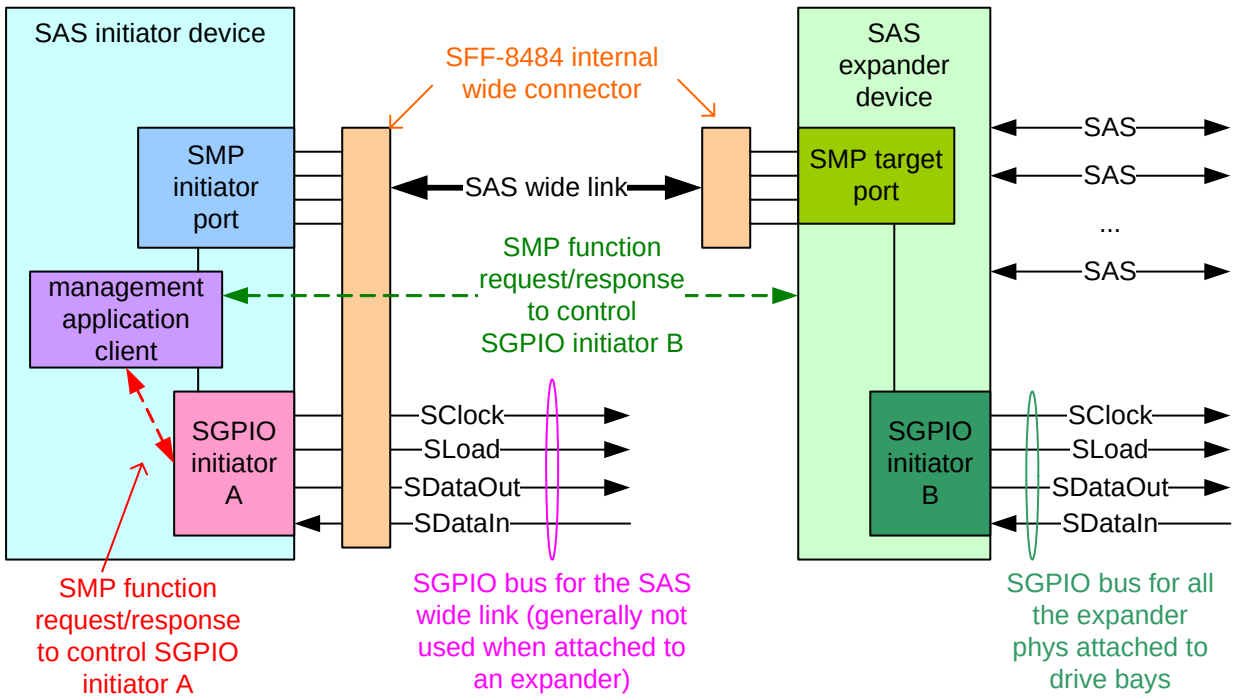


Figure 11 — SAS SMP function example

Table 7 defines the SMP functions.

Table 7 — SMP functions for GPIO

Code	SMP function	Description	Request frame size (in bytes)	Response frame size (in bytes)	Reference
02h	READ GPIO REGISTER	Read one or more GPIO registers	12	variable	8.2.2
82h	WRITE GPIO REGISTER	Write one or more GPIO registers	variable	8	8.2.3

NOTE 1 - Some devices may implement these functions using vendor-specific function codes 50h for READ GPIO REGISTER and D0h for WRITE GPIO REGISTER.

8.2.2 READ GPIO REGISTER function

The READ GPIO REGISTER function returns the contents of one or more GPIO registers.

Table 8 defines the request format.

Table 8 — READ GPIO REGISTER request

Byte\Bit	7	6	5	4	3	2	1	0
0	SMP FRAME TYPE (40h)							
1	FUNCTION (02h)							
2	REGISTER TYPE							
3	REGISTER INDEX							
4	REGISTER COUNT							
5	Reserved							
7								
8	(MSB)							
11	CRC							(LSB)

The SMP FRAME TYPE field shall be set to 40h.

The FUNCTION field shall be set to 02h.

The REGISTER TYPE field specifies the bank of registers to read.

The REGISTER INDEX field specifies the index of the first register in the bank to read.

The REGISTER COUNT field specifies the number of registers starting with the specified index to read.

If the REGISTER TYPE field, REGISTER INDEX field, and/or REGISTER COUNT field specifies an unsupported value, the SMP target port shall return a function result of SMP FUNCTION FAILED in the response frame.

The CRC field is defined in SAS-1.1.

Table 9 defines the response format.

Table 9 — READ GPIO REGISTER response

Byte\Bit	7	6	5	4	3	2	1	0
0	SMP FRAME TYPE (41h)							
1	FUNCTION (02h)							
2	FUNCTION RESULT							
3	Reserved							
4	READ DATA (first register)							
7								
...	...							
n - 7	READ DATA (last register)							
n - 4								
n - 3	(MSB)	CRC						
n								(LSB)

The SMP FRAME TYPE field shall be set to 41h.

The FUNCTION field shall be set to 02h.

The FUNCTION RESULT field is defined in SAS-1.1.

For each register specified by the SMP request frame, the READ DATA field indicates the value of the register.

The CRC field is defined in SAS-1.1.

8.2.3 WRITE GPIO REGISTER function

The WRITE GPIO REGISTER function writes one or more GPIO registers.

Table 10 defines the request format.

Table 10 — WRITE GPIO REGISTER request

Byte\Bit	7	6	5	4	3	2	1	0
0	SMP FRAME TYPE (40h)							
1	FUNCTION (82h)							
2	REGISTER TYPE							
3	REGISTER INDEX							
4	REGISTER COUNT							
5	Reserved							
7								
8	WRITE DATA (first register)							
11								
...	...							
n - 7	WRITE DATA (last register)							
n - 4								
n - 3	(MSB)	CRC						
n								(LSB)

The SMP FRAME TYPE field shall be set to 40h.

The FUNCTION field shall be set to 82h.

The REGISTER TYPE field specifies the bank of registers to write.

The REGISTER INDEX field specifies the index of the first register in the bank to write.

The REGISTER COUNT field specifies the number of registers starting with the specified index to write.

If the REGISTER TYPE field, REGISTER INDEX field, and/or REGISTER COUNT field specifies an unsupported value, the SMP target port shall return a function result of SMP FUNCTION FAILED in the response frame.

For each register specified by the REGISTER TYPE field, REGISTER INDEX field, and REGISTER COUNT field, the WRITE DATA field specifies the value to be written.

The CRC field is defined in SAS-1.1.

Table 11 defines the response format.

Table 11 — WRITE GPIO REGISTER response

Byte\Bit	7	6	5	4	3	2	1	0
0	SMP FRAME TYPE (41h)							
1	FUNCTION (82h)							
2	FUNCTION RESULT							
3	Reserved							
4	(MSB)	CRC						
7								(LSB)

The SMP FRAME TYPE field shall be set to 41h.

The FUNCTION field shall be set to 82h.

The FUNCTION RESULT field is defined in SAS-1.1.

The CRC field is defined in SAS-1.1.

8.3 GPIO register functionality

The SGPIO initiator includes two blink generators A and B that may be used to control the output patterns.

The SGPIO initiator operates in one of two modes:

a) normal: drive-by-drive basis access to the SDataOut and SDataIn bit streams. Uses hardware-based activity trackers and blink generators; and
b) general-purpose: bit-by-bit access to the SLoad, SDataOut and SDataIn bit streams.

The SGPIO initiator defaults to the normal mode, entering general-purpose mode only when requested. During normal mode, the SLoad pattern shall be 0000b.

8.4 GPIO registers

8.4.1 GPIO register overview

Table 12 defines the GPIO register types (i.e., banks).

Table 12 — GPIO register types

Register Type	Name	Description	Reference
00h	GPIO_CFG	Configuration registers	8.4.2
01h	GPIO_RX	Receive registers (drive-by-drive)	8.4.3
02h	GPIO_RX_GP	General purpose receive registers (raw bit stream)	8.4.5
03h	GPIO_TX	Transmit registers (drive-by-drive)	8.4.4
04h	GPIO_TX_GP	General purpose transmit registers (raw bit stream)	8.4.6
05h - BFh	Reserved		
C0h - FFh	Vendor-specific		

8.4.2 GPIO configuration registers

8.4.2.1 GPIO configuration registers overview

Table 13 defines the GPIO configuration registers.

Table 13 — GPIO register indexes for the GPIO_CFG register type

Register Index	Name	Description	Reference
00h	GPIO_CFG[0]	Configuration register 0	8.4.2.2
01h	GPIO_CFG[1]	Configuration register 1	8.4.2.3
02h - FFh	Reserved		

8.4.2.2 GPIO_CFG[0] register

Table 14 defines GPIO configuration register 0.

Table 14 — GPIO_CFG[0] register

Byte\Bit	7	6	5	4	3	2	1	0
0	Reserved							
1	Reserved						VERSION (0h)	
2	GPIO ENABLE	CFG REGISTER COUNT					GP REGISTER COUNT	
3	SUPPORTED DRIVE COUNT							

The VERSION field is read-only and shall be set to 0h.

A GPIO ENABLE bit set to one specifies that GPIO outputs and inputs be enabled. A GPIO ENABLE BIT set to zero specifies that GPIO outputs and inputs be disabled. A change from enabled to disabled shall not take effect until the current bit stream has completed.

The CFG REGISTER COUNT field is read-only and indicates the number of configuration registers.

The GP REGISTER COUNT field is read-only and indicates the number of general purpose data registers.

The SUPPORTED DRIVE COUNT field is read-only and indicates the number of supported drives.

8.4.2.3 GPIO_CFG[1] register

Table 15 defines GPIO configuration register 1.

Table 15 — GPIO_CFG[1] register

Byte\Bit	7	6	5	4	3	2	1	0
0	Reserved							
1	BLINK GENERATOR RATE B				BLINK GENERATOR RATE A			
2	FORCE ACTIVITY OFF				MAXIMUM ACTIVITY ON			
3	STRETCH ACTIVITY OFF				STRETCH ACTIVITY ON			

The VERSION field is read-only and shall be set to 0h.

The BLINK GENERATOR RATE B field specifies the rate for the second blink generator as defined in table 16.

The BLINK GENERATOR RATE A field specifies the rate for the first blink generator as defined in table 16.

Table 16 — BLINK GENERATOR RATE A **field and** BLINK GENERATOR RATE B **field**

Code	Description
0h	1/8 s (default)
1h	2/8 s
...	...
Fh	16/8 s

The FORCE ACTIVITY OFF field, defined in table 17, specifies the minimum amount of time the SGPIO initiator shall disable the activity indicator (i.e., set the ODn.0 bit to zero) if it has been continually enabled for the interval specified in the MAXIMUM ACTIVITY ON field and if the DRIVE M+Y ACTIVITY field (see table 25 in 8.4.4) is set to 100b or 101b.

Table 17 — FORCE ACTIVITY OFF **field**

Code	Description
0h	No minimum amount of time
1h	1/8 s (default)
...	...
Fh	15/8 s

The MAXIMUM ACTIVITY ON field, defined in table 18, specifies the maximum amount of time the SGPIO initiator is allowed to enable the activity indicator (i.e., set the ODn.0 bit to one) if the DRIVE M+Y ACTIVITY field (see table 25 in 8.4.4) is set to 100b or 101b. Once the SGPIO initiator reaches this time, it shall disable the activity indicator for at least as long as the time specified by the FORCE ACTIVITY OFF field.

Table 18 — MAXIMUM ACTIVITY ON **field**

Code	Description
0h	No maximum amount of time
1h	1/4 s
...	...
2h	2/4 s (default)
...	...
Fh	15/4 s

NOTE 2 - The SGPIO initiator should ensure that, if activity indicators for multiple drives are being toggled based on the MAXIMUM ACTIVITY ON field, they do not all toggle in unison or sequentially from one drive to the next adjacent drive (patterns that might be confused with other meanings). The activity should appear somewhat random.

The STRETCH ACTIVITY OFF field, defined in table 19, specifies the minimum amount of time the SGPIO initiator shall disable the activity indicator (i.e., set the ODn.0 bit to zero) if the DRIVE M+Y ACTIVITY field (see table 25 in 8.4.4) is set to 100b or 101b. If the activity indicator is being disabled due to the MAXIMUM ACTIVITY ON field, the

SGPIO initiator shall use the larger of the two times specified by the FORCE ACTIVITY OFF field (which has units of 8th of seconds) and the STRETCH ACTIVITY OFF field (which has units of 64th of seconds).

Table 19 — STRETCH ACTIVITY OFF field

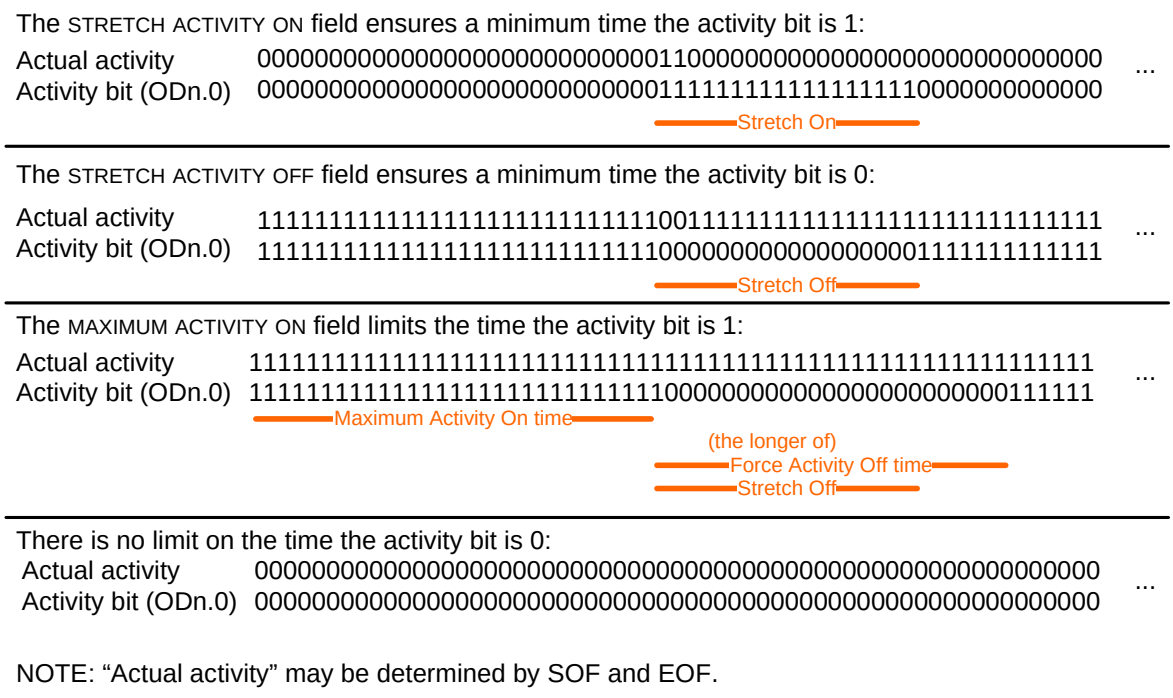
Code	Description
0h	No minimum amount of time (default)
1h	1/64 s
...	...
Fh	15/64 s

The STRETCH ACTIVITY ON field, defined in table 20, specifies the minimum amount of time the SGPIO initiator shall enable the activity indicator (i.e., set the ODn.0 bit to one) if the DRIVE M+Y ACTIVITY field (see table 25 in 8.4.4) is set to 100b or 101b.

Table 20 — STRETCH ACTIVITY ON field

Code	Description
0h	1/64 s (default)
1h	2/64 s
...	...
Fh	16/64 s

Figure 12 shows the interactions of the FORCE ACTIVITY OFF field, the MAXIMUM ACTIVITY ON field, the STRETCH ACTIVITY OFF field, and the STRETCH ACTIVITY ON field.



NOTE: “Actual activity” may be determined by SOF and EOF.

Figure 12 — Interaction of the FORCE ACTIVITY OFF, MAXIMUM ACTIVITY ON, STRETCH ACTIVITY OFF, and STRETCH ACTIVITY ON fields

8.4.3 GPIO receive registers

Table 21 defines the GPIO receive registers.

Table 21 — GPIO register indexes for the GPIO_RX register type

Register index	Name	Description
00h	GPIO_RX[0]	Receive for drives 0 through 3
01h	GPIO_RX[1]	Receive for drives 4 through 7
nnh	GPIO_RX[nn]	...

Table 22 defines the format of each GPIO receive register.

Table 22 — GPIO_RX[n] register

Byte\Bit	7	6	5	4	3	2	1	0
0	Reserved					DRIVE M+3 GPIO INPUT		
						IDm+3.2	IDm+3.1	IDm+3.0
1	Reserved					DRIVE M+2 GPIO INPUT		
						IDm+2.2	IDm+2.1	IDm+2.0
2	Reserved					DRIVE M+1 GPIO INPUT		
						IDm+1.2	IDm+1.1	IDm+1.0
3	Reserved					DRIVE M+0 GPIO INPUT		
						IDm+0.2	IDm+0.1	IDm+0.0

NOTE 3 - The endianness of each four-byte GPIO receive register is not pure big-endian, because the highest numbered drive of the four appears in the first byte (byte 0) and the lowest numbered drive appears in the fourth byte (byte 3).

Each DRIVE M+Y GPIO INPUT field indicates the values received on the SDataIn bit stream for the corresponding drive (where M=4 x n).

8.4.4 GPIO transmit registers

Table 23 defines the GPIO transmit registers.

Table 23 — GPIO register indexes for the GPIO_TX register type

Register index	Name	Description
00h	GPIO_TX[0]	Transmit for drives 0 through 3
01h	GPIO_TX[1]	Transmit for drives 4 through 7
nnh	GPIO_TX[nn]	...

Table 24 defines the format of each GPIO transmit register.

Table 24 — GPIO_TX[n] register

Byte\Bit	7	6	5	4	3	2	1	0
0	DRIVE M+3 ACTIVITY			DRIVE M+3 LOCATE		DRIVE M+3 ERROR		
1	DRIVE M+2 ACTIVITY			DRIVE M+2 LOCATE		DRIVE M+2 ERROR		
2	DRIVE M+1 ACTIVITY			DRIVE M+1 LOCATE		DRIVE M+1 ERROR		
3	DRIVE M+0 ACTIVITY			DRIVE M+0 LOCATE		DRIVE M+0 ERROR		

NOTE 4 - The endianness of each four-byte GPIO transmit register is not pure big-endian, because the highest numbered drive of the four appears in the first byte (byte 0) and the lowest numbered drive appears in the fourth byte (byte 3).

The DRIVE M+Y ACTIVITY field, defined in table 25, controls the activity indicator for the corresponding drive (where M=4 x n). The DRIVE M+Y ACTIVITY field recommended default value is 101b.

Table 25 — DRIVE M+(0,1,2,3) ACTIVITY **field**

Code	Description
000b	Disable the activity indicator (i.e., set the ODn.0 bit to 0)
001b	Enable the activity indicator (i.e., set the ODn.0 bit to 1)
010b	Select blink generator A, 50% duty cycle, on for the first half-cycle, off for the second half-cycle
011b	Select blink generator A, 50% duty cycle, off for the first half-cycle, on for the second half-cycle
100b	Briefly enable (i.e., set the ODn.0 bit to 1) the activity indicator based on the end of activity (e.g., an EOF), subject to the FORCE ACTIVITY OFF field, the MAXIMUM ACTIVITY ON field, the STRETCH ACTIVITY OFF field, and the STRETCH ACTIVITY ON fields in the GPIO_CFG[1] register (see 8.4.2.3).
101b	Briefly enable (i.e., set the ODn.0 bit to 1) the activity indicator based on the start of activity (e.g., an SOF), subject to the FORCE ACTIVITY OFF field, the MAXIMUM ACTIVITY ON field, the STRETCH ACTIVITY OFF field, and the STRETCH ACTIVITY ON fields in the GPIO_CFG[1] register (see 8.4.2.3).
110b	Select blink generator B, 50% duty cycle, on for the first half-cycle, off for the second half-cycle
111b	Select blink generator B, 50% duty cycle, off for the first half-cycle, on for the second half-cycle

The DRIVE M+Y LOCATE field, defined in table 26, controls the locate indicator for the corresponding drive (where M=4 x n). The DRIVE M+Y LOCATE field recommended default value is 00b.

Table 26 — DRIVE M+(0,1,2,3) LOCATE **field**

Code	Description
00b	Disable the locate indicator (i.e., set the ODn.1 bit to 0)(default)
01b	Enable the locate indicator (i.e., set the ODn.1 bit to 1)
10b	Select blink generator A, 50% duty cycle, on for the first half-cycle, off for the second half-cycle
11b	Select blink generator A, 50% duty cycle, off for the first half-cycle, on for the second half-cycle

The DRIVE M+Y ERROR field, defined in table 27, controls the error indicator for the corresponding drive (where M=4 x n). The DRIVE M+Y ERROR field recommended default value is 000b.

Table 27 — DRIVE M+(0,1,2,3) ERROR **field**

Code	Description
000b	Disable the error indicator (i.e., set the ODn.2 bit to 0)(default)
001b	Enable the error indicator (i.e., set the ODn.2 bit to 1)
010b	Select blink generator A, 50% duty cycle, on for the first half-cycle, off for the second half-cycle
011b	Select blink generator A, 50% duty cycle, off for the first half-cycle, on for the second half-cycle
100b	Enable the error indicator (i.e., set the ODn.2 bit to 0)
101b	
110b	Select blink generator B, 50% duty cycle, on for the first half-cycle, off for the second half-cycle
111b	Select blink generator B, 50% duty cycle, off for the first half-cycle, on for the second half-cycle

8.4.5 GPIO general purpose receive registers

8.4.5.1 GPIO general purpose receive registers overview

Table 28 defines the GPIO general purpose receive registers.

Table 28 — GPIO register indexes for the GPIO_RX_GP register type

Register index	Name	Description
00h	GPIO_RX_GP_CFG	General purpose receive configuration
01h	GPIO_RX_GP[1]	General purpose receive first 32 bits
02h	GPIO_RX_GP[2]	General purpose receive second 32 bits
nnh	GPIO_RX_GP[nn]	...

8.4.5.2 GPIO_RX_GP_CFG register

Table 29 defines the format of the GPIO general purpose receive configuration register.

Table 29 — GPIO_RX_GP_CFG register

Byte\Bit	7	6	5	4	3	2	1	0
0	Reserved							
1								
2	COUNT							
3	Reserved							

The COUNT field is read-only and indicates the number of repetitions remaining. A COUNT field set to FFh indicates that infinite repetitions are remaining.

8.4.5.3 GPIO_RX_GP[1..n] register

Table 30 defines the format of each GPIO general purpose receive register.

Table 30 — GPIO_RX_GP[1..n] register

Byte\Bit	7	6	5	4	3	2	1	0
0	(last)							
1				SDATAIN BIT PATTERN				
2								
3								(first)

NOTE 5 - The endianness of each four-byte GPIO general purpose receive register is little-endian, because the highest numbered bit appears in the first byte (byte 0) and the lowest numbered bit appears in the fourth byte (byte 3).

The SDATAIN BIT PATTERN field contains the bits received on the SDataIn signal since the last SLoad.

In GPIO_RX[1], bit 0 of byte 3 contains the first bit (i.e., ID0.0) and bit 7 of byte 0 contains the 32nd bit (i.e., ID10.1).

In GPIO_RX[2], bit 0 of byte 3 contains the 33rd bit (i.e., ID10.2) and bit 7 of byte 0 contains the 64th bit (i.e., ID21.0).

8.4.6 GPIO general purpose transmit registers

8.4.6.1 GPIO general purpose transmit registers overview

Table 31 defines the GPIO general purpose receive registers.

Table 31 — GPIO register indexes for the GPIO_TX_GP register type

Register index	Name	Description
00h	GPIO_TX_GP_CFG	General purpose transmit configuration
01h	GPIO_TX_GP[1]	General purpose transmit first 32 bits
02h	GPIO_TX_GP[2]	General purpose transmit second 32 bits
nnh	GPIO_TX_GP[nn]	...

8.4.6.2 GPIO_TX_GP_CFG register

Table 32 defines the format of the GPIO general purpose transmit configuration register.

Table 32 — GPIO_TX_GP_CFG register

Byte\Bit	7	6	5	4	3	2	1	0
0	Reserved							
1								
2	COUNT							
3	Reserved				SLOAD PATTERN			
					L3	L2	L1	L0

The COUNT field specifies the number of times to transmit the specified SLoad pattern, transmit the GPIO_TX_GP register contents, and receive into GPIO_RX_GP before resuming normal operation. A COUNT field set to FFh specifies that the general purpose operation repeat until the COUNT field is changed.

The SLOAD PATTERN field specifies the four bit pattern to transmit on SLoad at the start of each general purpose bit stream. Bit 0 of the SLOAD PATTERN field corresponds to L0; bit 3 corresponds to L3.

8.4.6.3 GPIO_TX_GP[1..n] registers

Table 33 defines the format of each GPIO general purpose transmit register.

Table 33 — GPIO_TX_GP[1..n] register

Byte\Bit	7	6	5	4	3	2	1	0
0	(last)							
1				SDATAOUT BIT PATTERN				
2								
3								(first)

NOTE 6 - The endianness of each four-byte GPIO general purpose transmit register is little-endian, because the highest numbered bit appears in the first byte (byte 0) and the lowest numbered bit appears in the fourth byte (byte 3).

The SDATAOUT BIT PATTERN field specifies the bits to be transmitted on the SDataOut signal after SLoad.

In GPIO_TX[1], bit 0 of byte 3 contains the first bit (i.e., OD0.0) and bit 7 of byte 0 contains the 32nd bit (i.e., OD10.1).

In GPIO_TX[2], bit 0 of byte 3 contains the 33rd bit (i.e., OD10.2) and bit 7 of byte 0 contains the 64th bit (i.e., OD21.0).

9 Applications

9.1 Applications overview

SGPIO may be used in several applications:

a) Serial Attached SCSI SAS 4i or Mini SAS 4i connector (see SAS-1.1, SFF-8484, SFF-8086, and SFF-8087);
b) Serial Attached SCSI backplanes (see SAS-1.1);
c) Serial ATA internal 4 Lane connector (see SATA); and
d) PCI Express Server IO Module (see SIOM).

NOTE 7 - SGPIO may or may not have been endorsed for such usage by the corresponding standards bodies/consortiums.

9.2 SAS 4i connector

Table 34 defines the SGPIO signal assignments for the SAS 4i connector (see SAS-1.1 and SFF-8484).

Table 34 — SAS 4i connector signal assignments for SGPIO

Pin	Signal
Sideband 0	SClock
Sideband 1	SLoad
Sideband 2	Ground
Sideband 3	Ground
Sideband 4	SDataOut
Sideband 5	SDataIn

NOTE 8 - The Sideband 0..5 signals are assigned to different signal pins for controllers (e.g., Sideband 0 is on pin 14) and backplanes (e.g., Sideband 0 is on pin 19). See SAS-1.1.

Table 35 defines the SGPIO signal assignments for the Mini SAS 4i connector (see SAS-1.1, SFF-8086, and SFF-8087).

Table 35 — Mini SAS 4i connector signal assignments for SGPIO

Pin	Signal
Sideband 0	SClock
Sideband 1	SLoad
Sideband 2	Ground
Sideband 3	Ground
Sideband 4	SDataOut
Sideband 5	SDataIn
Sideband 6	Reserved
Sideband 7	Reserved

NOTE 9 - The Sideband 0..7 signals are assigned to different signal pins for controllers (e.g., Sideband 0 is on pin B8) and backplanes (e.g., Sideband 0 is on pin A8). See SAS-1.1.

Table 36 describes the relationship of the bits to the four SAS physical links using the same 4i connector.

Table 36 — SAS bit assignments

Bits	Usage
0 to 2	SAS physical link 0
3 to 5	SAS physical link 1
6 to 8	SAS physical link 2
9 to 11	SAS physical link 3
	SATA port multiplier bits, if needed
12 to 14	SATA physical link 0, port multiplier device 1
15 to 17	SATA physical link 1, port multiplier device 1
18 to 20	SATA physical link 2, port multiplier device 1
21 to 23	SATA physical link 3, port multiplier device 1
...	...
191	SATA physical link 3, port multiplier device 15
12 to m or 191 to m	Vendor-specific

If the initiator does not know whether a physical link supports SATA, it shall terminate the bit stream after bit 11. If the initiator determines that the target supports SATA on one or more of the physical links, it shall provide bits for SATA port multipliers for each of the physical links (192 bits total). If some of the physical links are using SAS or are not using a port multiplier, the target shall ignore the additional bits (but the initiator shall still transmit tristated bits in those positions).

HBAs supporting more than 4 phys are expected to support multiple SGPIO busses (e.g., an HBA with 8 phys is expected to support 2 SGPIO initiators). The SClock and SLoad outputs may be shared to reduce pin count (e.g., from 8 pins to 6).

9.3 SAS backplane

SGPIO may be used from a SAS expander to communicate a bit stream for all the drives in a backplane. The bit stream is not limited to 4 drives as with the SAS 4i connector. For example, an 8 port expander might employ a bit stream of 8 drives (one per phy). The SGPIO target would be designed to ignore the phys known not to be attached to drives.

SGPIO may also be used in a closed environment between an HBA and a backplane with a bitstream supporting more than 4 drives. HBAs may be designed to output multiple 4-drive bit streams for use with SAS 4i cable assemblies and a single n-drive bit stream for use in closed environments.

9.4 SATA internal 4 Lane connector

Table 37 defines the SGPIO signal assignments for the SATA internal 4 Lane connector (see SATA and SFF-8484).

Table 37 — SATA internal 4 Lane connector signal assignments for SGPIO

Pin	Signal
SIDEBAND0	SClock
SIDEBAND1	SLoad
SIDEBAND2	Ground
SIDEBAND3	Ground
SIDEBAND4	SDataOut
SIDEBAND5	SDataIn

Table 38 describes the relationship of the bits to the SATA physical links using the same internal 4 Lane connector.

Table 38 — SATA bit assignments

Bits	Usage
0 to 2	SATA physical link 0, port multiplier device 0
3 to 5	SATA physical link 1, port multiplier device 0
6 to 8	SATA physical link 2, port multiplier device 0
9 to 11	SATA physical link 3, port multiplier device 0
12 to 14	SATA physical link 0, port multiplier device 1
15 to 17	SATA physical link 1, port multiplier device 1
18 to 20	SATA physical link 2, port multiplier device 1
21 to 23	SATA physical link 3, port multiplier device 1
...	...
191	SATA physical link 3, port multiplier device 15
192 to z	Vendor-specific

If the SATA initiator supports port multipliers, the initiator shall provide bits for SATA port multipliers for each of the physical links (192 bits total). If some of the physical links are not using a port multiplier, the target shall ignore the additional bits (but the initiator shall still transmit tristated bits in those positions).

If the SATA initiator does not support port multipliers, the initiator shall provide bits 0 through 11 only and shall restart the bit stream with bit 12.

9.5 PCI Express ExpressModule

Table 39 defines the SGPIO signal assignments for the PCI Express ExpressModule (see PCI-EM).

Table 39 — PCI Express ExpressModule signal assignments for SGPIO

Pin	Signal
STOR_SB-1	SClock
STOR_SB-2	SDataOut
STOR_SB-3	SDataIn
STOR_SB-4	SLoad

Table 40 describes the relationship of the bits to the SAS physical links using the same ExpressModule connector.

Table 40 — PCI Express bit assignments

Bits	Usage
0 to 2	Internal drive physical link 0
3 to 5	Internal drive physical link 1
6 to 8	Internal drive physical link 2
9 to 11	Internal drive physical link 3
12 to 14	SATA physical link 0, port multiplier device 1
15 to 17	SATA physical link 1, port multiplier device 1
18 to 20	SATA physical link 2, port multiplier device 1
21 to 23	SATA physical link 3, port multiplier device 1
...	...
191	SATA physical link 3, port multiplier device 15
192 to z	Vendor-specific

If the initiator does not know whether the target supports SATA, it shall terminate the bit stream after bit 11 and follow the rules for a SAS 4i connector (see 9.2). If the initiator determines that the target supports SATA on a physical link, it shall continue through bit 191 and follow the rules for a SATA internal 4 Lane connector (see 9.4).

10 Suggested SGPIO usage (informative)

10.1 Suggested SGPIO usage overview

This clause defines suggested one possible usage model for the vendor-specific fields defined in this standard.

A local SGPIO environment is where the SGPIO initiator is in an HBA attached to a backplane of directly attached drives. Each drive is assumed to be attached via a drive bay. Each SGPIO bus corresponds to the 4 physical links on the SFF-8484 connector. The SGPIO bit stream is 12 bits long.

A remote SGPIO environment is where the HBA talks to an expander on a backplane, the expander provides the SGPIO initiator to control the drives attached to it, and the SMP functions described in this standard are used to access the SGPIO initiator. There is one SGPIO bus per expander device, corresponding to all the phys in the expander device (starting with phy 0). The SGPIO bit stream is a multiple of 12 bits (i.e., 4 bays) long. Each drive is assumed to be attached via a drive bay.

Each bay has a number from 1-16 which is physically presented to the user (e.g., on the outside of the enclosure).

The backplane provides 3 LEDs for each bay as described in table 41.

Table 41 — Bay LED meanings

Code	Meaning			
	On (1)	**Off (0)**	**Blinking at 1 Hz with 50% duty cycle (0101...)**	**Other pattern**
Activity	configured && online && no activity	not configured || not online || (inactive and not rebuilding)	rebuilding || capacity expansion || RAID migration	Mostly on, but off during activity: configured && online && activity && !(rebuilding || capacity expansion || RAID migration)
Locate	selected	not selected	none	Blinking at 1 Hz with 50% duty cycle, alternating Locate and Error: selected && (failed || predicted failure)
Error	drive has failed	drive is OK	predicted failure	

10.2 SDataOut

The SGPIO SDataOut bit stream defined in table 42 controls 3 LEDs per bay. In table 42, m (0, 4, 8, or 12) is the lowest phy number of the four phys. The bay number (1-16) of each bay is determined by the Reverse Bay

Numbers bit and Group ID field in the SDataIn bit stream. The bays within each set of 4 bays are referred to as relative bays A, B, C, and D for coordinating the description in this standard.

Table 42 — SDataOut bit stream for set of 4 bays

Bit	Relative bay	Name
m.0	A	Activity
m.1		Locate
m.2		Error
m+1.0	B	Activity
m+1.1		Locate
m+1.2		Error
m+2.0	C	Activity
m+2.1		Locate
m+2.2		Error
m+3.0	D	Activity
m+3.1		Locate
m+3.2		Error

10.3 SDataIn

The SGPIO SDataIn bit stream defined in table 43 reports a mixture of bay-specific information (e.g. Drive Installed and Bay Present bits) and information that is related to the set of 4 bays rather than related to the

specific bay (e.g. Group ID and Reverse Bay Numbers). The bays within each set of 4 bays are referred to as relative bays A, B, C, and D for coordinating the description in this standard.

Table 43 — SDataIn bit stream for set of 4 bays

Bit	Relative bay	Name	Description
m.0	A	Drive Installed	0=installed, 1=not installed
m.1		Bay Present	0=present, 1=not present
m.2	N/A	Group ID MSB	Identifies the range of bay numbers of these bays (see table 44)
m+1.0	B	Drive Installed	0=installed, 1=not installed
m+1.1		Bay Present	0=present, 1=not present
m+1.2	N/A	Group ID LSB	Identifies the range of bay numbers of these bays (see table 44)
m+2.0	C	Drive Installed	0=installed, 1=not installed
m+2.1		Bay Present	0=present, 1=not present
m+2.2	N/A	Reverse Bay Numbers	0=Bay D (i.e., bits m+3.x) maps to the lowest bay number and bay A (i.e., bits m+0.x) maps to the highest bay number 1=Bay A (i.e., bits m+0.x) maps to the lowest bay number and bay D (i.e., bits m+3.x) maps to the highest bay number
m+3.0	D	Drive Installed	0=installed, 1=not installed
m+3.1		Bay Present	0=present, 1=not present
m+3.2	N/A	Reserved	Reserved for definition in future revisions of this standard. Although currently reserved, the value of this bit from the SDataIn bit stream shall be included in the GPIO receive registers (see 8.4.3) by the SGPIO initiator.

A Drive Installed bit of 0 indicates that drive presence detect logic has determined a drive is present in the associated bay. This is based off detection of the voltage/ground pins. A bit of 1 indicates that presence detect logic has determined a drive is not present (or that no such logic exists).

Each Bay Installed bit indicates whether or not a bay exists in that position. If the bay does not exist, the Drive Installed bit shall be ignored and the SDataOut bits for that bay are ignored by the backplane and shall be set to 1 (tristate) by the SGPIO initiator.

The Group ID field indicates the range of bay numbers controlled by this set of bays and is specified in table 44. The MSB (bit m.2) is on the left and the LSB (bit m+1.2) is on the right.

Table 44 — Group ID field

Code	Description
11b	This set of bays has bay numbers 1-4.
10b	This set of bays has bay numbers 5-8.
01b	This set of bays has bay numbers 9-12.
00b	This set of bays has bay numbers 13-16.

The Reverse Bay Numbers bit indicates the order the bay numbers are assigned to the set of 4 bays. A Reserve Bay Numbers bit of 1 indicates that the bay numbers controlled by this set of bays are swapped (e.g., physical link 0 corresponds to the highest bay number controlled by this set of bays). A bit of 0 indicates they are not swapped (e.g., physical link 0 corresponds to the lowest bay number controlled by this set of bays).

Table 45 shows how the Reverse Bay Numbers bit and Group ID field combine to define the bay numbers.

Table 45 — Bay numbers

SDataIn bit values			Bay number
Reverse Bay Numbers	**Group ID**	**Relative bay**	
1b	11b	A	1
		B	2
		C	3
		D	4
	10b	A	5
		B	6
		C	7
		D	8
	01b	A	9
		B	10
		C	11
		D	12
	00b	A	13
		B	14
		C	15
		D	16
0b	11b	A	4
		B	3
		C	2
		D	1
	10b	A	8
		B	7
		C	6
		D	5
	01b	A	12
		B	11
		C	10
		D	9
	00b	A	16
		B	15
		C	14
		D	13