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SFF-8460

Former Specification for

HSS Backplane Design Guidelines

Rev 1.3 August 7, 2018

SECRETARIAT: SFF TA TWG

ABSTRACT: This expired specification contains guidelines to help in the design and implementation of backplanes for successful operation at high frequencies.

REASON FOR EXPIRATION: Voided
Alvin Cox (Seagate; former editor of this document) requested that this published document be retracted because it is out of date and there is no intention of updating it. Technical content was retained at the request of the former editor.

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EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

Compaq
DDK Fujikura
ENDL
FCI/Berg
IBM
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Tyco AMP
Unisys

The following member companies of the SFF Committee voted to abstain on this industry specification.

Circuit Assembly
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SFF Committee --

HSS Backplane Design Guidelines

1. Scope

This specification is a guideline to provide information that will help in the design and implementation of backplanes for successful operation at high frequencies.

A long list of parameters have to be considered, and the characteristics of one balanced relative to others if a backplane is to operate at the desired speeds and meet EMI (Electro Magnetic Interference) requirements.

In an effort to broaden the applications for storage devices, an ad hoc industry group of companies representing system integrators, peripheral suppliers, and component suppliers decided to address the issues involved.

The SFF Committee was formed in August, 1990 and the first working document was introduced in January, 1991.

1.1 Description of Clauses

Clause 1 contains the Scope and Purpose.

Clause 2 contains Referenced and Related Standards and SFF Specifications.

Clause 3 contains the list of Figures and Tables

Clause 4 contains the General Description

Clause 5 contains the Definitions and Conventions

Clause 6 defines the Guidelines

2. References

The SFF Committee activities support the requirements of the storage industry, and it is involved with several standards.

2.1 Industry Documents

The following interface standards are relevant to this Specification.

- X3.230-1994 FC-PH Fibre Channel Physical Interface
- X3.297-199x FC-PH-2 Fibre Channel Physical Interface -2
- X3.303-199x FC-PH-3 Fibre Channel Physical Interface -3
- FC-PI Fibre Channel Physical Interface

2.2 SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at ftp://ftp.seagate.com/sff/SFF-8000.TXT.

2.3 Sources

Copies of ANSI standards or proposed ANSI standards may be purchased from Global Engineering.

15 Inverness Way East 800-854-7179 or 303-792-2181
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Copies of SFF Specifications are available by joining the SFF Committee as an Observer or Member.

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2.4 Glossary

dB	decibel
EMI	electromagnetic interference
ESD	electrostatic discharge
GHz	gigahertz
IC	integrated circuit
MHz	megahertz
PBC	Port Bypass Circuit
PCB	printed circuit board
pF	picofarad
psec	picosecond
RF	radio frequency
SCA	single connector attachment
TDR	time domain reflectometer

ELECTRONIC COPIES

The status of SFF Specifications is summarized in SFF-8000, which is the only specification which can now be obtained over FaxAccess.

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3 RF Design of Backplanes

RF design principles must be built into the design and implementation of a backplane for it to operate successfully at high data rates. Low frequency or steady state lines can be of minimal width and routed on the surfaces of the PCB. High frequency data lines should be routed first to assure the best layout possible.

The high-speed data lines must be considered as transmission lines requiring controlled impedance and straight-as-possible routing. There are two approaches to routing the transmission lines, stripline and microstrip. With stripline transmission lines, data paths are buried between power and ground layers. Microstrip transmission lines are routed external to the power-ground layer pair. Stripline is recommended for superior shielding and electromagnetic compatibility (EMC). Avoid sharp bends and feedthroughs and minimize impedance discontinuities. At high frequencies, the surface area of the trace, rather than its cross-sectional area, determine its impedance. This is due to skin effect limiting the penetration depth of current in the trace.

4 Trace Widths

The width of traces used in the backplane design is essentially arbitrary, determined primarily by board lamination stack-up and impedance considerations. As a beginning point, select 0.38 mm as an appropriate trace width. Widths of less than 0.25 mm for long lengths are not recommended for high-frequency traces. Skin effects at high frequencies result in higher impedance if the trace surface area is reduced. This is virtually independent of the thickness of the trace (alternatively stated, independent of the weight of the copper). An observed advantage to the wider trace widths is that it helps keep routing more simple by limiting the possible routing paths as compared to narrower traces. Tightly coupled designs without long lengths can be built with traces as narrow as 0.1 mm.

5 Trace Separation

The separation of the high frequency traces is primarily determined by the desire to have minimum radiating loop area in the differential signal pair (this area is directly proportional to trace separation), to have minimum trace-to-trace capacitive coupling, and to maintain the characteristic microstrip or stripline impedance. Both capacitive coupling and characteristic impedance are inversely affected by trace spacing. Generally, an edge-to-edge trace spacing of 2.5 times the trace width should prove successful. Specifying the PCB differential impedance and providing test traces on the board at least 75 mm long for a verification purpose is recommended.

An alternative to physical separation of the traces for prevention of crosstalk is the inclusion of a ground trace between differential signal pairs. This is less desirable primarily because trace-to-ground-to-trace spacing increases the physical size of the radiating loop, thus significantly increasing radiated emissions for a possible marginal improvement in crosstalk immunity.

It is also important to ensure that noise from other signals does not couple into parallel high frequency signal lines. Coupling between nets occurs between lines primarily by two methods:

- When two lines are routed so that one is directly above the other, capacitive coupling occurs.
- When two lines are routed in parallel (side by side), inductive coupling occurs.

The amount of coupling that occurs is primarily related to the following physical parameters:

- The height of the traces above the power plane
- The separation of the traces
- The length of the parallelism.

Two types of crosstalk exist. As a signal propagates down a line, both backward and forward crosstalk will be induced into adjacent, closely spaced, parallel lines. Forward crosstalk propagates in the direction of the coupling signal, while backward crosstalk propagates in a direction opposite of the coupling signal (hence, the names). Forward crosstalk increases constantly with coupled length, while backward crosstalk increases only until a critical coupling length is reached. Also, forward crosstalk amplitude increases as the rise time of the incident signal increases. Figure 1 illustrates these principles.

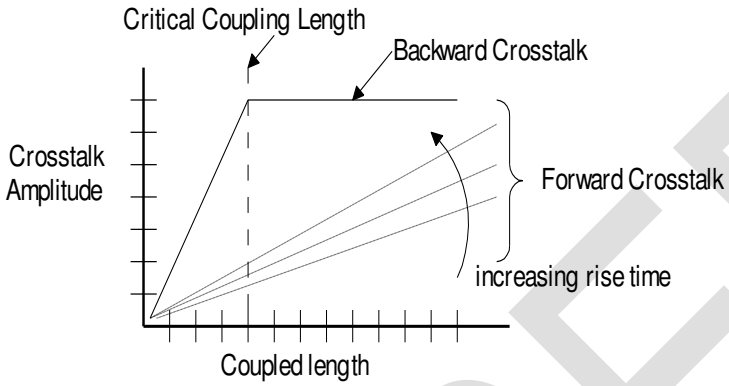


Figure 1. Crosstalk Charting.

Figure 2 will be used to discuss magnitude of coupling between signals. The magnitude of inductive coupling between two parallel lines is a function of the ratio of s_2 to d. The magnitude of capacitive coupling between two overlapping lines (which is generally worse than inductive coupling, given the same separation ratios and parallelism length) is a function of the ratio of s_1 to d. If these ratios, s_2/d and s_1/d, are equal to 1, coupling will be approximately 15 to 20% of the incident wave amplitude. If the ratio is equal to 2, the coupling will be approximately 5 to 10%. If the ratio is 3, the coupling will be approximately 2 to 5%. Other signals should be widely separated (ratio ≥ 3) from the high-speed differential lines to ensure unwanted noise is not coupled into these signals.

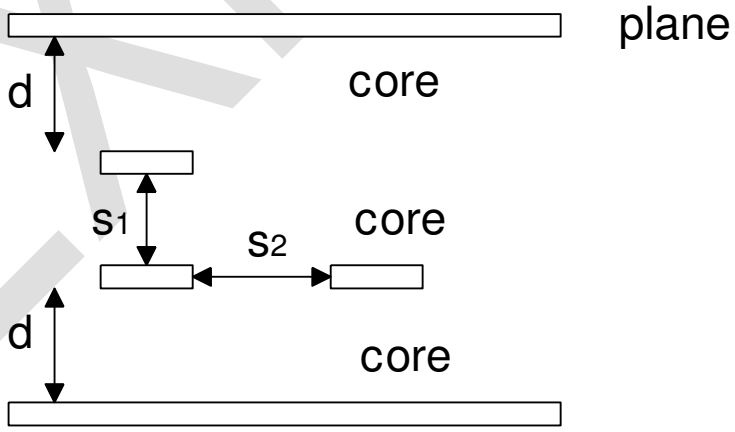


Figure 2. Signal Separation.

6 Trace Routing

The physical routing of the traces, particularly the high-speed data lines, should be done with the objective of a smooth flow with minimal interruptions. Every impedance discontinuity is both a source of signal reflections and a source of radiated

emissions. Controlling the number and severity of impedance discontinuities, including sharp turns, minimizes these two factors. Minimizing the number of required feedthroughs by intelligent selection of component placement is desirable at high frequencies. Each additional feedthrough adds 1-4 pF in parasitic capacitance unless the feedthrough structure is designed to minimize excess capacitance. In summary, avoid or minimize feedthroughs and sharp turns (no angles sharper than 45°, including another layer).

Figure 3 illustrates these principles used in the layout of a backplane for use with the Fibre Channel interface. Note particularly the smooth, uninterrupted flow of the high-speed data lines. Data paths must be skew controlled. These signals travel approximately 180 psec/in. The paths must be equal length or cumulative skew buildup will occur. Port Bypass Circuits and I/O connectors in this layout were handled so as to ensure that interconnections could be made with minimal use of feedthroughs and with no crossing of data lines. Also, note the standalone transmission lines on the right side of the backplane for testing the differential signal impedance of the board.

The high-speed data lines are not routed through the field of feedthroughs for the SCA-2 backplane connector. The proximity to the feedthroughs results in parasitic capacitance and impedance discontinuities.

Figure 3 shows tear drops and blisters for the surface mount component pads. They are no longer recommended, as they add parasitic capacitance. Depending upon the layer stack-up and transmission line width, creating a void in the power/ground plane immediately under a component footprint can reduce the impedance discontinuity at the component's physical location on the board. A starting point for analyzing this technique is to consider the impedance of a trace that is equivalent to the width of the component (i.e. .76mm trace for a .76mm part: the component and it's pads are acting like a trace for the length of the component) in the stack-up. Unless the trace is already this width, the impedance of this wider trace will be much lower (this indicates the magnitude of the impedance discontinuity that the placement of this part in the transmission line path will cause in the system). However, if the impedance is considered to the next ground/power plane in the stack-up, the impedance will rise (the target that the impedance be maintained in the transmission line path). This analysis will indicate if the power plane must be removed under the wider components on one or several layers. This technique does not account for fringing effects (which may be very small: this is dependent on individual stack-ups), and must therefore be verified through actual physical analysis (differential TDR, etc.) on initial layouts to determine how much optimization may be required. 3D field solving software can be of great benefit during the layout process.

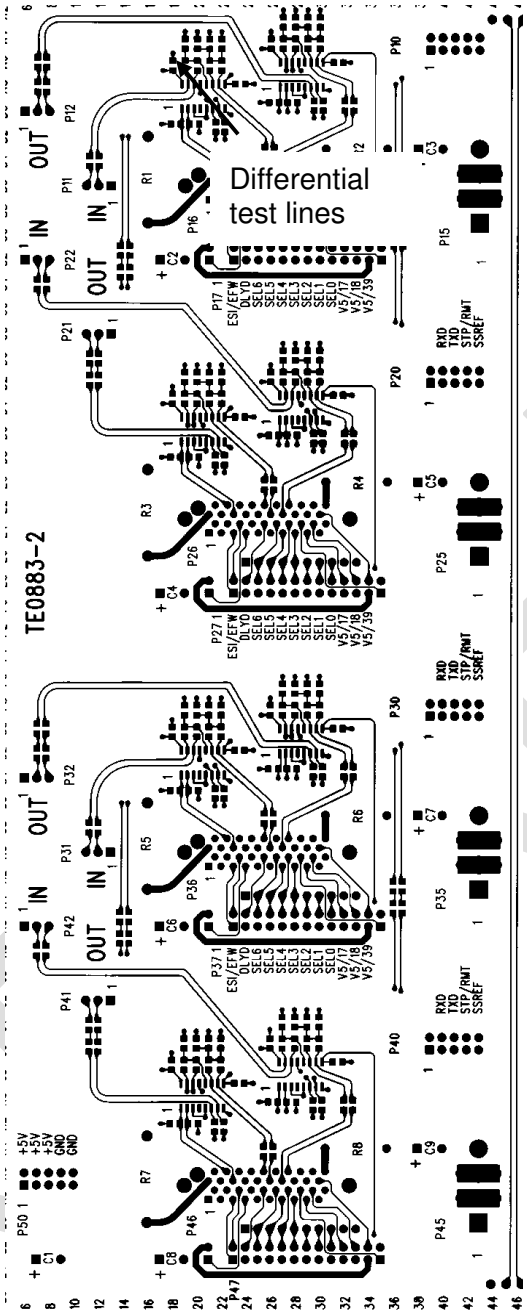


Figure 3. Fibre Channel Backplane Signal Lines.

7 Skew

Skew is the major board related loss that must be successfully handled or poor margins will result. Skew is the electrically different lengths of the data path and not the dispersion of the tangential offset of signal. See Table 1. Skew can be evaluated using a differential TDR. Single-ended TDR's will give varying time measurements that will not accurately predict skew. The differential TDR will measure skew more accurately than a strict path length prediction. The differential skew measured with a differential TDR includes the mutual capacitance between the lines and the phenomenon that the two legs of the differential pair seem to "pull" themselves along for less skew. Try to control skew by "spreading" one of the transmission legs apart as opposed to routing several tight loops of signal trace, which might appear inductive at high edge rates.

	Coupled Microstrip	Coupled Stripline
Loss Tangent	0.012	0.012
1.0625 GHz Highest Fundamental	557.25 ps	658.28 ps
3.1875 GHz Third Harmonic	557.38 ps	658.28 ps
Dispersion at 1 meter	0.13 ps	0 ps

Table 1. Dispersion due to Tangential offset in FR-4

8 Fly-Through Termination Recommendation

The serial nature of the Fibre Channel interface makes for a relatively easy task to route the high frequency paths in a simple and effective fashion. Even the termination required for high frequency operation can be placed simply and optimally in a fly through termination, as shown in
.

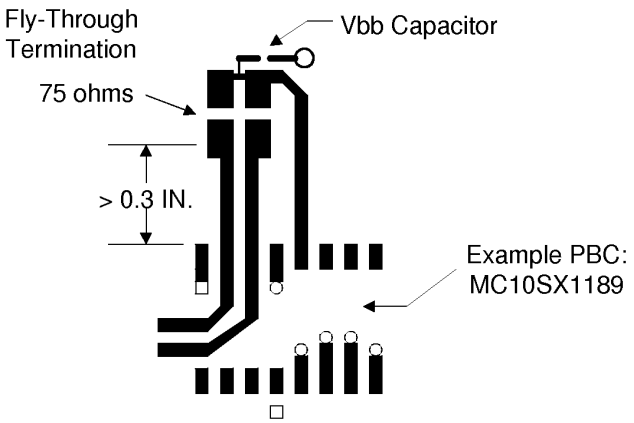


Figure 4. Terminator Resistor Placement.

The terminating resistors are recommended to be the smaller surface mount packages (0603 case size). The 0402 case size parts are better for 2.125 gigabaud.

It is recommended that terminations fly-through (see) the package of the receiver and be placed at least 7.6 mm from the input leads. The reasons for this layout is two-fold:

1. By locating the terminations away from the integrated circuit (IC), the parasitic losses are more distributed, resulting in better performance.
2. Minimizing parasitic capacitance by the package results in less degradation of rise/fall time.

9 Backplane Impedance

Various programs exist that calculate the transmission line impedance. One has been used to calculate the impedance of a prototype Fibre Channel backplane with a predicted impedance error of approximately 5%, as indicated in Table 2.

FR-4 Material, with 75 ohm Microstrip Transmission Lines		
Frequency	3.000	GHz
Diel. Constant	4.30	
Trace Width	0.381	mm
Height above Ground	0.457	mm
Trace Length	2.540	mm
Predicted Z_0	78.10 ohms	

Table 2. Sample Impedance - Microstrip.

The detail of the Fibre Channel backplane construction for the sample calculation in Table 2 is illustrated in Figure 5.

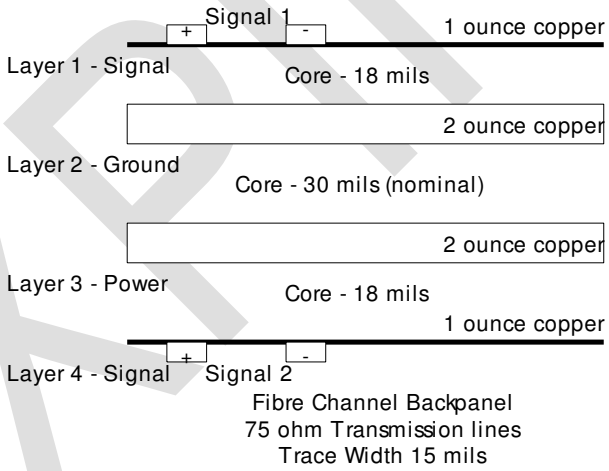


Figure 5. Backplane Microstrip.

10 Stripline Techniques

The impedance calculation for a preferred construction using stripline techniques is shown in Table 3. This should be a very useful construction for backplanes operating at high frequencies. 2 oz. copper should be used for the ground and power planes and 1/2 oz. or 1 oz. copper should be used for the signal planes. The construction details are shown in Figure 6.

FR-4 Material, with 75 ohm Stripline Transmission Lines		
Frequency	3.000	GHz
Dielectric Constant	4.30	
Trace Width	13.000	mils
Height above Ground	35	mils
Trace Length	100	mils
Predicted Z_0 Even Layers	90.18 ohms	
Predicted Z_0 Odd Layers	65.26 ohms	
Predicted Z_0	76.71 ohms	

Table 3. Sample Impedance – Stripline

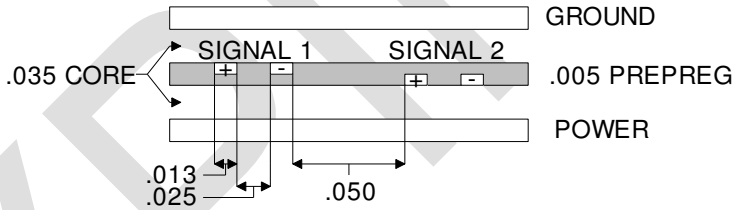


Figure 6. Stripline Backplane Construction - Example 1 - Recommended

Figure 7 shows an alternate stripline construction that has been proposed to minimize emissions. This involves locating the + signal and - signal conductors above each other rather than side-by-side. This method of board construction is discouraged because the differential impedance is lowered and the parasitic capacitive coupling between + signal and - signal is greatly increased due to the small spacing between the two traces. While it is true that the radiating loop area of the signal is minimized, the RF characteristics of this design suffer greatly. This construction should only be used for high density or tight areas.

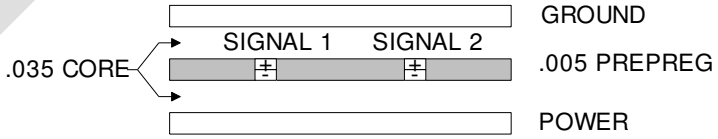


Figure 7. Stripline Backplane Construction - Example 2 - Use with caution

11 Impedance Matching

The world of RF is full of losses and instances where impedance is not perfectly matched. RF design needs to be flexible. For Fibre Channel backplanes, there are excellent designs implemented in both 150 ohm and 100 ohm variations. From a pure board layout perspective, 100 ohms can offer the advantages of layout density and use of thinner board layers, however, the Fibre Channel devices are typically 150 ohms differential. When impedance discontinuities exist, a decision must be made to accommodate the reflection or to match the impedance.

Impedance spreading is an approach to accommodate reflections. It is a gradual change in the impedance of the transmission lines to avoid sharp impedance mismatches that would cause severe reflections. Generally, impedance is changed by gradually increasing or decreasing the spacing between the high-speed data traces. This approach has more reflection than impedance matching, but if the transmitter is well matched, it can still result excellent transmit and receive eyes. The TDR trace in Figure 8 illustrates the results of this technique.

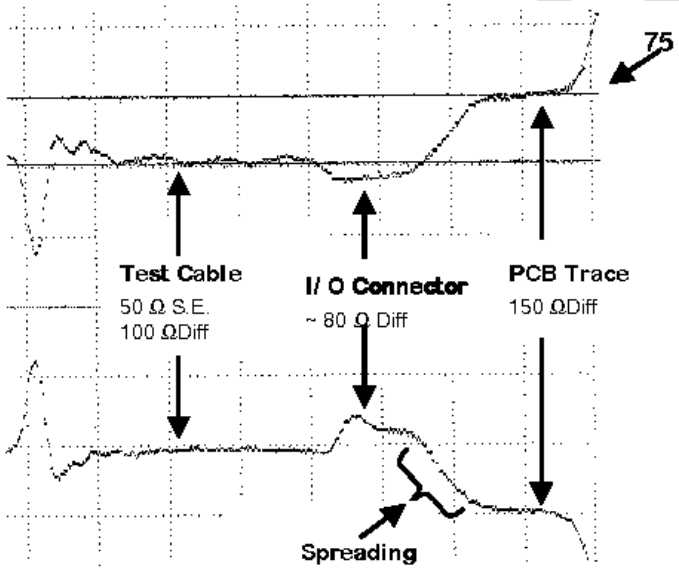


Figure 8. Example of Impedance Spreading

Closely coupled over/under transmission lines (one trace on one board layer and the other trace directly underneath it on an adjacent layer, 100 ohms differential) with impedance spreading have been observed to work well. One must be careful that over/under transmission lines are not too capacitive. This could destroy the rise/fall times at 2 gigabaud or higher transfer rates.

Another approach to dealing with impedance discontinuities is to use impedance-matching attenuators. These are commonly used to match impedance in RF designs. Impedance-matching attenuators work extremely well, but they reduce signal amplitude. This can be critical depending upon the total transmission line run and the losses. The pads, feedthroughs, and layout routing of impedance-matching attenuators must be done carefully in order to not destroy the impedance match due to parasitics. Reference Figure 9 for an example of an impedance-matching attenuator.

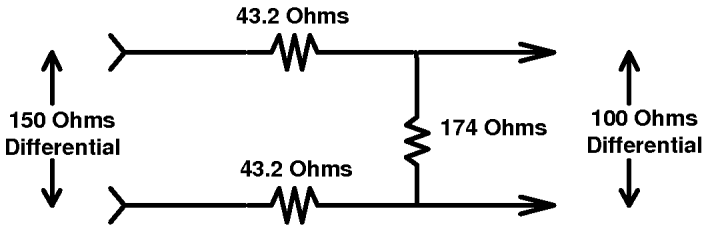


Figure 9. 150 to 100 ohm Impedance-Matching Attenuator

12 Internal Connectors

If a connector is rated at a lower impedance differentially and is also very short electrically, there are ways to raise its impedance by using smaller pads for the RF signal pins and using a minimum annular ring around the connector pin hole for interior layers of the PCB. This style of RF feedthrough helps to eliminate any sharp discontinuities that could cause reflections. Despite the mismatch of the connector, excellent transmit and receive eyes are achievable.

Twinax with the AMPMODU® style connector is often used for the intra-cabinet wiring. Using RF feedthroughs for the signal lines is recommended to achieve the least impedance discontinuity at the I/O connector. The natural impedance of this connector is approximately 100 ohms.

For board-to-board connectors within the enclosure, the SCA connectors and Metral style connector are successfully used at 1 gigabaud. Both of these are "100 ohm" connectors, but by controlling impedance discontinuities at the pads for the RF signals, their performance is acceptable. It is recommended to use a minimum size pad for these connectors on the RF signals. At 2 gigabaud or greater, be concerned about longer lead length and possible radiation. A shielded, impedance controlled connector is preferred at these frequencies.

13 External Connectors

The venerable DB-9 connector works at high frequencies, but it is very important to implement RF feedthroughs for the RF signals. Failure to do so can result in severe impedance discontinuities. Some DB-9's have leads that surface mount to the board. Use pads as small as possible for the RF signals and consider relieving the power and ground planes in the area of the pads to minimize parasitics that cause impedance discontinuities. Additionally, there may be problems with closure and the number of contacts on the DB-9 shielding shell. Insist upon a design that provides a robust, tightly fitting shell.

The HSSDC connector is electrically much better than the DB-9 connector, but originally suffered from lack of enclosed shielding attachment to the cabinet panels. That problem has been solved in several recent designs.

14 Reducing Parasitic Capacitance

Maintaining the characteristic impedance of a transmission line at gigabit rates requires minimizing parasitic capacitance. PCB structures such as drilled holes (feedthroughs) or surface mount pads for components and connectors cause parasitic capacitance. The affect of parasitic capacitance can be seen by considering the formula for characteristic impedance:

$$Z_o = \sqrt{\frac{L}{C}} \qquad \text{Equation (1)}$$

Where L = the distributed inductance of the transmission line and
C = the distributed capacitance of the transmission line.

The effect of parasitic capacitance on the characteristic impedance can be accounted for in the following manner:

$$Z_o = \sqrt{\frac{L}{C_T + C_p}} \qquad \text{Equation (2)}$$

where L = distributed inductance of the transmission line,
C_T = distributed capacitance of the transmission line, and
C_p = value of parasitic capacitance.

For a 150 ohm differential impedance in an FR4 board with a propagation speed of 180 psec/inch,

$Z_o = \sqrt{\frac{27\text{nh/in}}{1.2\text{pF/in}}}$ =150 ohms

If a differential parasitic capacitance of 1.2 pF is encountered at regular 1 inch intervals on the above transmission line, the new impedance from this point forward can be approximated by adding this parasitic capacitance into equation (2).The new characteristic impedance is:

$Z_o^1 = \sqrt{\frac{L}{CT_T + C_P}} = \sqrt{\frac{27{,}000\,\text{ph/in}}{1.2\text{pF/in} + 1.2\text{pF/in}}}$

$Z_o^1 = \sqrt{\frac{27{,}000}{2.4}} \cong 106$ ohms.

While parasitic capacitance does not occur at regular intervals, from the above formulation, it is seen that even a small 1.2 pF parasitic capacitance can cause a sharp decrease in characteristic impedance, and hence, reflections, causing loss of signal integrity.

The feedthrough is a common source of stray parasitic capacitance. See Figure 10.

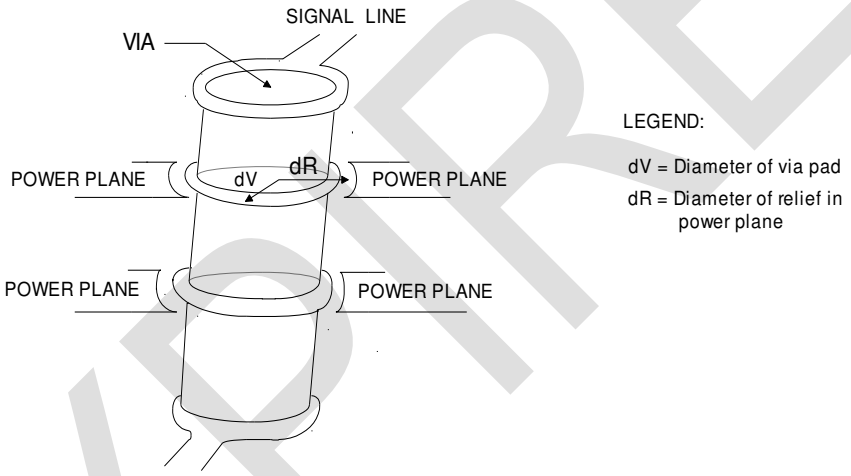


Figure 10. Feedthrough Parasitic Capacitance.

A formula is given in the textbook, Johnson and Graham, *High Speed Digital Design*, Prentice Hall, pages 257-258, ISBN 0-13-395724-1, which gives the value of feedthrough capacitance within an order of magnitude. It is listed in the following equation:

$C_{VIA} = \frac{(1.41\ Er\ T)\ (dV)}{(dR-dV)}$ Equation (3)

Where Er = Dielectric constant of PCB
T = Thickness of PCB
dV = Diameter of the feedthrough pad
dR = Diameter of the relief in the power plane.

The exactness of equation (3) is not critical; the method of controlling the capacitance given in the equation is. To see this, split the formula:

$C_{VIA} = (1.41\ Er\ T)\left(\frac{dV}{dR-dV}\right)$

$= C_{inherent} \times \left(\frac{dV}{dR-dV}\right)$

$= C_i \left(\frac{dV}{dR-dV}\right)$

The inherent capacitance, C_i, is multiplied by the ratio of the feedthrough pad size to the relief pad size minus feedthrough pad size. Call this the ratio Ri where Ri = $\left(\frac{dV}{dR - dV}\right)$.

For example, in a PCB, a possible feedthrough construction could be:

- Drill size: .38 mm diameter
- Finished hole size: .25 mm diameter
- feedthrough pad size: .76 mm diameter
- relief pad size: 1.14 mm diameter.

The Ri in this case is:

$$\frac{.76}{1.14 - .76} = \frac{.76}{.38} = 2$$

This relief pad size essentially doubles Ci. If the relief pad size is increased, the situations shown in Table 4 can be achieved.

Relief Pad Size (mm)	Ri	C_{FINAL}
1.52	1	C_i
1.91	2/3	2/3 C_i
2.29	½	$C_i/2$
3.05	1/3	$C_i/3$

Table 4. Effects of Increasing Relief Pad Size.

The amount of capacitance in a feedthrough can be multiplied or divided by changing the size of the relief pad in the power plane. For high frequency signals, if feedthroughs are unavoidable, the parasitic capacitance of the feedthrough should be minimized to avoid impedance discontinuities in the controlled impedance path. Typical examples of RF Feedthroughs are shown in Table 5.

	Low Cost RF Feedthrough	High Performance RF Feedthrough
Hole	0.46 mm	0.25 mm
Pad	0.76 mm	0.50 mm
Relief	1.50 mm	2.54 mm
Capacitance	2-4 pF*	1-2 pF*
Note: * = Dependent upon board stack-up.		

Table 5. Recommended RF Feedthroughs.

Through-hole connectors can also exhibit large parasitic capacitance values. The parasitic capacitance of connector through-hole feedthroughs can be minimized by expanding relief pads in the power plane. When the relief pads are large enough to touch between the through-holes of adjacent connector pins, parasitic capacitance approaches its minimal value. The power planes are then absent between the connector pin feedthroughs. The capacitance of the parallel feedthroughs is now primarily determined by the capacitance between these parallel feedthroughs and any fringing capacitance to the power planes in other directions.

The pads of surface mount devices are another source of capacitance that can cause impedance discontinuities in trace lines or add excess load capacitance at the end of the transmission lines. Consider Figure 11 which shows parallel transmission lines connecting to two sets of 0805 pads to accommodate a pair of coupling capacitors.

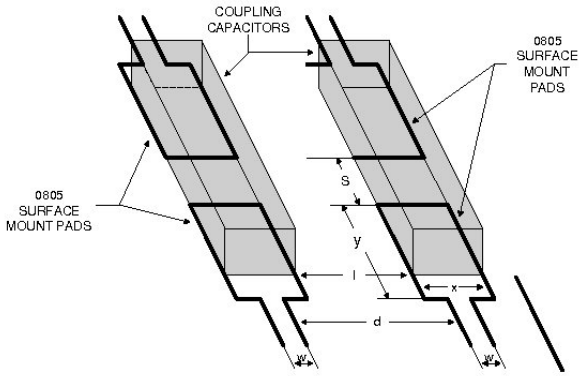


Figure 11. Parallel Transmission Lines-0805.

The parallel transmission line is composed of two transmission lines of width *w* and separation *d* at a distance *z* (not shown) above a power plane. The parameters *w*, *d*, and *z* are chosen to achieve a characteristic impedance of 150 ohms. This relationship exists before and after the 0805 PCB structures. However, at the structures: *w* is now *x* , *d* is now reduced to *l*, the separation of the 0805 structures, and *z* is unchanged.

This new condition exists for the length of the 0805 structure: 2 *y* + *s*. The characteristic impedance for this distance is much lower due to the excess capacitance created by the wider trace path and the narrowing of the separation between the traces (pads). If space permits, moving the 0805 structures apart can alleviate the narrowing of the separation between the traces. This is usually possible for coupling capacitors, which can be placed anywhere in the transmission path. It may not be possible for resistors at the source of the high frequency signal, as they must be placed near the signal source. Figure 12 shows separated 0805 structures with *l* similar to *d*.

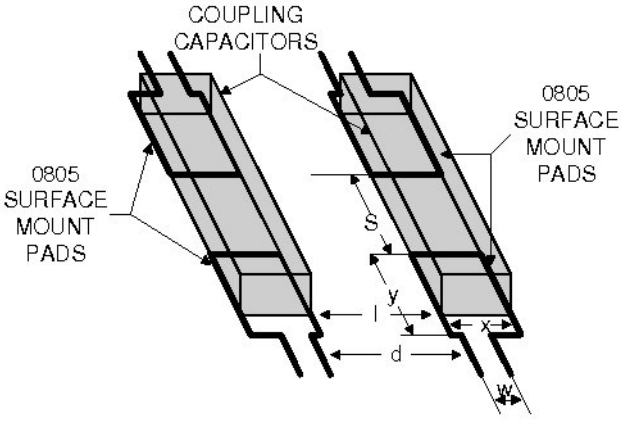


Figure 12. Separated 0805 Structure.

To reduce capacitance, the near power plane under the 0805 structures can be removed as shown in Figure 13.

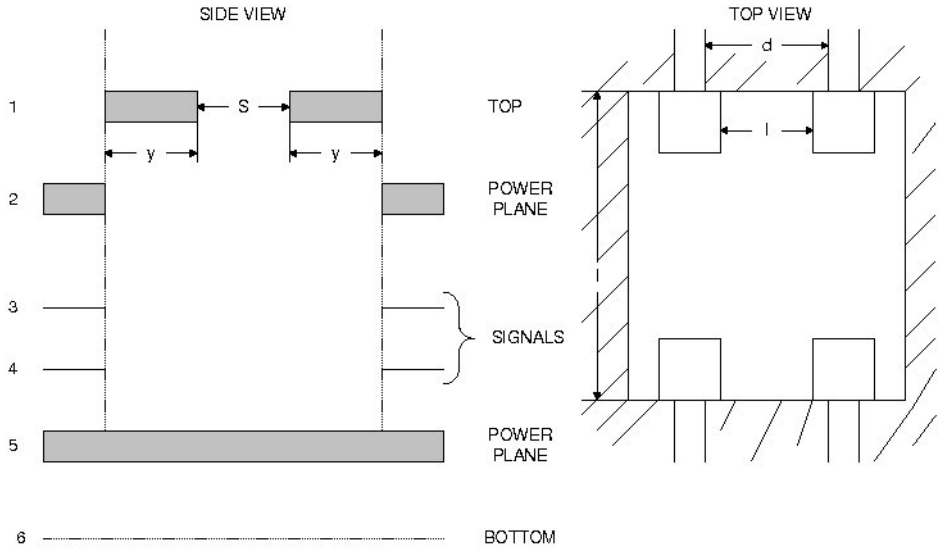


Figure 13. 0805 Power Plane Removed.

The capacitance of the 0805 structure to the power plane is reduced by this technique because the distance *d* between the 0805 structure and the nearest power plane has been increased: $C = \left(\frac{EoA}{d}\right)$. Generally, signals should not be routed under such cutouts as they are a region in the board where the normal impedance of the inner layer has been changed. Also, signals routed under the cutouts are not shielded from the 0805 pads by a power plane, greatly increasing the coupling between the high frequency signal and the signal routed under the cutout. The plane can similarly be removed under the pads of integrated component packages.

In addition to the above methods, avoiding the grouping of components into a small area can decrease the capacitance in a region. Consider the layout shown in Figure 14.

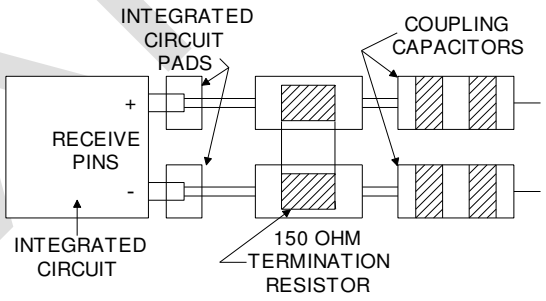


Figure 14. Component Group Placing.

In this small area, the load capacitance seen by the signal is C parasitic integrated circuit (C_{pic}), C parasitic resistor (C_{pr}), C parasitic coupling capacitors (C_{pcc}), and C input capacitance (C_i). So $C_{load} = C_{p(ic)} + C_{p(r)} + C_{p\ (cc)} + C_i$. This load capacitance can be reduced by the above mentioned technique and distributed by moving them as shown in Figure 15.

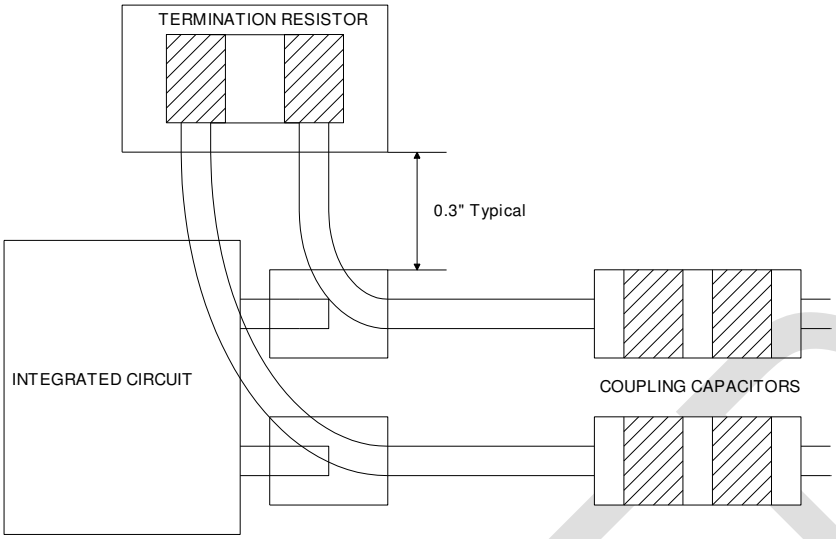


Figure 15. Distributing Components.

The lumped capacitance at the integrated circuit (IC) input pins is now $C_{load} = C_{p(ic)} + C_i$. The degradation caused by C_{pr} does not occur until after the signal passes the IC. Also, the affect of small, electrically short discontinuities are generally less extreme than a large, electrically longer, single discontinuity. By placing the termination away from the IC, the signal is terminated at a point where the transmission line impedance is again 150 ohms. (Termination is not at the IC pads where the impedance is reactive due to the lumped non-distributed elements at that point.)

15 PCB Manufacturing Factors

PCB suppliers may not have the equipment to test board impedance differentially. Most, however, are quite adept at achieving and measuring single ended impedance. It is recommended that the impedance of differential lines be specified as a single ended impedance. If the single ended impedance is specified to be 75 ohms (1/2 of 150 ohms), the differential impedance will be less than 150 ohms. This results from the fact that, in a PCB, the differential impedance of two lines routed in parallel is controlled by the physical distance of the traces from the power plane and by the physical separation of the complementary trace lines. Refer to Figure 16.

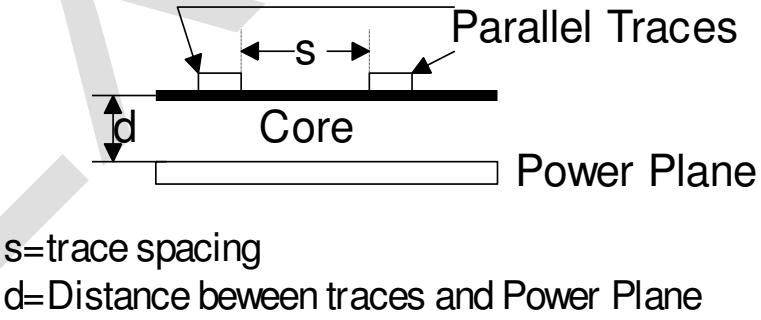


Figure 16. Differential Impedance Factors.

When a TDR is performed differentially, the net effect of these two physical factors will be displayed. When these same two lines are observed singly (without a complementary signal on the parallel line), the physical factor controlling impedance will be the distance of the traces to the power plane. This single-ended impedance is higher than 75 ohms. (If the separation guidelines listed in this document are followed, the single ended impedance tends to be 10% high, or about 83 ohms.) The

single-ended impedance is the target specification that should be given to most PCB suppliers.

Tools used in designing PCB layouts that will provide a 150 ohm differential line pair set can also be used to predict the single-ended impedance that should be specified to the PCB supplier. After the tool has been used to achieve the desired line width and spacing requirements to achieve 150 ohms differential impedance, remove one of the signal lines and rerun the tool to find the single-ended impedance. (Hint: the resulting single-ended impedance should not be 75 ohms unless the distance between the traces is much larger than the height of the traces above the power plane. If this is not the case, the tool may not be modeling the differential impedance accurately.)

If the high frequency differential lines are covered with solder mask, this will affect the final impedance. See Figure 17.

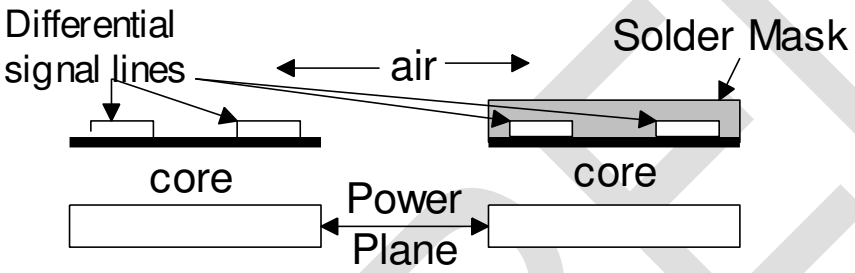


Figure 17. Solder Mask Impact on Differential Impedance.

This additional dielectric will lower the impedance of the differential pair, as less of the electric field will now pass through the air. If the differential traces are on the top or bottom surface of the PCB, the affect of the solder mask (if used) on the final impedance must be accounted for.

16 Skin Effect

At high frequencies, skin effects begin to dominate, making the surface area of traces of high importance. The skin depth is defined as the depth in a conductor at which the current density is attenuated by 1 neper ($1/e = -8.7$ decibels) from its surface value. Table 6 shows the skin depth, δ, as a function of frequency. Note that the skin depth is inversely proportional to the square root of the frequency. The current distribution is exponential, dropping to essentially zero after some 6-9 skin depths.

Frequency	Skin Depth δ,in mm
1 KHz	2.1082
1 MHz	0.066
10 MHz	0.0211
100 MHz	0.0066
1 GHz	0.0021

Table 6. Skin Depth δ, at Various Frequencies.

This explains why increasing copper thickness does not lower impedance when the copper thickness already exceeds skin depth by a factor of 6 or more at the frequency of interest.

It also explains why the impedance (actually pure resistance) rises with the square root of frequency ratio, subject to the limiting condition of the lower frequency skin depth being 10-15% of trace thickness or less.

As an example, consider the cases of a printed circuit trace of a given width and two copper thicknesses, 1/2 oz. copper and 1 oz. copper. Doubling the trace thickness at 100 MHz results in less than an 8% drop in impedance, and at 1 GHz, results in no decrease in impedance. In addition to trace resistance becoming more dependent on surface area than on cross-sectional area at higher frequencies, there is the complicating factor that smaller geometries become better radiators at higher frequencies. One consultant has suggested a 1/20 wavelength rule: if a trace has a length exceeding 1/20 wavelength for a frequency of interest, it has the potential to become a strong radiator. Following this rule results in the guidelines in Table 7. It is clear from Table 7 that the 1 GHz signal, and the higher harmonics of that signal are prone to radiate.

Frequency	Limiting Length of Traces, mm
1 KHz	1.51×10^7
1 MHz	1.51×10^4
10 MHz	1.51×10^3
100 MHz	151
1 GHz	15.1

Table 7. 1/20th Rule.

The physical length of traces required to traverse the length of the backplane limit the designer to relying on means other than limiting the antenna's physical dimensions; the rule is presented here because it can be effectively used in areas other than the high frequency sections of designs.

17 Layout Considerations

As previously mentioned, it is important to keep trace routing as simple and free-flowing as possible when dealing with high frequencies. Every impedance discontinuity, including a severe change in direction of current flow, can result in increased emissions. The routings suggested in Figure 18 will help to minimize such effects. The guidelines presented here are designed to minimize emissions.

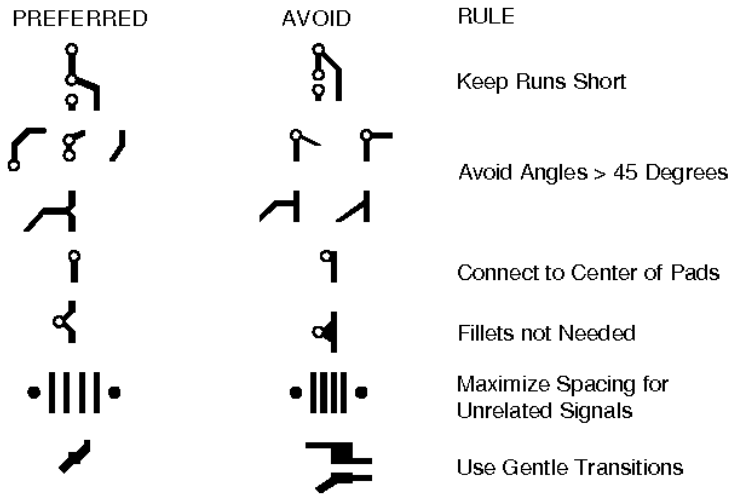


Figure 18. Trace Routing Rules.

It is imperative that connections between the traces and components be done properly. Careful attention must be paid to interconnections between components and to interconnections between components and ground. All leads contain inductance and this inductance becomes a measurable factor at high frequencies.

The principles of Figure 19 should be universally applied unless true *star* grounding can be accomplished. At DC, a ground is just a ground. At higher frequencies, beware of the traces connecting components to ground. Trace inductance can make these connections perform electrically different than a true ground connection. Up to 6 dB has been measured across a 9.5 mm long trace connecting the low side of a decoupling capacitor to the nearest ground feedthrough. For decoupling capacitors in particular, the grounded side must connect to ground directly through the shortest path possible, preferably a ground feedthrough.

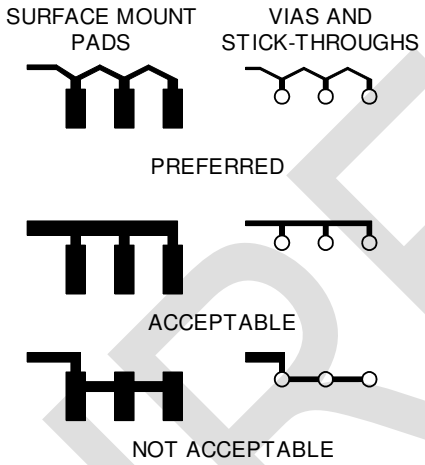
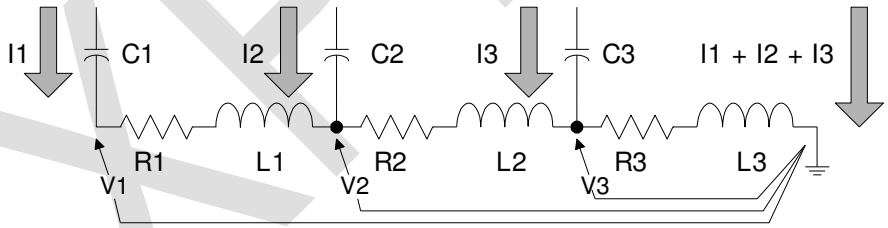


Figure 19. Grounding Connections and Interconnections.

Figure 20 illustrates why star grounding is preferred by presenting the schematic of a series arrangement, including the inductance but not parasitic capacitance.



$$V1 = V2 + I1(R1) + L1(d(I1)/dt)$$
$$V2 = V3 + (I1 + I2)(R2) + L2(d(I1+ I2)/dt)$$
$$V3 = (I1 + I2 + I3)(R3) + L3(d(I1+ I2 + I3)/dt)$$

Figure 20. Series Grounding Schematic.

Note that the voltage at the closest node to ground, V3, depends on the total current (I1 + I2 +I3) through R3 and L3. The circuit of C1 is faced with a similar situation, but with V3 plus the IR and L losses of the C2 circuit impressed on it as noise. Clearly, this situation cannot be tolerated where the L(dI/dt) factors get large, which is precisely the case at higher frequencies.

It is important to consider the overall grounding scheme of the backplane. Power and ground are usually brought to the backplane through a pluggable connector from the power supply. Connecting the chassis ground directly to the backplane through the backplane mounting provisions is also recommended. Figure 21 provides a suggestion for chassis grounding provision when the backplane is mounted to the chassis by screws. Note the number of ground feedthroughs suggested. This is due to the surface area constraint at high frequencies.

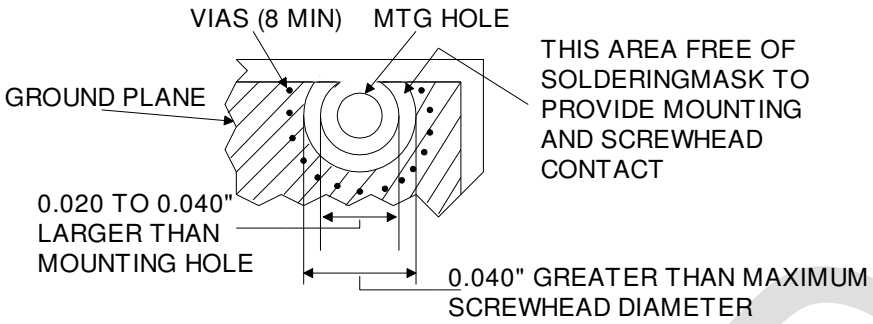


Figure 21. Backplane Grounding Provisions.

18 Signal Return Integrity

In the Trace Separation section of this document, it was mentioned that there are conflicting requirements on trace separation for the purposes of RF transmission line design. There are also associated EMI factors that must be dealt with. Figure 22 shows two situations involving a differential pair.

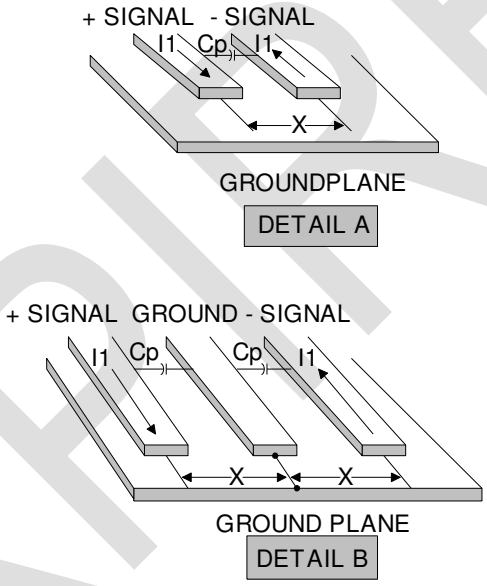


Figure 22. Differential Pairs Signal Return.

Detail A in Figure 22 shows a differential pair located above a ground plane. Crosstalk is reduced about 90% from what it would be with the same trace geometry but without the ground plane present. Remaining crosstalk is due to the parasitic capacitance Cp coupling the two traces. As separation X of the traces increases, the parasitic capacitance decreases.

At the same time the radiated emissions of this circuit are dependent on two inter-related factors - the frequency and the dimensions of the radiating loop formed by the signal path and return path. Assuming that the dimensions are significant with respect to the wavelength involved, the radiating loop dimensions become the major controllable factor. The spacing and the trace length determine the area of this loop. As X is increased, the area of the radiating loop increases directly for a given length of trace and return path. Crosstalk and EMI radiation tend to be at direct odds. What improves one of these factors may significantly worsen the other.

Where differential pairs are routed without an intervening ground trace, it is imperative that these two factors be balanced. If crosstalk immunity of the circuits involved is inherently high, then concentrate on reducing trace spacing to improve radiated emissions. If package design is good enough to tolerate increased emissions

from components within, concentrate on increasing trace spacing where crosstalk may be a problem.

Detail B of Figure 22 shows the same differential pair, but with an intervening ground trace. Note that crosstalk is virtually eliminated, since the vast bulk of the parasitic capacitive coupling from each trace is now to the intervening ground trace. This ground trace must be stitched (connected to the plane at multiple distributed points along the trace) to the ground plane to be effective. The area of the radiating loop has now doubled in respect to detail A, since the signal and its return are now spaced about 2X apart.

This is obviously bad for radiated emissions, but there are some compensating advantages to this arrangement. If spacing X is now reduced, crosstalk is still held to near zero since coupling is predominantly to the intervening ground trace. The radiating loop area is reduced, improving emissions. Contrast this to the case in the upper illustration, where changing X improves one factor and worsens the other. With an intervening ground trace, the minimum possible spacing between traces should be used, consistent with other requirements such as EMI immunity and ESD, and the width of the ground trace should never exceed the width of the signal trace.

Signal return integrity requires that the return path for the signal follow the signal path as closely as possible (this is another way of saying the radiating loop area must be minimized). With differential pairs, routing controls this factor. Differential pairs should always be routed parallel with minimum spacing where possible. This rule applies whether or not an intervening ground trace is present.

When unrelated signals are considered instead of differential pairs, signal return integrity increases in importance. Figure 23 shows unrelated signal pairs, both with and without an intervening ground trace.

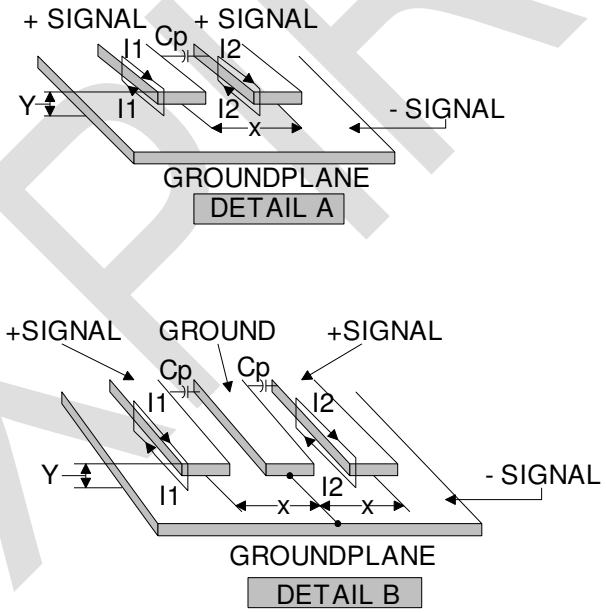


Figure 23. Unrelated Signal Returns.

Detail A in Figure 23 shows signal 1, with its associated current I1, and signal 2, with its associated current I2. Each signal current is imaged in the groundplane by an equal return current. This return current will take the lowest impedance path back to the signal source, and that is normally the shortest path as well. Note that the currents have no interference with each other, and that the only coupling between the two signals is crosstalk via the parasitic capacitance Cp. Again, increasing spacing X minimizes this crosstalk, and X can be varied as desired without affecting the integrity of the current return paths.

The radiating loops of these signals are independent of spacing X, and are determined simply by the layer-to-layer separation Y and the length of the traces.

Detail B in Figure 23 adds an intervening ground trace to the case shown in Detail A. It should be immediately clear that the radiating loops are independent of spacing X, and that crosstalk should be essentially eliminated, independent of X. The intervening ground trace should be stitched to the groundplane, but now the width of the trace is essentially unimportant (as long as it is wide enough for the magnetic flux lines from the signal traces to terminate upon). This technique can be especially valuable in areas where unrelated signals are inherently closely spaced (I/O lines for example).

The signal return currents tend to closely follow the routing of the signal traces if possible. There is some fan-out, but it is not significant in design considerations; the current distribution is essentially an image of the signal current. If the signal return current cannot follow the image path, then it must find the lowest impedance route to return to the signal source.

Small deviations in geometry may not noticeably contribute to increased emissions. If the ground plane is so obstructed that the return current is forced into an area from which it selects a low-impedance path to the signal source that does not closely match the signal path, then a large-area radiating loop occurs. Emissions will be greatly increased. Figure 24 is an example of a single slot interrupting a ground plane, and the consequent re-routing of the return signal.

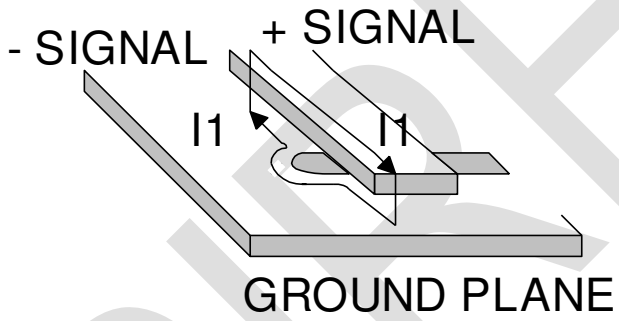


Figure 24. Ground Plane Discontinuity.

As shown in Figure 24 it is apparent that a radiating loop has been increased in size. Imagine how large it could be if the lowest impedance path from the point of maximum departure from the signal path back to the signal source had been parallel to the signal path.

These types of interruptions of return currents for high frequency signals must be avoided in the design of a backplane. Obviously, a slot is an easy obstruction to avoid, or at least one that is easy to not route signals over. This can be much more subtle, though. Some designs may feature separated ground planes for various sections of circuitry. The only proper way to route signals over such separations is across a bridge of some kind. Otherwise, the radiating loop can go all the way back to system power supply ground! Designs that are very dense (usually not the case for backplanes) and feature many feedthroughs can create the same effect by allowing ground plane clearance holes for feedthroughs to touch; the interruption to return currents is as if a separation was designed to be present.

19 Port Bypass Circuits

Some port bypass circuits (PBC's) have equalizers built in which can be very beneficial to restoring eye margins as signals are passed through long routes, connectors, or successive PBC's. Additionally, care must be taken to avoid "near end" transmitter reflections. Traditionally, this has been accomplished by the use of series resistors. The classical approach has been to put external pull-down resistors on the transmitter output and then a series resistor that matches the line impedance (1/2 of differential impedance less the internal on resistance of the transmitter {approximately 6 ohms}). Another approach that has been found to work well is to put the series resistor out of the transmitter first and then place the pull-down resistors afterwards as illustrated in Figure 25. Sizing of the pull-down resistor may result in relatively large currents, but good impedance matching can result.

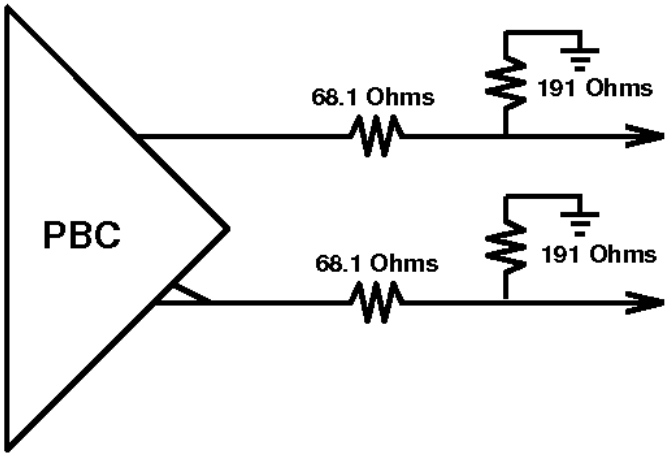


Figure 25. Output Impedance Matching Example

Some PBC's have all of the external pulldowns and terminations built into the PBC. This technique can result in superior eye quality that is very tolerant to impedance mismatches. If required for the application, it is highly recommended that PBC's with either internal termination or fly-through termination be used. Signals at 2 gigabaud are very sensitive to parasitics. Feedthroughs, pads for components, and other impedance discontinuities should be spaced such that the high frequency trace runs a distance of at least 5 mm between the discontinuity geometries to minimize the effect of lumping parasitic capacitance. Likewise, decoupling capacitors should be spaced further apart than normal transmission line spacing and located at least 5 mm away from the PBC to minimize lumping.