SFF specifications are available at http://www.snia.org/sff/specifications
or ftp://ftp.seagate.com/sff

This specification was developed by the SFF Committee prior to it becoming the SFF TA (Technology Affiliate) TWG (Technical Working Group) of SNIA (Storage Networking Industry Association).

The information below should be used instead of the equivalent herein.

POINTS OF CONTACT:

Chairman SFF TA TWG
Email: SFF-Chair@snia.org

If you are interested in participating in the activities of the SFF TWG, the membership application can be found at:
http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on can be found at:
http://www.snia.org/sff/specifications/SFF-8000.TXT

The operations which complement the SNIA's TWG Policies & Procedures to guide the SFF TWG can be found at:
http://www.snia.org/sff/specifications/SFF-8032.PDF

Suggestions for improvement of this specification will be welcome, they should be submitted to:
http://www.snia.org/feedback

SFF Committee documentation may be purchased in hard copy or electronic form.
SFF specifications are available at ftp://ftp.seagate.com/sff

SFF Committee

SFF-8437 Specification for

Small Formfactor Pin Through Hole Transceivers

Rev 1.1 November 13, 2006

Secretariat: SFF Committee

Abstract: This specification documents the legacy and emerging mechanical and electrical requirements of SFT (Small Formfactor Transceivers) pin through hole transceivers. It documents the public ad-hoc Multi Source Agreement of July 2000 for reference and adds alternative pin outs and requirements as needed to meet the needs of the networking, storage and communications industry.

This specification provides a common reference for systems manufacturers, system integrators, and suppliers. This is an internal working specification of the SFF Committee, an industry ad hoc group.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

Support: This specification is supported by the identified member companies of the SFF Committee.

POINTS OF CONTACT:

Hossein Hashemi
Emulex
3333 Susan St
Costa Mesa CA 92626
714-885-3609
hossein.hashemi@emulex.com

I. Dal Allan
Chairman SFF Committee
14426 Black Walnut Court
Saratoga CA 95070
408-867-6630
endlcom@acm.org

EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

Comax
EMC
Foxconn
Hewlett Packard
Hitachi GST
LSI Logic
Picolight
Sumitomo
Sun Microsystems
Tyco AMP

The following member companies of the SFF Committee voted to abstain on this industry specification.

Clariphy
FCI
Fujitsu CPA
Gennum
Hewlett Packard
Hitachi Cable
Intel
Molex
Seagate
Toshiba America
Unisys

Foreword

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:

www.sffcommittee.com/ie/join.html

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:

ftp://ftp.seagate.com/sff/SFF-8032.TXT

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

Table of Contents

1.0 Scope

This specification replicates the operational requirements for SFT (2x5/2x10) Pin Through Hole Form Factor transceivers as documented in the original July 5, 2000 Multi-source Agreement. The purpose of generating this document is to make public a baseline from which industry enhancements in pin definitions can be made.

1.1 Description of Clauses

Clause 1 contains the Scope and Purpose.
Clause 2 contains Referenced and Related Standards and SFF Specifications.
Clause 3 contains the General Description.

2.0 References

The SFF Committee activities support the requirements of the storage industry, and it is involved with several standards.

2.1 Industry Documents

The following interface standards may be relevant to this specification.

- INCITS 230-1994	FC-PH Fibre Channel Physical Interface
- INCITS 297-1997	FC-PH-2 Fibre Channel Physical Interface
- INCITS 352-2002	FC-PI Fibre Channel Physical Interface
- INCITS Project 1506-D	FC-PI-2 Fibre Channel Physical Interfaces
- INCITS 364-200x	10GFC Fibre Channel - 10 Gigabit
- IEEE-802.3 Edition 2002	Ethernet Specification - 10M, 100M, 1G, 10G
- Telcordia GR-253-CORE	Synchronous Optical Network (SONET) Transport Systems
- ITU-T G.691	Transmission Systems/Media, Digital Systems/Networks
- SFF Committee INF-8074	SFT (Small Formfactor Transceivers)Transceiver
- SFF Committee SFF-8472	Diagnostic Monitoring Interface for Optical Xcrvs

2.2 SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at ftp://ftp.seagate.com/sff/SFF-8000.TXT

2.3 Sources

Those who join the SFF Committee as an Observer or Member receive electronic copies of the minutes and SFF specifications (http://www.sffcommittee.com/ie/join.html).

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://tinyurl.com/c4psg).

Copies of SFF, ASC T10 (SCSI), T11 (Fibre Channel) and T13 (ATA/SATA) standards and standards still in development are available on the HPE version of CD_Access (http://tinyurl.com/85fts).

3.0 General Description

An industry ad-hoc group comprised of eight companies ratified the “Small Formfactor Transceiver Multi-source Agreement” dated July 5, 2000. The outcome was an electrical and mechanical solution covering 2x5 and 2x10 pin options for providing embedded (i.e. soldered) solutions compatible with high-density fiber optic connectors, such as MTRJ and LC systems.

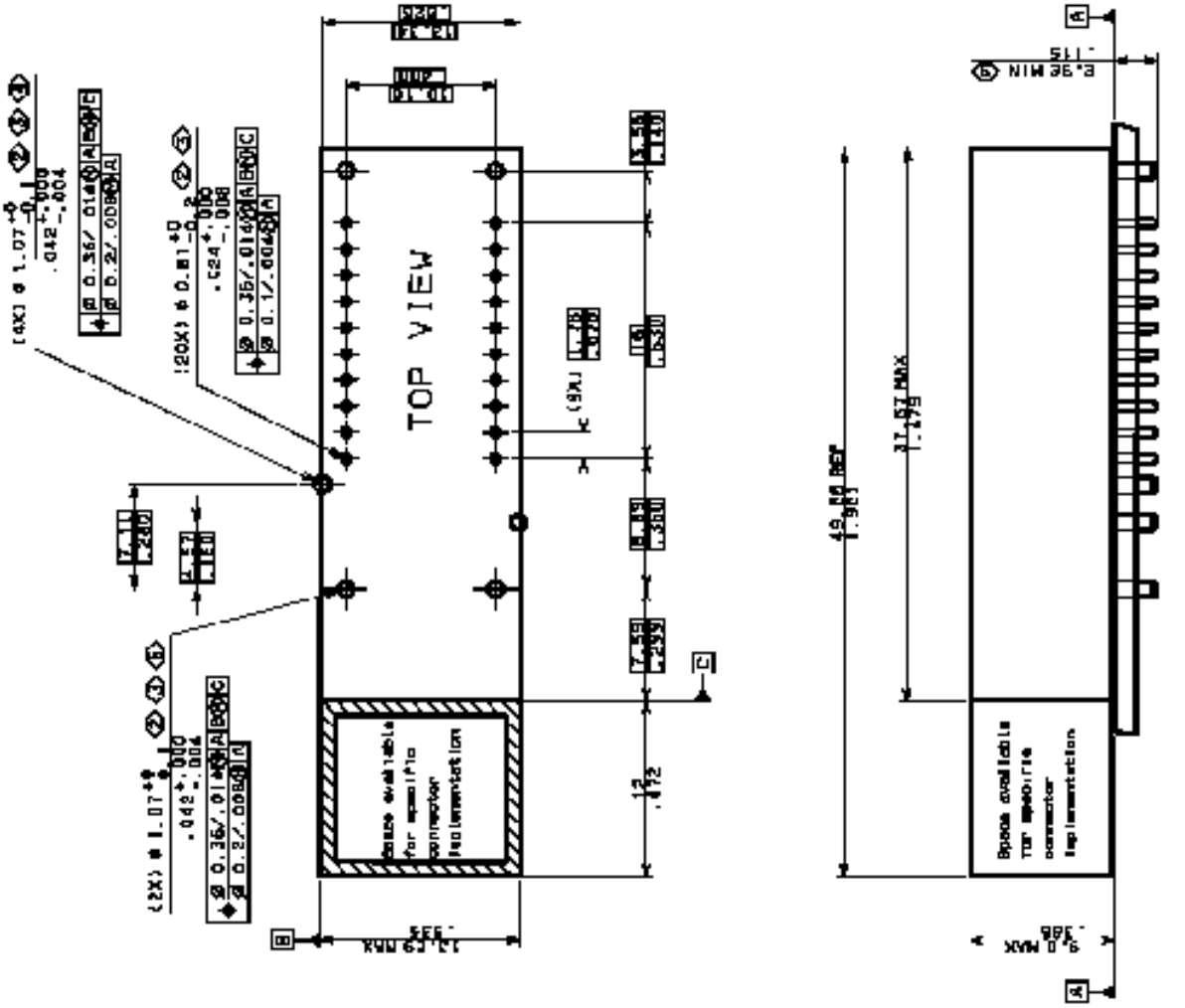
The document is divided into two parts. The first part documents the literal requirements of the original July 5, 2000 MSA, covering *Package Outline*, *Circuit Board Layout* and *Pin Function Definitions* as outlined in that document.

The second provides for emerging alternative pin definitions and functionality as needed to support emerging applications not foreseen by the original MSA.

4.0 Small Formfactor Transceiver Multi-source Agreement

This clause documents the mechanical and electrical requirements of the original July 2000 agreement. These should not be modified. Other clauses will be used to reflect any updates or changes needed to meet emerging industry demands.

4.1 Package Outline [MSA Appendix A.1.1]



1. THIS PAGE DESCRIBES THE MAXIMUM PACKAGE OUTLINE. MOUNTING STUDS, PINS AND THEIR RELATIONSHIPS TO EACH OTHER.
2. TOLERANCED TO ACCOMMODATE ROUND OR SQUARE LEADS.
3. ALL 26 PINS AND POSTS ARE TO BE TREATED AS A SINGLE PATTERN.
4. OPTIONAL POSTS FOR HOUSING LEADS MUST BE TIED TO SIGNAL GROUND.
5. POSTS FOR STUDS ARE RECOMMENDED TO BE TIED TO CHASSIS GROUND.
6. SEE SFF TRANSCEIVER PIN FUNCTION DEFINITION TABLE FOR DETAILS.
7. IF DATUM C DOES NOT EXIST FOR A SPECIFIC CONNECTOR IMPLEMENTATION, AN ALTERNATE SURFACE OR FEATURE CAN BE CHOSEN TO ESTABLISH A DATUM FOR THE 26 PIN PATTERN
8. DATUM A IS ESTABLISHED BY THE TOP SURFACE OF THE HOST BOARD.
9. NOTES DIMENSION APPLIES TO ALL 26 PINS AND POSTS.

SMALL FORM FACTOR
TRANSCEIVER
MAY. 08 2000
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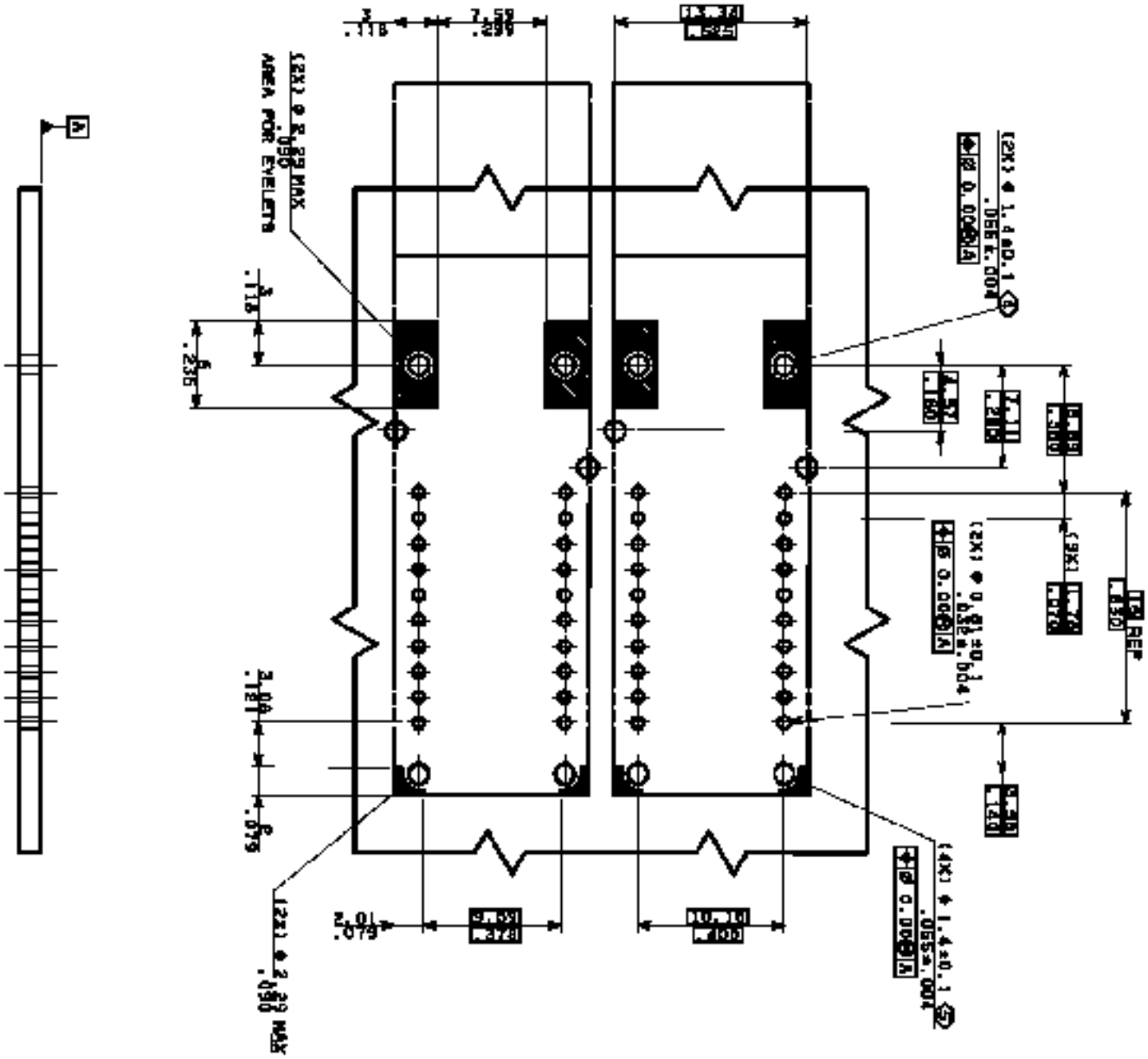
4.2 Circuit Board Layout Package Outline [MSA Appendix A.1.2]



1 THIS PAGE DESCRIBES THE RECOMMENDED CIRUIT BOARD LAYOUT FOR THE SFF TRANSCEIVER.

2 THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUSING STANDOFFS. NO METAL TRACES OF GROUND CONNECTION IN KEEPOUT AREA.

3 20 PIN MODULE SHOWN. 10 PIN MODULE REQUIRES ONLY 18 PCB HOLES.

④ HOLES FOR MOUNTING STUDS MUST BE TIED TO CHASSIS GROUND.

⑤ HOLES FOR HOUSING LEADS MUST BE TIED TO SIGNAL GROUND.

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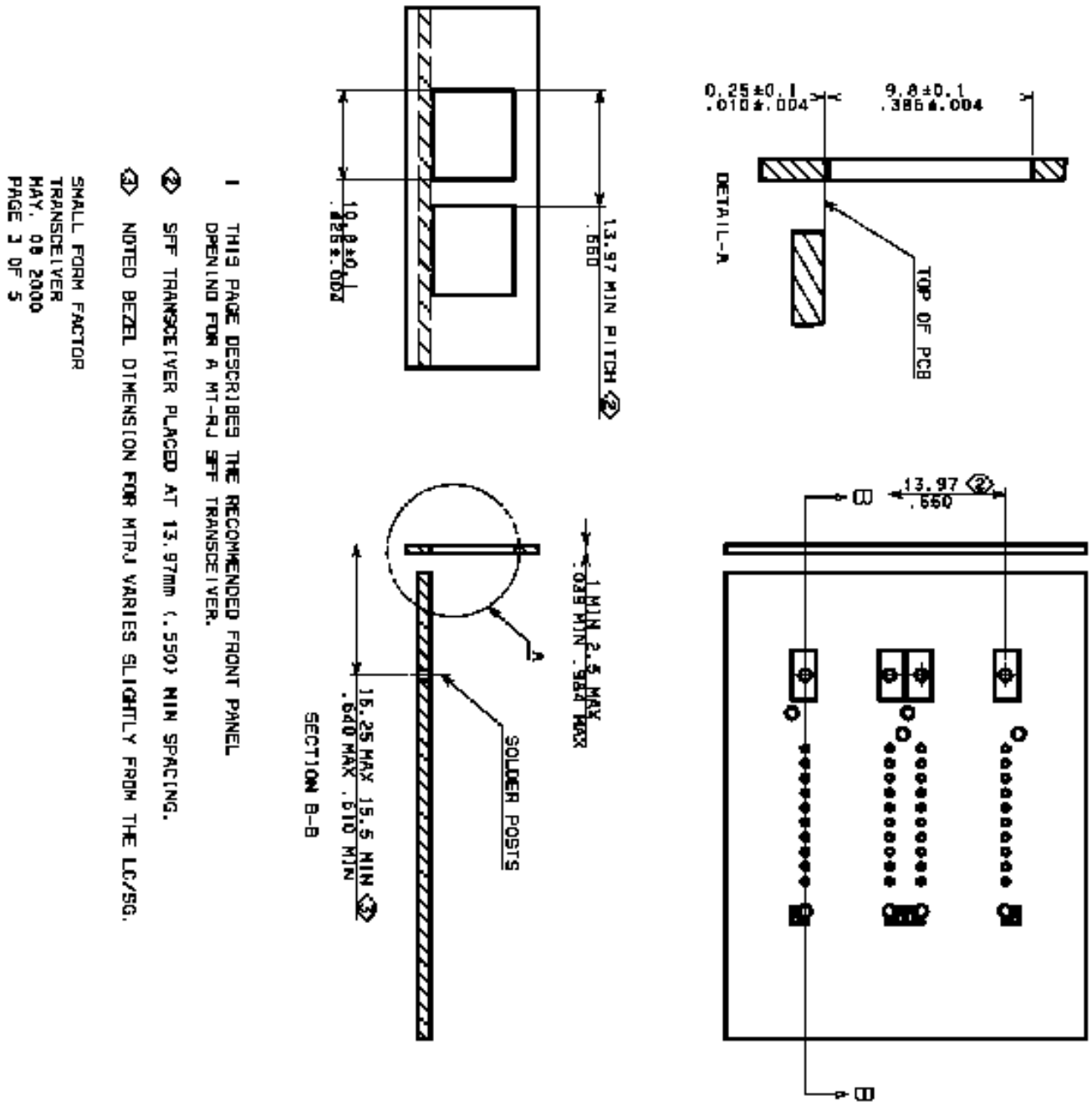
4.3 Front Panel Opening for MT-RJ [MSA Appendix A.1.3]

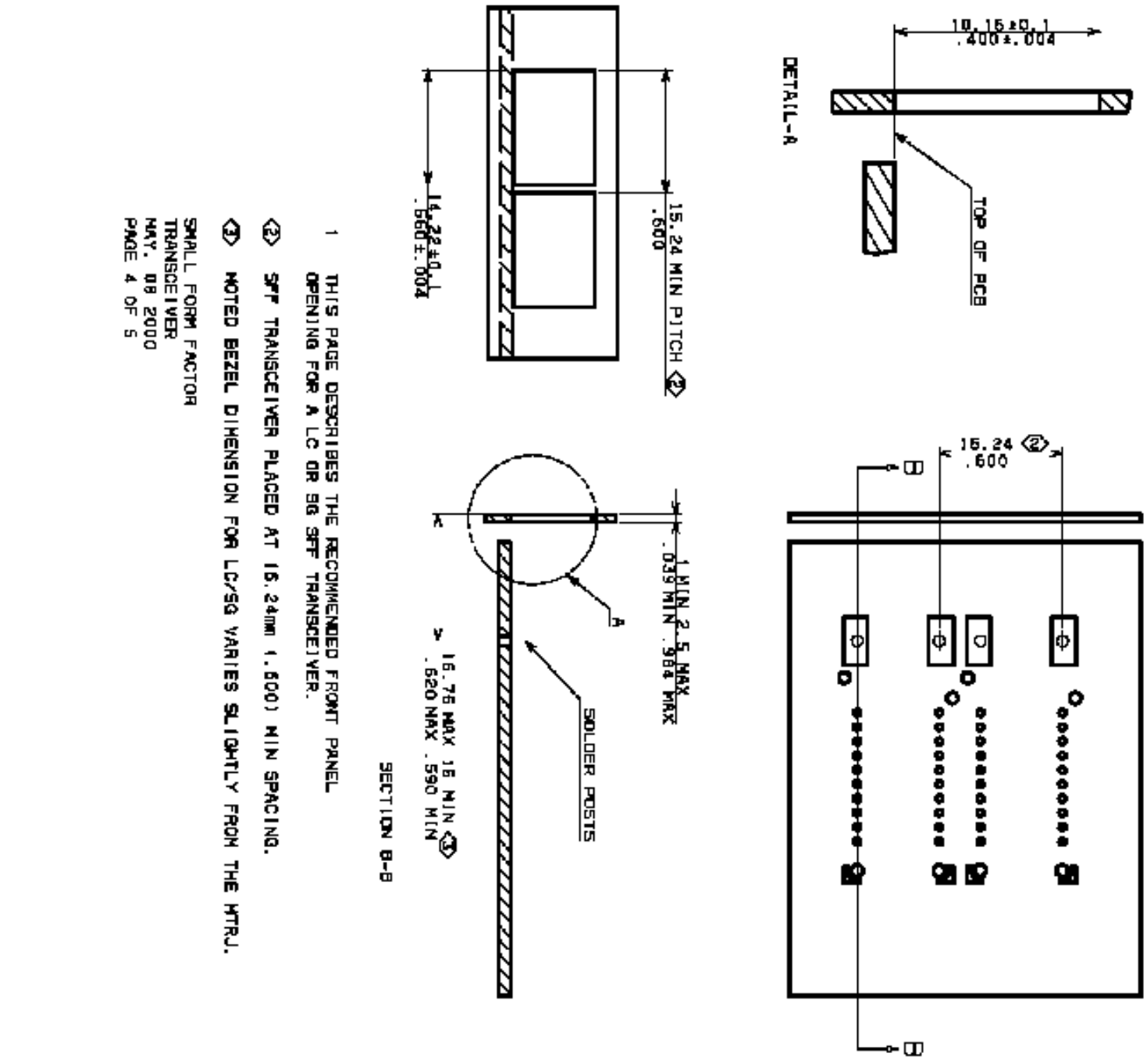


1 THIS PAGE DESCRIBES THE RECOMMENDED FRONT PANEL OPENING FOR A MT-RJ SFF TRANSCEIVER.

② SFF TRANSCEIVER PLACED AT 13.97mm (.550) MIN SPACING.

③ NOTED BEZEL DIMENSION FOR MTRJ VARIES SLIGHTLY FROM THE LC/SG.

4.4 Recommended Front Panel Opening for LC or SG [MSA Appendix A.1.4]



1 THIS PAGE DESCRIBES THE RECOMMENDED FRONT PANEL OPENING FOR A LC OR SG SFF TRANSCEIVER.

② SFF TRANSCEIVER PLACED AT 16.24mm (.600) MIN SPACING.

③ NOTED BEZEL DIMENSION FOR LC/SG VARIES SLIGHTLY FROM THE MTRJ.

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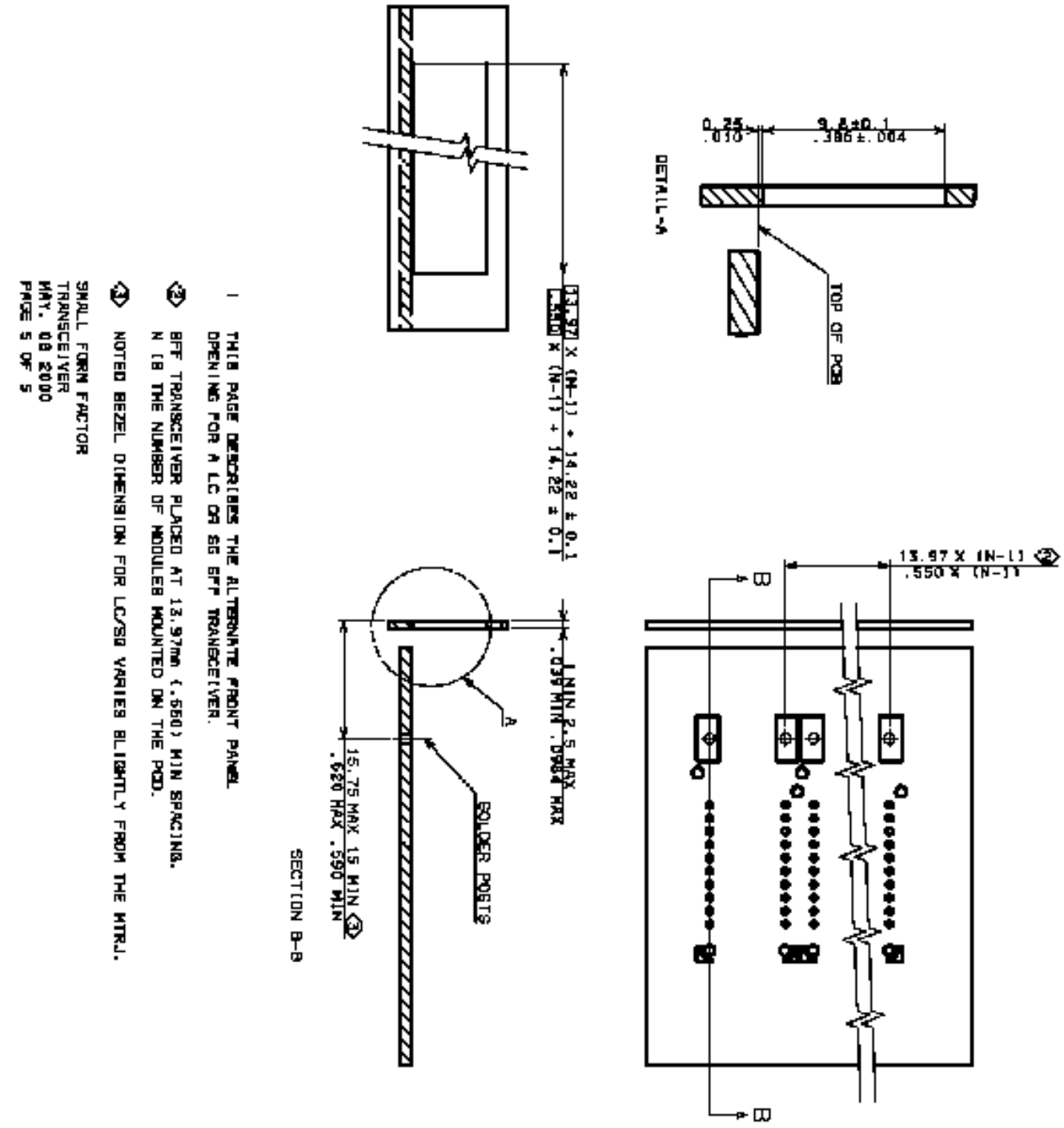
4.5 Alternate Front Panel Opening for LC or SG [MSA Appendix A.1.5]



4.6 Transceiver Receiver Pin Function Definition [MSA Appendix A.2.1]

10 and 20 Pin Part Versions (See Package Outline Drawing for Pin Positions within the Package)			Two versions of this transceiver are intended. The 10 pin version is intended for applications where the extra features of the 20 pin version are not required. The 20 pin version provides extra pins for features beyond data in and out such as recovered clock and laser transmitter monitors and alarms		
10 Pin Part	**20 Pin Part**	**Symbol**	**Notes**	**Functional Description**	**Logic Family**
MS	MS	MS	The holes in the circuit board must be tied to chassis ground	Mounting Studs The mounting studs are provided for transceiver mechanical attachment to circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground.	NA
HL	HL	HL	The holes in the circuit board must be included and be tied to signal ground	Housing Leads The optional transceiver housing leads may be provided for additional signal grounding. These additional grounds may improve signal integrity, EMC, or ESD performance	NA
No Pin	1	Photo-detector Bias	This hole in the circuit board must be tied to the most positive power supply.	Photodetector Bias: Optional Feature This lead supplies bias for the PIN photodetector diode when provided as a feature of a transceiver.	NA
No Pin	2	Vee_R		Receiver Signal Ground	NA
No Pin	3	Vee_R		Receiver Signal Ground	NA
No Pin	4	CRX-	If feature is not used, do not connect	Received Recover Clock Out Bar Optional Feature The rising edge occurs at the rising edge of the Received Data output. The falling edge occurs in the middle of the Received Data baud period	PECL
No Pin	5	CRX+	If feature is not used, do not connect	Received Recover Clock Out Optional Feature The falling edge occurs at the rising edge of the Received Data output. The rising edge occurs in the middle of the Received Data baud period	PECL
1	6	Vee_R		Receiver Signal Ground	NA
2	7	Vcc_R		Receiver Power Supply	NA
3	8	SD		Signal Detect Normal Operation: Logic"1" Output Fault Condition: Logic"0" Output This signal will be TTL for all Gb/s transceivers. For Legacy applications (622 Mb/s and below), PECL will be provided	TTL is preferred, but PECL may be provided
4	9	RD-		Received Data Out Bar No internal terminations will be provided	PECL
5	10	RD+		Received Data Out No internal terminations will be provided	PECL

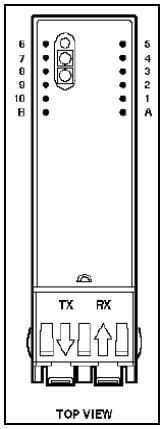
4.7 Transceiver Receiver Pin Function Definition [MSA Appendix A.2.2]

10 and 20 Pin Part Versions (See Package Outline Drawing for Pin Positions within the Package)			Two versions of this transceiver are intended. The 10 pin version is intended for applications where the extra features of the 20 pin version are not required. The 20 pin version provides extra pins for features beyond data in and out such as recovered clock and laser transmitter monitors and alarms		
10 Pin Part	**20 Pin Part**	**Symbol**	**Notes**	**Functional Description**	**Logic Family**
MS	MS	MS	The holes in the circuit board must be tied to chassis ground.	Mounting Studs The mounting studs are provided for transceiver mechanical attachment to circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground.	NA
HL	HL	HL	The holes in the circuit board must be included and be tied to signal ground	Housing Leads The optional transceiver housing leads may be provided for additional signal grounding. These additional grounds may improve signal integrity, EMC, or ESD performance	NA
6	11	V_{ccT}		Transmitter Power Supply.	NA
7	12	V_{eeT}		Transmitter Signal Ground	NA
8	13	TDis	Optional use for laser based products only	Transmitter Disable: Optional Feature Transmitter Output Disabled: $(V_{ccT} - 1.3V) < V < V_{ccT}$ Transmitter Output Enabled: $V_{eeT} < V < (V_{eeT} + 0.8V)$ or open circuit	TTL
9	14	TD+		Transmitter Data In An internal 50 ohm termination will be provided for gigabit/sec transceivers consisting of 100 ohm resistor between the TD+ and the TD- pins. No internal termination will be provided for lower speed parts (622 Mb/s and below)	PECL
10	15	TD-		Transmitter Data In Bar See TD+ pin for terminations	PECL
No Pin	16	V_{eeT}		Transmitter Signal Ground	NA
No Pin	17	Bmon (-)	If feature is not used, do not connect	Laser Diode Bias Current Monitor - Negative End: Optional Feature The laser bias current is accessible as a dc-voltage by measuring the voltage developed across pins 17 and 18. Dividing the voltage by 10 ohms will yield the value of the laser bias current. The stand-off resistors should be 3k ohms. At an ambient of 25 degrees C, the voltage should range up to a maximum of 0.70 volts.	NA
No Pin	18	Bmon (+)	If feature is not used, do not connect.	Laser Diode Bias Current Monitor - Positive End: Optional Feature See pin 17 description	NA
No Pin	19	Pmon(-)	If feature is not used, do not connect.	Laser Diode Optical Power Monitor - Negative End: Optional Feature The backface diode monitor current is accessible as a voltage proportional to the photocurrent through a 200 ohm resistor between pins 19 and 20. The stand-off resistors should be 3k ohms. At 50% duty cycle, this voltage can range between 0.01 and 0.20 volts.	NA
No Pin	20	Pmon (+)	If feature is not used, do not connect	Laser Diode Optical Power Monitor - Positive End Optional Feature See Pin 19 description	NA

5.0 Alternate 2x6 [SCL/SDA] Pin Definition – Proposed Nov 2002.

12 Pin Part – [SCL/SDA]				
12 Pin Part	**Symbol**	**Notes**	**Functional Description**	**Logic Family**
MS	MS	The holes in the circuit board must be tied to chassis ground.	**Mounting Studs** The mounting studs are provided for transceiver mechanical attachment to circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground.	NA
HL	HL	The holes in the circuit board must be included and be tied to signal ground.	**Housing Leads** The optional transceiver housing leads may be provided for additional signal grounding. These additional grounds may improve signal integrity, EMC or ESD performance.	NA
A	SDA		**Serial Interface Data I/O Pin** Functionality per INF-8074 SFP transceiver specification.	TTL
1	Vee_r		**Receiver Signal Ground**	NA
2	Vcc_r		**Receiver Power Supply**	NA
3	SD		**Signal Detect** Normal Operation: Logic "1" Output Fault Condition: Logic "0" Output This signal will be TTL for all Gb/s transceivers. For legacy applications (622 Mb/s and below) PECL will be provided.	TTL is preferred but PECL may be provided
4	RD-		**Received Data Out Bar** No internal terminations will be provided.	PECL
5	RD+		**Received Data Out** No internal terminations will be provided.	PECL
6	Vcc_t		**Transmitter Power Supply**	NA
7	Vee_t		**Transmitter Signal Ground**	NA
8	TDis	Optional use for laser based products only	**Transmitter Disable: Optional Feature** Transmitter Output Disabled: $(Vcc_t-1.3V) < V < Vcc$ Transmitter Output Enabled: $Vee_t < V < (Vee_t+0.8V)$ or Open Circuit	TTL
9	TD+		**Transmitter Data In** An internal 50 Ohm termination will be provided for gigabit/sec transceivers consisting of 100 Ohm resistor between the TD+ and TD- pins. No internal termination will be provided for lower speed parts (622 Mb/s and below)	PECL
10	TD-		**Transmitter Data In Bar**	PECL

			See TD+ pin for terminations.	
B	SCL		**Serial Interface Clock Pin** Functionality per INF-8074 SFP transceiver specification.	TTL

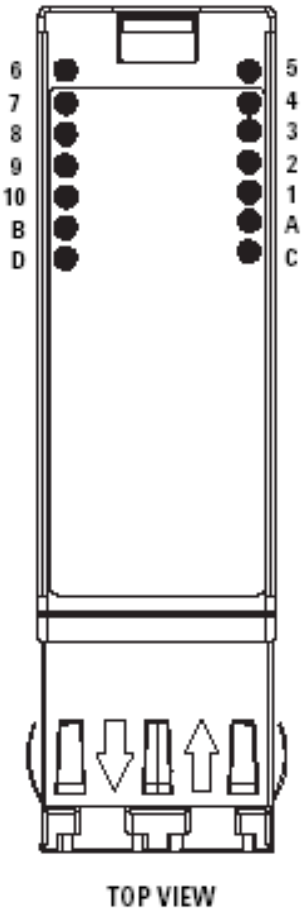


SCL/SDA 2x6 SFF Transceiver Pinout

6.0 2x7 [SCL/SDA/Tx_Fault/Rx_Rate] Pin Definition – Proposed Sept 2003.

14 Pin Part – [SCL/SDA/Tx_Fault/Rx_Rate]				
12 Pin Part	**Symbol**	**Notes**	**Functional Description**	**Logic Family**
MS	MS	The holes in the circuit board must be tied to chassis ground.	**Mounting Studs** The mounting studs are provided for transceiver mechanical attachment to circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground.	NA
HL	HL	The holes in the circuit board must be included and be tied to signal ground.	**Housing Leads** The optional transceiver housing leads may be provided for additional signal grounding. These additional grounds may improve signal integrity, EMC or ESD performance.	NA
C	Rate_Select	If feature is not used, do not connect	**Rate Select Input: Optional Feature** Functionality per INF-8074 SFP transceiver specification. If implemented, the input will be internally pulled down with a > 30k Ohm resistor.	TTL
A	SDA		**Serial Interface Data I/O Pin** Functionality per INF-8074 SFP transceiver specification.	TTL
1	Vee_r		**Receiver Signal Ground**	NA
2	Vcc_r		**Receiver Power Supply**	NA
3	SD		**Signal Detect** Normal Operation: Logic “1” Output Fault Condition: Logic “0” Output This signal will be TTL for all Gb/s transceivers. For legacy applications (622 Mb/s and below) PECL will be provided.	TTL is preferred but PECL may be provided
4	RD-		**Received Data Out Bar** No internal terminations will be provided.	PECL
5	RD+		**Received Data Out** No internal terminations will be provided.	PECL
6	Vcc_t		**Transmitter Power Supply**	NA
7	Vee_t		**Transmitter Signal Ground**	NA
8	TDis	Optional use for laser based products only	**Transmitter Disable: Optional Feature** Transmitter Output Disabled: $(Vcc_t-1.3V) < V < Vcc$ Transmitter Output Enabled: $Vee_t < V < (Vee_t+0.8V)$ or Open Circuit	TTL
9	TD+		**Transmitter Data In** An internal 50 Ohm termination will be provided for gigabit/sec transceivers consisting of 100 Ohm	PECL

			resistor between the TD+ and TD- pins. No internal termination will be provided for lower speed parts (622 Mb/s and below)	
10	TD-		**Transmitter Data In Bar** See TD+ pin for terminations.	PECL
B	SCL		**Serial Interface Clock Pin** Functionality per INF-8074 SFP transceiver specification.	TTL
D	Tx_Fault		**Transmit Fault Output** Functionality per INF-8074 SFP transceiver specification. Should be pulled up with a 4.7k to 10k Ohm resistor on the host board. When high, indicates a laser fault of some kind.	TTL



2x7 [SCL/SDA/Tx_Fault/Rx_Rate] SFF Transceiver Pinout