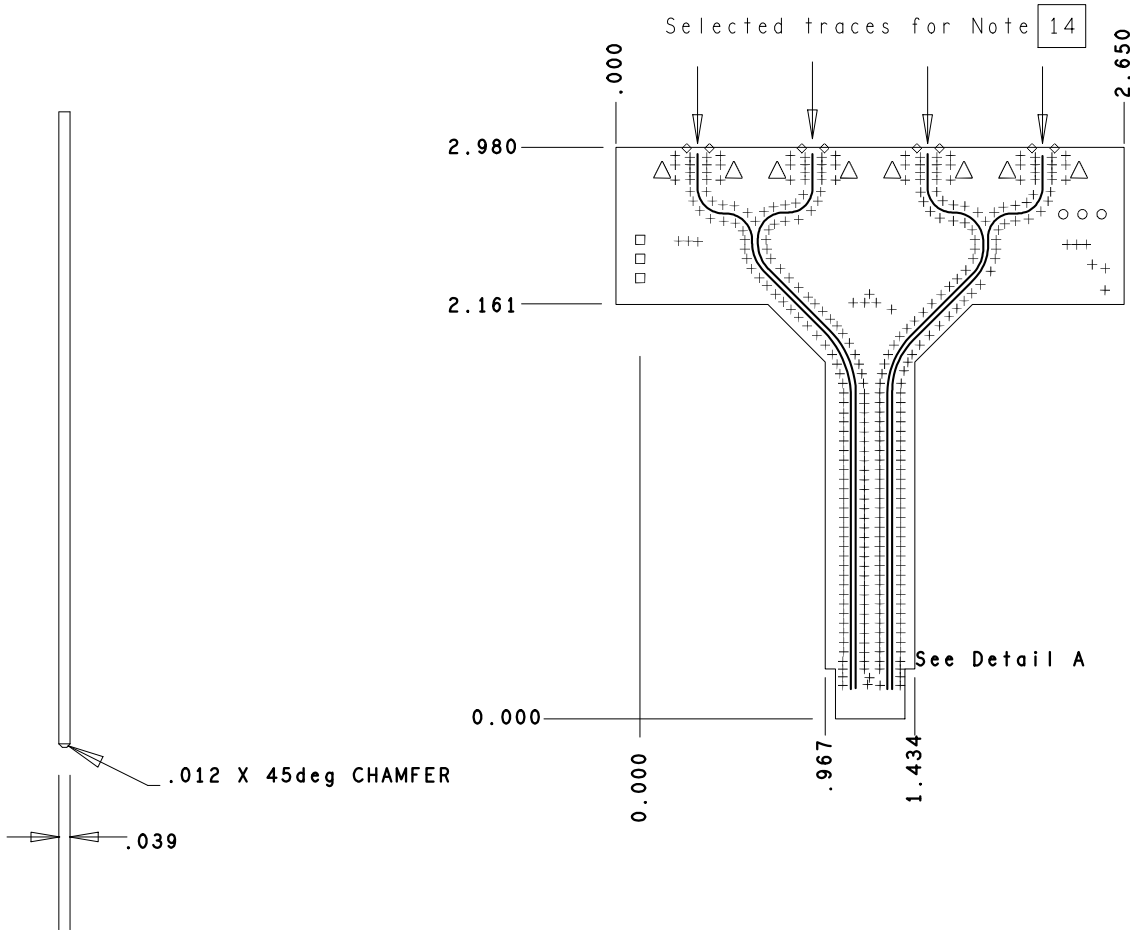


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REVISIONS

| REV | DESCRIPTION | DATE | APPROVED |
|-----|---|----------|----------|
| A | PROTOTYPE RELEASE | 12/14/06 | |
| A1 | Corrected edge connector | 12/18/06 | |
| B | Changed differentials to 12-14.5-12 | 2/5/07 | |
| C | Changed diffs to 11.5-15-11.5 | 3/2/07 | |
| D | Added note about finish of top layer traces | 6/5/07 | |
| E | Expanded soldermask opening | 7/13/07 | |
| F | Changed thickness of uncoupled diff | 9/18/07 | |

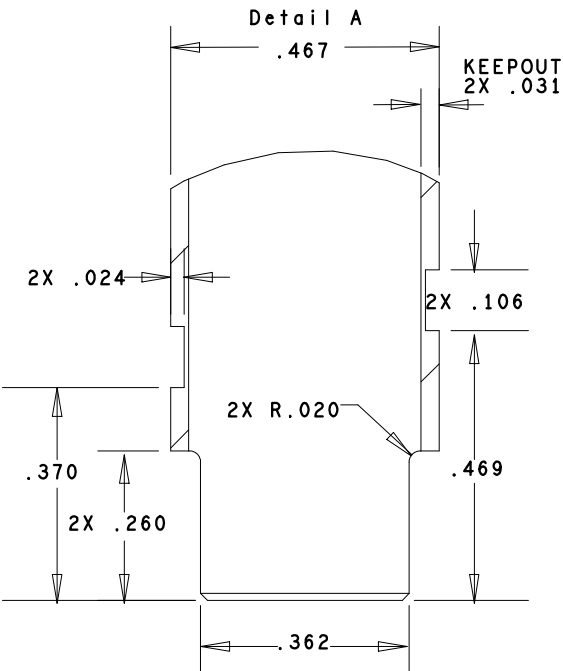


| 6-Layer, 2-Plane (COMPONENT SIDE SILKSCREEN) (COMPONENT SIDE SOLDER MASK LPI or equivalent) | |
|---|--|
| L1-TOP | Signal 0.5 OZ CU + plating (1oz minimum) |
| L2-GND | Plane 1.0 OZ CU |
| L3-INT1 | Signal 0.5 OZ CU |
| L4-INT2 | Signal 0.5 OZ CU |
| L5-VCC | Plane 1.0 OZ CU |
| L6-BOTTOM | Signal 0.5 OZ CU + plating (1oz minimum) |
| (SOLDER SIDE SOLDER MASK) (SOLDER SIDE SILK SCREEN IF PRESENT) | |
| L1 | 0.0066" Rogers 4350B |
| L2 | 0.0055" FR-4 |
| L3 | 0.007" FR-4 |
| L4 | 0.0055" FR-4 |
| L5 | 0.0066" Rogers 4350B |
| L6 | |
| Maintain 39 +/-4 mil total thickness including CU and Soldermask | |

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

| FIGURE | SIZE | TOLERANCE | PLATED | QTY |
|--------|------|------------|--------|-----|
| + | 15.0 | +0.0/-15.0 | PLATED | 314 |
| o | 37.0 | +3.0/-3.0 | PLATED | 3 |
| □ | 39.0 | +3.0/-3.0 | PLATED | 3 |
| ◇ | 40.0 | +3.0/-3.0 | PLATED | 8 |
| △ | 90.0 | +3.0/-3.0 | PLATED | 8 |



16. Top layer single ended 0.0125 traces are to be 50 ohms +/- 4%.
15. PCB to be marked the same Rev as this fab drawing (F).
14. Surface finish on the selected top layer traces to be of at least 100 micro inches of hard gold over at most 50 micro inches of nickel.
13. Top layer differential pairs consists of 0.0115" traces with 0.015" spaces to be 100 ohms +2% / -3%.
12. This is a not a lead free board.
11. Edge Castellations: 40 mil holes on the edge of the board are meant to be cut in half but plated.
10. Edge Connector 0.38 micrometers min hard gold over 1.27 micrometers min thick nickel.
9. Soldermask to be green.
8. Final electrical test to be performed at 250VDC min.
7. All plane layers <= 0.003" to be highpot tested to adjacent planes at 500VDC min.
6. All hole dimensions are finished sizes.
5. Surface finish with .13" 4 micron Gold over 4.7 micron thick Nickel.
4. Use supplied IPC356 test list (64-001663-401 F IPC.TXT) to perform testlist comparison with gerber data prior to manufacturing.
3. Use artwork 64-001663-401 F ZIP
2. Printed circuit boards will be manufactured from copper clad hybrid laminates of Rogers 4350B and NEMA Grade FR-4 per IPC-4101A/24, TG170, TD340.
1. This PCB to be fabricated in accordance with the most current revision of specification 900-0207-001 or higher.
- Notes: Unless otherwise specified
Fab Notes for PN 40-001663-401 Rev F (SFF-8431)

| | | | | | | | |
|--|--|-------------|--|---------------------------|-----------|--|--------------|
| UNLESS OTHERWISE SPECIFIED | | CONTRACT NO | | SPIRENT COMMUNICATIONS | | | |
| DIMENSIONS ARE IN INCHES TOLERANCES ARE 2 PL DECIMALS +/- .010 3 PL DECIMALS +/- .005 ANGLES +/- 1/2 Degree FRACTIONS +/- | | | | 999 Bishop St, Suite 1700 | | 26750 Auoua Road | |
| | | | | Honolulu, HI 96813 | | Calabasas, CA 91302 | |
| | | APPROVALS | | DATE | | FAB DRAWING SF-8431 HOST SYSTEM COMPLIANCE BOARD | |
| DRAWN S Wong | | 9/18/07 | | | | | |
| MATERIAL | | CHECKED | | | | | |
| FINISH | | PROJ ENGRG | | SIZE | CAGE CODE | BOARD NO | REV |
| | | MFG ENGRG | | B | | 40-001663-401 | F |
| | | | | SCALE | SHEET | OF | FILENAME |
| DO NOT SCALE DRAWING | | | | NTS | 1 | 1 | SFF-8431.BRD |