

SFF specifications are available at <http://www.snia.org/sff/specifications>  
or <ftp://ftp.seagate.com/sff>

**This specification was developed by the SFF Committee prior to it becoming the SFF TA (Technology Affiliate) TWG (Technical Working Group) of SNIA (Storage Networking Industry Association).**

The information below should be used instead of the equivalent herein.

POINTS OF CONTACT:

Chairman SFF TA TWG  
Email: [SFF-Chair@snia.org](mailto:SFF-Chair@snia.org)

If you are interested in participating in the activities of the SFF TWG, the membership application can be found at:

<http://www.snia.org/sff/join>

The complete list of SFF Specifications which have been completed or are currently being worked on can be found at:

<http://www.snia.org/sff/specifications/SFF-8000.TXT>

The operations which complement the SNIA's TWG Policies & Procedures to guide the SFF TWG can be found at:

<http://www.snia.org/sff/specifications/SFF-8032.PDF>

Suggestions for improvement of this specification will be welcome, they should be submitted to:

<http://www.snia.org/feedback>

SFF Committee documentation may be purchased (see 2.3).  
SFF Committee documents are available by FaxAccess at 408-741-1600

SFF Committee

**SFF-8410 Specification for**

HSS Copper Testing and Performance Requirements

Rev 16.1 March 20, 2000

Secretariat: SFF Committee

**Abstract:** This document defines the electrical and performance requirements for duplex serial copper cable assemblies and associated system connections operating at high speeds (> 1 Gbaud in each direction). This architecture is used in most applications requiring high speed serial copper connections: Fibre Channel, Gigabit Ethernet, NGIO, Future I/O, 1394, and SSA. Other applications for this general-purpose specification are also possible, including parallel structures.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of components in the referenced area. This is an internal working document of the SFF Committee, an industry ad hoc group.

The description of a test procedure in this document does not assure that the specific hardware necessary for executing the procedure is actually available from instrumentation suppliers. If such hardware is supplied, it must comply with this specification to achieve interoperability between suppliers.

This document is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this document.

**Support:** This document is supported by the identified member companies of the SFF Committee.

**Documentation:** This document has been prepared in a similar style to that of the ISO (International Organization of Standards).

**POINTS OF CONTACT:**

Bill Ham  
Compaq Computer  
334 South St  
Shrewsbury, MA 01545

I. Dal Allan  
Chairman SFF Committee  
14426 Black Walnut Court  
Saratoga CA 95070

Ph: 508-841-2629 Fx: 508-841-5266  
Email: Bill\_Ham@compaq.com

Ph: 408-867-6630 Fx: 408-867-2115

## EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

Adaptec  
AMP  
Amphenol  
Compaq  
DDK Fujikura  
ENDL  
FCI/Berg  
Fujitsu CPA  
Hitachi Cable  
Honda Connector  
Montrose/CDT  
Quantum  
TI Japan  
Toshiba America  
Tyco AMP  
Unisys  
Yamagata Fujitsu

The following member companies of the SFF Committee voted to abstain on this industry specification.

DDK Electronics  
Foxconn Int'l  
IBM  
Matsushita  
Maxtor  
Molex  
Pioneer NewMedia  
Seagate  
Sun Microsystems  
Thomas & Betts  
YC Cable

The user's attention is called to the possibility that implementation to this Specification may require use of an invention covered by patent rights. By distribution of this Specification, no position is taken with respect to the validity of this claim or of any patent rights in connection therewith. The patent holder has filed a statement of willingness to grant a license under these rights on reasonable and non-discriminatory terms and conditions to applicants desiring to obtain such a license.

If you are not a member of the SFF Committee, but you are interested in participating, the following principles have been reprinted here for your information.

#### PRINCIPLES OF THE SFF COMMITTEE

The SFF Committee is an ad hoc group formed to address storage industry needs in a prompt manner. When formed in 1990, the original goals were limited to defining de facto mechanical envelopes within which disk drives can be developed to fit compact computer and other small products.

Adopting a common industry size simplifies the integration of small drives (2 1/2" or less) into such systems. Board-board connectors carrying power and signals, and their position relative to the envelope are critical parameters in a product that has no cables to provide packaging leeway for the integrator.

In November 1992, the SFF Committee objectives were broadened to encompass other areas which needed similar attention, such as pinouts for interface applications, and form factor issues on larger disk drives. SFF is a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Documents created by the SFF Committee are expected to be submitted to bodies such as EIA (Electronic Industries Association) or an ASC (Accredited Standards Committee). They may be accepted for separate standards, or incorporated into other standards activities.

The principles of operation for the SFF Committee are not unlike those of an accredited standards committee. There are 3 levels of participation:

- Attending the meetings is open to all, but taking part in discussions is limited to member companies, or those invited by member companies
- The minutes and copies of material which are discussed during meetings are distributed only to those who sign up to receive documentation.
- The individuals who represent member companies of the SFF Committee receive documentation and vote on issues that arise. Votes are not taken during meetings, only guidance on directions. All voting is by letter ballot, which ensures all members an equal opportunity to be heard.

Material presented at SFF Committee meetings becomes public domain. There are no restrictions on the open mailing of material presented at committee meetings. In order to reduce disagreements and misunderstandings, copies must be provided for all agenda items that are discussed. Copies of the material presented, or revisions if completed in time, are included in the documentation mailings.

The sites for SFF Committee meetings rotate based on which member companies volunteer to host the meetings. Meetings have typically been held during the ASC T10 weeks.

If you are not receiving the documentation of SFF Committee activities or are interested in becoming a member, the following signup information is reprinted here for your information.

Annual SFF Committee Membership Fee	\$ 1,800.00
Annual SFF Committee Paper Documentation Fee	\$ 300.00
Annual Surcharge for AIR MAIL to Overseas	\$ 100.00
Annual Surcharge for Electronic Documentation	\$ 360.00

Name: \_\_\_\_\_

Title: \_\_\_\_\_

Company: \_\_\_\_\_

Address: \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

Phone: \_\_\_\_\_

Fax: \_\_\_\_\_

Email: \_\_\_\_\_

Please register me as a Member of the SFF Committee for one year.

Paper documentation	\$ 1,800
Electronic documentation	\$ 2,160

Check Payable to SFF Committee for \$\_\_\_\_\_ is Enclosed

Please invoice me \$\_\_\_\_\_ on PO #: \_\_\_\_\_

MC/Visa/AmX\_\_\_\_\_ Expires\_\_\_\_\_

Please register me as an Observer on the SFF Committee for one year.

Paper documentation	\$ 300 U.S.	\$ 400 Overseas
Electronic documentation	\$ 660 U.S.	\$ 760 Overseas

Check Payable to SFF Committee for \$\_\_\_\_\_ (POs Not Accepted)

MC/Visa/AmX\_\_\_\_\_ Expires\_\_\_\_\_

SFF Committee	408-867-6630
14426 Black Walnut Ct	408-867-2115Fx
Saratoga CA 95070	250-1752@mcimail.com

## Foreword

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers in which space was at a premium and time to market with the latest machine was an important factor. System integrators worked individually with vendors to develop the packaging. The result was wide diversity, and with space being such a major consideration in packaging, it was not possible to replace one vendor's drive with a competitive product.

The desire to reduce disk drive sizes to even smaller dimensions such as 1.8" and 1.3" made it likely that devices would become even more constrained in dimensions because of a possibility that such small devices could be inserted into a socket, not unlike the method of retaining semiconductor devices.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology in disk drives. After two informal gatherings on the subject in the summer of 1990, the SFF Committee held its first meeting in August.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced problems other than the physical form factors of disk drives. In November 1992, the members approved an expansion in charter to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

At the same time, the principle was adopted of restricting the scope of an SFF project to a narrow area, so that the majority of documents would be small and the projects could be completed in a rapid timeframe. If proposals are made by a number of contributors, the participating members select the best concepts and uses them to develop specifications which address specific issues in emerging storage markets.

Those companies which have agreed to support a documented specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

Suggestions for improvement of this document will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in 1990 has included a mix of companies which are leaders across the industry.

SFF Committee --

## HSSDC-1 Shielded Connections

### 1. Scope

This specification defines the terminology and physical requirements for shielded HSSDC-1 (High Speed Serial Data Connector) connections, complete connectors, and the immediate electrical neighborhood of the connector proper that also influences the behavior of the connector. There is a single mating interface for all versions.

The HSSDC-1 connector style is specified in Fibre Channel, SSA, and Gigabit Ethernet and may be suitable for use with other high speed serial interface standards. These are all external shielded systems that require inter-enclosure connections. These standards only specify the mating interface and have no specific performance requirements so this document, along with the IEC 61076-3-103, define such requirements.

The relevant parts of this IEC document are included in this specification for easy reference. The Fibre Channel, SSA, and Gigabit Ethernet standards call out the contact position numbering for the respective application uses and are the normative sources.

The mating sides (including retention) are compatible for all versions of complete connector and the termination side is specified for a variety of practically important schemes. The controlling document for the dimensional values is the IEC (International Electronics Commission) standard.

The specific versions of complete connectors specified for use with FC-AL, SSA, Gigabit Ethernet, (and P1394) is controlled by this SFF document as not all possible combinations of mating side and termination side are supported.

The HSSDC-1 system was designed from the beginning for the specific purpose of satisfying the needs for gigabit serial data transmissions in a nominal 150 ohm differential balanced copper link. The shield connector mating interface has been designed to provide an EMI-tight (Electro Magnetic Interference) seal. Design goals are minimization of cross talk, minimum transmission line impedance discontinuity across the connector, and management of EMI (caused by the connector or its mating interfaces).

The transmission line impedance of the connector itself (not including the termination interface to the wire or board) matches the electrical media within the tolerances allowed for the media. This connection scheme may be used in multiple places within a cabling environment. Though optimized for a 150 ohm environment this connector will function acceptably at other impedance levels (to be optimized on a case by case basis).

The retention scheme consists of a single press-to-release catch similar to those found on the extremely popular and common ergonomic RJ style network and telephone unshielded connectors. The look and feel of the HSSDC-1 family is well suited for advanced high speed transmission applications. The panel space required is significantly less than that for other styles of connectors.

The physically robust design (e. g. no pins to bend) and relatively small size enable the HSSDC-1 to be usable in all applications from notebooks to data centers. The connector is of a straightforward construction which does not rely

on advanced materials or processes.

The mating sides (including retention) are the same for all versions of complete connector and there is a variety of choices on the termination side.

This document specifies the requirements on the mating and termination sides of the connectors to enable functional multiple sourcing of the complete connectors. The construction of the connectors between the mating and termination sides are not specified by this document.

In the present selection of complete connectors specified all are fully shielded at the mating interface with provision for connecting shields together and for terminating shields. Therefore specifications are included for the backshell-to-connector interfaces. Fibre Channel and SSA standards presently incorporate requirements on the characteristic impedance and ability to transmit Gigabaud signals for cable assemblies and backplanes. As the HSSDC-1 connector system may form part of this interconnect it is also subject to these requirements.

The high speed electrical performance requirements for the connector and its electrical neighborhood are specified in SFF-8410 which is incorporated by reference into this specification. These requirements include operation at 1 Gigabit/second and higher rates.

In an effort to broaden the applications for storage devices, an ad hoc industry group of companies representing system integrators, peripheral suppliers, and component suppliers decided to address the issues involved.

The SFF Committee was formed in August, 1990 and the first working document was introduced in January, 1991.

## 1.1 Description of Clauses

Clause 1 contains the Scope and Purpose.

Clause 2 contains Referenced and Related Standards and SFF Specifications.

Clause 3 contains the list of Figures and Tables

Clause 4 contains the General Description

Clause 5 contains the Definitions and Conventions

Clause 6 defines the Connector Descriptions and Dimensions.

## 2. References

The SFF Committee activities support the requirements of the storage industry, and it is involved with several standards.

### 2.1 Industry Documents

The following interface standards are relevant to this Specification.

- X3.230-1994 FC-PH Fibre Channel Physical Interface
- X3.297-199x FC-PH-2 Fibre Channel Physical Interface -2
- X3.303-199x FC-PH-3 Fibre Channel Physical Interface -3

- X3.293-199x SSA-PH1 SSA Physical Interface
- T10-1146 SSA-PH2 SSA Physical Interface -2
- IEEE P802.3z Gigabit Task Force
- IEC 61076-3-103 High Speed Serial Data Connector

## 2.2 SFF Specifications

There are several projects active within the SFF Committee. At the date of printing document numbers had been assigned to the following projects. The status of Specifications is dependent on committee activities.

- F = Forwarded The document has been approved by the members for forwarding to a formal standards body.
- P = Published The document has been balloted by members and is available as a published SFF Specification.
- A = Approved The document has been approved by ballot of the members and is in preparation as an SFF Specification.
- C = Canceled The project was canceled, and no Specification was Published.
- D = Development The document is under development at SFF.
- E = Expired The document has been published as an SFF Specification, and the members voted against re-publishing it when it came up for annual review.
- e = electronic Used as a suffix to indicate an SFF Specification which has Expired but is still available in electronic form from SFF e.g. a specification has been incorporated into a draft or published standard which is only available in hard copy.
- i = Information The document has no SFF project activity in progress, but it defines features in developing industry standards. The document was provided by a company, editor of an accredited standard in development, or an individual. It is provided for broad review (comments to the author are encouraged).
- s = submitted The document is a proposal to the members for consideration to become an SFF Specification.

### Spec # Rev List of Specifications as of March 26, 2000

Spec #	Rev	List of Specifications as of March 26, 2000
SFF-8000		SFF Committee Information
SFF-8001i	E	44-pin ATA (AT Attachment) Pinouts for SFF Drives
SFF-8002i	E	68-pin ATA (AT Attachment) for SFF Drives
SFF-8003	E	SCSI Pinouts for SFF Drives
SFF-8004	E	Small Form Factor 2.5" Drives
SFF-8005	E	Small Form Factor 1.8" Drives
SFF-8006	E	Small Form Factor 1.3" Drives
SFF-8007	E	2mm Connector Alternatives
SFF-8008	E	68-pin Embedded Interface for SFF Drives
SFF-8009	4.1	Unitized Connector for Cabled Drives
SFF-8010	E	Small Form Factor 15mm 1.8" Drives
SFF-8011i	E	ATA Timing Extensions for Local Bus
SFF-8012	2.3	4-Pin Power Connector Dimensions
SFF-8013	E	ATA Download Microcode Command
SFF-8014	C	Unitized Connector for Rack Mounted Drives
SFF-8015	E	SCA Connector for Rack Mounted SFF SCSI Drives
SFF-8016	C	Small Form Factor 10mm 2.5" Drives

SFF-8017 E SCSI Wiring Rules for Mixed Cable Plants  
 SFF-8018 E ATA Low Power Modes  
 SFF-8019 E Identify Drive Data for ATA Disks up to 8 GB  
  
 INF-8020i E ATA Packet Interface for CD-ROMs  
 SFF-8028i E - Errata to SFF-8020 Rev 2.5  
 SFF-8029 E - Errata to SFF-8020 Rev 1.2  
  
 SFF-8030 1.8 SFF Committee Charter  
 SFF-8031 Named Representatives of SFF Committee Members  
 SFF-8032 1.4 SFF Committee Principles of Operation  
 SFF-8033i E Improved ATA Timing Extensions to 16.6 MBs  
 SFF-8034i E High Speed Local Bus ATA Line Termination Issues  
 SFF-8035i E Self-Monitoring, Analysis and Reporting Technology  
 SFF-8036i E ATA Signal Integrity Issues  
 INF-8037i E Intel Small PCI SIG  
 INF-8038i E Intel Bus Master IDE ATA Specification  
 SFF-8039i E Phoenix EDD (Enhanced Disk Drive) Specification  
  
 SFF-8040 1.2 25-pin Asynchronous SCSI Pinout  
 SFF-8041 C SCA-2 Connector Backend Configurations  
 SFF-8042 C VHDCI Connector Backend Configurations  
 SFF-8043 E 40-pin MicroSCSI Pinout  
 SFF-8045 4.2 40-pin SCA-2 Connector w/Parallel Selection  
 SFF-8046 E 80-pin SCA-2 Connector for SCSI Disk Drives  
 SFF-8047 C 40-pin SCA-2 Connector w/Serial Selection  
 SFF-8048 C 80-pin SCA-2 Connector w/Parallel ESI  
 SFF-8049 E 80-conductor ATA Cable Assembly  
  
 INF-8050i 1.0 Bootable CD-ROM  
 INF-8051i E Small Form Factor 3" Drives  
 INF-8052i E ATA Interface for 3" Removable Devices  
 SFF-8053 5.4 GBIC (Gigabit Interface Converter)  
 INF-8055i E SMART Application Guide for ATA Interface  
 SFF-8056 C 50-pin 2mm Connector  
 SFF-8057 E Unitized ATA 2-plus Connector  
 SFF-8058 E Unitized ATA 3-in-1 Connector  
 SFF-8059 E 40-pin ATA Connector  
  
 SFF-8060 1.1 SFF Committee Patent Policy  
 SFF-8061 1.1 Emailing drawings over the SFF Reflector  
 SFF-8065 C 40-pin SCA-2 Connector w/High Voltage  
 SFF-8066 C 80-pin SCA-2 Connector w/High Voltage  
 SFF-8067 2.6 40-pin SCA-2 Connector w/Bidirectional ESI  
 INF-8068i 1.0 Guidelines to Import Drawings into SFF Specs  
 SFF-8069 E Fax-Access Instructions  
  
 INF-8070i 1.2 ATAPI for Rewritable Removable Media  
 SFF-8072 1.2 80-pin SCA-2 for Fibre Channel Tape Applications  
 SFF-8073 - 20-pin SCA-2 for GBIC Applications  
  
 SFF-8080 E ATAPI for CD-Recordable Media  
  
 INF-8090i 3.6 ATAPI for DVD (Digital Video Data)  
  
 SFF-8200e 1.1 2 1/2" drive form factors (all of 82xx family)  
 SFF-8201e 1.3 2 1/2" drive form factor dimensions

SFF-8212e 1.2 2 1/2" drive w/SFF-8001 44-pin ATA Connector

SFF-8300e 1.1 3 1/2" drive form factors (all of 83xx family)

SFF-8301e 1.2 3 1/2" drive form factor dimensions

SFF-8302e 1.1 3 1/2" Cabled Connector locations

SFF-8332e 1.2 3 1/2" drive w/80-pin SFF-8015 SCA Connector

SFF-8337e 1.2 3 1/2" drive w/SCA-2 Connector

SFF-8342e 1.3 3 1/2" drive w/Serial Unitized Connector

SFF-8400 C Very High Density Cable Interconnect

SFF-8410 16.1 High Speed Serial Testing for Copper Links

SFF-8411 - High Speed Serial Testing for Backplanes

SFF-8412 - HSS Requirements for Duplex Optical Links D

SFF-8420 11.1 HSSDC-1 Shielded Connections

SFF-8421 tbd HSSDC-2 Shielded Connections

SFF-8422 tbd \*\*FCI\*\* Shielded Connections

SFF-8423 tbd \*Molex\* Shielded Connections

SFF-8430 4.1 MT-RJ Duplex Optical Connections

SFF-8441 14.1 VHDCI Shielded Configurations

SFF-8451 10.1 HSS (High Speed Serial) SCA-2 Connections

SFF-8480 2.1 HSS (High Speed Serial) DB9 Connections

SFF-8500e 1.1 5 1/4" drive form factors (all of 85xx family)

SFF-8501e 1.1 5 1/4" drive form factor dimensions

SFF-8508e 1.1 5 1/4" ATAPI CD-ROM w/audio connectors

SFF-8551 3.0 5 1/4" CD-ROM 1" High form factor

SFF-8572 - 5 1/4" Tape form factor

SFF-8610 C SDX (Storage Device Architecture)

### 2.3 Sources

Copies of ANSI standards or proposed ANSI standards may be purchased from Global Engineering.

15 Inverness Way East 800-854-7179 or 303-792-2181  
 Englewood 303-792-2192Fx  
 CO 80112-5704

Copies of SFF Specifications are available by joining the SFF Committee as an Observer or Member.

14426 Black Walnut Ct 408-867-6630x303  
 Saratoga 408-867-2115Fx  
 CA 95070 FaxAccess: 408-741-1600

The increasing size of SFF Specifications has made FaxAccess impractical to obtain large documents. Document subscribers and members are automatically updated every two months with the latest specifications. Specifications are available by FTP at [fission.dt.wdc.com/pub/standards/sff/spec](http://fission.dt.wdc.com/pub/standards/sff/spec)

Electronic copies of documents are also made available via CD\_Access, a service which provides copies of all the specifications plus SFF reflector traffic. CDs are mailed every 2 months as part of the document service, and provide the letter ballot and paper copies of what was distributed at the meeting as well as the meeting minutes.

## Editor's notes:

This revision incorporates editorial changes from Rev 15 as recommended by the February 23, 2000 SSWG. The technical content is unchanged. Note that the title has changed. This revision is now a final draft ready for a publication vote. Further technical enhancements will be made in a document to be created under a different SFF project number so that this revision may be used as a stable reference.

## TABLE OF CONTENTS

3. Introduction.....	14
4. General requirements.....	14
5. Framework for HSS testing.....	17
5.1 HSS test levels.....	18
5.1.1 Level 1 test definition.....	18
5.1.2 Level 2 test definition.....	18
5.1.3 Relationship between level 1 and level 2 tests.....	18
5.2 Applicability to specific connectors.....	19
5.3 Electrical Neighborhood.....	20
5.4 Definition of level 1 HSS electrical performance parameters....	22
5.4.1 Definition of PUT and PUT <sub>NOT</sub> .....	22
5.4.2 Definition of level 1 electrical performance parameters...23	
5.5 Definition of level 2 HSS electrical performance parameters....	25
5.6 Basic requirements for executing a test.....	26
5.7 Definition of the HSS interconnect under test (IUT).....	27
5.8 Special considerations for test fixtures.....	28
5.9 Extensions to parallel - serial constructions.....	28
5.9.1 Impedance profile for p-s constructions.....	30
5.9.2 Signal degradation for p-s constructions.....	30
5.9.3 Balance degradation for p-s constructions.....	31
5.9.4 EMC for p-s constructions.....	31
5.9.5 Near end cross talk for p-s constructions.....	31
5.9.6 Summary of extensions to p-s constructions.....	32
5.10 Map of the HSS parameters.....	32
6. Level 1 tests.....	32
6.1 Impedance profile.....	33
6.1.1 Test fixture and measurement equipment.....	33
6.1.1.1 Test fixture.....	33
6.1.1.2 Measurement equipment.....	34
6.1.2 Calibration and verification procedure.....	34
6.1.2.1 Instrument calibration.....	34
6.1.2.2 Test fixture verification.....	35
6.1.2.3 Differential signal transition duration calibration..35	
6.1.3 Testing procedure.....	38
6.1.3.1 Impedance profile in connector region.....	38
6.1.3.2 Impedance profile in the media region.....	39
6.1.4 Acceptable ranges.....	40
6.2 Signal degradation.....	41
6.2.1 Measurement test fixtures and measurement equipment.....	42
6.2.2 Calibration procedure.....	44
6.2.2.1 Calibration test fixture.....	45
6.2.2.2 Calibration for S1 and signal measurement instrument.45	
6.2.2.3 Calibration for S2.....	49
6.2.3 Testing procedure.....	50
6.2.4 Acceptable ranges.....	51
6.3 Balance degradation.....	51

6.3.1	Test fixture and measurement equipment.....	53
6.3.2	Calibration procedures.....	53
6.3.2.1	Calibration for S1 and SMI1.....	53
6.3.2.2	Calibration for S2.....	54
6.3.3	Testing procedure.....	55
6.3.4	Acceptable ranges.....	57
6.4	Electromagnetic compatibility (EMC).....	57
6.4.1	Common mode power transfer (CMPT).....	58
6.4.1.1	Test fixture and measurement equipment.....	58
6.4.1.2	Calibration procedure.....	61
6.4.1.3	Testing procedure.....	62
6.4.1.4	Acceptable Ranges.....	64
6.4.2	Electromagnetic radiation (EMR).....	65
6.4.2.1	Test fixture and measurement equipment.....	65
6.4.2.1.1	Measurement equipment.....	65
6.4.2.1.2	Test fixture.....	67
6.4.2.2	Calibration and verification procedure.....	68
6.4.2.2.1	Test setup.....	68
6.4.2.2.2	Calibration procedure.....	68
6.4.2.3	Testing procedure.....	69
6.4.2.4	Acceptable levels.....	70
6.5	Near end cross talk (quiescent noise).....	70
6.5.1	Test fixture and measurement equipment.....	71
6.5.2	Calibration procedure.....	72
6.5.3	Testing procedure.....	74
6.5.4	Acceptable ranges.....	76
7.	Level 2 tests.....	76
7.1	Attenuation.....	77
7.1.1	Measurement test fixture and measurement equipment.....	82
7.1.2	Calibration procedure.....	83
7.1.3	Testing procedure.....	84
7.1.4	Acceptable ranges.....	86
7.2	Propagation time and propagation time skew.....	86
7.2.1	Test fixture and measurement equipment.....	86
7.2.2	Calibration procedure.....	86
7.2.3	Testing procedure.....	88
7.2.4	Acceptable ranges.....	89
7.3	Amplitude imbalance between the + signal and - signal.....	89
7.3.1	Test fixture and measurement equipment.....	90
7.3.2	Calibration procedure.....	90
7.3.3	Testing procedure.....	90
7.3.4	Acceptable ranges.....	91
7.4	Signal transition duration.....	91
7.4.1	Test fixture and measurement equipment.....	91
7.4.2	Calibration procedure.....	91
7.4.3	Testing procedure.....	91
7.4.4	Acceptable ranges.....	94
7.5	Cross talk component of signal degradation.....	94
7.5.1	Removal of second source.....	94
7.5.2	Single pulse.....	96
7.5.3	Sinusoidal.....	96
7.5.3.1	Test fixture and measurement equipment.....	96
7.5.3.2	Calibration procedure.....	96
7.5.3.3	Testing procedure.....	97
7.5.3.4	Acceptable ranges.....	98
8.	ANNEX A Acceptable ranges.....	99
8.1	Impedance profile.....	99

8.2 Signal degradation.....99  
8.3 Balance degradation.....102  
8.4 EMC.....102  
8.5 NEXT (Quiescent noise).....102

### 3. Introduction

This document contains specifications for validating the electrical performance of high speed serial copper interconnects. It is intended specifically to be used in conjunction with the HSSDC, HSSDB9, and other connector families used in a duplex serial application. These tests may also be useful for other high speed copper interconnects such as SCSI and IDE. SFF-8410 is one of the family of SFF documents.

Although the specifications specifically document the testing required for a single transmit and a single receive path in a single cable assembly the methods are directly extensible to parallel implementations that use multiple high speed paths. Requirements for extending the documented tests for multiple paths constructions are also contained.

This document should be treated as a new specification relating to implementing the testing required to meet the requirements in various published standards.

The methods described herein may be more stringent than some common industry practice due to lack of complete specification of testing methods in the published standards.

This specification is intended to reflect actual system operation and worst case transceivers - this means that all signals that are normally active during system operation must be active at the extreme allowed stress condition during the testing and that the poorest quality compliant transmitters and poorest quality compliant receivers are assumed. Test methods are developed to evaluate component behavior under these worst case conditions. This scheme is needed for implementing an "open" interconnect model where it is not known a priori where the HSS cable assembly will be connected on either end.

This more stringent testing is a natural part of the maturation of high speed serial technology and will be even more important at higher speeds in the future.

In real systems, opportunities for trading off margins between transmitter, cable assemblies, and receivers commonly exist. Therefore it may be possible to qualify a cable assembly for use in specific bounded applications where the cable assembly does not meet the stringent requirements described herein because, for example, it is known that the receivers used in this application are more sensitive than required by the standard. However, taking this same cable assembly into an open, unbounded application may cause link failures because less sensitive, but still compliant, receivers happen to be on the attached FC ports.

### 4. General requirements

The boundary where high speed testing (as opposed to low speed testing) becomes necessary is not sharp and this document does not attempt to define the boundary. The signals of interest in this document range from a few hundred MBaud to several GBaud with rise times from approximately 0.5 ns to tens of ps.

Testing techniques for HSS duplex copper interconnect in this speed range lack good standardization and methods. This deficiency leads to unintended incompatibilities between suppliers and users. Further, the specific conditions existing when a duplex connection is required are explicitly addressed. This document is not a general specification for testing all high speed copper interconnect but rather is aimed at the architectures used in Fibre Channel, Gigabit Ethernet, 1394, and the like. Although the specifications are written around a 150 ohm balanced transmission the methods are readily adaptable to other transmission line impedance levels such as the 110 ohm used by 1394.

It is assumed that a completed cable assembly (media with connectors on both ends) constitutes the primary interconnect component of interest. This does not mean that the raw cable media is not important in producing good interconnect but rather means that the focus of this document includes all the effects of adding connectors, of placing connectors on boards, and of mating the finished assembly to a shielded bulkhead. Except for the electromagnetic compatibility tests, all tests apply to both shielded and unshielded constructions. The test fixturing for testing raw media is not considered directly in this document.

All tests except the impedance profile are intended to apply to all constructions of cable assembly including those with equalizers and those with known non uniformities such as intermediate connection points.

The general requirements are:

- for a launched signal with the most degraded allowed parameters to traverse the interconnect without further degrading beyond the allowed input specifications for the receiver
- for the interconnect to not export more noise to other parts of the system than specified (anti pollution requirements)
- to behave like a matched transmission line for devices and other cable assemblies attached to the ends

The received signal and exported noise are influenced both by the properties of the launched signals and by the degradations occurring during the transmission process. The goal is to deliver adequate signal quality to the receiver and to not export excessive noise under the worst allowed cases. This means that both the properties of the launched signals and the properties of the interconnect must be considered in the testing processes.

Real launched signals always contain some level of imperfection so it is not practical to require perfect launch signals. Similarly it is essentially impossible to create a launched signal that is degraded to all the allowed limits at the same time. There is a requirement to accommodate these two facts into the testing strategy. Essentially there are two risks associated with this issue.

One risk comes from inadequately characterizing the launched signals used in the tests. Since the properties of the signals at the receiver are the only properties that matter to an operating system, the standards only consider the final result at the receiver. If launched signals used during the test are degraded more than that allowed then the interconnect will be called on to

cause less degradation so that the result at the receiver will still be within specification. The use of excessively degraded launched signals places unfair burden on the interconnect. Conversely, if the launched signals are better than allowed, the interconnect may cause more degradation than allowed for the interconnect but still deliver compliant signals to the receiver. This condition permits defective interconnect to be measured as good interconnect. The way to avoid these risks is to execute an adequate characterization of the launched signals and to compensate in the test requirements for the amount of excess goodness or badness in the launched signals. Figure 1 illustrates this general scheme.

Another risk derives from the fact that some parameters in launched signals can be corrected by interconnect that introduces degradation of equal and opposite sign. If this happens it gives a false sense of goodness since launched signals from other transmitters may have the parameters degraded in the same sense as the interconnect with a resulting doubling in the negative effects at the receiver.

In general, if the polarity of connection of the interconnect to the launched signals is reversed then the polarity of the degradation in the interconnect is also reversed (for those parameters that are sensitive to polarity, like balance degradation and near end cross talk). Therefore the second risk can be managed by performing a second test with reversed connections but changing nothing else.

In order to avoid this risk one must take two measurements: (1) with the + signal of the transmitter connected to the + line of the PUT and the - signal of the transmitter connected to the - line of the PUT and (2) with the + signal of the transmitter connected to the - line of the PUT and the - signal of the transmitter connected to the + line of the PUT. Figure 2 illustrates this scheme.

Summarizing, the combination of real launched signal properties and interconnect properties causes additional burden on the testing process. The compensation for real launched signals is likely to be a one time cost for the same transmitter. The polarity reversal, however, requires that two independent tests be executed because one cannot be sure which sense of degradation is present in the interconnect under test.

During the calibration processes for the tests the properties of launched signals are measured. Procedures are specified that do not require the adjustment of the launched signal to the maximum allowed degradation. By noting how much degradation could be added to the actual launched signal before exceeding the maximum degradation and adding this difference to the requirements for the received signals one achieves the equivalent effect as actually degrading the launched signals as far as measuring the properties of the interconnect is concerned. Said differently, if the launched signals are better than allowed (as is usually the case) then the requirements on the received signals are tightened by the same amount that the launched signals were better. Similarly, if the launched signals are more degraded than allowed then the received signal range is broadened.

This process eliminates a major problem with creating calibrated degraded high frequency signals, uses the linear property of copper interconnect to good advantage, and allows the properties of the interconnect to be fairly and accurately measured.

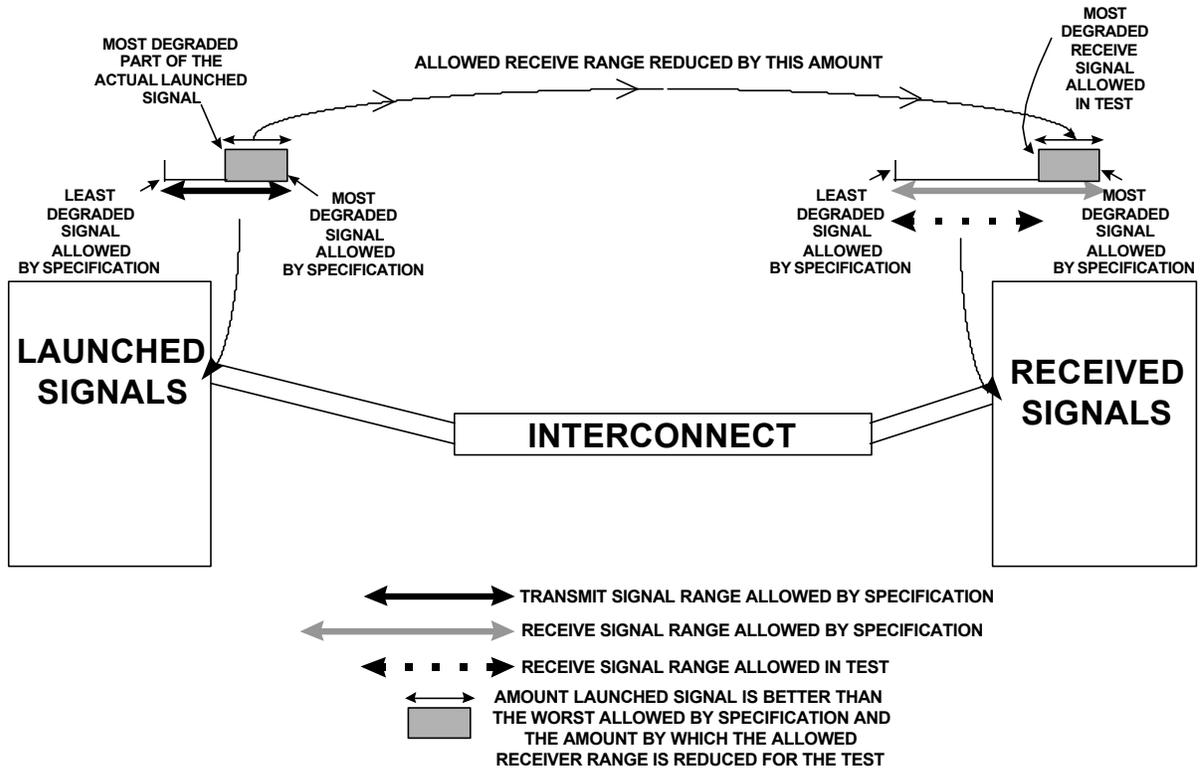


Figure 1 - Range compensation strategy

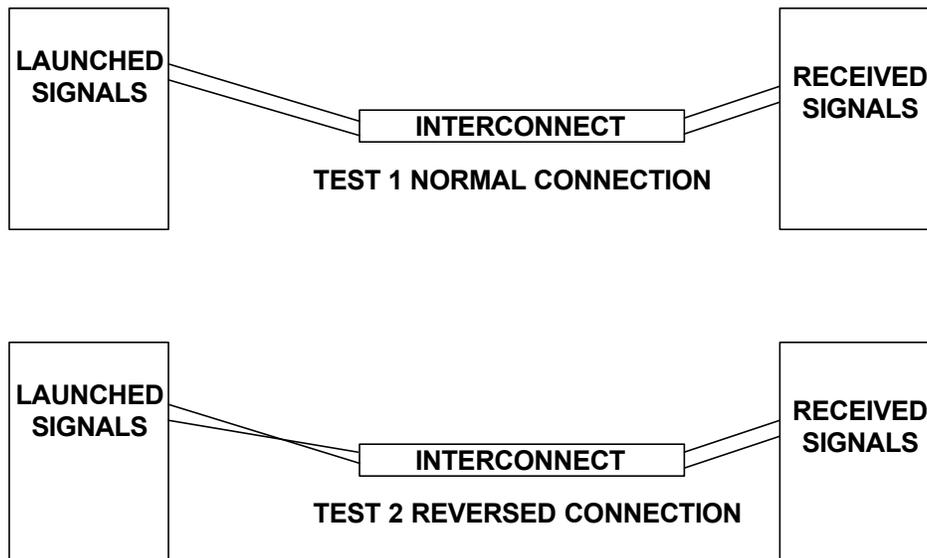


Figure 2 - Degradation sense compensation / detection

5. Framework for HSS testing

This section specifies the framework used for the high frequency performance requirements and test methods to be used for measurement and verification of properties of the interconnect. These requirements apply to the physical connector and to its electrical neighborhood. See section 5.3. Since the connector does not exist alone in a serial link the electrical properties of (1) the wire (or other conductor) termination to the connector contact and (2) any other non-uniformities within the electrical neighborhood of the connector are intrinsic parts of the performance of the connector and its associated interconnect. The electrical performance requirements are on the finished cable assembly, board, the mated partner to the connector and whatever exists within the electrical neighborhood of the physical connector. Tests that are used to measure the high frequency performance properties are termed HSS tests.

## **5.1 HSS test levels**

Two broad levels of HSS tests are described:

### **5.1.1 Level 1 test definition**

Level 1 tests are those that are needed to ensure that the interconnect is capable of (a) transporting minimum integrity (maximum degradation) launched signals to the far end of the interconnect without excessive additional degradation to the launched signals and without exporting excessive interference to other parts of the system in the process and (b) to operate as an effective transmission line between HSS ports.

### **5.1.2 Level 2 test definition**

Level 2 tests are those that characterize specific contributors to the level 1 results and may thereby aid in diagnosing and revealing the source causes of degradations measured in level 1 tests. Level 2 tests are expected to be useful for designing and manufacturing interconnect components that satisfy level 1 tests but are not individually required as direct performance measures of the interconnect. It may be required to use specific level 2 tests to establish the test conditions for level 1 tests.

### **5.1.3 Relationship between level 1 and level 2 tests**

This separation of tests into two levels will be specified in detail in later sections. By separating the testing requirements into the two very different levels, testing resources may be more efficiently utilized compared with the former schemes that required all tests to be individually satisfied. In effect, only the level 1 tests need be used to verify an interconnect for sale or use by both the supplier and the user. The level 2 tests are available to the interconnect designer and manufacturer to more efficiently create designs and manufacturing processes that produce good interconnect. Figure 3 shows a graphical relationship between the two levels of test.

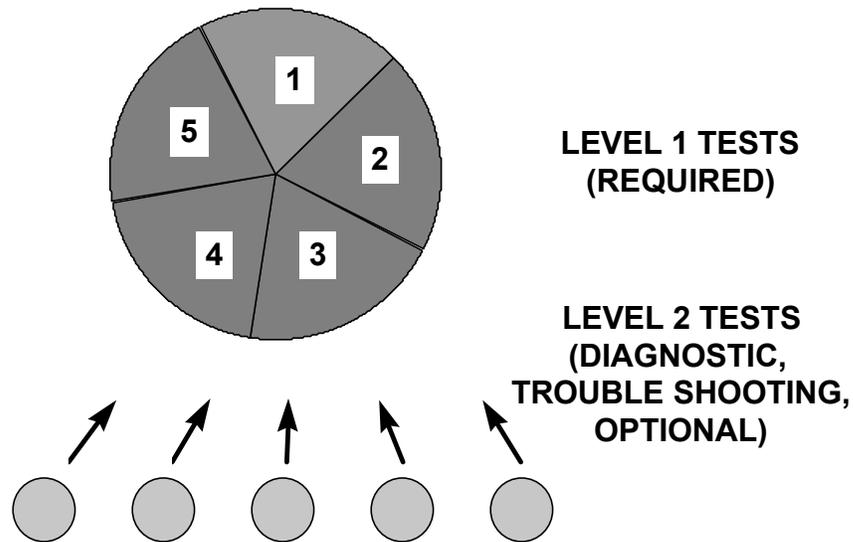


Figure 3 - Two levels of test for HSS interconnect

## 5.2 Applicability to specific connectors

This document contains electrical testing requirements for HSS copper interconnect applications relating to the HSSDC and HSSDB9 connectors. The test methods could also be applied to the SCA-2 40 position connector and other legacy connectors. While these legacy connectors formally have the same performance requirements in the standards as the HSSDC and HSSDB9 (since they are used in the same kind of link) this specification is not attempting to place new requirements on legacy connectors. If an interconnect containing an SCA-2 connector, for example, were to meet the requirements in this specification the connector could be considered an HSSCA-2.

It is assumed that the connectors will be used in a duplex connection where one pair of balanced signal lines is propagating a high speed differential signal through the connector in one direction and another pair of balanced signal lines is propagating an uncorrelated (to the first signal) differential signal through the connector in the opposite direction. Other connectors that may be defined in future specifications when used in a duplex signal application may also be subject to the requirements in this document

Many of the test philosophies and methods documented herein may be applied, with minor modification, to other physical interconnect variants such as unbalanced copper cables, balanced copper backplanes, single mode optical links and multimode optical links. This document is intended to provide the foundation for developing specific test procedures for all high speed serial interconnects.

### 5.3 Electrical Neighborhood

The electrical neighborhood is defined as being those physical electrically conducting structures that have the following properties:

- not part of the physical connector
- attached to a connector termination contact through a signal path
- any part of the signal path that affects the measurement (excluding a 1-2% allowance for multiple reflections)

For time domain reflectometry the electrical neighborhood extends up to the distance occupied by three times the rise or fall lengths from a physical connector part. The largest rise or fall length (rise time or fall time times the propagation velocity) is for the slowest signal under consideration. Examples of properties that may affect the measurement are transmission line impedance mismatches and discontinuities. From this point forward the terms "rise time" and "fall time" have been replaced in this document by the more general term "signal transition duration" or "STD".

For other measurements the electrical neighborhood may extend far beyond the physical connector. Examples of extended electrical neighborhoods are attenuation or cross talk measurements that are affected by the far end termination and media impedance far away from the connectors.

two types of electrical neighborhood are defined:

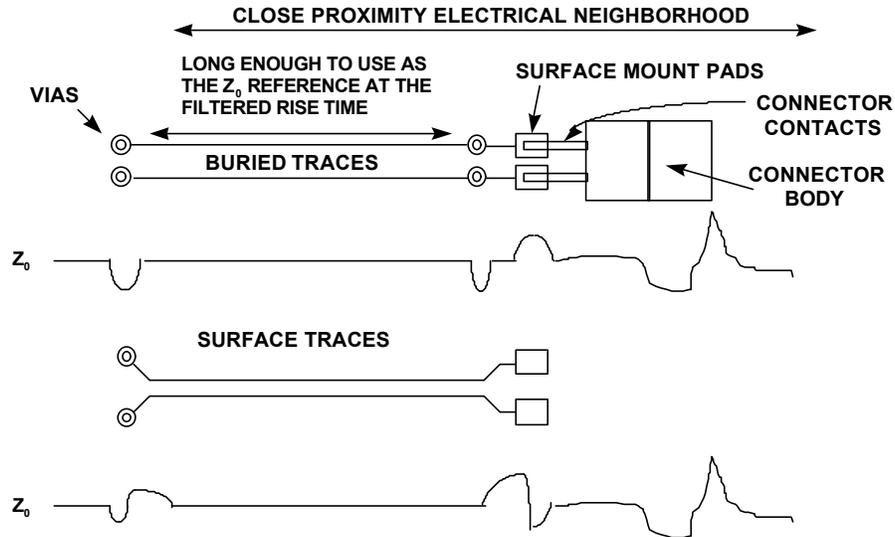
- close proximity (within three STD lengths of the physical connector)
- extended: not close proximity

For example, for a 200 ps (0.2 ns) STD and a media with a propagation velocity of 6 cm/ns the close proximity electrical neighborhood would be all the electrical paths within  $0.2 \times 6 \times 3 = 3.6$  cm from the closest physical connector part. Notice that the slower signals dominate the extent of the close proximity electrical neighborhood but the faster signals that stress the electrical performance the most will have a smaller electrical neighborhood.

Features within the close proximity electrical neighborhood may act as if they were part of the connector itself as far as contribution to the overall performance of the interconnect is concerned. For measurements not requiring high accuracy, smaller close proximity electrical neighborhoods may be allowed.

PCB features such as vias, corners in PCB traces, and pads for board mounting applications all typically fall within the close proximity electrical neighborhood for board mounting applications. Dressing of wire paths near the connector termination, the termination contacts, and metallic strain relief parts typically fall within the close proximity electrical neighborhood in wire termination applications.

Some examples of close proximity electrical neighborhood features that may apply are shown in Figure 4.



**Figure 4 - Some key design areas for pcb features**

Close proximity electrical neighborhoods find their greatest application in the use of time domain reflectometry (TDR) and in the behavior of connectors used as media or transmission line termination elements.

Figure 5 shows an example of a TDR measurement on the same sample with different STD's. The effect of the discontinuities appears larger when shorter STD's are used. It is very important to make measurements using STD's over the entire allowed range. For the shortest allowed STD the maximum amplitude of effects of the discontinuities are revealed. For the longest allowed STD the maximum extent of the close proximity electrical neighborhood is shown.

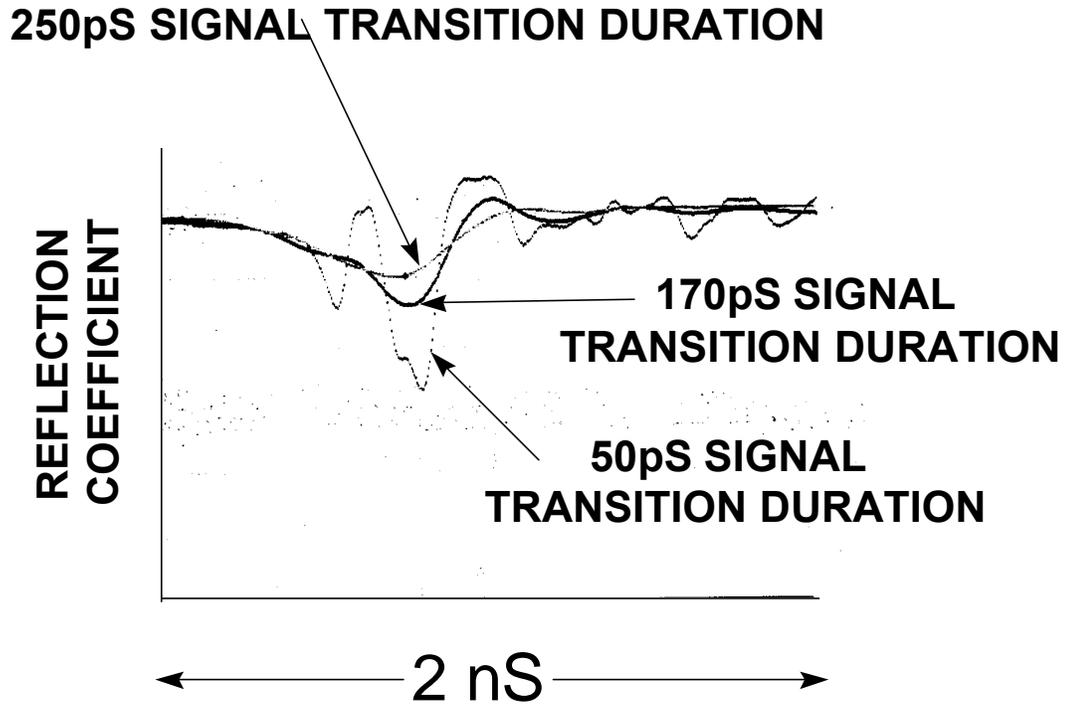


Figure 5 - TDR data in a typical HSS cable assembly

#### 5.4 Definition of level 1 HSS electrical performance parameters

This section gives more detail concerning the level 1 performance requirements.

##### 5.4.1 Definition of PUT and PUT<sub>NOT</sub>

Duplex cable assemblies have two basic parts: (1) the half of the duplex containing the signal path under test and (2) the other half of the duplex containing the half NOT under test. The part that is under test is called the "pair under test" or the PUT. The part that is not under test is called the "pair not under test" or the PUT<sub>NOT</sub>.

The PUT and the PUT<sub>NOT</sub> each have an associated transmitter and receiver. Figure 6 illustrates the relationships.

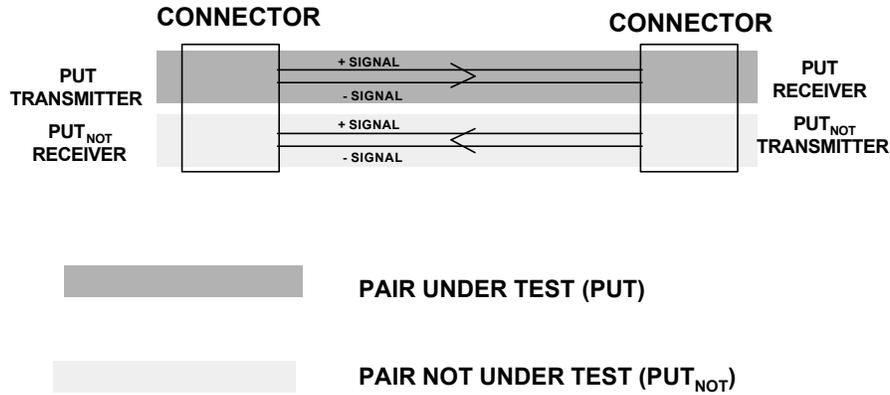
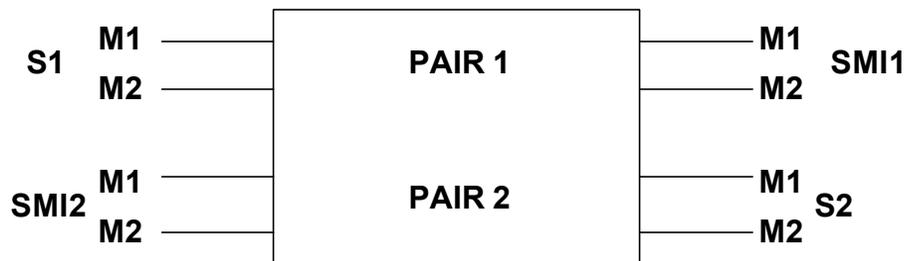


Figure 6 - Terminology for duplex interconnect under test

Figure 7 shows the conventions and abbreviations used for signals and instruments.



**M1 = + SIGNAL**

**M2 = - SIGNAL**

**S1 = DIFFERENTIAL SIGNAL SOURCE 1 (LAUNCH)**

**S2 = DIFFERENTIAL SIGNAL SOURCE 2 (LAUNCH)**

**SMI1 = SIGNAL MEASUREMENT INSTRUMENT 1**

**SMI2 = SIGNAL MEASUREMENT INSTRUMENT 2**

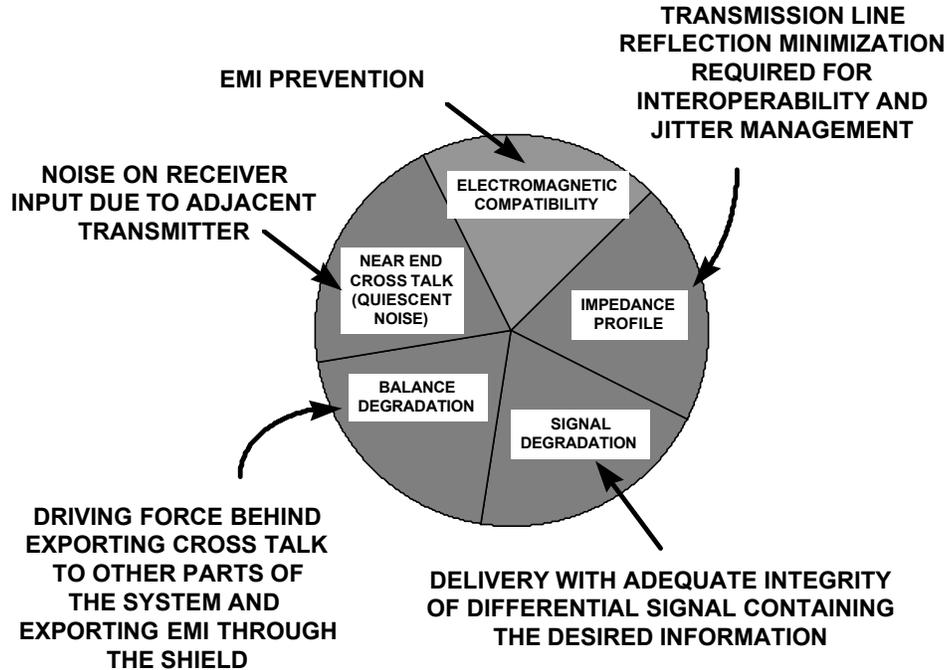
(SMI1 AND SMI2 SHALL BE CAPABLE OF SUBTRACTING  
 M1 AND M2 TO PRODUCE A DIFFERENTIAL SIGNAL AND  
 ADDING M1 AND M2 TO PRODUCE A COMMON MODE  
 SIGNAL)

Figure 7 - Definition of abbreviations used for signals and instruments

#### 5.4.2 Definition of level 1 electrical performance parameters

There are five level 1 electrical performance parameters defined:

- Impedance profile:  $Z_0$  (differential) reflection coefficient versus distance at minimum signal transition duration for the application - measures the ability of the interconnect to function within specifications as a transmission line in the electrical neighborhood of the connector by the use of time domain reflectometry. Also includes requirements on the transmission line outside the electrical neighborhood of the connector in the cable media through the use of differential reflection coefficient with suitable modifications.
- Differential transmission signal degradation (signal degradation): eye pattern comparison test where differential signals from the PUT transmitter (the difference of the +signal and the - signal) having minimum allowed differential amplitude and maximum allowed jitter for transmitters are transferred to the PUT receiver without losing amplitude and without increasing the jitter beyond the allowed specification for the receiver. The PUT<sub>NOT</sub> transmitter has uncorrelated worst case signals (maximum amplitude, minimum STD, maximum allowed imbalance) present during the testing. The signals from the PUT<sub>NOT</sub> transmitter consist of data patterns with both a run length of at least 5 and run length of 1 - e.g. the K28.5 pattern or individually programmed patterns.
- Signal transmission balance degradation (balance degradation): eye pattern - like (no open "eye" expected for this test) limit comparison test. Launched differential signals into the PUT with known common mode content ( the sum of the + signal and the - signal) and data patterns with a run length of at least 5 and minimum run length of 1 - e.g. the K28.5 pattern are transferred to the other end of the PUT interconnect without adding common mode amplitude beyond the allowed specification for the PUT. The PUT<sub>NOT</sub> transmitter uses a different clock source from the PUT transmitter and has uncorrelated (to the line under test) differential signals with the maximum signal amplitude, minimum signal transition duration, maximum allowed common mode content and a data pattern with both a run length of at least 5 and run length of 1 - e.g. the K28.5 pattern present during the testing.
- Electromagnetic compatibility (EMC): the energy that may be coupled to the world external to the IUT shield. Two methods for measuring this performance requirement are available: (1) Common mode power transfer, CMPT, (formerly known as "transfer impedance" or shield effectiveness) and (2) Electromagnetic radiation.
- Near end cross talk, NEXT, (Quiescent noise): the amplitude of the signal at the PUT<sub>NOT</sub> receiver (adjacent to the PUT transmitter) when no signal is driven into the PUT<sub>NOT</sub> receiver from the PUT<sub>NOT</sub> transmitter. The signals from the PUT transmitter are individual isolated pulses that have the maximum permitted amplitude, minimum permitted signal transition duration, and maximum unbalance.



**Figure 8 - Level 1 tests**

### 5.5 Definition of level 2 HSS electrical performance parameters

Five level 2 electrical performance parameters are defined below.

1. Attenuation (insertion loss): The ratio of output to input differential voltage amplitudes at a specific sinusoidal frequency is used to calculate the attenuation in dB. The frequency is swept across the range of interest, typically 100 kHz to 3 GHz. Note that square waves are not allowed for this test due to difficulties with measurement calibration. Attenuation is a primary contributor to eye closure and intersymbol interference for differential signals.
2. Propagation time and propagation time skew: the propagation time is the time required for the midpoint of a signal edge to propagate between an input and output measurement point. The propagation time skew is the difference in the time required for the midpoint of the signal edges to simultaneously propagate down two nominally identical paths between an input and output measurement point. The line to line propagation time skew within the same pair (used in this document) is the difference in the propagation time between the single ended signals in the + signal and - signal lines. The pair to pair propagation time skew (not used in this document because each pair operates under a different timing domain) is the difference in the propagation time between the differential signals in two different pairs. Propagation time skew is a primary result of physically unbalanced media construction and of launched signal skew.
3. Amplitude imbalance between the + signal and - signal: the maximum magnitude of the difference between the peak amplitudes on the + signal and - signal lines at any point in time.

4. Signal transition duration (rise / fall time): the time required for a differential signal edge to traverse between 20 and 80 percent of the difference between the low level and the high level in a signal edge (rising edge) or between 80 and 20 percent of the difference for a falling edge - very important parameter in setting up the level 1 tests as it significantly determines the induced common mode levels, the EMI, the impedance profile, quiescent noise and intersymbol interference.
5. Cross talk component of signal degradation: The effect of uncorrelated signals on  $PUT_{NOT}$  on the signals in the PUT. Cross talk generally degrades signal quality including increased jitter and amplitude parameters on the differential eye pattern. Three different approaches are described: individual pulses, eye diagram with broad spectral data pattern, and swept sinusoidal.

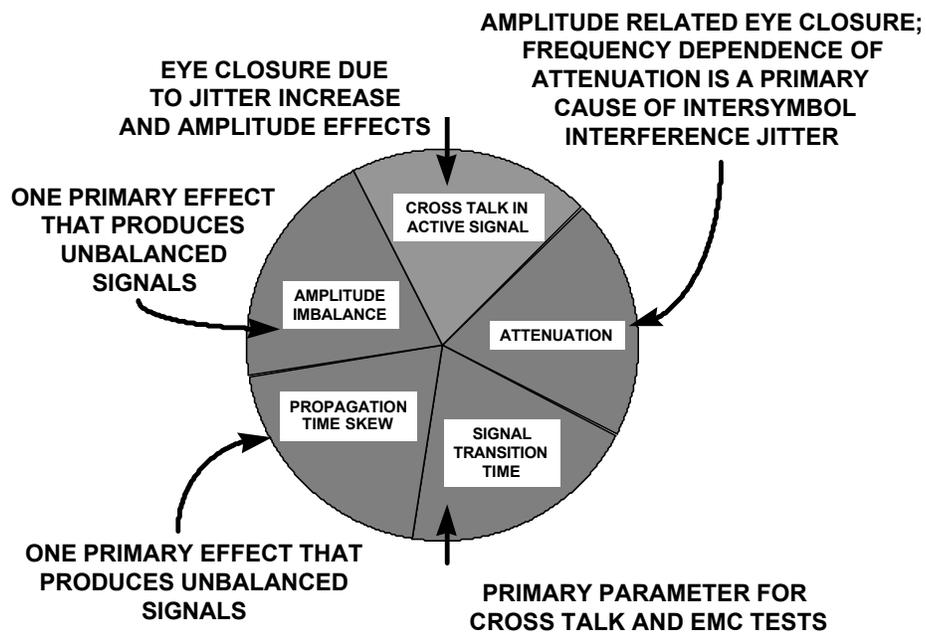


Figure 9 - Level 2 tests

### 5.6 Basic requirements for executing a test

Each parameter has specific allowed ranges as determined from a test measurement. Each measurement requires:

- test fixturing to allow connection of instrumentation and interconnect under test (IUT)
- calibration procedures to account for the effect of fixturing
- applied stimuli and measured responses that contain the results of the HSS test

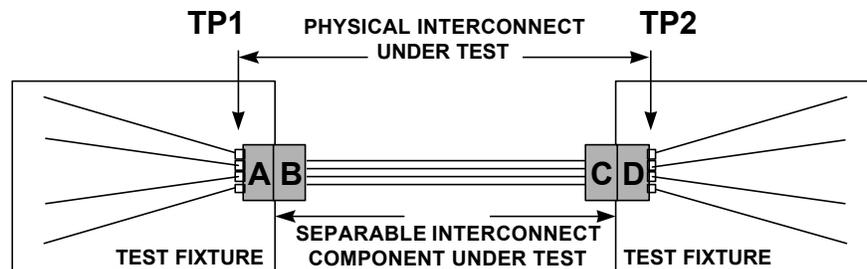
In general, different fixturing and measurement requirements exist for each parameter. In practice, it is very desirable to have the same test fixture for several, if not all, tests.

The calibration procedure will usually be different for the different tests.

The acceptable range for each parameter may differ for different performance classes.

### 5.7 Definition of the HSS interconnect under test (IUT)

The interconnect under test (IUT) is always at least a mated connector pair (for example connectors A and B in Figure 10), the terminations for each side of the mated connector, and the electrical features within the electrical neighborhood for each side of the mated connector. In some cases the interconnect under test is a completed cable assembly having a specific length, the mated connectors on each end and the electrical features within the electrical neighborhood of each end.



**A, D = PERMANENTLY MOUNTED CONNECTOR ON THE TEST FIXTURE  
B, C = PART OF THE SEPARABLE INTERCONNECT UNDER TEST**

**TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED  
TO REPORT VALUES AT TP1 AND TP2**

**SEPARABLE INTERCONNECT PERFORMANCE IS JUDGED  
BY ITS PERFORMANCE AT TP1 AND TP2 (WHICH INCLUDES  
THE EFFECTS OF CONNECTORS A AND D)**

**Figure 10 - Definition of the interconnect under test**

This definition of the interconnect under test does not allow electrical performance specification of a connector outside the context of a specific application. Some tests, such as impedance profile may allow visibility of the contribution of the connector while other tests will show only the net effect of the complete interconnect system under test without directly offering visibility to the contribution of the connector. If the interconnect system performs adequately according to the tests in this document then the connectors or other pieces of the interconnect system are adequate.

## 5.8 Special considerations for test fixtures

Using the definition of the IUT in section 5.7 parts of the total IUT remains attached to the test fixtures and are typically used many times when testing different removable parts of the IUT (see Figure 10). The "A" and "D" halves of the mated connectors are permanently attached and are termed the "stationary" parts of the IUT.

This definition for the IUT is necessary in order to measure the performance of the total connection but it has several consequences that may not be obvious.

The contribution of the stationary parts of the IUT to the measured result for the total IUT may not be small. The stationary parts could compensate for or exacerbate degradations caused by the removable parts of the IUT. It is generally expected that different removable parts of the IUT will cause different total IUT test results. What may be less obvious is that IUT's with the same removable part but with different test fixtures with different stationary parts may also yield different results. In both cases the differences in the IUT test results exist even if identical instrumentation and calibration processes are used.

Therefore:

- Differences in the IUT test results from different laboratories are to be expected unless the same total IUT (both the same stationary and the same removable parts) are tested together
- If the stationary parts of the IUT compensate for the removable parts then it is to be expected that other laboratories testing the same removable part may find that the removable part fails (since their stationary parts may not deliver the same level of compensation)
- If the stationary parts of the IUT exacerbate the degradation in the removable parts to the extreme allowed without allowing the total IUT to fail then a more conservative total IUT test results and it becomes unlikely that testing with different stationary IUT parts will show failures in the total IUT

Suppliers of removable IUT parts (typical cable assemblies) will need to carefully understand the effects of the stationary parts of the IUT in their testing so that unintentional compensation of removable parts is not occurring.

Although the stationary parts of the IUT are attached to the test fixture they are not formally part of the test fixture (even though it may appear so in a casual observation since they are attached). Anything within the electrical neighborhood of the stationary parts of the IUT is also formally part of the IUT and not part of the test fixture.

## 5.9 Extensions to parallel - serial constructions

This section describes how to extend the tests described in this document to constructions beyond the simple duplex. Such constructions are useful for example when one needs higher bandwidth without sacrificing length and more paths carrying information is easier than a single path because clock rate

increase on a single path is not desirable. Other possible reasons include needing additional independent control paths and needing some paths to be bi-directional. When the basic transmission on a single path is serial unidirectional and there are multiple paths following the same physical routing (for example multiple twin-axes in the same overall jacket) the construction is termed parallel - serial (p-s) in this document.

Several new transports, including FC, are considering using p-s constructions because the problems facing increasing the data rate on a single path are greater than the problems of introducing multiple paths.

The extensions described here apply only to point to point applications (which may or may not contain equalizers or active circuits in the path for most tests). Specifically, multidrop constructions are not considered.

In general one uses superposition along with worse case alignments and polarities (to avoid cancellations) to deal with the more complex structures. A generalized p-s construction is shown in Figure 11. The  $S_n$  is a source for the  $n$ th path while the  $SMIn$  is the signal measurement instrument corresponding to the  $n$ th source.

## GENERALIZED PARALLEL SERIAL PATHS FOR POINT TO POINT CONNECTIONS

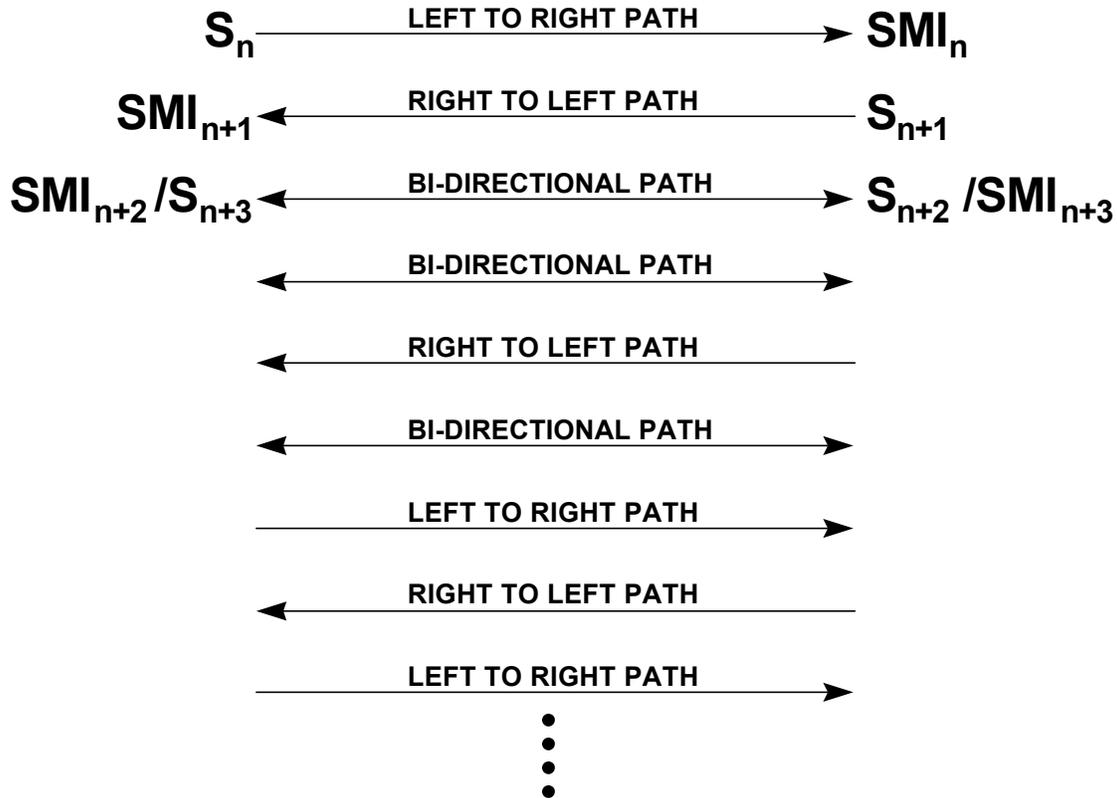


Figure 11 - Sources and instruments for a general p-s construction

The five level 1 tests for duplex assemblies each have a counterpart in p-s constructions. Each will be briefly considered separately.

### 5.9.1 Impedance profile for p-s constructions

The impedance profile test is exactly the same as for a duplex PUT. Each path in the p-s construction is measured separately and uses the same test procedures described in this document.

### 5.9.2 Signal degradation for p-s constructions

This test is essentially the same as for duplex assemblies except that additional second sources may be required for all the  $PUT_{NOT}$ 's and a test fixture suitable for the p-s construction is needed. Note that there may be second sources on the same side of the IUT as the primary source.

A general feature of p-s constructions is that one does not need to use second

sources for the paths that are not coupling significantly to the PUT. However, until proven otherwise, ALL PUT<sub>NOT</sub>'s shall have worst case signals applied. Unfortunately there is no simple way to use superposition for this test (unlike the cross talk test described below) so all second sources shall be on at the same time the PUT is being tested.

All the second sources on the same side may be derived from the same clock source as would be normal in a real application and may be distributed to several PUT<sub>NOT</sub>'s from the same second source. Many times the second sources on the same side as the Sn will be derived from the same clock source as the Sn and Sn may also be used as a second source in this case. It is up to the user to determine the requirements of the transport protocol and to structure the test accordingly.

For the bi-directional case where each direction is used at different times by the transport protocol the path must be tested separately in each direction. There is at least one implementation used in Ethernet where the launched signal simultaneously contains the received signal and signal processing is used to subtract the transmitted signal so that the received signal may be revealed. This document does not describe how to test simultaneous bi-directional transmissions.

A complete test of a p-s construction is therefore a combination of tests where each PUT is separately tested. For example, a p-s construction containing 4 left to right, 4 right to left, and 2 bi-directional paths a total of  $4+4+2 \times 2=12$  tests are needed.

### **5.9.3 Balance degradation for p-s constructions**

The balance degradation tests follow exactly the same flow as described in 5.9.2 for the signal degradation except using the balance degradation methodology instead of the signal degradation methodology.

### **5.9.4 EMC for p-s constructions**

The CMPT test applies to p-s constructions essentially without modification. The EMR test requires that the excitation be set up to simulate actual signals on all paths simultaneously but is otherwise identical to the duplex case.

### **5.9.5 Near end cross talk for p-s constructions**

Near end cross talk for p-s constructions is determined by sequentially applying aggressor pulses on every path except the victim path and recording the cross talk contribution from each aggressor path. The absolute value of the results are then added to produce to total cross talk on that victim line. The test conditions are identical to the duplex case described in this document with suitable modifications to the test fixtures to accommodate the p-s constructions.

This extension methodology was originally developed for use on parallel SCSI cables and does produce a conservative (i.e. more stringent) test on the IUT

than actually exists in service. However, since there is no correlation assumed (either time or amplitude) between the aggressor signal and the service signals in this test the resulting noise measurement (calculation) is the worst possible condition and there cannot be a more intense cross talk in service than revealed by this test.

The process is repeated for every victim line in the p-s construction.

Note that for bi-directional paths that two tests are required.

### 5.9.6 Summary of extensions to p-s constructions

With simple modifications to the test process and test fixtures a very broad array of complex p-s constructions can be tested using the basic procedures described in this document for duplex constructions. It is not practical to attempt to detail every possible p-s construction but the formula for constructing these details are contained herein.

### 5.10 Map of the HSS parameters

Table 1 shows the map of the HSS performance parameters

**Table 1 - Map of the HSS testing requirements**

PARAMETER	TEST FIXTURE AND MEASUREMENT EQUIPMENT DESCRIPTION	CALIBRATION PROCEDURE	TEST PROCEDURE	ACCEPTABLE RANGES
IMPEDANCE PROFILE	SECTION 6.1.1	SECTION 6.1.2	SECTION 6.1.3	SECTION 6.1.4
SIGNAL DEGRADATION	SECTION 6.2.1	SECTION 6.2.2	SECTION 6.2.3	SECTION 6.2.4
BALANCE DEGRADATION	SECTION 6.3.1	SECTION 6.3.2	SECTION 6.3.3	SECTION 6.3.4
EMC	SECTION 6.4.1.1 SECTION 6.4.2.1	SECTION 6.4.1.2 SECTION 6.4.2.2	SECTION 6.4.1.3 SECTION 6.4.2.3	SECTION 6.4.1.4
NEAR END CROSS TALK	SECTION 6.5.1	SECTION 6.5.2	SECTION 6.5.3	SECTION 6.5.4
ATTENUATION	SECTION 7.1.1	SECTION 7.1.2	SECTION 7.1.3	NA
PROPAGATION TIME SKEW	SECTION 7.2.1	SECTION 7.2.2	SECTION 7.2.3	NA
AMPLITUDE IMBALANCE	SECTION 7.3.1	SECTION 7.3.2	SECTION 7.3.3	NA
SIGNAL TRANSITION DURATION	SECTION 7.4.1	SECTION 7.4.2	SECTION 7.4.3	NA
CROSS TALK COMPONENT OF SIGNAL DEGRADATION	SECTION 7.5.3.1	SECTION 7.5.3.2	SECTION 7.5.3.3	NA

## 6. Level 1 tests

## 6.1 Impedance profile

The impedance profile of an HSS cable assembly is a measure of the disturbance to the signals passing through caused by the connector and the signal paths directly attached to the connector. An ideal connector system will exactly match the media impedance at all time points associated with the connector. The intensity of the disturbance to the signals is directly affected by the STD of the signal and the impedance, therefore, shall be measured with signals that span the extremes of the STD's for the application.

This impedance profile test is intended to be used on cable assemblies that do not have passive or active components in the path other than the connector contacts and the media wires. Specifically, passive equalizers typically introduce resistors, inductors and capacitors into the path and may cause the impedance profile to exceed the allowed limits for this test. The equalized cable assembly may fail the test limits described but actually be acceptable for use in the link.

If passive equalizers are used in a cable assembly the media impedance portion of the profile will be affected by the equivalent d. c. resistor network of the equalizer (typically causing the media portion to appear much higher impedance than without the equalizer) and also may affect the profile near the connector. This impedance profile test may be used as a level 2 test for assemblies with passive equalizers.

The impedance profile is a plot of characteristic or transmission line impedance as recorded by a time domain reflectometer instrument. There is an indirect mapping of the measurements to the physical position within the device under test. This test is needed to control signal reflections within the close proximity electrical neighborhood of the connector. The test shall be performed at both extremes of the allowed signal transition times for the end use application. Fast transitions enhance the effect of non-uniformities. Slow transitions increase the extent of the close proximity electrical neighborhood.

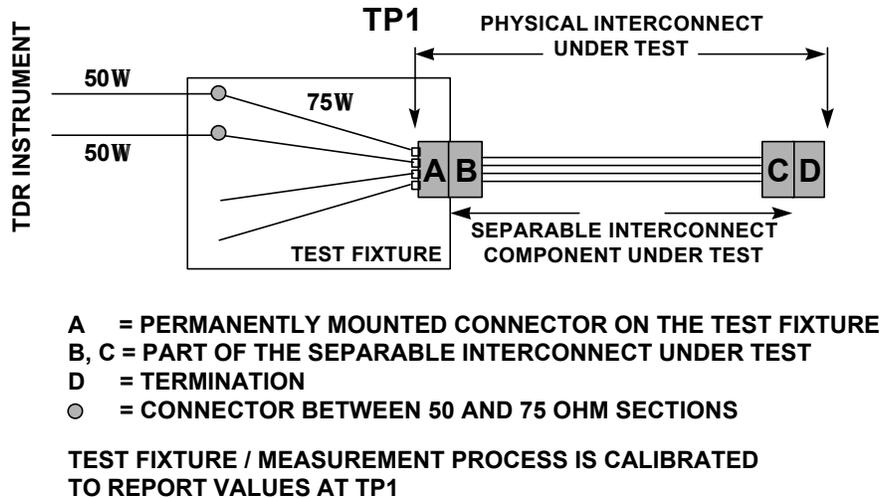
The signal driven by the TDR heads in some equipment are dual channel complementary single ended signals that start out at non-zero voltage and rise, with a matched rise time, in opposite directions to produce a collapsing differential signal that ends at zero volts.

These TDR signals may be different from that driven from most functional HSS transmitters. Functional HSS transmitters drive the + signal high and the - signal low or the + signal low and the - signal high -- they do not dwell at the zero output level. The calibration for the impedance profile tests is therefore somewhat different than that required for other tests that require controlled signal transition duration.

### 6.1.1 Test fixture and measurement equipment

#### 6.1.1.1 Test fixture

Figure 12 shows the test configuration for the impedance profile tests.



**Figure 12 - Test configuration for impedance profile**

The test fixture may be constructed of semi rigid coax, precision coax, microstrip PCB, or stripline PCB. The test fixture must contain the entire close proximity electrical neighborhood on the side of the connector near the instrumentation and have a section where there are no non uniformities such as vias. This section is used as an aid in calibrating the TDR for transmission line impedance. The far end of the unit under test shall be terminated in the nominal transmission line impedance of the media in the unit under test, differential impedance =  $150\Omega$ , within 5% (to minimize multiple reflections). The signal line to ground termination impedance is whatever it needs to be to meet the  $150\Omega$  differential requirement. Typically the signal line to ground impedance is approximately  $75\Omega$ .

#### 6.1.1.2 Measurement equipment

Equipment such as the Tektronix 11801 with SD24 TDR/sampling heads or equivalent shall be used. This equipment has features such as software filters to simulate the effects of different STD's, auto readout of cursor positions, and conversion between reflection coefficient and transmission line impedance.

#### 6.1.2 Calibration and verification procedure

##### 6.1.2.1 Instrument calibration

Connect a known separate  $50\Omega \pm 1\%$  load at the far end of each of the  $50\Omega$  cables attached to the TDR that will be used to connect to the test fixture. The differential impedance recorded at the end of the cable should be  $100\Omega$ . This calibration will account for the losses in the cable and validates the instrument calibration.

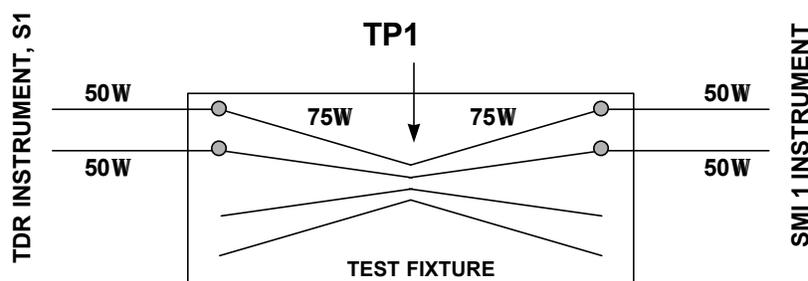
### 6.1.2.2 Test fixture verification

Connect the 50Ω cables to the test fixture and record the value when the trace is in the uniform portion of the test fixture. The other end can be open or have a cable assembly attached. This establishes the effects of the reflection from the 50Ω to the 75Ω discontinuity between the test fixture and the 50Ω cable. If the differential impedance in the uniform portion of the trace is  $150 \pm 10\Omega$  then the test fixture is satisfactory. This measurement should be independent of the TDR filter setting (signal transition duration) over the range of the measurement.

### 6.1.2.3 Differential signal transition duration calibration

This ensures that the proper signal transition time is being presented to the IUT.

A special test fixture is required for this calibration. Progressing from left to right the test fixture is exactly like the test fixture in Figure 12 up to the TP1 point and continues as a mirror image through TP1 as illustrated in Figure 13. Previous versions of this calibration procedure used a reflected pulse measured at the source, S1, that required an electrical short at TP1 using the test fixture shown in Figure 12. The previous method has been found to be prone to serious error due to the effects of reflections within the test fixture. These reflections can be a very significant part of the measured signal at the TDR head (position S1 in Figure 13). However, when using the transmitted signal through TP1 in a thru connection sense as shown in Figure 13 the effects of the reflections in the test fixture are second order. The signal measured at SMI1 accurately represents the signal presented to the IUT at TP1.



○ = CONNECTOR BETWEEN 50 AND 75 OHM SECTIONS

TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED  
TO REPORT VALUES AT TP1

Figure 13 - Test fixture for STD calibration

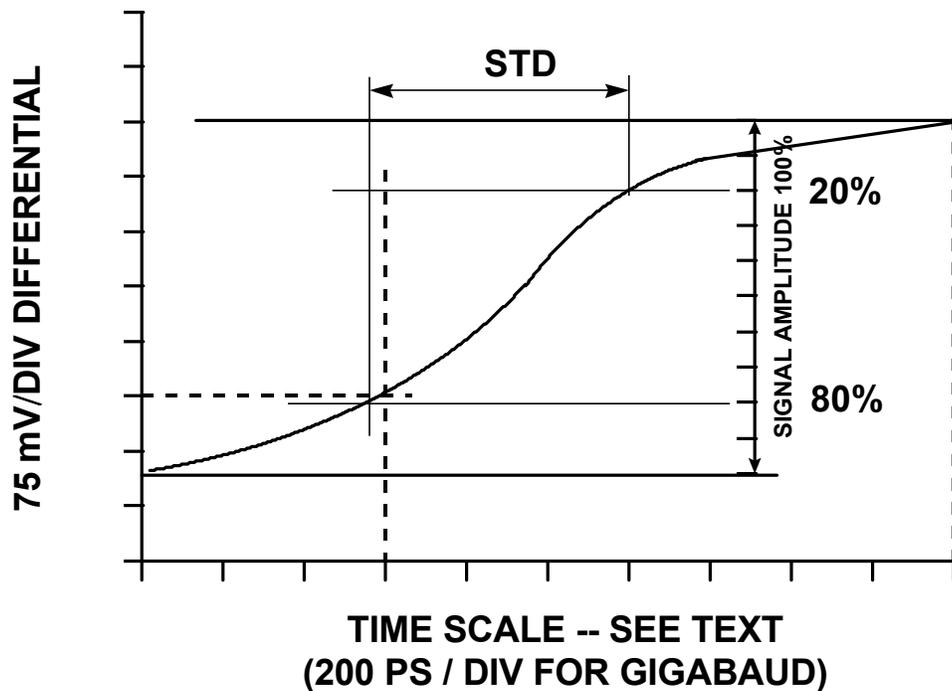
Using the test fixture and configuration shown in Figure 13 apply a differential pulse from S1 as large as possible within the capabilities of S1 (if the amplitude is adjustable on S1 otherwise use the default pulse from S1) and measure the received differential pulse at SMI1. Most practical TDR instruments present the signal resulting at SMI1 as a rising differential pulse.

To calibrate the STD for the rising pulse edge set up the display on the SMI1 as shown in Figure 14. The following procedure results in a calibrated STD:

- The span of the time scale on the display is approximately twice the nominal bit period for the data rate being used. Ten divisions are used on the time axis. Specifically Table 2 shows the time scales to use.
- Set the vertical axis at 75 mV per division.
- Move the displayed curve to the right and adjust the vertical position such that the flat portion of the curve (flat for at least three time divisions) passes through the first graticule (division) from the bottom.
- Set the horizontal position such that the displayed curve passes through the third graticule on the time axis and the third graticule on the vertical axis.
- Use the measure function on SMI1 to find the peak to peak signal amplitude of the displayed portion of the trace as shown in Figure 14. This amplitude may also be read directly off the display. This signal amplitude of the displayed trace may or may not accurately represent the asymptotic signal levels that may exist at times not displayed.
- The signal transition duration (STD) is the time between the 20% and 80% values of the displayed signal amplitude.

**Table 2 - Scale to be used for STD calibrations**

Bit rate * (Mbits/s)	Time axis scale (ps/div)
20 ST	5000
40 ST	2500
40 DT	5000
80 ST	1250
80 DT	2500
100 DT	2000
200 DT	1000
400 DT	500
800 DT	250
1062.5	200
1250	200
1600	100
2125	100
2500	100
3200	50
4250	50
5000	50
* ST = single transition clocking DT = double transition clocking	



• **Figure 14 - Signal transition duration calibration**

It may be found with some practical test fixtures that the extreme level is not found at the 10<sup>th</sup> graticule. An example of such a trace is shown in Figure 15 (for a falling pulse example) where a reflection causes the lowest level to be at approximately the 8<sup>th</sup> horizontal graticule instead of at the 10<sup>th</sup> graticule. Using automatic features of some instruments will cause the reflection to be used to set the level. If the peaks are not at the 0 and 10<sup>th</sup> horizontal graticules then an extrapolation should be used to determine the peak level as shown in Figure 15. It is important that this step not be avoided because the STD can be seriously affected if the signal edge rolls off slowly near one or both ends of the transition region.

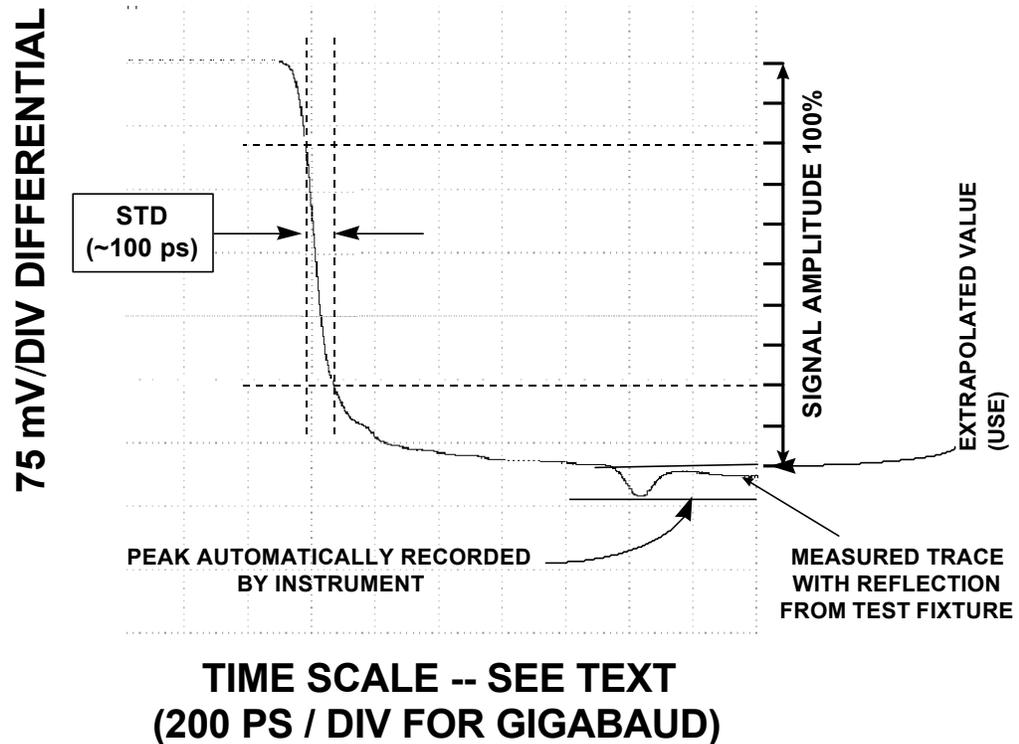


Figure 15 - Setting amplitude for STD with degraded test fixture

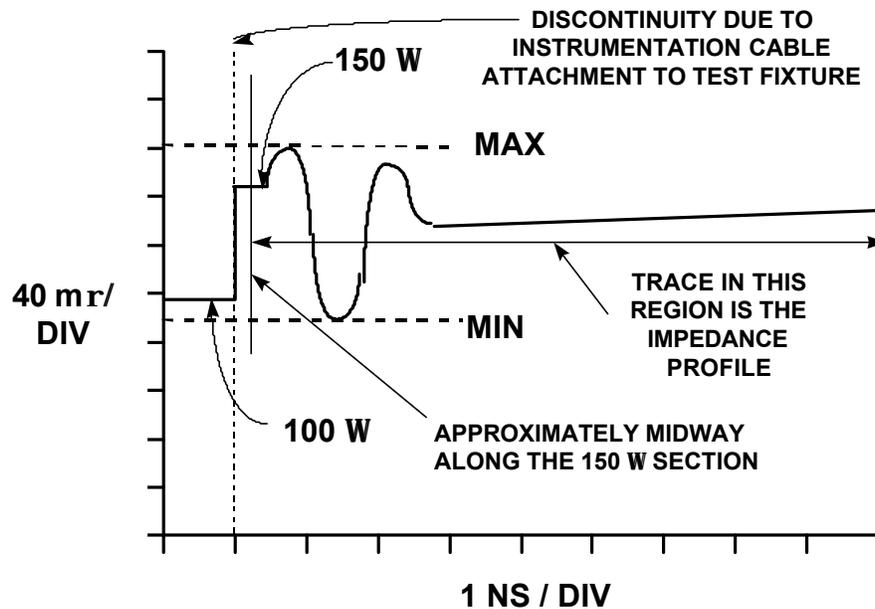
Adjust the filter function on SMI1 so that the desired STD is displayed. Note that there will usually be two values of STD required: one for each extreme of the specification. For gigabit FC the extremes are 100 ps to 385 ps. The value of the filter setting required to achieve these STD conditions should be used during the impedance profile measurement.

Retain all the settings for reuse in the measurement.

### 6.1.3 Testing procedure

#### 6.1.3.1 Impedance profile in connector region

Connect the separable interconnect under test to the test fixture receptacle connector, terminate the separable interconnect under test with its nominal transmission line impedance (passive) and record the TDR trace using the method described below. Figure 16 shows the TDR display setup to use for this measurement.



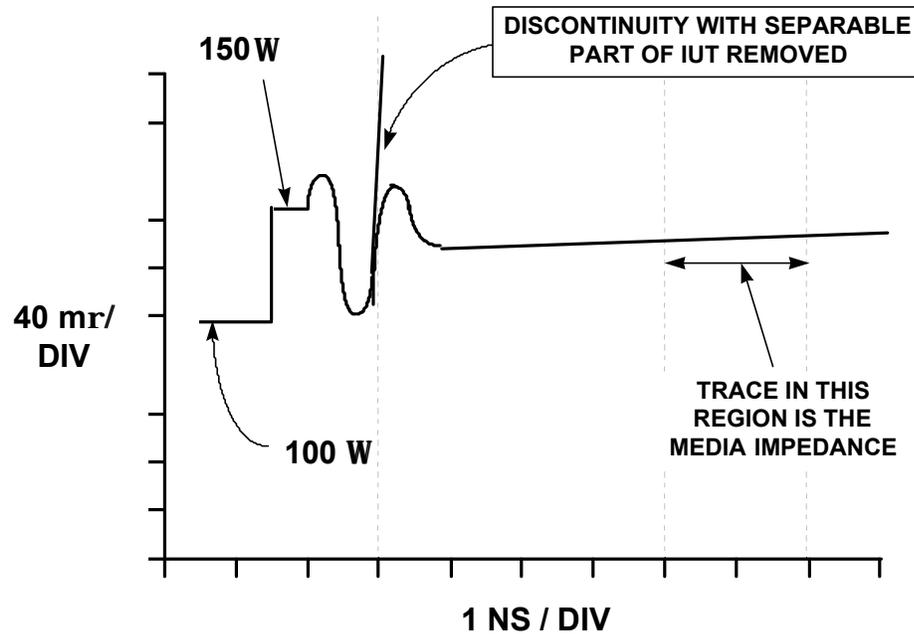
• **Figure 16 - Transmission line impedance profile measurements**

- Set the time scale to 1 ns /div (total time axis span of 10 ns).
- Set the vertical scale (mp) to 40 mp /div
- Adjust the vertical position to approximately center the trace on the display
- Adjust the horizontal position such that the discontinuity between the instrumentation cables and the test fixture is on the first division. (It may be necessary to disconnect the instrumentation cables from the test fixture and disable the filter to find this time position - if disconnected, reconnect the cables and re-enable the filter)
- Set the TDR cursor to read ohms
- Use the cursor to measure the minimum and maximum values in ohms near the left side of the trace that shows the disturbances from the connector

Execute the test with both extremes of transition time allowed (e.g. 100 ps and 385 ps for Gigabit FC) using the above method to record the trace. Note: a separate calibration and verification should have been done at these STD extremes. Different test fixtures may be required to accommodate the three STD length requirement for the uniform 150  $\Omega$  region.

#### 6.1.3.2 Impedance profile in the media region

Using the same setup as for section 6.1.3.1 execute the following:



**Figure 17 - Media impedance measurement**

- Set the time scale to 1 ns /div (total time axis span of 10 ns).
- Set the vertical scale (mp) to 40 mp /div
- Adjust the vertical position to approximately center the trace on the display
- Disconnect the separable part of the IUT and adjust the horizontal position such that the discontinuity at the open produced is on the third division. (Pick any convenient part of the discontinuity signal to use to set this position).
- Set the TDR cursor to read ohms
- Record the min, max and average of the trace between 7<sup>th</sup> and 9<sup>th</sup> divisions displayed (4 to 6 ns from the IUT separation point). (see Figure 17).

The media impedance measurement contains a small error caused by losses in the wire which increases the measured value slightly.

#### 6.1.4 Acceptable ranges

The trace within the close proximity electrical neighborhood should be within in the range shown in Table 6 in Annex A for all signal transition times allowed for the application. If an exception window is allowed where the values may be outside the nominal range for a period of time it is noted in the table.

The FC standards allow a 800 ps exception window (see Annex A) for this test. The FC standard is applied to constructions beyond cable assemblies, for example GBIC's, and does not distinguish between the details of the applications. The SFF HSS group recommends that a reduced exception window be allowed for duplex copper cable assemblies. The requirements recommended are a

window of no more than 300 ps with impedance between 90 and 190 ohms in the window (this is a reduction in the exception window width of 500 ps). This 300 ps exception window applies for full speed and double speed applications.

## 6.2 Signal degradation

There are three major planks in the strategy for this test:

- Use linearity and superposition as much as possible to simulate the worst case input signals
- Use linearity and superposition as much as possible to simulate the allowed output mask
- Ensure that the activity on  $PUT_{NOT}$  is close to the most extreme allowed

The test ideally consists of applying the most degraded allowed transmitter output signal to the PUT and verifying that the signal into the receiver (out of the PUT) does not violate the specified receiver mask. The main technical challenges are to actually produce the worst case legal signal into the interconnect and to not violate the requirements of the signal levels available to/from real test instruments.

For purposes of this test it is assumed that only two properties of the transmitted signal are important: the vertical eye opening (amplitude) and the horizontal eye opening (jitter). If the actual applied signal does not match the allowed transmit eye mask in other areas no further attempts are made to make a more perfect fit. The procedure for simulating a worst case signal is:

1. Using an available signal from a real source (while transmitting a 2\*\*7-1, K28.5 or other data pattern with run lengths of at least 5 max and 1 min and frequency within 1% of the nominal data rate) the reported amplitude for the eye opening is adjusted using software compensation such that it appears that the minimum allowed transmit eye opening is being applied. This same amplitude scale and scaling factor is used to record the received eye.
2. The difference between the actual jitter in the transmitted signal and the maximum allowed jitter is used to adjust the receive eye mask by an equal amount in the opposite direction (making the receive mask wider and therefore more difficult to achieve). This procedure is shown in Figure 18. The minimum jitter margin in the transmit mask is the value added to the receiver mask. Jitter in the transmit signal is transmitted unattenuated to the receiver across the PUT - superposition applies.

Also shown in Figure 18 is a timing reference for both sides of the eye that is needed to position the signals along the time axis so that the signals have the specified relationship with the position of the mask. This timing reference is created by finding the mean of the population of the transmit signals at the zero differential voltage crossing points.

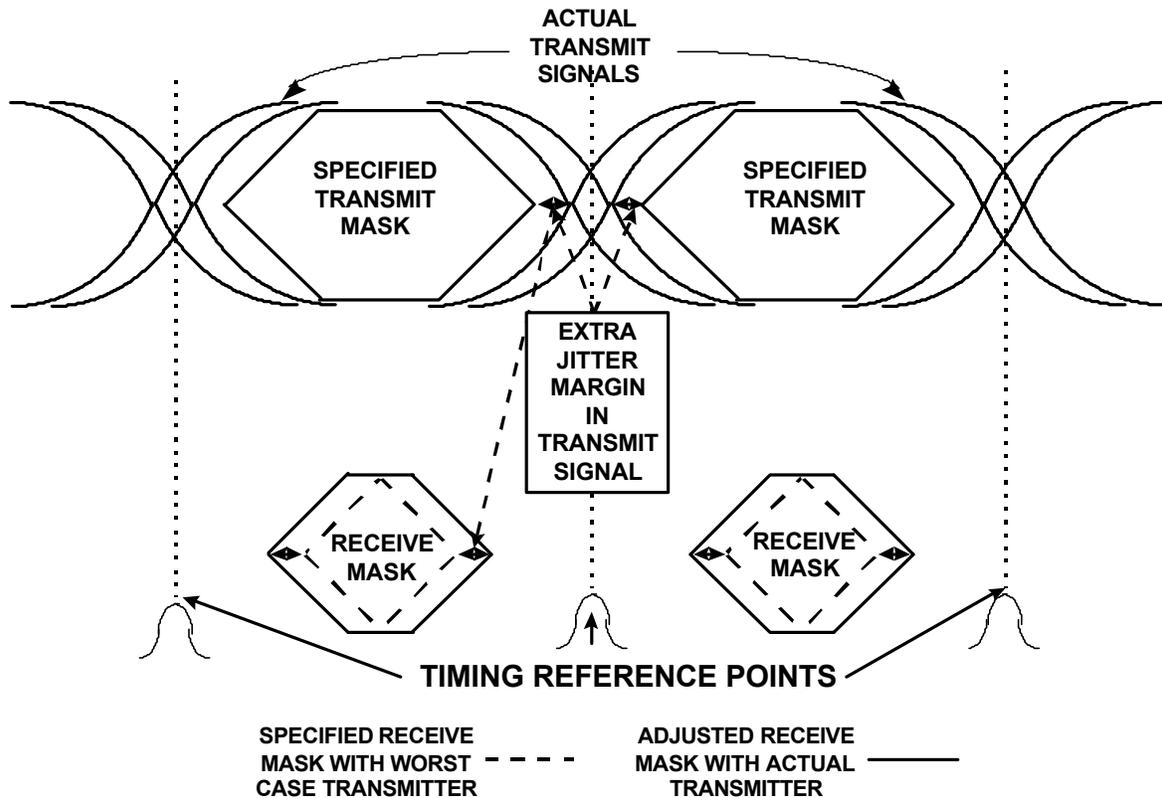
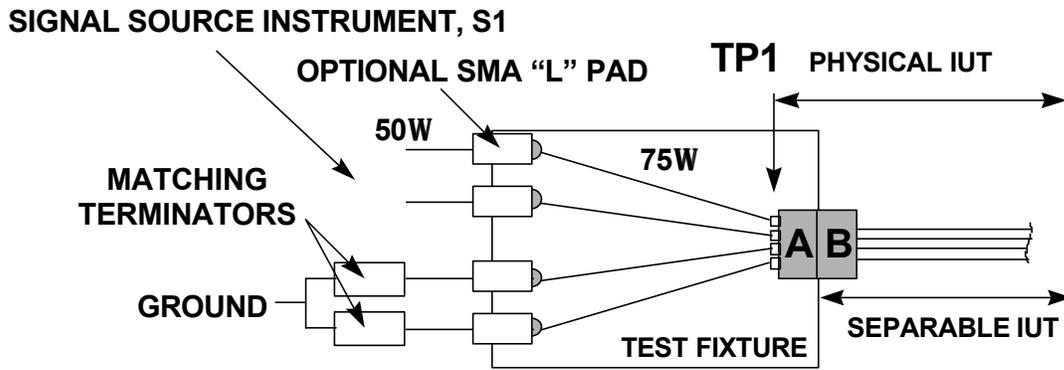


Figure 18 - Compensation for real transmitter jitter

The signal degradation test is intended to apply to all constructions of cable assembly including those with equalizers and those with known non uniformities such as intermediate connection points. It is basically a four port test requirement that does not specify the internal construction of the cable assembly.

### 6.2.1 Measurement test fixtures and measurement equipment

Figure 19 shows the source side measurement test fixture.

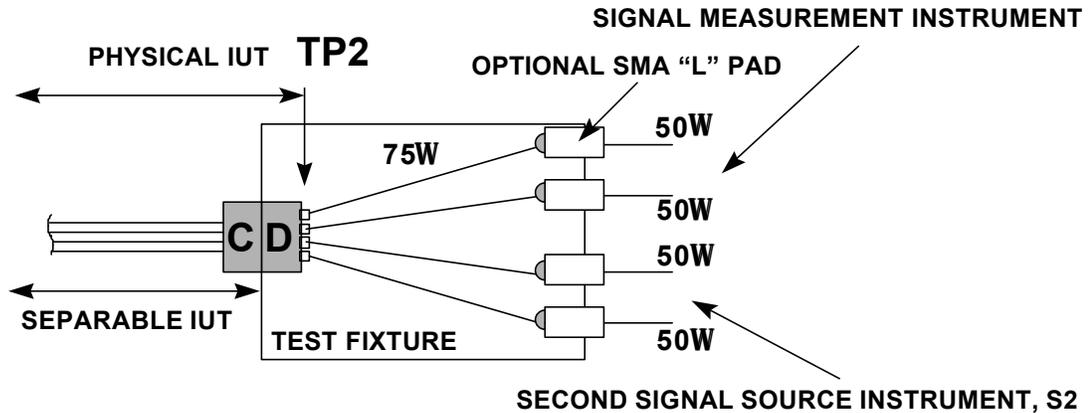


- A = PERMANENTLY MOUNTED CONNECTOR ON THE TEST FIXTURE
- B = PART OF THE SEPARABLE INTERCONNECT UNDER TEST
- ) = 75 SMA CONNECTOR

TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED TO REPORT VALUES AT TP1

Figure 19 - Source side measurement test fixture for signal degradation test

Figure 20 shows the receiver side test fixture.



- C = PERMANENTLY MOUNTED CONNECTOR ON THE TEST FIXTURE
- D = PART OF THE SEPARABLE INTERCONNECT UNDER TEST
- = 75 SMA CONNECTOR

TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED TO REPORT VALUES AT TP2

Figure 20 - Receiver side measurement test fixture for signal degradation tests

Measurement equipment consists of two signal sources, S1 and S2, and a sampling oscilloscope. The Tektronix Gigabert or equivalent is used for S1. This instrument delivers a differential signal containing any of several data

patterns. Both the + signal and the - signal are 50  $\Omega$  output impedance. High quality 50  $\Omega$  coaxial cables are used to attach all instruments to the test fixture.

A sampling oscilloscope such as the Tektronix 11801 or equivalent is used for the signal measurement instrument. S2 is a source that has the following properties:

- Differential outputs, 50  $\Omega$  each side
- No correlation to the signal driving the PUT (cannot be derived from the same timing source)
- Maximum amplitude allowed from a transmitter (2.0 volt p-p differential for full speed FC)
- Minimum allowed signal transition duration (100 ps for full speed FC)
- Maximum allowed unbalance (can be produced by using different path lengths for the + signal and the - signal between the signal source and the untested line, phase trimmers are another method for adjusting the imbalance)
- Signal is similar to a normal active data transmission: data is present with a run length of at least 5 max and 1 min, frequency within 1% of the nominal data rate. Lower Baud signals are not allowed for this signal due to balance dependence on frequency effects.

This signal can be generated by readily available sources (e.g. HP 8133) with some special purposefully unbalanced interconnect between the source and the PUT<sub>NOT</sub>.

One repeating data pattern that is acceptable is:  
11000001010011111010110000010101.

### 6.2.2 Calibration procedure

The highest signal level used is from S2 and that level will determine the scaling factor needed for signal measurement instruments that cannot accept real signals as large as the specified maximum for S2. For the case of full speed FC the amplitude of S2 is set to 2.0V differential pp. Since the maximum voltage level that can be applied to some common signal measurement instruments is around 800 mV pp one must scale the actual signals so that the input levels stay within the capabilities of the instruments.

It is further important to do the calibration in a way that has the fine adjustments done by instruments that are capable of fine tuning the amplitude of the signals. Some common S1 sources do not have adjustable output signal levels so the fine adjustment must come from the signal measurement instrument and the S2 source.

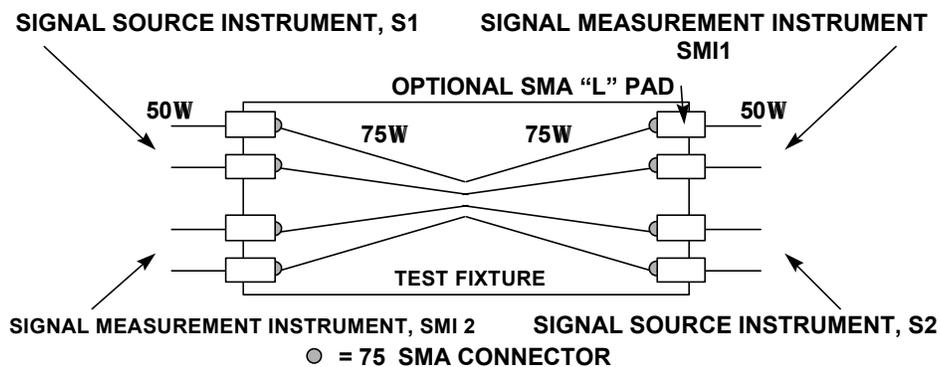
Because of the limited adjustability of S1 the calibration of S1 and the signal measurement instrument will therefore be done before the calibration of S2. However, since the same signal measurement instrument is used to calibrate both S1 and S2 the compliance range of the signal measurement instrument for S2 must be considered when calibrating S1. The same settings on the signal measurement instrument as determined in the calibration of S1 is used in the calibration of S2. This may force S1 to have a coarse adjustment in its output level to approximately half the amplitude it would normally use. For the case of full speed FC S1 needs to appear to be approximately 1.1 V differential pp. If the

signal measurement instrument can handle no more than 800 mV the actual S1 output must be reduced to approximately 400 mV differential pp. This coarse adjustment may be accomplished through the use of in-line attenuators (around 9dB).

This allows an S2 actual output of slightly less than 800 mV to appear as 2.0 V. When the signal measurement instrument is calibrated the 400 mV output appears as 1.1V and an 800 mV output appears as 2.2V. Note that the exact values of the S1 actual output are not critical - the fine tuning will take place in the software scale adjustments of the signal measurement instrument.

### 6.2.2.1 Calibration test fixture

A special calibration test fixture is required as shown in Figure 21. This test fixture is exactly the same on each side as the measurement test fixtures up to the mounting pads/holes for the connectors. No mounting pads/holes exist on the calibration test fixture. This fixture is intended to determine the effects of the actual measurement test fixtures.



**Figure 21 - Calibration test fixture**

It is possible to use the top traces for both S1 and S2 calibration if the fixture used for the tests is identical for both the PUT and the PUT<sub>NOT</sub>.

### 6.2.2.2 Calibration for S1 and signal measurement instrument

The following procedure assumes that the signal measurement instrument needs input signals less than 800 mV differential pp.

Using the calibration test fixture in Figure 21 with S2 disconnected:

1. Select in-line attenuators such that the differential pp output of S1 measured through the calibration test fixture is near but less than 400 mV differential pp at the time representing the closest approach to the top and bottom of the (vertically scaled) transmit mask
2. Select hardware filters and/or connecting cables attached to the output of S1 to produce the minimum STD values allowed for the application as indicated on the signal measurement instrument
3. With the filters / cables in place for the minimum STD value verify that the

STD is that expected

4. If STD is not that expected or the amplitude does not satisfy step 1, repeat steps 2 and 3 until the desired STD and amplitude is achieved
5. Adjust signal measurement instrument scale using the internal software of the instrument to report the minimum acceptable differential pp amplitude at the closest approach to the top and bottom of the (vertically scaled) transmit mask (See Figure 22)\*\* (e.g. 1.1V pp for full speed FC)
6. Measure jitter (see Figure 18) and record
7. Subtract the measured jitter in the actual transmit signal from the maximum specified jitter allowed for transmitters (see Figure 18)
8. Create a test mask for the received signal using the method shown in Figure 18
9. Record all the settings and hardware needed to create steps 5,6, and 7 as the calibration conditions for the minimum STD tests
10. Repeat steps 1 thru 9 with the maximum STD values allowed for the application

If the minimum allowed STD is not achievable (due to losses in L pads, test fixtures and cables) then use the lowest possible STD. NO allowance is made in the acceptable ranges due to inability to achieve minimum STD.

\*\* The transmitted signals measured may contain high frequency noise due to resonances and reflections within the test fixture (especially if the matching "L" pads are not used). Figure 22 shows a representation of a well behaved launched signal that contains HF noise. Other launch signals may show more separation between the rails and the transitions, as shown in Figure 23. Regardless of whether there is a separation or not in all cases all the "dots" shown above or below the horizontal parts of the transmit eye mask are considered in taking the averages.

In Figure 22 and Figure 23 the adjustment on the signals was done graphically for purposes of illustration by keeping the mask exactly the same size and scaling the signals in the vertical direction only. Unfortunately, since there is no practical way to separate the signal from the graticules, this scheme also scales the graticules along with the signals. The amplitudes of the adjusted signals should be related to the size of the graticules before the adjustment in upper part of the figures. The graticules in the lower parts of the figures should be ignored. The absolute scale in the figures is the same for everything except the lower graticules.

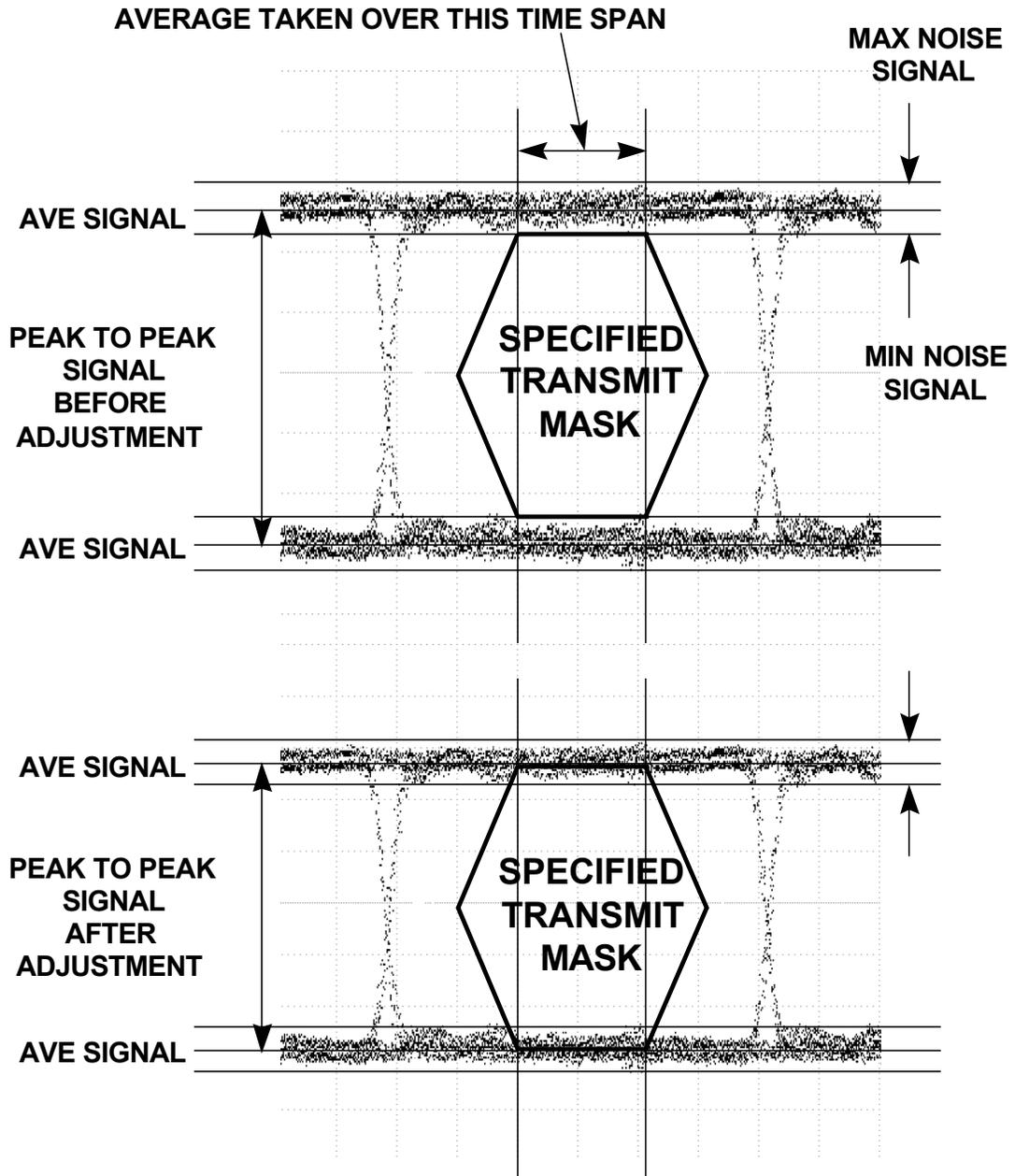


Figure 22 - Adjustment of launch amplitude (example 1)

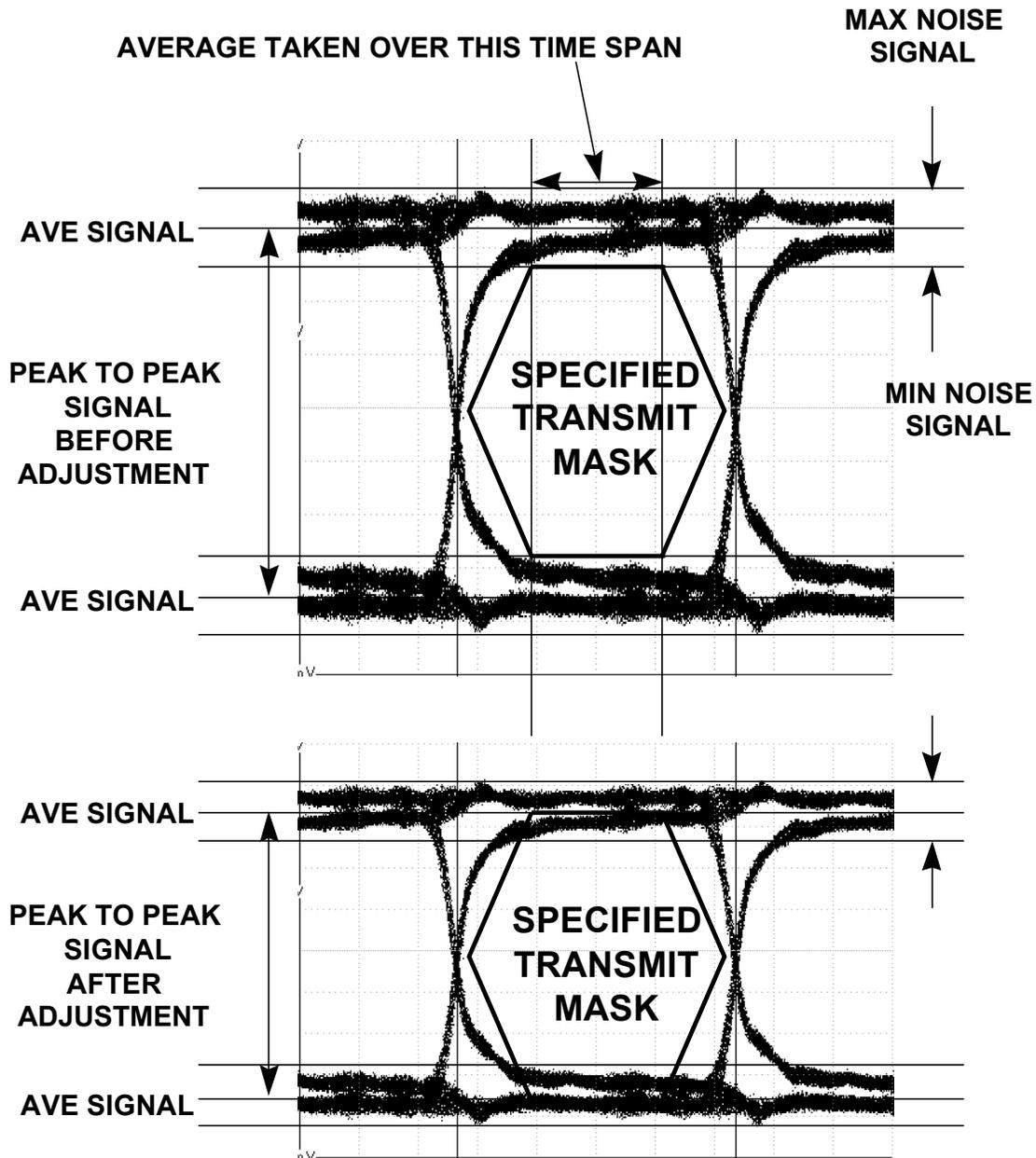


Figure 23 - Adjustment of launch amplitude (example 2)

It is in general not possible to determine from examination of the eye whether the amplitude broadening is caused by very high frequency noise or by signals more closely related to the basic data pattern. Since these very high frequency signals will not propagate very far into the interconnect and will not reach the receiver they are not really part of the launched signal for purposes of this test. However, the presence of the very high frequency noise can seriously affect the measurement of the launched signal amplitude and needs to be limited and accounted for.

There are two requirements relating to launched signals containing significant broadening of the eye pattern bands:

- the peak to peak launched signal amplitude shall be measured from the mean of the vertical population between the closest approach points at the top and bottom of the transmit mask (see upper part of Figure 22 and Figure 23)
- the test fixture and test environment shall be designed and built such that the peak to peak amplitude noise in the signal (see upper part of Figure 22 and Figure 23 max noise signal - min noise signal) between the closest approach points at the top and bottom of the transmit mask is no more than 20% of the peak to peak average.

The mean or average of the vertical population in the specified time band shall be calculated using the averaging function of the instrument.

Failing to follow these requirements may allow a bad test fixture and/or environment to launch higher amplitude signals than intended and effectively gives the IUT a larger signal degradation budget than intended. The received eye opening is larger without the adjustments for HF noise than it would be with a HF noise-free launched signal with the same amplitude.

Note that the amplitude of the signal for purposes of this test does NOT occur at the center of the eye unless that happens to coincide with the point of closest approach to the top and bottom of the transmit eye mask. This is particularly evident when there is some slope to the transitioning signals while over the flat part of the mask as shown in Figure 23. In these cases the amplitude is determined significantly from the signal not in the center of the mask.

For a signal of the type shown in Figure 22 note that the visible edge of the measured eye after adjustment penetrates into the transmit mask area by an amount equal to half the peak to peak local noise on the signal as shown in the lower part of Figure 22.

For a signal of the type shown in Figure 23 note that the visible edge of the measured eye after adjustment penetrates into the transmit mask area more at the left end of the flats of the mask and has greater penetration than for the signals shown in Figure 22.

The lower part of Figure 22 and Figure 23 illustrates the way a properly adjusted launch signal should appear.

The better the quality of the test fixture the more launched signal amplitude is available for the IUT. Said differently, poor quality test fixtures place more burden on the IUT to deliver the signals to the receiver.

#### **6.2.2.3 Calibration for S2**

The calibration procedure for S2 uses the same signal measurement instrument as for S1. This is required to maintain the same scale factors for all measurements. The data pattern described in section 6.2.1 shall be used on S2.

Using the calibration test fixture in Figure 21 with S1 disconnected and the signal measurement instrument used and calibrated in 6.2.2.2 attached to the output of PUT<sub>NOT</sub>:

1. Select hardware filters and/or connecting cables attached to the output of S2 to produce the minimum STD values allowed for the application as indicated on the signal measurement instrument
2. With the filters / cables in place for the minimum STD value verify that the STD is that expected
3. If STD is not that expected repeat steps 1 and 2 until the desired STD is achieved
4. Adjust the output of S2 such that the maximum allowed differential peak to peak amplitude is indicated (note the actual signal is less due to the calibration process) (this indicated amplitude is 2.0V for full speed FC) - the peak to peak amplitude for this adjustment is the maximum local average signal recorded anywhere in the eye (see Figure 22 for definition of amplitude)
5. Using the same settings and conditions produced in step 4, set the signal measurement instrument to add the + signal and the - signals
6. If needed, add lengths of cable or phase trimmers to either the + signal or - signal cable from S2 to the calibration test fixture until the signal measurement instrument indicates the maximum peak amplitude allowed for imbalance (see section 6.3 for definition of imbalance - 12.5% of differential peak to peak signal amplitude, i.e. 250 mV for a 2.0 V p-p launched signal is the maximum allowed launch imbalance in this document) if the launch imbalance exceeds the allowed levels without adding extra lengths of cable or phase trimmers then S2 must be adjusted so that it does not deliver more imbalance than allowed)
7. Record all the settings and hardware selections needed to satisfy steps 4 and 6

The S2 calibration does not need to be done for the maximum allowed STD or minimum allowed amplitude.

### 6.2.3 Testing procedure

Use S1 calibrated as described in 6.2.2.2 and running a data pattern with a run length of at least 5 max and 1 min such as 2\*\*7-1 or K28.5 with a bit rate within 1% of the nominal data rate. Use S2 calibrated and running a data pattern as described in 6.2.2.3. The bit rate for S2 shall be supplied from a timing source different from that used for S1.

The eye pattern on SMI1 is recorded as the result of the signal degradation test.

There are four specific measurements required for each PUT in the IUT. Table 3 shows the matrix.

**Table 3 - Test conditions for signal degradation**

Polarity of S2	normal (see Figure 2)	reversed (see Figure 2)
STD for S1		
minimum	Test 1	Test 2
maximum	Test 3	Test 4

Every measurement is executed the same way except with the conditions indicated

in Table 3 set according to the measurement being done. The separable IUT is connected between the test fixtures shown in Figure 19 and Figure 20 and the resulting eye diagram is recorded and compared to the modified receive signal mask.

Data acquisition should be continued long enough to ensure that all the noise from the  $PUT_{NOT}$  has a chance to experience the worst case interaction with the PUT signals. This time can be determined by running some test cases for extended times and backing off until good confidence is felt at the data acquisition times to be used for the tests.

Any intrusion into the mask constitutes a failure. The allowed receive mask is the same for all tests.

Notice that the trigger for SMI1 must come from the S1 trigger output and that the polarity reversals for S2 must be done between S2 and the IUT.

#### **6.2.4 Acceptable ranges**

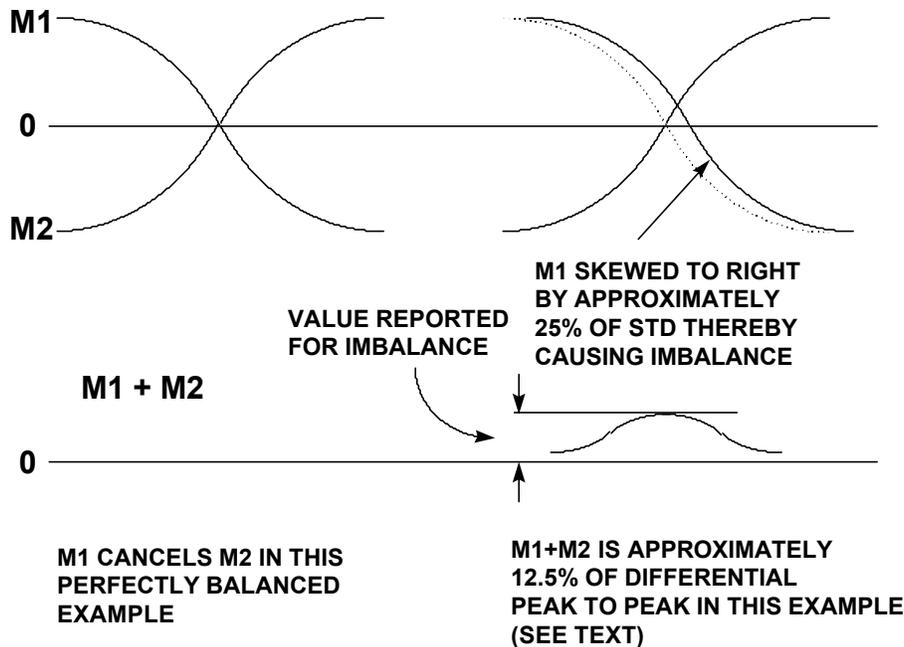
The acceptable ranges for full speed FC are shown in Annex A.

#### **6.3 Balance degradation**

The balance degradation test uses the same strategy to produce the worst case input signals as is used for the signal degradation test (section 6.2) except that the maximum input differential amplitude from both S1 and S2 is applied and there is no jitter component specified.

Balance is generally associated with the difference between the slopes of the + signal and the - signal at the same point in time along the line. However, when the STD is known, as in this test, one may use the peak instantaneous sum of the + signal, M1, and the - signal, M2, to approximately define the imbalance. The peak sum divided by the STD is the difference in the average slopes of the + signal and the - signal. This method avoids needing to use single ended differentiators and allows the use of the same signal measurement instrument that is used to make the signal degradation measurements. This not only simplifies the test but also reduces the cost of the equipment.

Figure 24 shows a simple example of two balanced single ended signals within a differential pair and imbalanced single ended signals caused by a time skew on the M1 line.



**Figure 24 - Example of imbalance measurement**

The imbalance is recorded as the peak value of M1 + M2 minus the average of all M1 + M2 data sampled and is reported in mV peak. The imbalance reported may be referred to the peak to peak launched differential signal amplitude regardless of the point in the PUT where the measurement is taken. For a 2.0 mV peak to peak launched differential signal a 12.5% imbalance is  $2000 \text{ mV} \times 0.125 = 250 \text{ mV}$ .

In Figure 24, if the peak value of M1 and M2 is 0.5V the peak differential voltage is 1.0V and the peak to peak differential voltage is 2.0 V. The peak sum of M1 +M2 (the imbalance) is shown as approximately half of the peak of M1 or M2 and is approximately 250 mV. Therefore, the imbalance shown in Figure 24 is approximately 12.5%.

Since the maximum imbalance is the only feature of interest only the minimum STD is used for both S1 and S2.

The possibility of an unbalanced transmitted signal compensating for an unbalanced (in the other direction) connector/cable was noted in section 4. Therefore it is important to make this test with all four permutations of S1 and S2 polarity connections.

The reported imbalance for the IUT is the imbalance measured at the receiver less that present in the transmit signal.

The balance degradation test is intended to apply to all constructions of cable assembly including those with equalizers and those with known non uniformities such as intermediate connection points. It is basically a four port test requirement that does not specify the internal construction of the cable assembly.

### 6.3.1 Test fixture and measurement equipment

The same test fixture and measurement equipment is used as for the signal degradation tests. See Figure 19 and Figure 20.

### 6.3.2 Calibration procedures

#### 6.3.2.1 Calibration for S1 and SMI1

The following procedure assumes that the signal measurement instrument needs input signals less than 800 mV differential pp.

Using the calibration test fixture in Figure 21 with S2 disconnected:

1. Select in-line attenuators such that the differential pp output of S1 measured through the calibration test fixture is near but less than 750 mV differential pp as defined in Figure 22.
2. Select hardware filters and/or connecting cables attached to the output of S1 to produce the minimum STD values allowed for the application as indicated on the SMI1
3. With the filters / cables in place for the minimum STD value verify that the STD is that expected on SMI1 (the procedures in section 7.4 shall be used to measure the STD)
4. If STD is not that expected or the amplitude does not satisfy step 1, repeat steps 2 and 3 until the desired STD and amplitude is achieved
5. Adjust signal measurement instrument scale using the internal software of the instrument to report the maximum acceptable differential pp amplitude anywhere in the display (e.g. 2.0V pp for full speed FC)
6. Under the conditions of step 5 set SMI1 to display the sum of the + signal and the - signal using a horizontal scale that displays at least 30 bit times. Record the display pattern
7. Determine the average level of the displayed pattern (this average should be close to zero)
8. Measure the peak deviation from the average level (see Figure 26) and record - this is the launched imbalance in the S1 signal
9. Record all the settings and hardware needed to create the conditions in step 5 for future use

If the minimum allowed STD is not achievable (due to losses in L pads, test fixtures and cables) then use the lowest possible STD. NO allowance is made in the acceptable ranges due to inability to achieve minimum STD.

An example of the launched imbalance is shown in Figure 25. This example does not use the correct horizontal scale for this bit rate. Note that high frequency noise is blurring the signal.

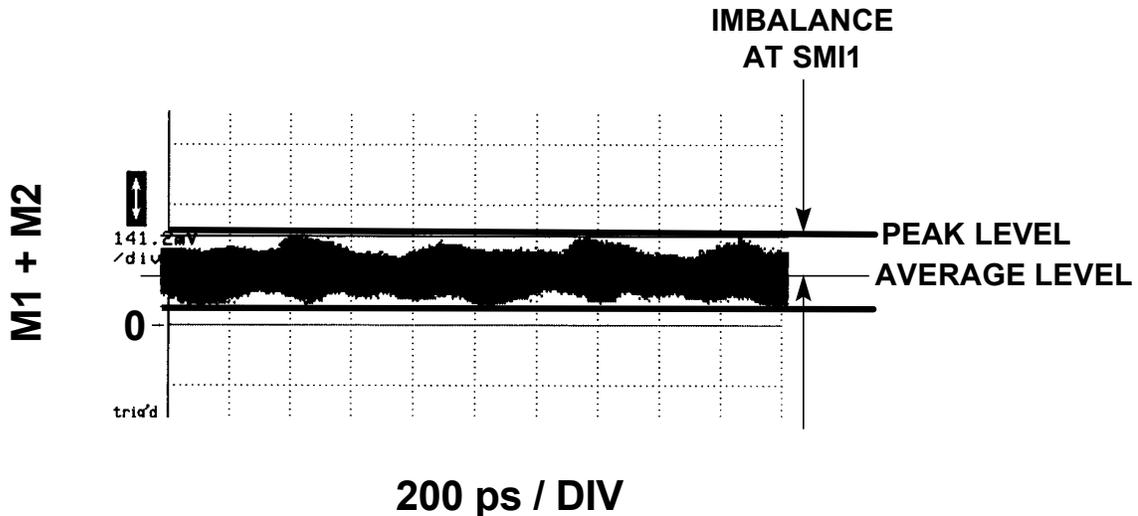


Figure 25 - Launched signal imbalance example

#### 6.3.2.2 Calibration for S2

The calibration procedure for S2 uses the same signal measurement instrument as for S1. This is required to maintain the same scale factors for all measurements. The data pattern described in section 6.2.1 shall be used on S2.

Using the calibration test fixture in Figure 21 with S1 disconnected and using the same signal measurement instrument as was used and calibrated in 6.2.2.2 attached to the output of PUT<sub>NOT</sub> as SMI2:

1. Select hardware filters and/or connecting cables attached to the output of S2 to produce the minimum STD values allowed for the application as indicated on the signal measurement instrument
2. With the filters / cables in place for the minimum STD value verify that the STD measured on SMI2 is that expected using the steps described in section 7.4
3. If STD is not that expected repeat steps 1 and 2 until the desired STD is achieved
4. Adjust the output of S2 such that the maximum allowed differential peak to peak amplitude is indicated on SMI2 (note the actual signal is less due to the calibration process) (this indicated amplitude is 2.0V for full speed FC)
5. Using the same settings and conditions produced in step 4, set SMI2 add the + signal and the - signals
6. If needed, add lengths of cable or phase trimmers to either the + signal or - signal cable from S2 to the calibration test fixture until SMI2 indicates the maximum peak amplitude allowed for imbalance (this maximum is 12.5% of peak to peak differential launched voltage for this document) -- if the measured imbalance exceeds 12.5% of peak to peak differential launched amplitude without adding extra lengths of cable then S2 must be adjusted so that it does not deliver more than 12.5% imbalance)
7. Record all the settings and hardware selections needed to satisfy steps 4 and 6

The S2 calibration does not need to be done for the maximum allowed STD or minimum allowed amplitude.

### 6.3.3 Testing procedure

Use S1 calibrated as described in 6.3.2.1 and running a data pattern with a run length of at least 5 max and 1 min such as 2\*\*7-1 or K28.5 with a bit rate within 1% of the nominal data rate. Use S2 calibrated and running a data pattern as described in 6.3.2.2. The bit rate for S2 shall be supplied from a timing source different from that used for S1.

Using a horizontal scale such that at least 30 bit times are displayed the pattern displayed on SMI1 is recorded as the result of the balance degradation test.

There are four specific tests required for every PUT. Table 4 shows the matrix.

**Table 4 - Test conditions for balance degradation**

Polarity of S2	normal (see Figure 2)	reversed (see Figure 2)
Polarity of S1		
normal (see Figure 2)	Test 1	Test 2
reversed (see Figure 2)	Test 3	Test 4

Every test is executed the same way except with the conditions indicated in Table 4 set according to the test being done. The separable IUT is connected between the test fixtures shown in Figure 19 and Figure 20 and the resulting signal pattern from the sum of the + signal and the - signal is recorded. The average value of the pattern is the reference level and will account for any D.C. content. D.C. content shifts the entire pattern up or down. The imbalance is intrinsically an A.C. effect and shall be calculated as the difference from the average level of the measured signal. For signals with no D.C. content this average level is zero. Figure 26 shows an example of an imbalance output test where no d.c. content exists and the average level is therefore zero. The horizontal scale does not meet the 30 bit time requirement but is expanded to show some detail.

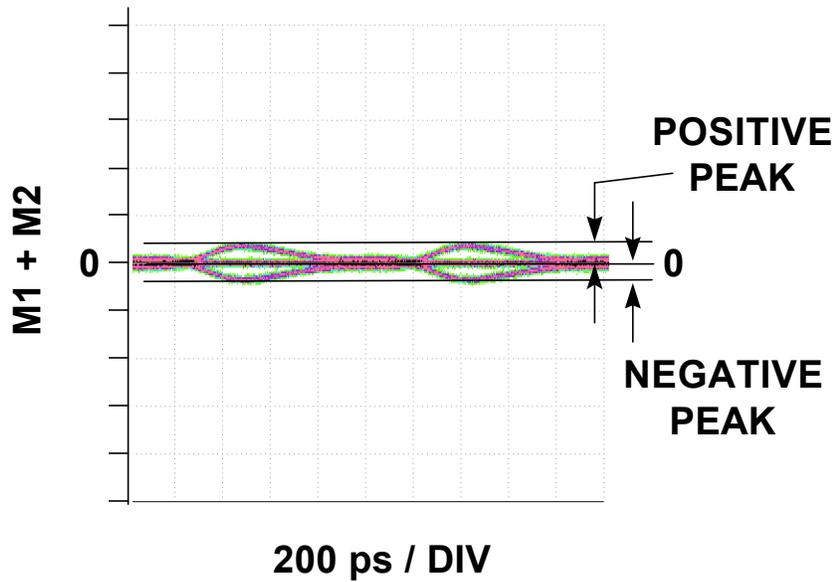


Figure 26 - Example of an imbalance output measurement

If SMI1 is not balanced, that is if the same signal applied to both M1 and M2 does not yield exactly the same value on both M1 and M2, then the balance measurement will be shifted in the same way as if there were common mode D. C. content in the signals.

An example of a received imbalance display with D. C. content (or unbalanced channels on SMI1) and many bit times is shown in Figure 27.

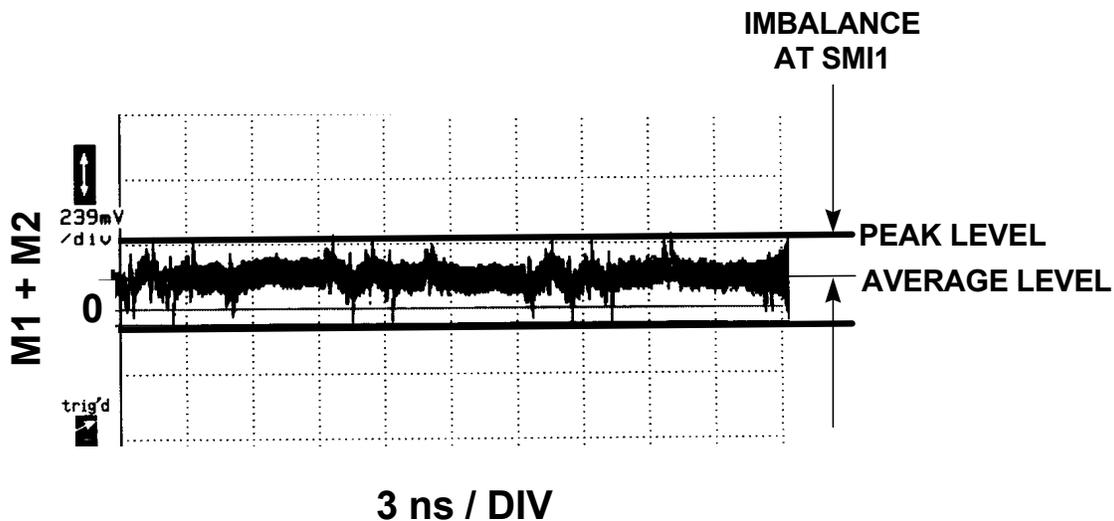


Figure 27 - Imbalance output with d. c. content

This the output through the IUT using the source shown in Figure 25 but with time and amplitude scales significantly different from that used for Figure 25.

Note that the imbalance display in Figure 27 has quasi-periodic features that probably indicate the difference between the S1 timing source and the S2 timing source.

The maximum difference from the average level noted from any of the four tests is the imbalance in the received signal. In Figure 26 the imbalance is the positive peak less the average level (zero). Since the negative peak is the same magnitude as the positive peak the same imbalance result is obtained using the negative peak.

To obtain the imbalance added by the IUT subtract the value of the launched imbalance determined during the S1 calibration described in section 6.3.2.1.

IMBALANCE CREATED BY IUT, mV = (RECEIVED IMBALANCE, mV) - (LAUNCHED IMBALANCE, mV)

The recorded imbalance shall be given in percentage of the peak to peak launched differential signal.

RECORDED IMBALANCE FOR IUT = 
$$\frac{\text{IMBALANCE CREATED BY IUT, mV}}{\text{LAUNCHED P-P DIFFERENTIAL SIGNAL, mV}}$$

Notice that the trigger for SMI1 must come from the S1 trigger output and that the polarity reversals must be done between S1 and the IUT and S2 and the IUT.

#### 6.3.4 Acceptable ranges

For this document the maximum allowed launch imbalance (peak) is 12.5% of the differential peak to peak launched signal and the maximum added imbalance (peak) by the IUT is 12.5% of the differential peak to peak launched signal for a total of 25% of differential peak to peak launched signal in the received signal. These values are based partly on the skew specifications in the FC standard for launched signals and partly on the measured performance of known good cable assemblies.

#### 6.4 Electromagnetic compatibility (EMC)

EMC is a measure of the intensity of electromagnetic energy exported from the IUT. Although these tests can be applied to any IUT they are generally applicable only to shielded external types.

Two options are specified for determining the electromagnetic compatibility of HSS cable assemblies: (1) common mode power transfer (CMPT) and (2) electromagnetic radiation (EMR). Either or both may be used.

The launched signals are nominally balanced for the EMR test and are nominally unbalanced in the CMPT test. The EMR test approximates the normal use condition better than the CMPT test but the cost of the test environment is vastly larger than for the CMPT test. A typical EMR test chamber may cost up to several million dollars. The cost of the CMPT test environment is typically thousands of dollars, mostly for the measurement equipment.

Data acquisition times for EMR tests are much longer than the CMPT tests

Both options have the ability to reliably specify and measure EMC performance requirements on HSS cable assemblies and associated bulkhead attachments.

The EMC tests are intended to apply to all constructions of cable assembly including those with equalizers and those with known non uniformities such as intermediate connection points.

#### **6.4.1 Common mode power transfer (CMPT)**

Common mode power transfer (previously known as transfer impedance or shield effectiveness) applies to external shielded cables and the associated attachments to enclosures. When cables are attached to a system, they can add to the overall radiated emissions of the system. This additional radiation, is due in part, to the amount of energy transferred to the outside of the cable shield from inside the EMI enclosure. How much energy a particular cable and connection system will allow to escape the enclosure can be determined by measuring the "CMPT" of the system.

Common mode power transfer is the power transfer from signals inside a shielded interconnect to the shield outside of the interconnect. Within the context of a specific test condition, one may assume linearity between the intensity of the signal inside the shield to that transferred to the outside.

The CMPT test produces direct stress on the shielding system by using unbalanced driven signals. By contrast the EMR test (section 6.4.2) uses a nominally balanced driven signal scheme that does not produce this additional stress on the shielding system. Another difference is the CMPT captures energy placed on the shield by the connector system and by leakage through the shield between the connector and the current clamp. The EMR test measures the radiation pattern from the entire shield and both connectors. Depending on the details of the construction of the IUT and the source of leakage one may not always get close agreement between the CMPT and EMR tests for these reasons.

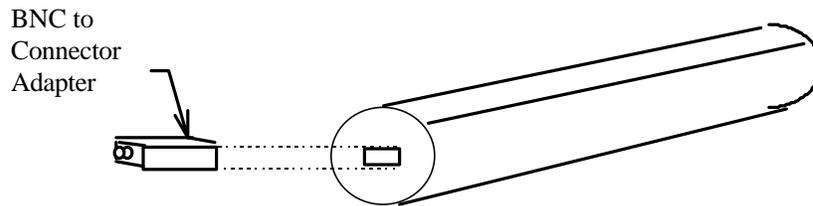
##### **6.4.1.1 Test fixture and measurement equipment.**

Test equipment needed:

Spectrum Analyzer	HP 8595E or equivalent
Signal Generator	HP 8657B or equivalent
Signal Amplifier	HP 8447D or equivalent
Absorbing / Current Clamp	Rhode and Schwarz MDS-21
Test Bed and Adapters	

The units under test fall generally into two categories: (1) cable assemblies and (2) bulkhead to cable assembly connectorization.

The test bed for both categories, consists of a 6" inch diameter flue pipe, whose seam has been separated to make a 7" diameter slotted flue pipe. Seven inch end caps are used at either end. The slot opening in the side of the pipe is used for inserting and removing cable assemblies under test. This slot opening could have a hinged cover if there is excessive RF noise in the test environment.

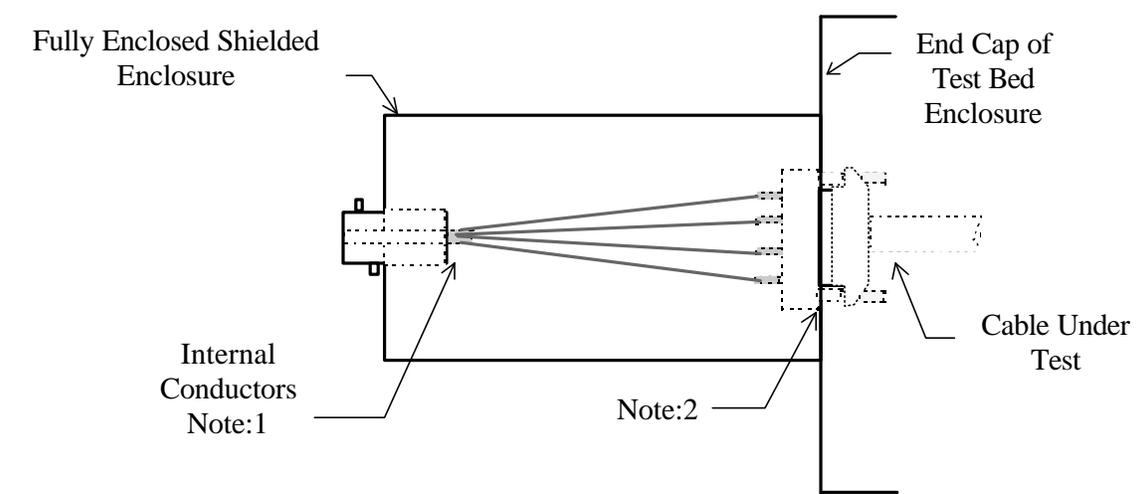


**Figure 28 - General view of IUT adapter (test fixture) and "stovepipe"**

The test bed needs a adapter to bring the signal from the signal generator to the IUT. The construction of this adapter is different for each of the following two testing categories.

The first test category, used for testing only individual cable assemblies, the bulkhead connection on the adapter is a solid connection through 360 degrees between the face of the connector and the bulkhead.

For the second category, used for testing the complete bulkhead connection with the cable assembly mated as it exists in service, the bulkhead connector is attached in the adapter just as it would be in normal service. For example a PCI bracket may be used on the adapter to simulate a PC option card connection.

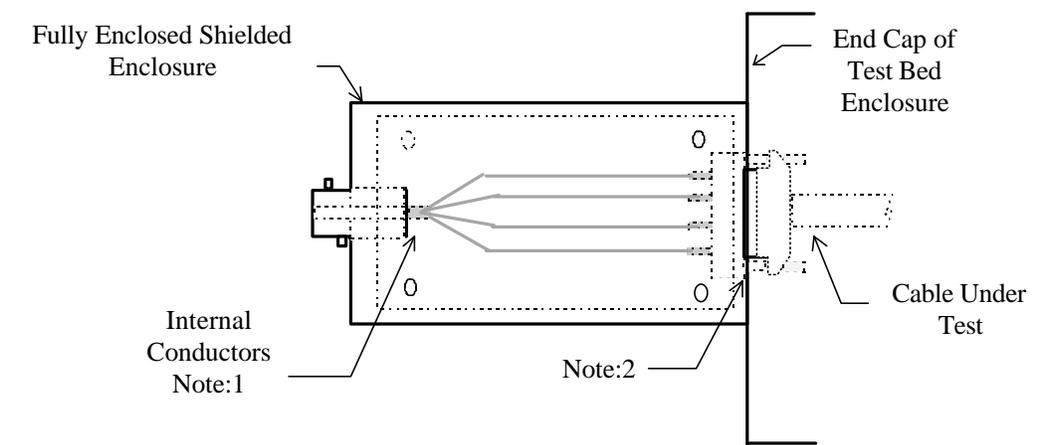


**Figure 29 - Test fixture for individual cable assemblies**

Notes:

1. All internal connector contacts bused together and attached to center pin of BNC connector.
2. For the first testing category a 360 degree connection between the connector housing and the end cap of the pipe is required. Use gasketing or soldering to insure there are no openings from the adapter enclosure to the testing area.
3. The connector shown is capable of being hard mounted on the bulkhead and can accept wire termination on the test fixture side
4. For connectors that get their mechanical support from being mounted on a PCB the test fixture will use a PCB instead of wires as shown in Figure 30 - only the PCB feature shown in Figure 30 applies to this test fixture
5. The distance from the BNC connector to the bulkhead should be kept as short as possible

In the case of the HSSDC connector system, for example, a PCB may have to be used in the adapter box because not all of the HSSDC bulkhead connector variations use hardware to hold the connector to the bulkhead. Some connector variants rely on a pressure fit or some kind of spring contact.



· **Figure 30 - Test fixture for complete bulkhead interface testing**

Notes:

1. All internal connector contacts bused together and attached to center pin of BNC connector.
2. The bulkhead interface is created in the fixture in the same way as it would be in normal service
3. The connector shown requires mounting on a PCB for mechanical support
4. The distance from the BNC connector to the bulkhead should be kept as short as possible

The IUT is terminated on the far end with the circuit shown in Figure 31,

Figure 32 and Figure 33.

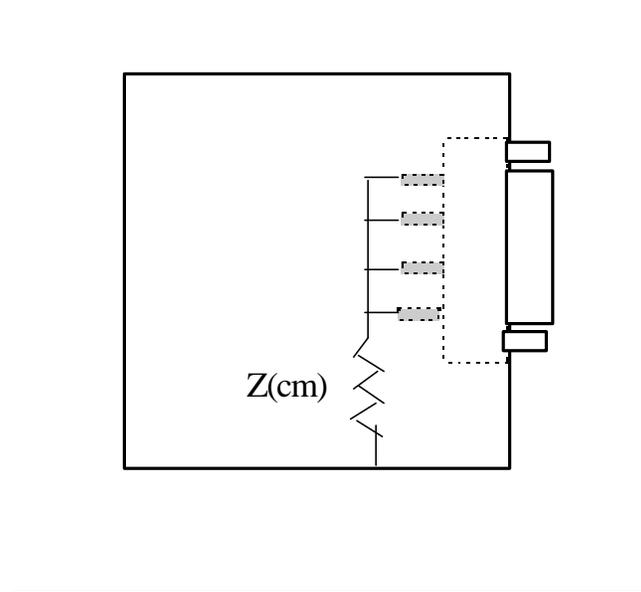
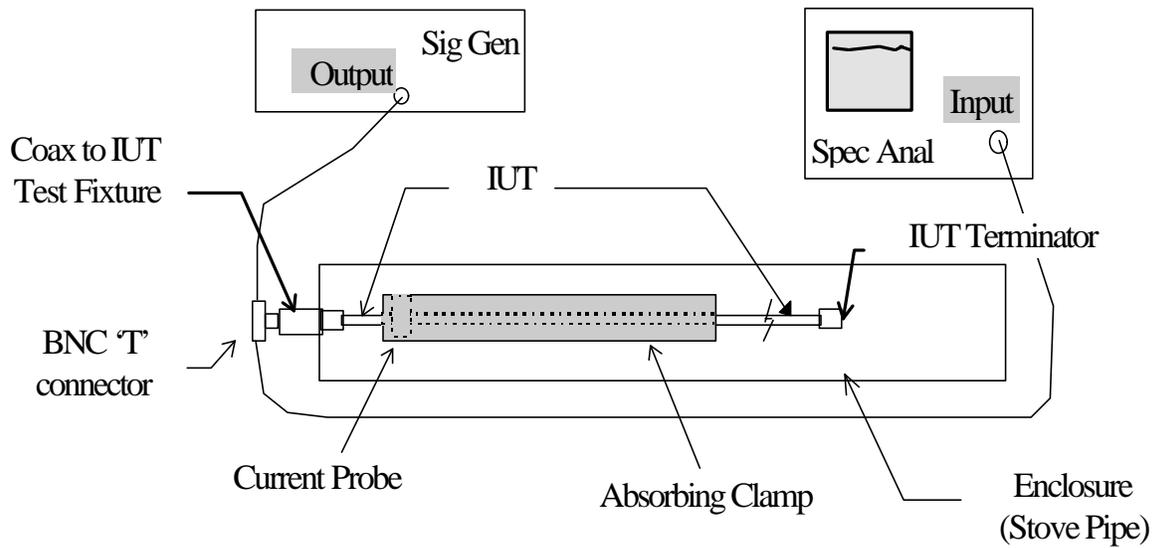


Figure 31 - IUT terminator

#### 6.4.1.2 Calibration procedure

Using a TDR, measure and record the single ended characteristic impedance of the cable assembly to be tested. This single ended characteristic impedance is measured with the four internal conductors shorted together and the shield of the cable connected to ground. This is easily accomplished using either test fixture in Figure 29 or Figure 30. This is the  $Z_{cm}$  shown in Figure 31 for the IUT terminator.

The internal common-mode current is established by inserting the IUT in to the stove pipe (measurement fixture) and absorbing / current clamp as shown in Figure 32, connecting the RF output of the signal generator and the input of the spectrum analyzer to the 'T' connection of the test fixture for the IUT. The center of the current clamp, in the MDS-21, is placed 10 cm away from the end of the test bed enclosure. The far end of the IUT is terminated in its characteristic impedance,  $Z_{cm}$ , with the IUT terminator.



**Figure 32 - Calibration configuration**

Set the signal generator's RF output to 0 dBm and sweep from 100 MHz to 1 GHz. Record this output with the spectrum analyzer in dBm as  $P_{in}$  to be used in the final CMPT calculation.  $P_{in}$  should be between 0 and -10 dBm.

#### 6.4.1.3 Testing procedure

$P_{out}$ , the power generated on the outside of the cable as a result of the common mode power transfer function is measured and recorded. The common mode power transfer, CMPT, is derived from  $P_{in}$  and  $P_{out}$ .

$$CMPT = P_{out} - P_{in}$$

$P_{out}$  is measured using the setup as shown in Figure 33. The only differences in the two setups is that the input of the spectrum analyzer is connected to the output of the amplifier, the current clamp is connected to the input of the amplifier and the spectrum analyzer 'T' connection is replaced with a 50 Ohm terminator. Leave the signal generator set to 0 dBm and sweep from 100 MHz through 1 GHz. The spectrum analyzer records the external power,  $P_{out}$ .

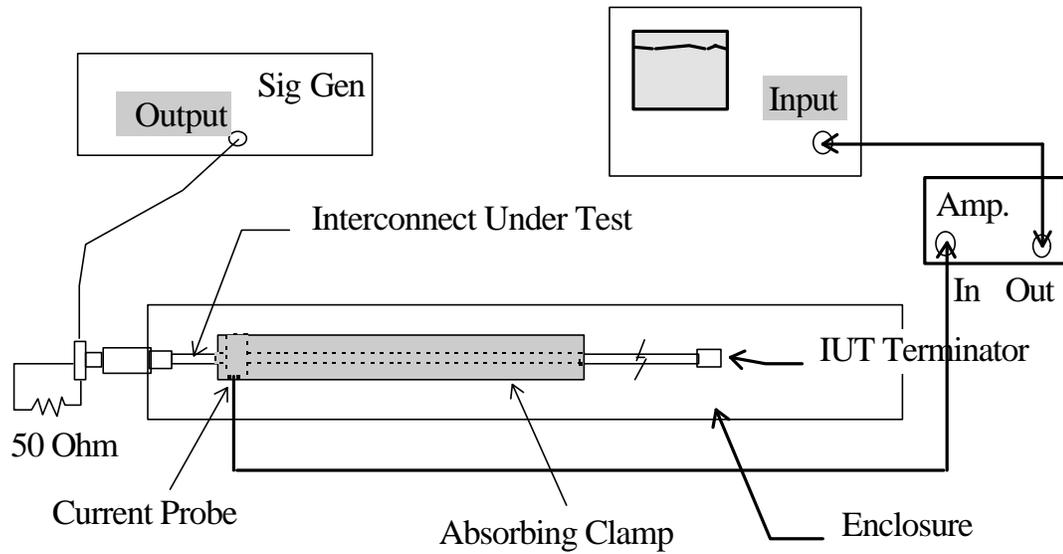


Figure 33 - Measurement configuration

A sample spectrum analyzer display is shown in Figure 34 and the calculated CMPT is shown in Figure 35.

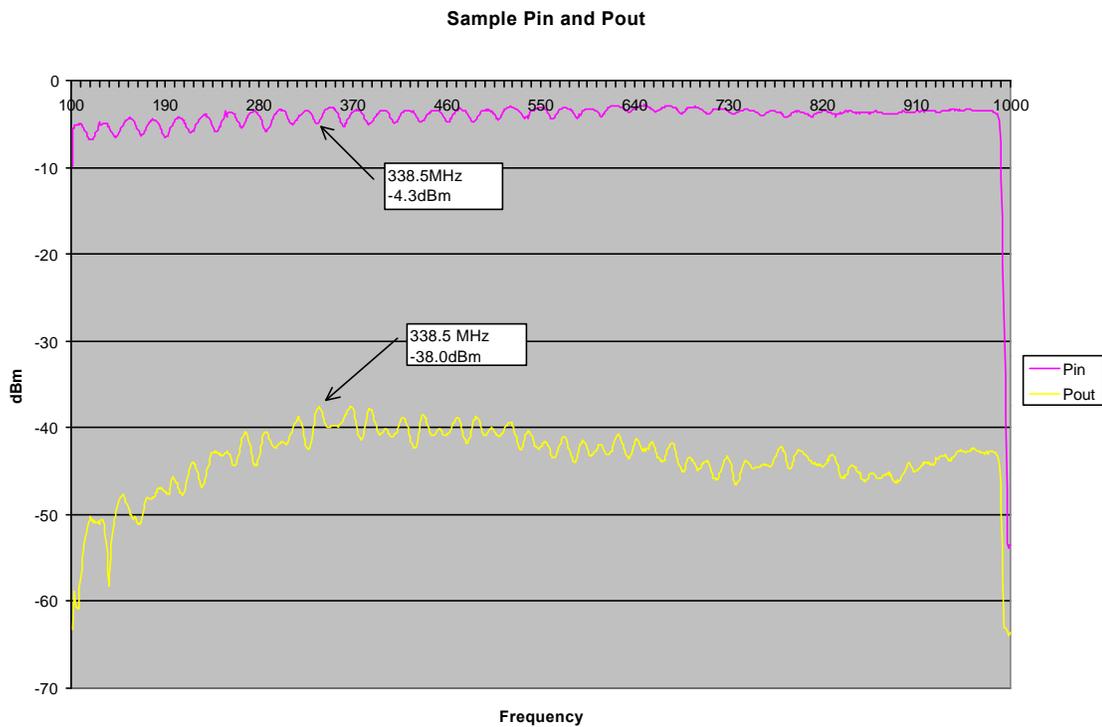
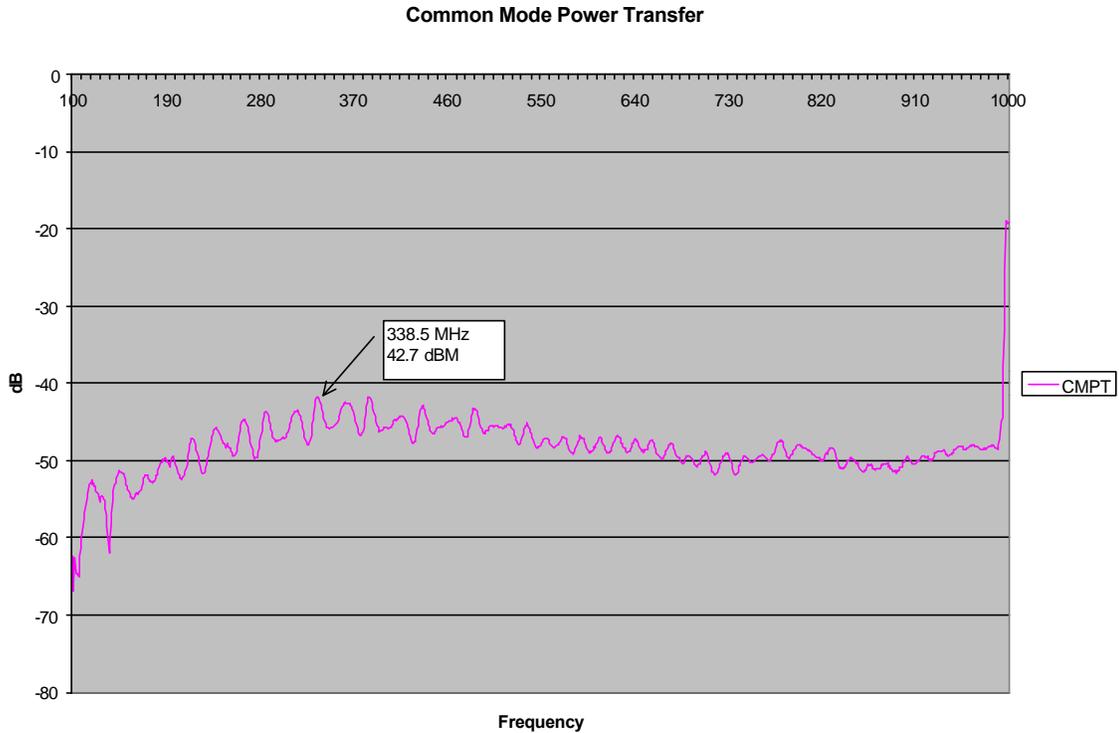


Figure 34 - Pin and Pout example



**Figure 35 - CMPT calculated using Pin and Pout in Figure 34**

At each frequency the common mode power transfer is calculated from the following equation:

$$\text{CMPT} = (\text{Pout} - \text{Amplifier gain} + \text{Insertion Loss}) - \text{Pin}$$

For example, in Figure 34 at 338.5 MHz Pout is -38.0 dB and Pin is -4.3 dB:

$$\text{CMPT} = (-38.0\text{dBm} - 26\text{dB} + 17\text{dB}) - (-4.3\text{dBm}) = -42.7\text{dB}$$

where Pin is the input signal that was established on the calibration procedure. Pout is the value displayed on the spectrum analyzer measured with the current probe. Insertion loss is provided by the clamp manufacturer and may be different at each frequency. Amplifier gain is from the inline amplifier, if used, and also may vary with frequency.

#### 6.4.1.4 Acceptable Ranges

The intent of the test affects the acceptable range. If the bulkhead attachment is not well sealed and is part of the test then the range specified below does not apply. If the intent is to measure the cable assembly and its mating connector then across the frequency range of 100 MHz to 1 GHz a recommended acceptable CMPT is less than -40 dB.

The CMPT requirement is unique to this document at the moment.

### **6.4.2 Electromagnetic radiation (EMR)**

Electromagnetic radiation testing is executed by using an antenna and the IUT together in a large chamber (known as a reverberation chamber) with metallic walls and a means to modify the fields in the chamber (mode stirring). The IUT in this test consists of the complete duplex cable assembly and the associated bulkhead attachments. Each end of the IUT is connected to connectors mounted on and penetrating through the walls of the chamber. Differential transmitters for both halves of the IUT are attached outside the chamber and apply maximum amplitude signals with minimum STD and maximum allowed imbalance to the IUT.

The EMR of the IUT is the difference between the radiation measured with the IUT and excitation in place and an identical test from a reference sample. An unshielded reference cable is required. The reference cable should have the outer shield stripped off and it should be of the same length as the cable under test within 5mm.

The significant difference between this specification and Method 3008 of MIL-STD-1344 is that in this technique the cable assembly is driven and the energy emitted from the sample is measured. Method 3008 drives the reverberation chamber and measure the energy received in the sample. By driving the cable assembly, differential signal excitation methods can be used which is representative of the intended application of the cable assembly.

Under these conditions and using a mode stirrer in the chamber the antenna detects all the radiation emanating from the IUT.

Notice that the signals applied in this test are much less likely to cause EMI than the CMPT tests because a nominally balanced signal is used in this test. In the CMPT test the conductors are all connected together to produce the worst possible (least balanced) case for producing EMI.

Evidence exists that shows that the EMR and CMPT tests both produce equivalent results for measuring balanced duplex copper interconnect.

#### **Related Documents:**

MIL-STD-1344, Method 3008 Shielding Effectiveness of Multicontact Connectors.

IEC 96-1 Reverberation Chamber method for measuring the screening effectiveness of passive microwave components.

#### **6.4.2.1 Test fixture and measurement equipment**

##### **6.4.2.1.1 Measurement equipment**

The following equipment is required to execute this test:

Reverberation chamber - a shielded enclosure fitted with a mode stirrer. The mode stirrer is a rotating vane generally under computer control. A shielded

enclosure of 20' x 10' x 12' can be used down to 200 MHz, possibly as low as 50 MHz.

Signal Generator - the signal generator should have roughly 0 to 10 dBm output power capability and controllable via an external interface bus. Bandwidth should be 50 MHz or less to at least 1 GHz.

Power Amplifier - measuring very well shielded cable assemblies may require a 1-watt power amplifier with a bandwidth of 50 MHz or less to at least 1 GHz.

Differential Coupler - required for differential excitation of the cable assembly and should have a bandwidth of 50 MHz or less to at least 1 GHz.

Log periodic antenna - a sense antenna to measure the field from the cable assembly with a typical bandwidth of 200 MHz to at least 1 GHz

Biconnical antenna - a sense antenna to measure the field from the cable assembly with a typical bandwidth of 50 MHz or less to at least 200 MHz

Pre-amplifier - broad band low noise pre-amplifier is useful in measuring well shielded cable assemblies. Typical specifications are a gain of 40 dB and a bandwidth of 50 MHz or less to at least 1 GHz.

Spectrum analyzer - the analyzer should be instrument bus configurable and have a bandwidth of 50 MHz or less to at least 1 GHz.

PC controller - A PC with a stable operating system and software for instrument control is ideal. The PC will need to also perform motor control for the rotating vane.

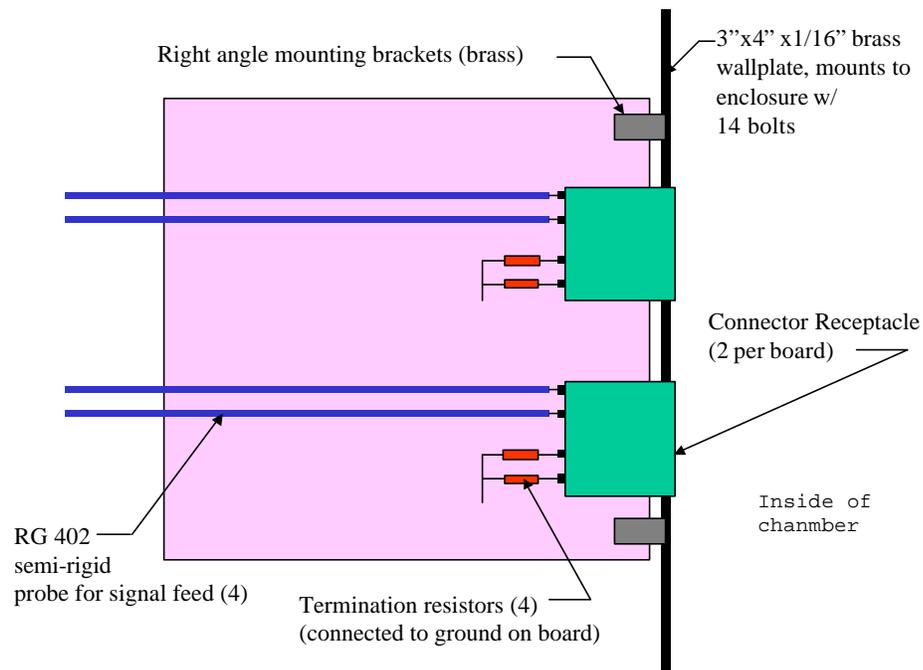
Data pattern generator - a data pattern generator is useful to evaluate cable assemblies using the exact data sequence the cable assemblies are expected to transport. The generator should support data rates of 200 MB/s to at least 1.4 GB/s.

See Figure 37 for examples of specific test equipment.

#### 6.4.2.1.2 Test fixture

Test fixture preparation can be involved, as it requires machining a brass plate with a pre-defined cutout for the connector receptacle. The connector receptacle to panel interface can be a significant leakage mechanism so installing the connector receptacle correctly is required for credible results.

Figure 36 shows a diagram of a typical fixture. The 3"x4" brass plate has 2 machined openings for the connector receptacle to penetrate through. The receptacles are mounted to a PCB substrate using the receptacle board mount features. The center conductor of RG402 semi rigid cabling is connected to the appropriate pins of the receptacle. The outer shield is soldered to the surface ground plane PCB material for referencing and mechanical stability. Termination resistors are soldered to the appropriate pins of the receptacle. Right angle brackets mount the PCB to the wallplate. Care must be taken to ensure that the electrical length of the semi-rigid feed is identical so that source induced skew is minimized in the differential excitation.



· Figure 36 - Diagram showing typical receptacle fixturing

### 6.4.2.2 Calibration and verification procedure

The calibration process uses the same test setup and equipment as during the test of the IUT but with different excitation and samples attached.

#### 6.4.2.2.1 Test setup

The test setup is shown in Figure 37. The connector receptacle fixturing is mounted to a bulkhead panel cutout in the MSC. The signal generator should be attached to the hybrid coupler with at least double braid coax (RG223 or equivalent). The electrical path length for differential excitation from the hybrid coupler to the receptacle needs to be well matched and consistent from test to test. It is recommended that semi-rigid coax be used for these connections.

The coaxial feed from the receive antenna to the pre-amp should use a well shielded cable. Ethernet thicknet trunk cable (double braid, double foil) has been used successfully. The main concern is that fields from the signal excitation path will couple to the input of the pre-amplifier.

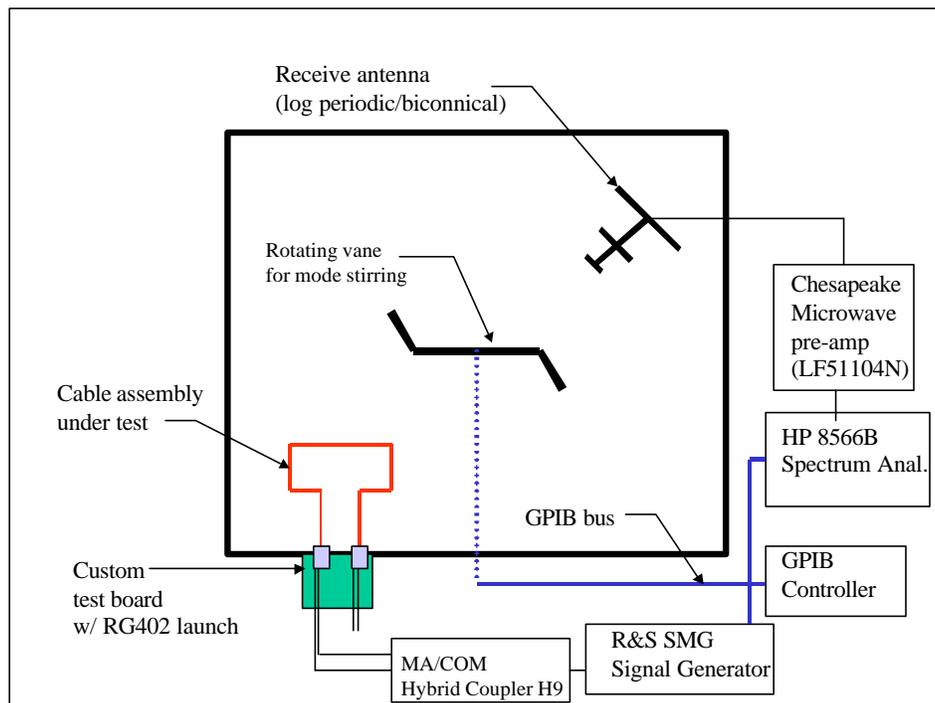


Figure 37 - Typical test setup

#### 6.4.2.2.2 Calibration procedure

It is recommended that prior to any testing of IUT samples that several ambient measurements be performed to verify that the received signal are indeed due to radiation from the cable assembly. Tests with no IUT installed and tests with the IUT installed but not excited are useful checks.

The placement and routing of the IUT is not critical but should extend into the MSC at least 3 feet. If the cable is very close to the wall of the MSC, fields from the cable assembly tend not to couple to the interior volume of the MSC.

Put the unshielded reference cable in place of the IUT in Figure 41.

For each test the following procedure is used to create a reference scan that effectively calibrates the test setup:

In all cases the signals are pure differential sinusoids with maximum allowed imbalance (25% of differential peak) and maximum allowed amplitude (2.0 v pp for FC).

The signal generator is set to an initial frequency (50 MHz) and radiated emission level is recorded. The signal generator is then incremented to the next frequency and the radiated emission level is again recorded. These emission levels are recorded in logarithmic space (dBm). This process is continued until the entire frequency range of 50 MHz to at least 1 GHz is covered. Linear frequency sweeps or logarithmic frequency sweeps are commonly used.

The rotating vane of the MSC is then moved 18 degrees and the process of recording the radiated emission level at each frequency is repeated. An 18 degree increment equates to 20 positions where radiated emission levels are recorded for all frequencies. More rotating vane positions could be used at the expense of longer test duration.

A 2-dimensional matrix of radiated emission measurements is created. For each frequency, the radiated emission level must be averaged over the 20+ rotating vane positions. This is accomplished by converting the levels from logarithmic space (dBm) to linear space (mW), summing the 20 values for each position and dividing the sum by the number of vane rotations (20+). This single value is then converted back to logarithmic space. This process is repeated for each frequency.

#### **6.4.2.3 Testing procedure**

Attach the IUT to the test fixture using the same physical routing as used for the reference cable.

Take a test spectrum scan as described in section 6.4.2.2

The shielding effectiveness is computed as the difference between the reference and the IUT at every frequency.

The reference cable should be excited in the same manner as the IUT i.e. with the same signal intensity and launched imbalance at every frequency.

Documentation: The final documentation should include the test results, description of cable assembly tested, source power level setting and source induced skew (if any).

#### 6.4.2.4 Acceptable levels

No acceptable levels have yet been identified for this test.

### 6.5 Near end cross talk (quiescent noise)

This test is limited to a single option: the single applied pulse method. In this method pulses with maximum differential amplitude, maximum allowed imbalance, maximum and minimum STD signal are applied to the IUT on one pair and the signal induced on the neighboring pair is measured. In this test both pairs are under test. The pair with the applied pulse is the aggressor pair and the pair with the induced noise is the victim pair. There are no signals coming into the victim pair from the remote transmitter for this test.

Single pulse tests eliminate the effects of resonance, are very deterministic in the causes of the induced noise (due to the mapping of the time and space as in the TDR tests), and produce the worst case results. It is necessary to reverse the polarity of the aggressor signal to ensure that balance compensation is not occurring.

The aggressor pulses are of the same type used for the impedance profile test: start with single ended signals: + signal at +/- 250 mV and the - signal at +/- 250 mV. The + signal and - signal pulses initiate in opposite directions to form a collapsing differential aggressor pulse ending at differential zero.

The use of actual worst case data patterns on the aggressor lines has been extensively debated and considered. This is the natural excitation that is initially considered. Extensive testing has shown that resonance conditions and effects of test fixtures can severely distort the measured results when using real data patterns. Sometimes these effects improve the cross talk performance and other times they exacerbate it. It is very difficult to diagnose the intensity and cause of resonance and fixture effects when using a real data pattern. The single pulse (with maximum allowed imbalance in the signals) eliminates these effects and gives a worst case result that can be attributed to as much of the system as desired. For example, if connector termination techniques are causing the cross talk then that can be revealed by examining the time points associated with the termination points.

Another important point is the value of the recorded disturbance in the victim line. Should the peak, peak to peak or some other feature of the induced noise be used? This document requires that the differential peak value of the induced noise at a time position within the IUT electrical neighborhood be used.

This requirement may appear contrary to logic that says the maximum disturbance occurs with the maximum signal swing and that occurs with a peak to peak measurement. The reason that the peak measurement is the important parameter is that receivers measure the differential signal from a differential zero

position. Even if the intensity of the cross talk signal is greater with a peak to peak measurement the receiver will only be affected by that portion that deviates from the zero differential level (i.e the peak level).

Since the cross talk is a linear function of amplitude it is not required that the actual aggressor signal be the maximum differential amplitude. A scaling technique is used to compensate for equipment that is not capable of launching maximum amplitude signals. (This is another reason why the pulse technique is desirable.)

Although cross talk is generally more intense with shorter STD aggressor signals, both the maximum and minimum STD signals are required to be used. This is to cover the case where a physical imbalance may extend over longer distances and therefore could yield a more intense cross talk with longer STD aggressor signals.

Effectively the aggressor pulse injects noise into the victim line as the aggressor pulse travels down the aggressor line. Therefore the measured victim noise signal is a direct map of the intensity of the coupling between the aggressor line and the victim line at different points along the path. It is generally found that the connector itself and the termination of the media to the connector are responsible for the most intense coupling. This is a localized coupling that produces a victim line noise pulse with a width approximately twice the electrical length of the coupling region.

In the case where the connector and termination are producing the most intense coupling, the victim line noise pulse returns to near zero as the aggressor pulse passes into the undisturbed media. In the case where the media itself has significant coupling, the noise pulse on the victim line persists for a time equal to approximately twice the electrical length of the coupling region. The factor of two arises because it takes one time for the aggressor pulse to travel and an equal time for the victim line to propagate the resulting noise pulse back to the receiver.

If the victim line noise pulse does not return to near zero after passing the connector/termination region that is a clear indication of high coupling within the media itself. Wiring of lines in the media to the wrong connector contact positions is one possible mechanism that can inadvertently produce much higher coupling than intended.

If there are significant non-uniformities in the coupling within the media these will be revealed by victim line noise pulses well away from the connectors.

This cross talk test is used to specify a performance requirement but is also exceptionally useful to diagnose the causes of the cross talk in all forms.

The near end cross talk test is intended to apply to all constructions of cable assembly including those with equalizers and those with known non uniformities such as intermediate connection points.

#### **6.5.1 Test fixture and measurement equipment**

The same basic test fixture is used as for the impedance profile tests. See Figure 12.

The measurement equipment is also the same as for the impedance profile tests except that a separate receiving head is used for SMI1.

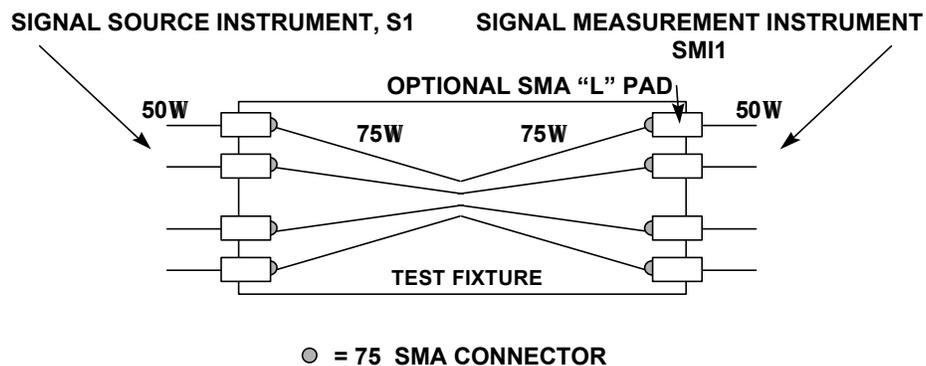
The length and properties of the 50 ohm leads connecting the aggressor signal and the victim measurement instrument to the test fixture should be the same (except as needed to induce imbalance).

### 6.5.2 Calibration procedure

The time reference calibration is done using the same test fixture and nearly the same procedure as for the TDR tests in section 6.1.1 (using a short in place of the IUT for reference time calibration).

Noting the time position of the short establishes a reference time for determining the parts of the tests configuration that are causing the cross talk.

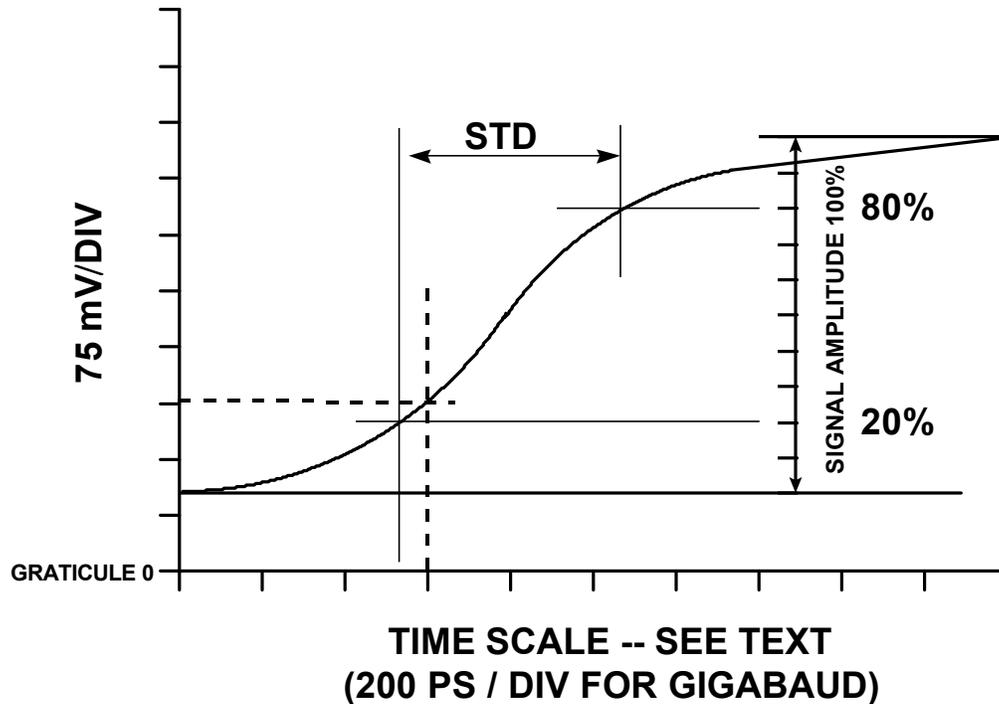
The STD calibration is done using a through fixture identical to that used for the signal degradation tests except that the lower traces are not used. See Figure 40.



**Figure 38 - Amplitude calibration test fixture**

Using the test fixture shown in Figure 38 apply a differential pulse from S1 as large as possible within the capabilities of S1 (if the amplitude is adjustable on S1 otherwise use the default pulse from S1) and measure the received differential pulse at SMI1. Move the displayed curve to the right until a clearly defined flat portion is observed on the lower left portion of the trace. Adjust the vertical position such that the flat portion of the curve (flat for at least three time divisions) passes through the first graticule from the bottom. Position the trace horizontally such that it passes through the third vertical and third horizontal graticule using the scales shown in Figure 39. Set S1 to the required STD by using software filtering or hardware filters. Record the amplitude as described in Figure 41.

Retain all the settings for reuse in the measurement.

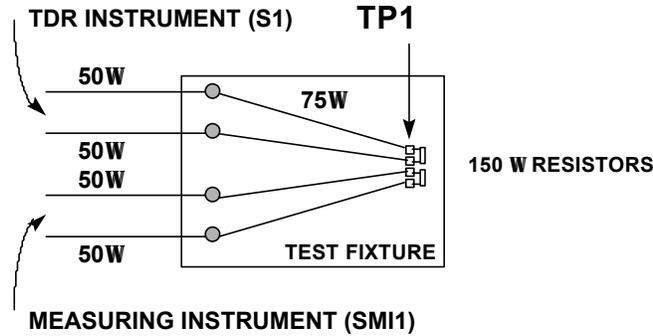


**Figure 39 - Signal transition duration and amplitude calibration**

To calibrate the imbalance in the aggressor signal use again the test fixture in Figure 38. Set SMI1 to measure sum of the + signal and - signal. Using the same signal settings as used for the STD and amplitude calibration adjust phase trimmers or use different length of cable for the + signal and - signal such that the launch imbalance (M1+M2) is approximately 25% of the differential peak established in the amplitude calibration.

Note the exact settings used for both the minimum and maximum STD conditions as these are reused when doing the actual measurement.

A second calibration fixture configuration is used to verify that the fixture is not causing excessive cross talk. This second fixture is identical to that described in section 6.1.1 but with 150 ohm resistors added instead of shorts. The second calibration setup is shown in Figure 40.



○ = CONNECTOR BETWEEN 50 AND 75 OHM SECTIONS

TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED  
TO REPORT VALUES AT TP1

**Figure 40 - Calibration system for NEXT**

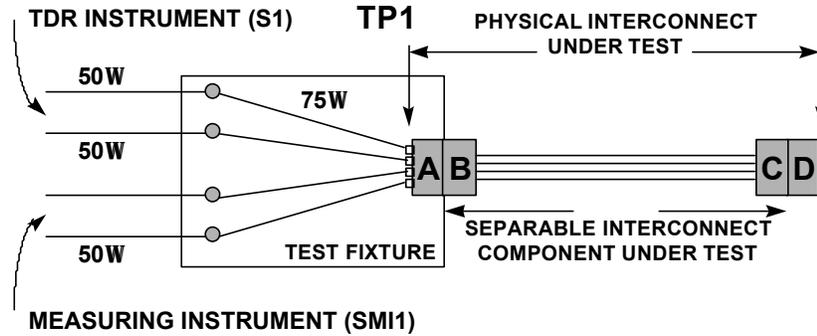
Use the calibrated S1 signal created in the previous steps with the test fixture in Figure 40 measure the cross talk produced.

The maximum allowed cross talk in the victim pair in this calibration condition is 1% for both the longer and shorter STD aggressor signals.

### 6.5.3 Testing procedure

Using the test setup shown in Figure 41 apply the calibrated aggressor pulse for the minimum STD to the aggressor line, S1, and measure the induced noise on the victim line at SMI1. The value of the aggressor signal amplitude as determined by the STD calibration used in the test shall be reported along with the cross talk noise results even if scaling is used. This is required to evaluate the effects of the noise floor for IUT's with small cross talk.

Repeat the test exactly except with the polarity of the leads to S1 reversed.



- A = PERMANENTLY MOUNTED CONNECTOR ON THE TEST FIXTURE
- B, C = PART OF THE SEPARABLE INTERCONNECT UNDER TEST
- D = TERMINATION
- = CONNECTOR BETWEEN 50 AND 75 OHM SECTIONS

TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED  
TO REPORT VALUES AT TP1

Figure 41 - Test configuration for NEXT

Note the largest peak (i.e. largest deviation from zero differential) on the victim line at a time position farther from S1 than the time position of the short determined in the calibration. This largest peak from either polarity is the value of the induced signal for that STD. Note that a peak to peak value is NOT used. Both the absolute value of the induced signal peak and its percentage with respect to the amplitude of the aggressor signal are recorded.

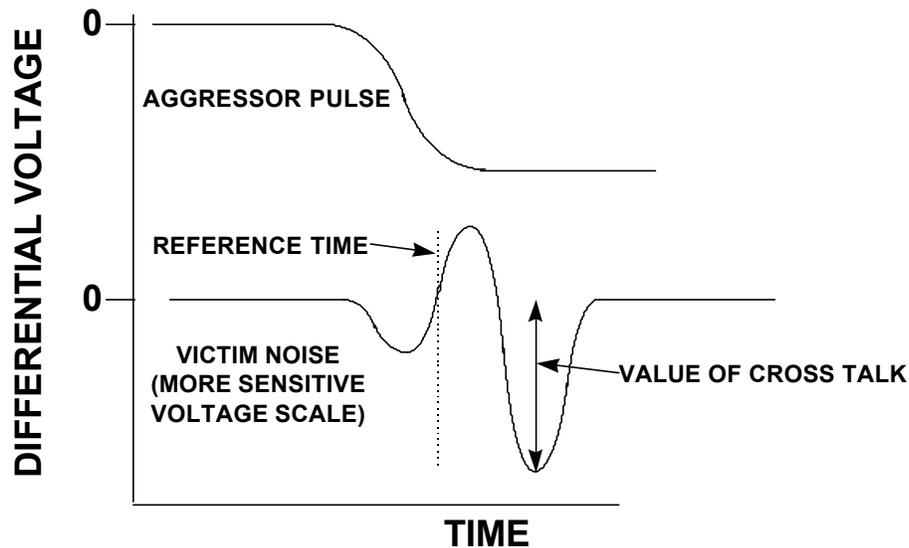


Figure 42 - Example of cross talk measurement

Repeat the tests for both polarity of lead attachment to S1 with the maximum STD aggressor signal.

The absolute value cross talk is scaled to account for the actual amplitude of the aggressor signal. For example if the actual aggressor signal is 500 mV peak and the maximum allowed aggressor signal is 1000 mV then the measured absolute cross talk result would be multiplied by 2.0.

The percentage result does not need to be scaled.

#### 6.5.4 Acceptable ranges

Acceptable values in this document for FC are less than 3%. No number or test procedure has been established in the formal standards.

The amplitude of the signal on the victim line should return to a level significantly lower than observed in the connector/termination region within a few STD's of the mating interface. If this is not observed it is an indication of serious degradation in the IUT. Other tests, notably balance degradation, will detect this degradation as a failure so the observation of the high media coupling is not a direct reason for failing the cross talk test.

## 7. Level 2 tests

## 7.1 Attenuation

Attenuation is calculated from the ratio of output voltage signal level to input voltage signal level through the PUT and is a measure of the losses experienced when transmitting a signal through the interconnect. Higher attenuation means less signal at the output or equivalently a gain of less than unity. A sinusoidal signal is used to eliminate the need for complex descriptions of real pulses and square or trapezoidal signals in terms of Fourier components. A complete attenuation specification requires examining all frequencies of interest to the application. A spectral description is recommended. The basic formula for attenuation in decibels is:

$$\text{Attenuation (dB)} = 20 \log_{10} (\text{input signal} / \text{output signal}).$$

Note that this formula gives the attenuation as a positive number since the argument of the log is greater than unity. Sometimes attenuation is casually reported as a negative number when the gain is really the intended mathematical statement. In any case the magnitude is the same for both gain and attenuation. The following formula expresses gain in decibels.

$$\text{Gain (dB)} = 20 \log_{10} (\text{output signal} / \text{input signal})$$

If the output and input signals are measured in power instead of voltage then the multiplier in the above equations is 10 instead of 20.

Since the argument of the log is less than unity the gain is a negative number.

This document requires that attenuation be expressed as a positive number unless there is active gain in the path from active circuits.

Therefore a typical attenuation plot has the form shown in Figure 43.

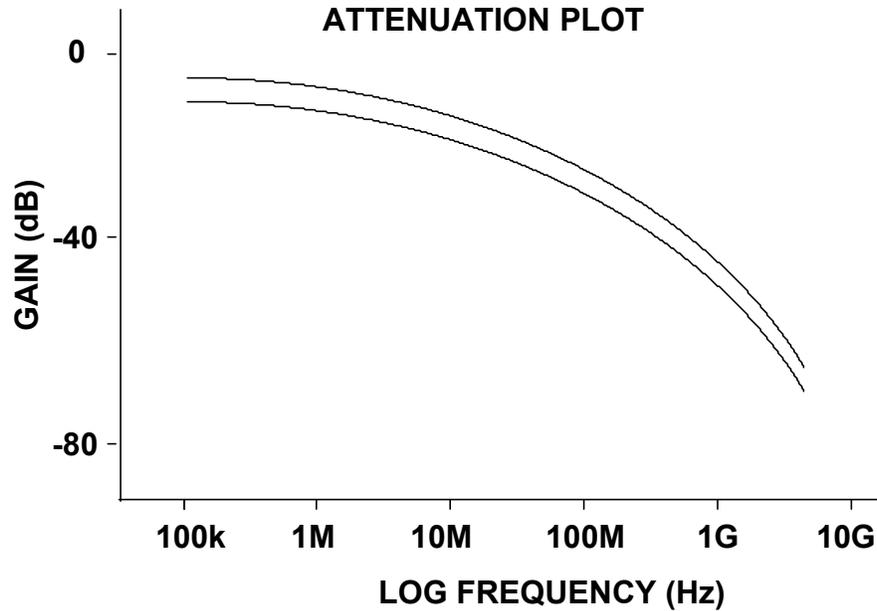


Figure 43 - Form of attenuation plots

Attenuation is a measurement of the dissipative losses on a balanced transmission line. The series resistive loss of the conductors (copper) and the shunt loss due to the dissipation factor of the dielectric covering the conductors dominate these losses. At higher frequencies, the conductor loss increases due to skin effect. Skin effect is where the current becomes increasingly confined in the outer "skin" of the conductor as the frequency increases. This effectively reduces the conductor area available for current flow. The attenuation for a given balanced transmission line is affected by the conductor metal composition and size and the composition, uniformity, and thickness of the dielectric that surrounds the conductors.

Attenuation can only be measured directly with an ideal test system that is perfectly matched to the balanced transmission line to be tested. In a practical test system, the quantity that is actually measured is insertion loss. Insertion loss is comprised of a component due to the attenuation of the balanced transmission line, a component due to the mismatch loss at the input or near end side of the transmission line and a component due to the mismatch loss at the output or far end side of the transmission line.

There is a mismatch loss component at any interface where the transmission line impedance is not perfectly matched on both sides of the interface. The amount of mismatch loss that is experienced at each interface is :

$$\text{Mismatch Loss (dB)} = (-10 \text{ LOG}_{10} (1 - |\Gamma|^2)) \text{ dB}$$

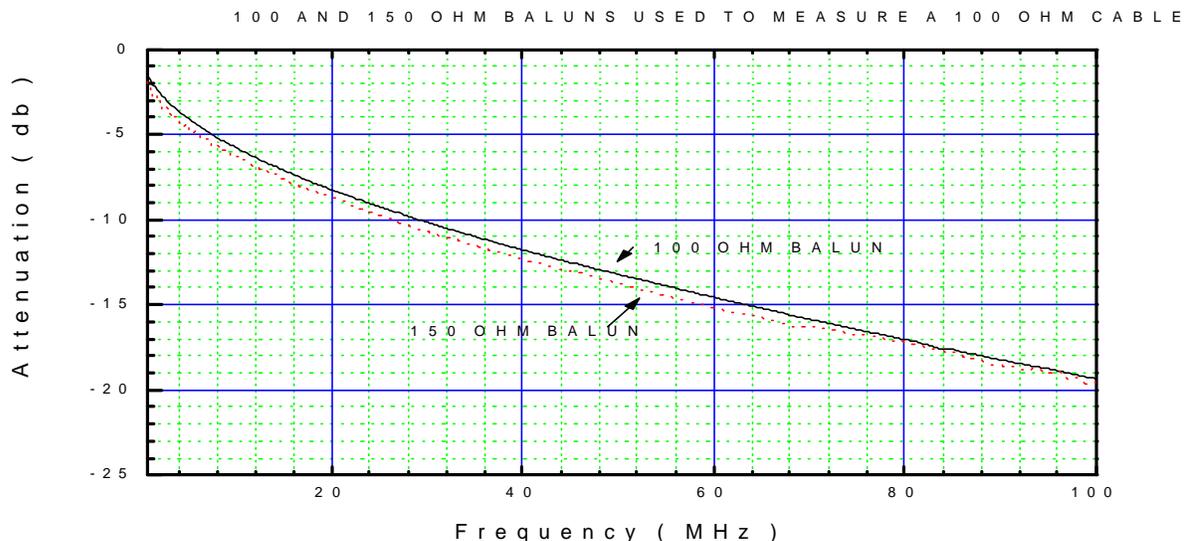
Balanced transmission lines are also susceptible to measurement errors when measuring high values of attenuation (>50 dB) due to radiated energy coupling into the transmission line. The largest source of this error is due to direct coupling of the near end side of the test system to the far end side of the test system. This coupled signal will combine with the test signal passing

through the transmission line under test and cause a significant ripple error in the insertion loss measurements at the higher frequencies where the attenuation of the transmission line under test is the largest.

Since the test instruments are single ended and the IUT is balanced a coupling device called a balun is required to connect the IUT to the test equipment.

**Balun Selection.** The impedance on the primary side of the balun must match the impedance of the test equipment, normally a network analyzer. The impedance on the secondary side of the balun must be matched as closely as possible to the nominal impedance of the IUT in the balanced state to minimize reflections. If reflections are present they will skew the data by introducing a mismatch loss ripple component.

Figure 44 shows the effect of different baluns on a very long cable (approximately 300 meters). There are no reflections visible because they are attenuated to insignificant levels by the long length. Another very important benefit to using long cables for these tests is the elimination of resonance effects for the same reason that reflections are not a problem. The main effect of using relatively seriously mismatched baluns on very long cables is a small error in the attenuation reported (less than 1 dB in the example shown).



**Figure 44 - Effect of balun selection on measured attenuation for very long cables**

**Sample Length.** The optimum sample length is such that there is at least ~ 1db of one way attenuation at the lowest frequency of interest. This will guarantee that there is at least 2 dB of additional loss experienced by that portion of the test signal that reflects from the far end.

This will reduce the uncertainty caused by multiple reflections due to the far end and will result in acceptable resolution / ripple. The resulting measurements is accurate and repeatable. If a sample is used that yields an attenuation of less than 1dB the mismatch ripple from the near end combined with the mismatch ripple from the far end can approach the same or greater

magnitude than the attenuation at the lowest frequency. For example in the unmatched balun case:

Case 1 :

Near End Balun  $Z = 100 \text{ Ohm}$

Far End Balun  $Z = 100 \text{ Ohm}$

Nominal Balanced Cable  $Z = 150 \text{ Ohm}$

Balanced Cable loss at lowest test frequency =  $0.5 \text{ dB} = 0.94406$

In case 1 there is only  $0.5\text{dB}$  attenuation in the presence of a ripple that will add anywhere from  $0.354 \text{ dB}$  to  $0.6972\text{dB}$  of measurement error as shown in Figure 45.

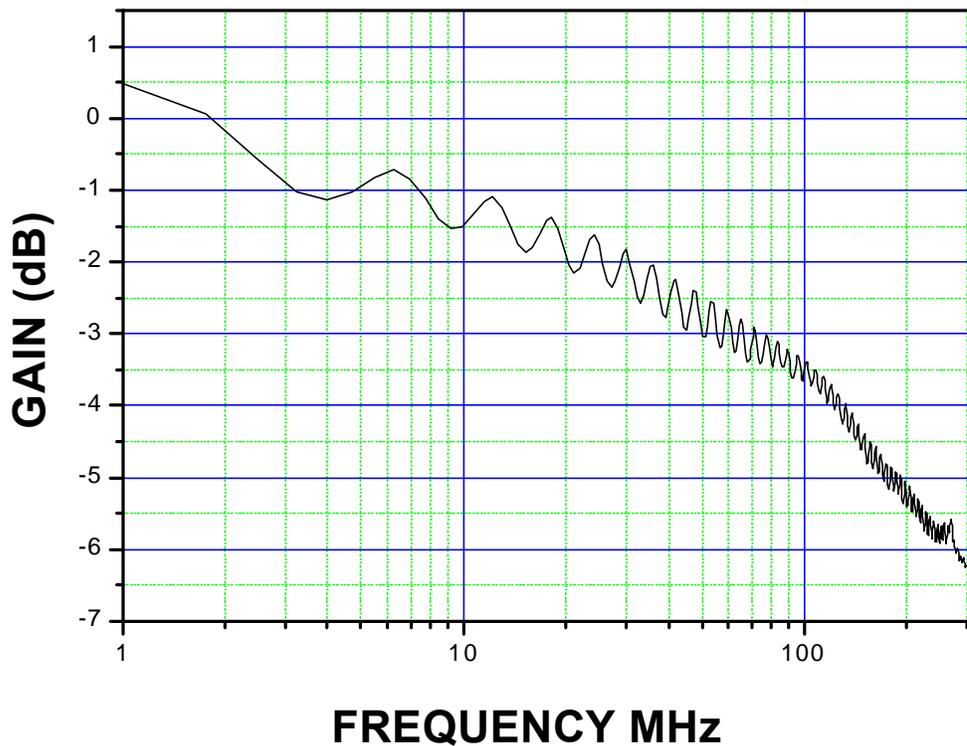


Figure 45 - Effects of mismatched baluns in a short IUT

For the matched case otherwise identical to case 1:

Case 2 :

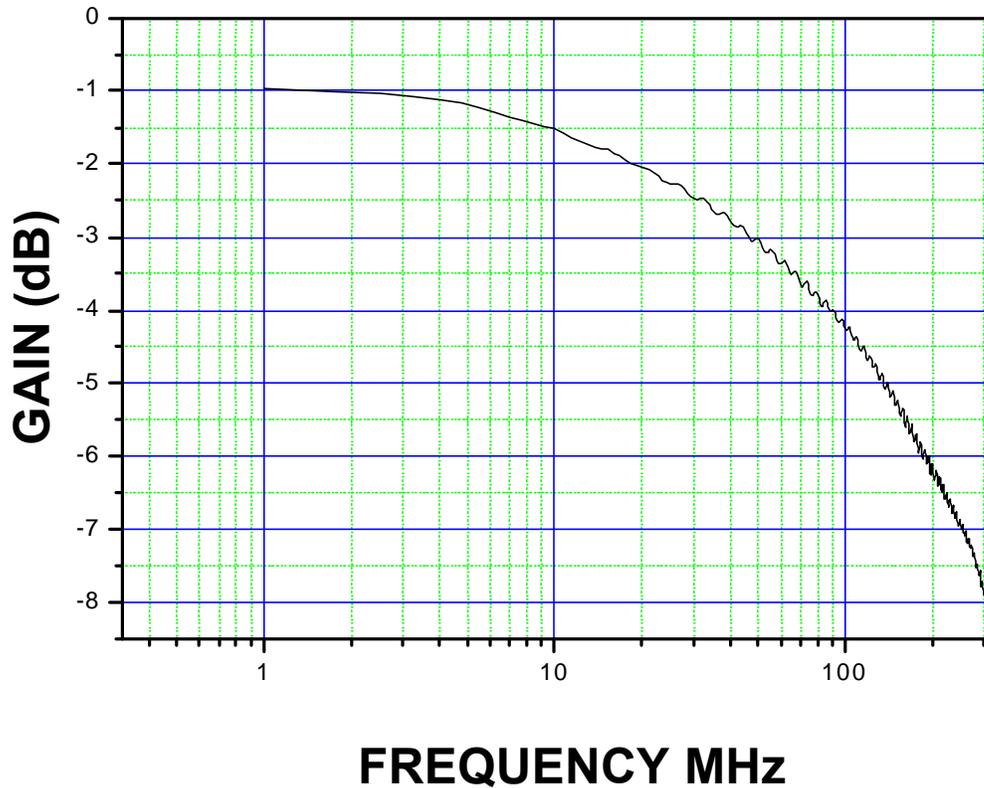
Near End Balun  $Z = 150 \text{ Ohm}$

Far End Balun  $Z = 150 \text{ Ohm}$

Nominal Balanced Cable  $Z = 150 \text{ Ohm}$

Balanced Cable loss at lowest test frequency =  $.5 \text{ dB} = .94406$

The insertion loss equals the desired attenuation result and there is no ripple to cause measurement uncertainty as shown in Figure 46.



**Figure 46 - Effect of matched baluns on a short sample**

Finally, for the case of at least 6 dB of low frequency attenuation the results are achieved without requiring a closely matched balun:

Case 3 :

Near End Balun  $Z = 100$  Ohm

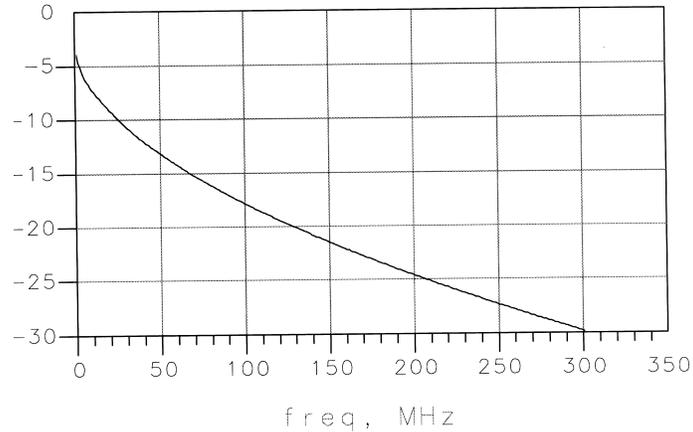
Far End Balun  $Z = 100$  Ohm

Nominal Balanced Cable  $Z = 150$  Ohm

Balanced Cable loss at lowest test frequency  $\sim 6$  dB

Under a mismatched condition, the insertion loss equals the attenuation plus the mismatch loss at the near end and at the far end. However, in this case, there is sufficient attenuation in the cable at the lowest frequency to make multiple reflections inconsequential, so there is no ripple component of measurement uncertainty. The mismatch loss error is still present, but it is  $\sim 0.3$  dB out of a measured insertion loss of  $\sim 6$  dB.

GAIN (dB)



**Figure 47 - Effects of mismatched baluns with 6 dB LF attenuation**

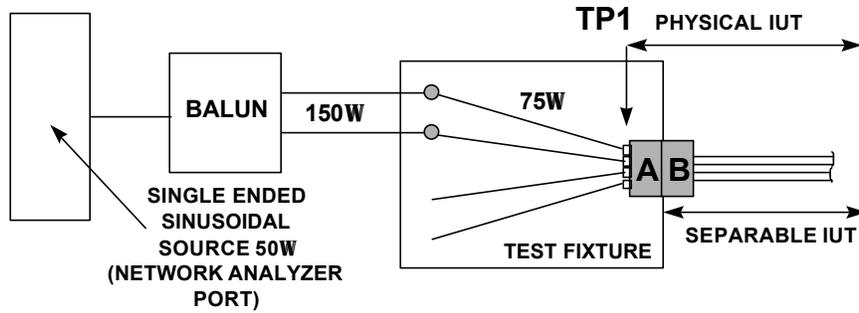
*Note: The use of an attenuator for measuring shorter lengths is not acceptable because there is still mismatch loss uncertainty due to the fact that the attenuator does not have any better match than the far end test port. Also an additional uncertainty is introduced because a small value (cable attenuation) is being subtracted from a large value, (attenuator attenuation). There are also dynamic range issues for the instrumentation.*

#### 7.1.1 Measurement test fixture and measurement equipment

An instrument capable of supplying a sinusoidal signal is used as the signal source and an instrument capable of detecting the amplitude of a sinusoidal signal is used as the signal sink. Two measurement test fixtures are required: one for the source end and one for the sink end. Since most source and sink instruments capable of using variable frequency sinusoidal signals are single ended, a balun [Picosecond Pulse Labs] or a hybrid [Picosecond Pulse Labs, Minicircuits] may be used between the instruments and the test fixtures. If a source or sink is used that is capable of sourcing or sinking differential signals then no balun is required for the differential source or sink.

Equipment Required: Network Analyzer ( HP 87xx Series )

A test fixture having  $75\Omega$  single ended paths for each signal line is used for the measurement as shown in Figure 48 and Figure 49 and calibrated as shown in Figure 50. This test fixture may be exactly the same as used for the impedance profile tests in 6.1.

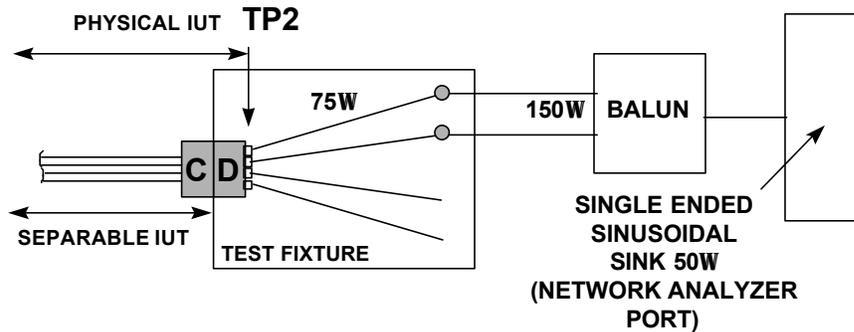


- A = PERMANENTLY MOUNTED CONNECTOR ON THE TEST FIXTURE
- B = PART OF THE SEPARABLE INTERCONNECT UNDER TEST
- = CONNECTOR

TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED TO REPORT AT TP1

Figure 48 - Source-end test fixture for attenuation tests

The balun shown in Figure 48 is 50 Ω single ended to 150 Ω differential.



- A = PERMANENTLY MOUNTED CONNECTOR ON THE TEST FIXTURE
- B = PART OF THE SEPARABLE INTERCONNECT UNDER TEST
- = CONNECTOR

TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED TO REPORT VALUES AT TP2

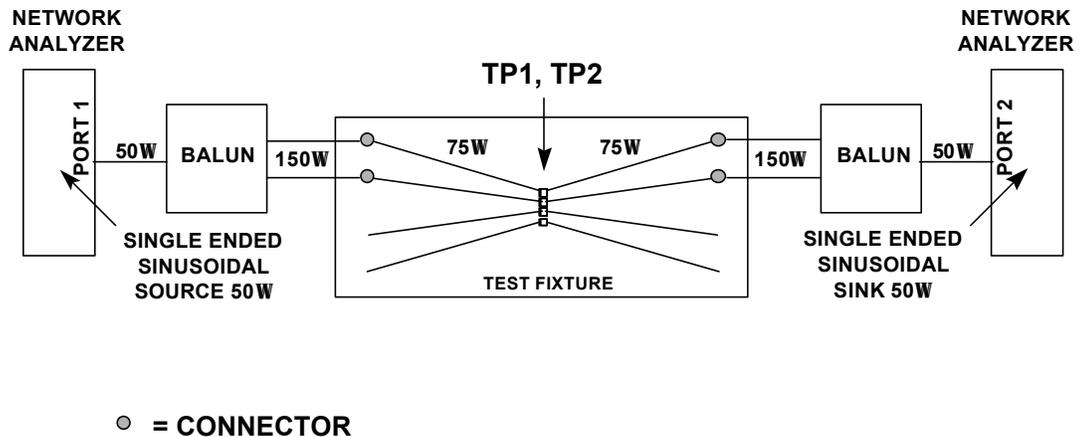
Figure 49 - Sink end test fixture for attenuation tests

The separable IUT is connected between the source and sink test fixtures.

### 7.1.2 Calibration procedure

A special "through" test fixture is used for the signal calibration process

which is exactly like the test fixture in Figure 48 and Figure 49 except that there are no IUT connectors (A, D). See Figure 50.



**TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED  
TO REPORT VALUES AT IUT CONNECTION POINT (TP1, TP2)**

**Figure 50 - Calibration configuration for attenuation tests**

Using the instructions from the network analyzer perform a calibration scan over the frequency of interest.

### 7.1.3 Testing procedure

Connect the IUT to the test fixtures shown in Figure 48 and Figure 49 (including the board mounted connectors).

Using the instructions from the network analyzer perform an attenuation scan over the frequency range of interest. The instrument automatically accounts for the attenuation found in the calibration scan.

It is important to either separate or shield the baluns from each other when measuring long cable samples. When the attenuation of the cable exceeds ~50 dB or the frequency is above approximately 150 MHz, potential direct coupling from the near end to the far end balun will create an increasingly large ripple in the attenuation measurement that can cause a significant amount of measurement uncertainty.

Figure 51 and Figure 52 show the effects of balun isolation.

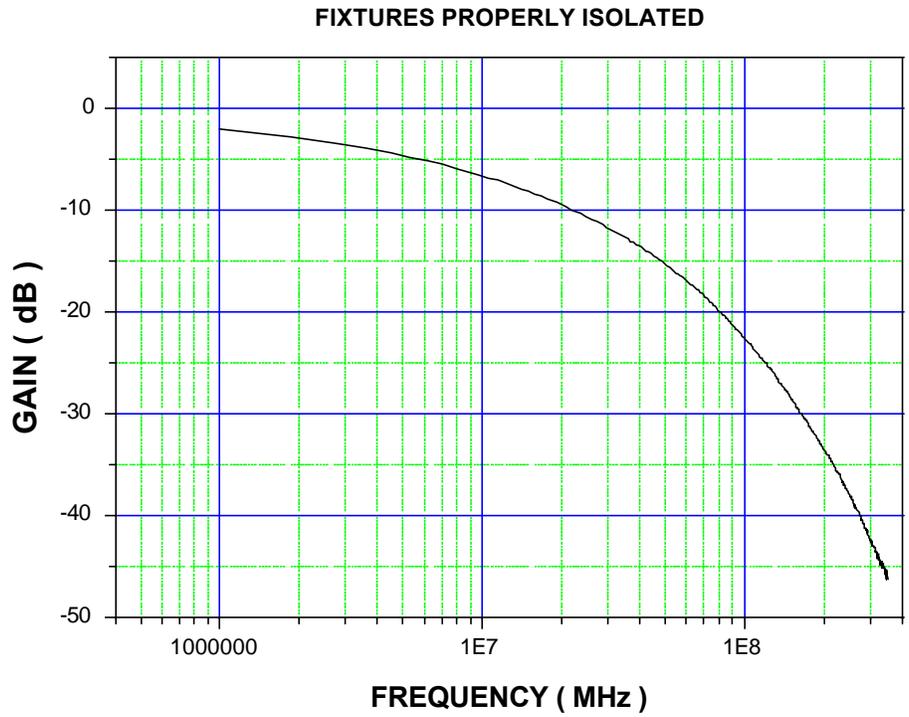


Figure 51 - Attenuation scan with proper balun isolation

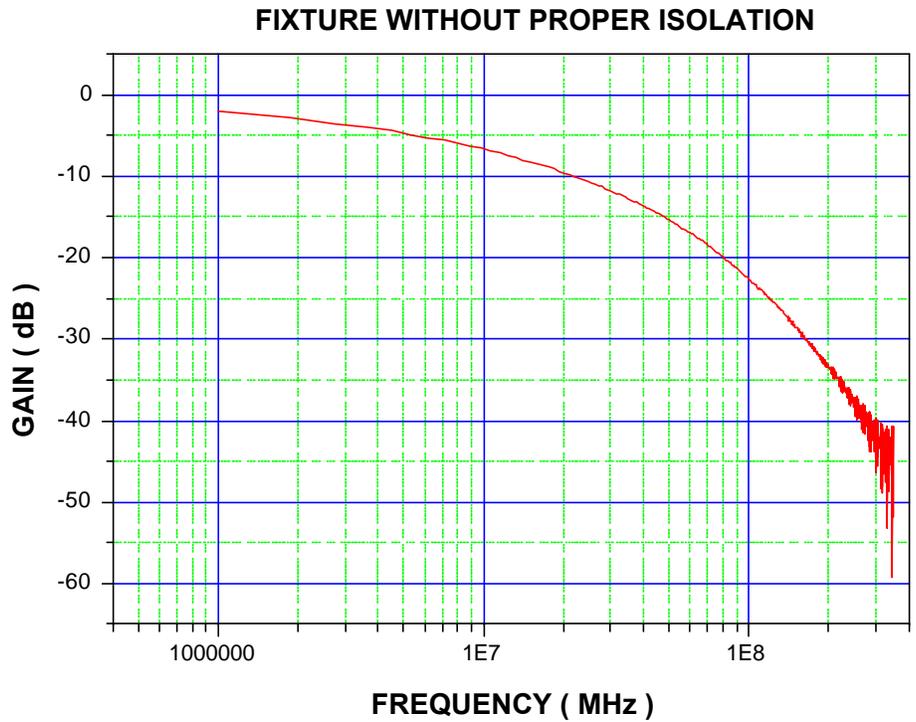


Figure 52 - Attenuation scan without good balun isolation

#### 7.1.4 Acceptable ranges

Since attenuation is a level 2 test there are no acceptable ranges defined in this document.

### 7.2 Propagation time and propagation time skew

Propagation time refers to the time required for a specific part of a signal to travel a specific distance along the path of the line. The propagation time skew is the difference between the propagation times for the + signal and the - signal over the same nominal path.

Since the only skew of interest for this document is between the + signal and the - signal the measurements are all single ended.

Propagation time skew is one major contributor to imbalance.

There are two basic approaches to this measurement:

- (1) single pulses are simultaneously launched on the + signal and the - signal. The time required for the midpoint of each to reach the other end of the interconnect is measured.
- (2) a repeating clock like data pattern is launched differentially onto the + signal and - signal at one end and the points where the + signal and - signal cross each other and respectively cross the d.c. common mode point (normally zero) are noted at the other end.

These methods are nearly identical in principle but the former method may be easier to use since there is only one pulse propagating while with a repeating pattern one must figure out which received edge goes with the respective transmit edge. The equipment needed is also different for the S1. Only the first method is documented in detail in this document.

This test is a close relative to the amplitude imbalance test described in section 7.3 and the same equipment and test fixtures may be used for both purposes.

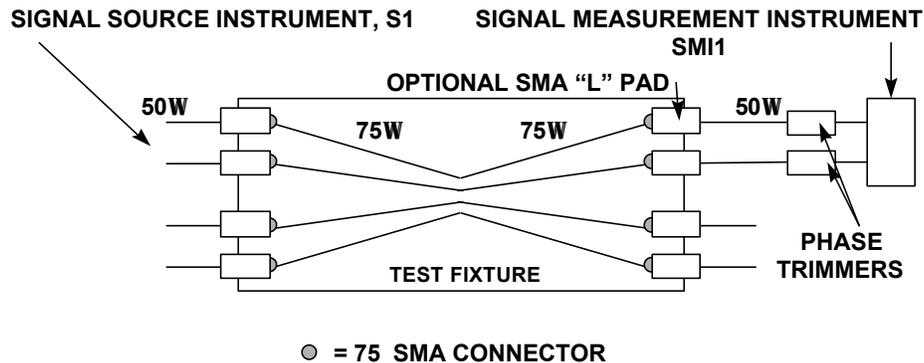
#### 7.2.1 Test fixture and measurement equipment

The same thru connection test fixture and measurement test fixtures as described in section 6.2 are used. There is no requirement for a second source for these tests.

The equipment consists of a Tektronix 11801 with SD24 heads or equivalent.

#### 7.2.2 Calibration procedure

The calibration configuration shown in Figure 53 is used.



**Figure 53 - Calibration configuration for propagation time tests**

A differential pulse signal is applied from S1 through the test fixture as shown in Figure 53. The trigger output from S1 is used to trigger SMI1. SMI1 is adjusted such that M1 and M2 are displayed on exactly the same scales but with the polarity reversed on one or the other. This will produce two nearly identical pulses overlaid on each other. The zero level is set the same for both channels.

Adjust the phase trimmers such that the midpoints of the M1 and M2 traces are coincident on SMI1. This will produce identical M1 and M2 traces if the causes of imbalance are purely due to propagation time skew. If the traces are not substantially coincident go to section 7.3 for further discussion of the causes. The test equipment and fixtures should produce substantially coincident traces for use with this test.

**Figure 54 - Use of phase trimmers for calibration**

If the traces are not coincident then amplitude imbalance is at least part of the imbalance in the received signal.

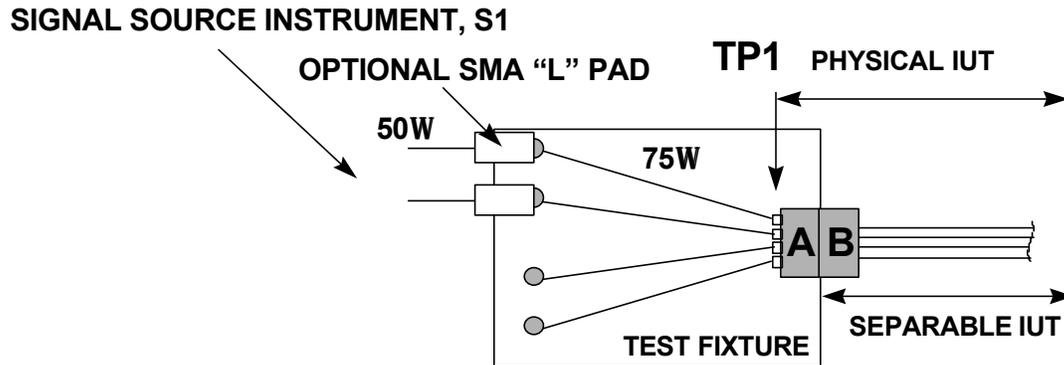
This calibration process effectively takes all the propagation time skew and other sources of equipment and test fixture imbalance out of the measurement process. There is some propagation time required to traverse the instrumentation cables and test fixture and this needs to be accounted for in the propagation time measurement.

Note the time position of the midpoint of the received pulses. During the testing procedure this time is subtracted from the measured propagation time since exactly the same trigger is used for SMI1.

In all measurements in this section averaging shall be used in SMI1 to eliminate the effects of jitter. The term "single pulse" refers to the time average of a series of widely spaced but repeating pulses.

### 7.2.3 Testing procedure

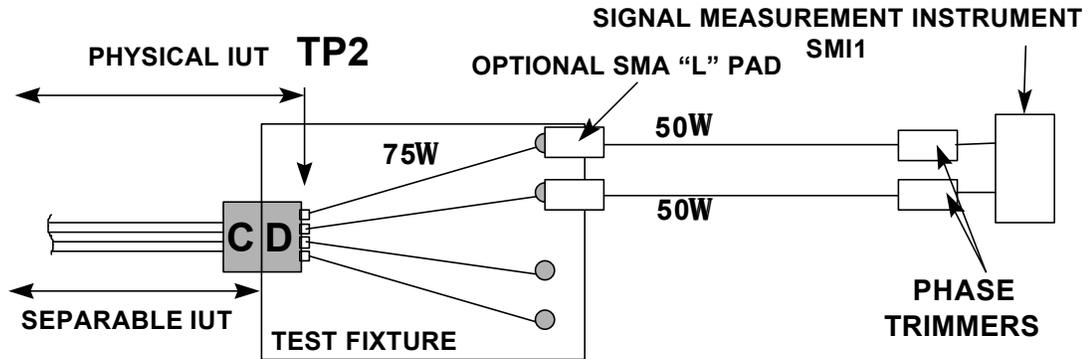
Using the test fixtures described in section 6.2.1 connected as shown in Figure 55 and Figure 56 apply the same pulses from S1 that were used during the calibration process.



- A = PERMANENTLY MOUNTED CONNECTOR ON THE TEST FIXTURE
- B = PART OF THE SEPARABLE INTERCONNECT UNDER TEST
- = 75 W SMA CONNECTOR

**TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED  
TO REPORT VALUES AT TP1**

Figure 55 - Source side measurement test fixture configuration for propagation time



- C** = PERMANENTLY MOUNTED CONNECTOR ON THE TEST FIXTURE
- D** = PART OF THE SEPARABLE INTERCONNECT UNDER TEST
- = 75 SMA CONNECTOR

**TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED  
TO REPORT VALUES AT TP2**

**Figure 56 - Receiver side measurement test fixture for propagation time tests**

Record the results in exactly the same manner as used for adjusting the phase trimmers in the calibration section. The time difference between the midpoints of the received pulses is the propagation time skew and the time position of the average of the midpoints of the pulses is the propagation time (including that of the test fixture and instrumentation). Subtract the time position noted during the calibration to attain the propagation time of the IUT.

Note that if the received traces cannot be made coincident by a simple time translation then effects other than pure propagation time are operating. See section 7.3.

#### 7.2.4 Acceptable ranges

Since propagation time and propagation time skew are level 2 tests there are no acceptable ranges defined in this document.

#### 7.3 Amplitude imbalance between the + signal and - signal

Amplitude imbalance is that not caused by propagation time skew. The test for amplitude imbalance is inability to make the traces match by a simple time translation. See section 7.2.

Figure 57 shows three kinds of imbalance and some example causes that may be experienced in real systems.

## RECEIVED PULSES

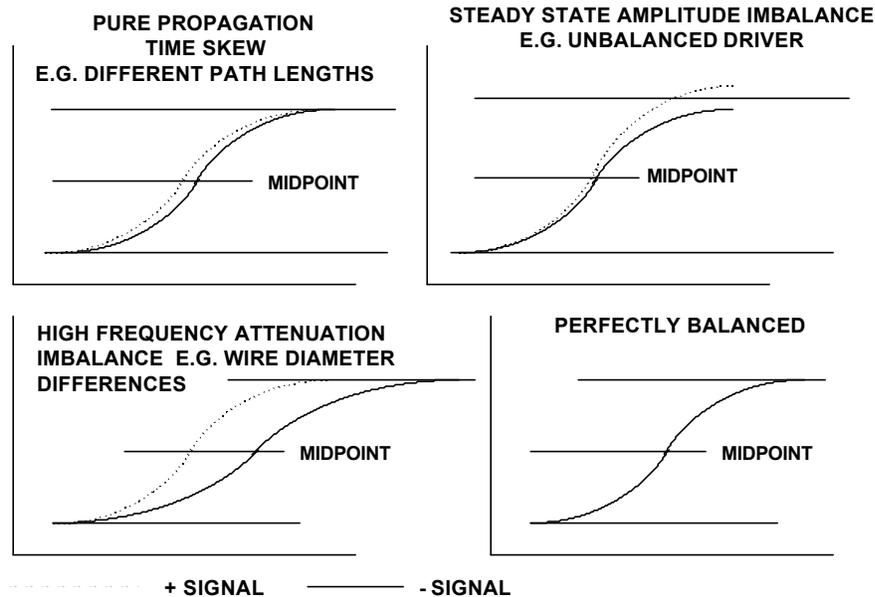


Figure 57 - Examples of received pulses

The path length propagation time skew imbalance can be corrected by a simple time translation. The steady state amplitude imbalance can be corrected by a simple gain adjustment. The high frequency attenuation, on the other hand, will not be corrected by either a time translation or a gain adjustment.

Examination of the structure of the received pulses can provide primary diagnosis of the cause of imbalance.

### 7.3.1 Test fixture and measurement equipment

The test fixtures and equipment are exactly the same as used for the propagation time tests in section 7.2.1.

### 7.3.2 Calibration procedure

The calibration procedure is exactly the same as for the propagation time tests in section 7.2.2. Note that it is necessary to remove any significant imbalance in the test equipment and test fixtures before proceeding.

### 7.3.3 Testing procedure

Connect the IUT and perform the tests exactly as described for the propagation time tests in section 7.2.3.

#### **7.3.4 Acceptable ranges**

Since amplitude imbalance is a level 2 test there are no acceptable ranges defined in this document.

#### **7.4 Signal transition duration**

This level 2 test is very similar to the level 1 STD calibrations described for the impedance profile tests in section 6.1 except that it is done on actual signals from a driver instead of using a TDR source. The main difference is that the driver source does not start with the single ended signals at zero but rather is always driving a logical "zero" or a logical "one". The purpose of this test is to measure a signal transition duration that is reproducible between different measurement equipment and to allow calibration of S2 sources.

The test is defined such that there are no user variables. The base data rate of the signals under consideration must be known.

##### **7.4.1 Test fixture and measurement equipment**

This test applies to whatever measurement point is of interest. Since this is a level 2 test its purpose is to aid in diagnosing and characterizing systems and measurements. As such there is no specific test fixture required.

The equipment is a sampling oscilloscope, such as the Tektronix 11801 that can provide the scales required for the time and voltage axes.

##### **7.4.2 Calibration procedure**

The only calibration required is that needed for the basic instrument. Use the manufacturers procedure.

##### **7.4.3 Testing procedure**

This same process applies for differential and single ended measurements.

In some applications there is a non zero average signal level even when when using perfectly symmetrical (clock like) or d. c. balanced coded data patterns (e.g. 8b10b) for the single ended signals. The single ended signals are always referenced to this average level for the STD test. This section assumes that the average level is zero. If the average level is not zero then the actual average level is used for the center of the display. One may determine the average level by adding the + signal and the - signal, taking the average to remove high frequency common mode (imbalance) content and dividing the average by two.

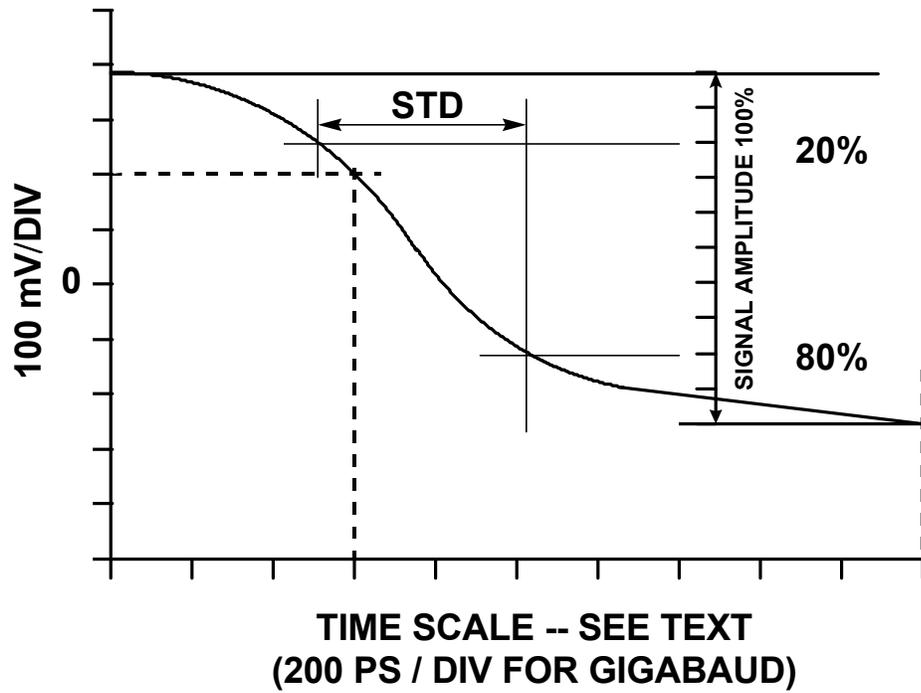
Assuming a falling edge, set up the display on the TDR as shown in Figure 14.

This display has the following properties:

- The span of the time scale on the display is approximately twice the nominal bit or half cycle period for the data rate being used. Ten divisions are used on the time axis. Specifically Table 5 shows the time scales to use.
- The vertical axis is set at 100 mV per division with the zero level set at the fifth division from the bottom (see Figure 14).
- Set the horizontal position such that the displayed curve passes through the third division on the time axis and the seventh division on the vertical axis
- Use the peak to peak function on the oscilloscope (if available) to find the signal amplitude of the displayed portion of the trace as shown in Figure 14. This amplitude may also be read directly off the display. This signal amplitude of the displayed trace may or may not accurately represent the asymptotic signal levels that may exist at times not displayed. If the signal amplitude is such that the minimum value exceeds  $\pm 500$  mV change the vertical scale to 200 mV/div and repeat this and the immediately preceding steps.
- The signal transition duration (STD) is the time between the 20% and 80% values of the displayed signal amplitude

**Table 5 - Scale to be used for STD calibrations**

Bit rate * (Mbits/s)	Time axis scale (ps/div)
20 ST	5000
40 ST	2500
40 DT	5000
80 ST	1250
80 DT	2500
100 DT	2000
200 DT	1000
400 DT	500
800 DT	250
1062.5	200
1250	200
1600	100
2125	100
2500	100
3200	50
4250	50
5000	50
* ST = single transition clocking DT = double transition clocking	



• Figure 58 - Signal transition duration measurement

For a rising edge signal the STD measurement is the same as for the falling edge with the changes noted in Figure 59.

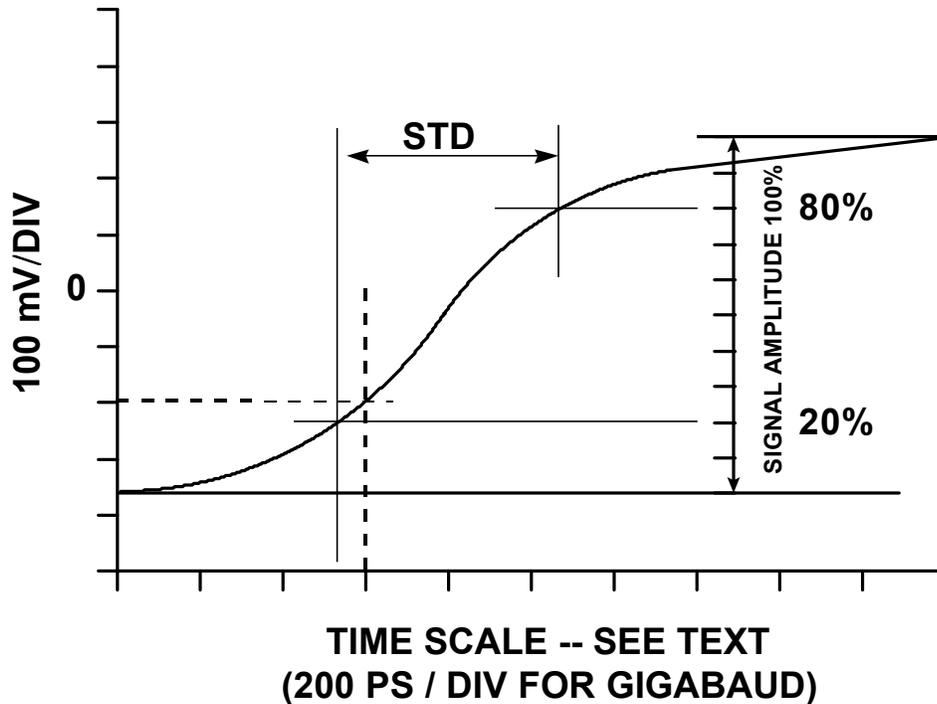


Figure 59 - Signal transition duration calibration

#### 7.4.4 Acceptable ranges

Since this is a level 2 test there are no acceptable ranges defined.

#### 7.5 Cross talk component of signal degradation

Cross talk provides one source of uncorrelated noise that degrades both the amplitude and jitter of the PUT signals. This section describes three methods that can be used to diagnose and characterize cross talk noise:

1. Noting effect of removal of second source on the signal degradation
2. Single pulse
3. Sinusoidal

Each of these is a separate test type and each yields different information. It may be desirable to use more than one technique on the same IUT.

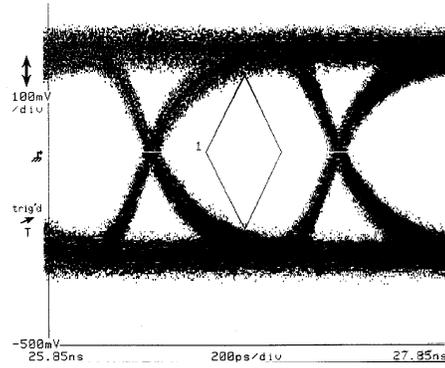
##### 7.5.1 Removal of second source

This test is identical to that described under sections 6.2 and 6.3 except that the second source is removed and the resulting eye pattern or signal display is

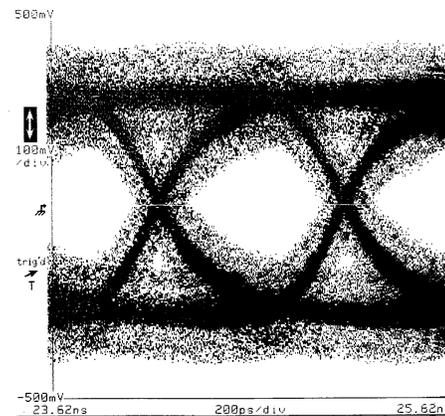
compared to that measured with the second source turned on. The difference between the two measurements provides a quantitative measure of the cross talk.

This technique has at least two significant drawbacks: (1) the results may be seriously affected by resonant conditions in the IUT and/or the test fixtures and (2) it is not possible to determine which part of the IUT/test fixture is the primary contributor to the cross talk.

### SIGNAL DEGRADATION TEST WITH SECOND SOURCE ACTIVE (SAMPLE A -NORMAL)



### SIGNAL DEGRADATION TEST WITH SECOND SOURCE ACTIVE (SAMPLE B - HIGH CROSS TALK)



### SIGNAL DEGRADATION TEST WITH SECOND SOURCE OFF -- NO CROSS TALK

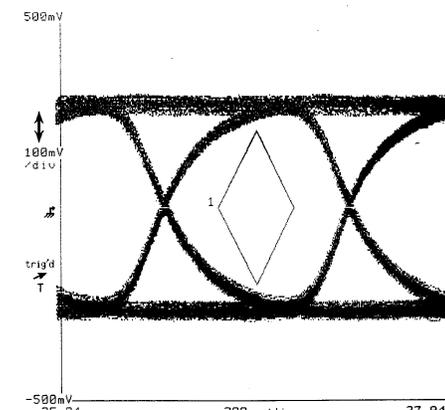


Figure 60 - Cross talk effects on signal degradation test results

### **7.5.2 Single pulse**

This method is exactly the same as that described in 6.5. The parts of the test fixture/IUT that are responsible for the cross talk are identifiable by noting the time position where the cross talk occurs.

### **7.5.3 Sinusoidal**

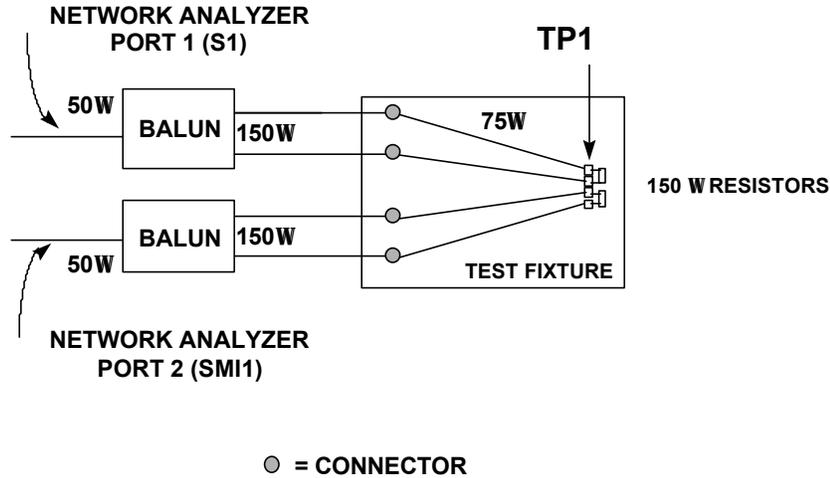
This test is very similar to the attenuation tests described in section 7.1 except that the signal on the victim line is measured rather than the signal from the far end of the IUT. A frequency scan is made over the entire range of interest.

This test is of interest because it can expose cross talk effects that have their origin well away from the connectors and because the effects of resonances can be seen.

#### **7.5.3.1 Test fixture and measurement equipment**

The test fixtures used for the NEXT tests in section 6.5 and the test equipment and baluns described in section 7.1.1 are used for this test .

#### **7.5.3.2 Calibration procedure**



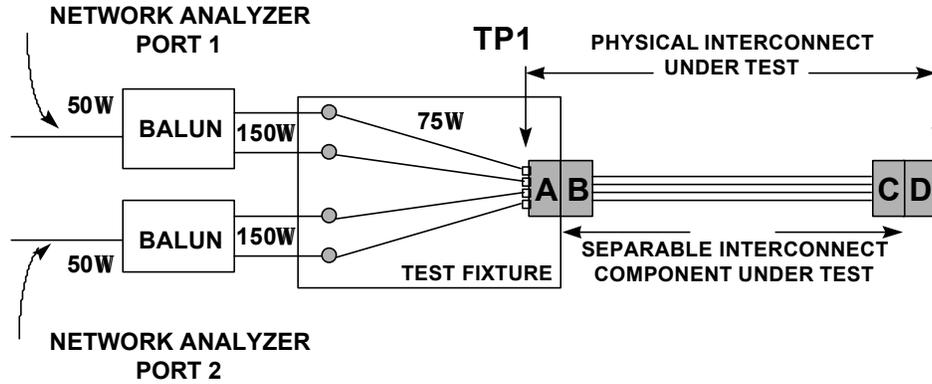
**TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED  
TO REPORT VALUES AT TP1**

**Figure 61 - Calibration configuration for sinusoidal cross talk**

Using the instructions from the network analyzer manufacturer run a calibration scan on the configuration shown in Figure 61.

#### 7.5.3.3 Testing procedure

Using the instructions from the network analyzer manufacturer run a test scan on the configuration shown in Figure 62.



**A** = PERMANENTLY MOUNTED CONNECTOR ON THE TEST FIXTURE  
**B, C** = PART OF THE SEPARABLE INTERCONNECT UNDER TEST  
**D** = TERMINATION  
 ○ = CONNECTOR

**TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED  
 TO REPORT VALUES AT TP1**

**Figure 62 - Test configuration for sinusoidal near end cross talk tests**

Subtract the calibration scan from the test scan to reveal the cross talk performance of the IUT.

The cautions concerning cross coupling between the baluns described in section 7.1.3 apply to these tests as well.

#### 7.5.3.4 Acceptable ranges

Since this is a level 2 test there are no acceptable ranges defined.

## 8. ANNEX A Acceptable ranges

### 8.1 Impedance profile

Table 6 lists some of the known requirements for impedance profile parameters.

· **Table 6 - Allowed ranges for impedance profile**

Application	Allowed values in close proximity electrical neighborhood	Exception windows	Signal transition duration ranges (ps)	Media
Full speed FC	150 $\pm$ 30 $\Omega$	800 ps *	100 to 385	150 $\pm$ 10 $\Omega$
Double speed FC	150 $\pm$ 30 $\Omega$	800 ps *	75 to 200	150 $\pm$ 10 $\Omega$
GBE				
1394				
SSA				
NGIO				
Future I/O				
* This SFF document recommends a 300 ps exception window for cable assemblies (see 6.1.4)				

### 8.2 Signal degradation

The acceptable ranges are specified by eye diagrams for the respective technologies. The allowed ranges for full speed FC are given in Figure 63, Figure 64, Figure 65, and Figure 66. Note that these are not the allowed test ranges for the receive signals per the test procedures defined in this document. The allowed test ranges must be modified to account for launch test signals that are better than the worst case allowed. Refer to earlier sections for a detailed discussion.

Ranges for other technologies will be added as they become available.

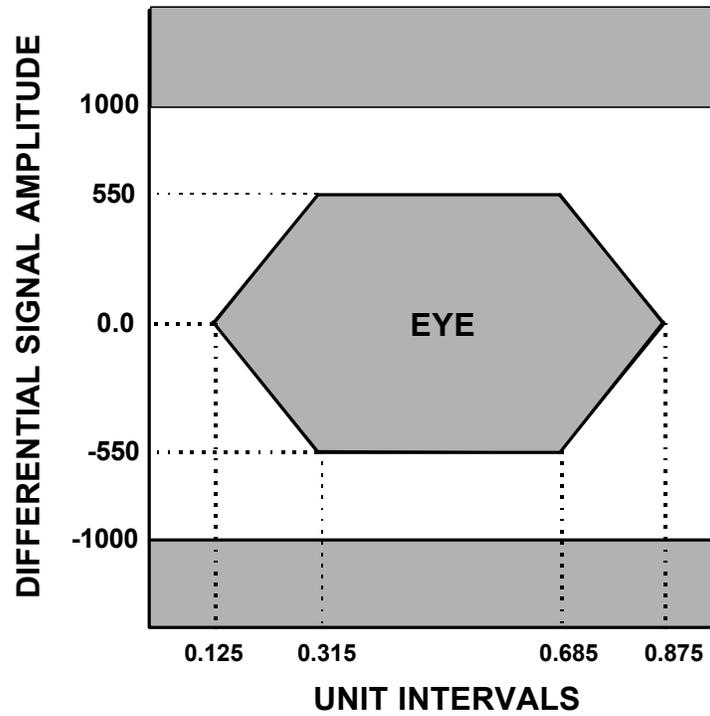


Figure 63 - Specified transmit mask for full speed FC external

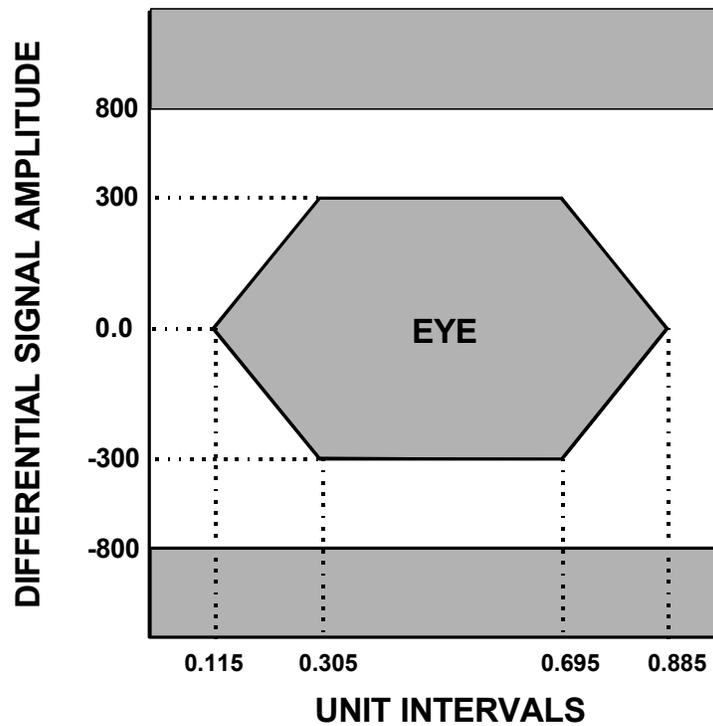


Figure 64 - Specified transmit mask for full speed FC internal

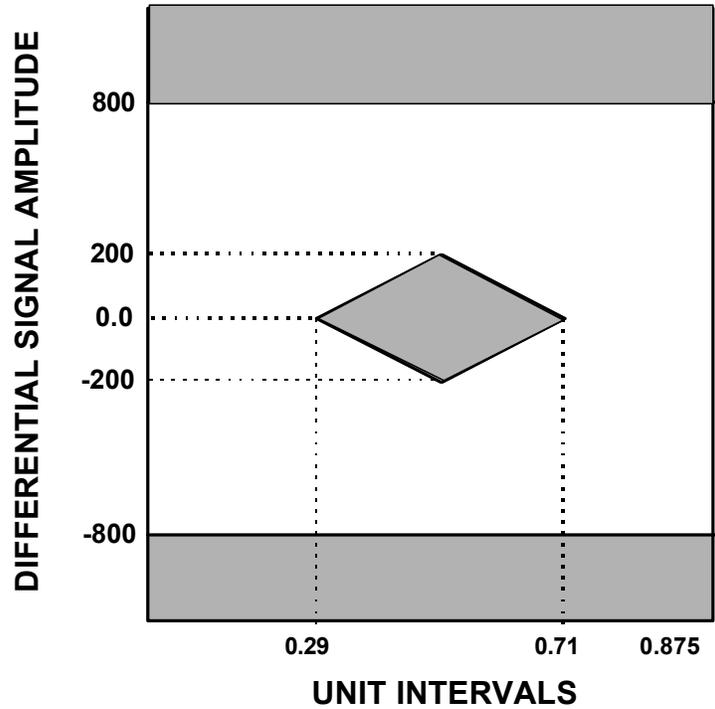


Figure 65 - Specified receive mask for full speed FC external

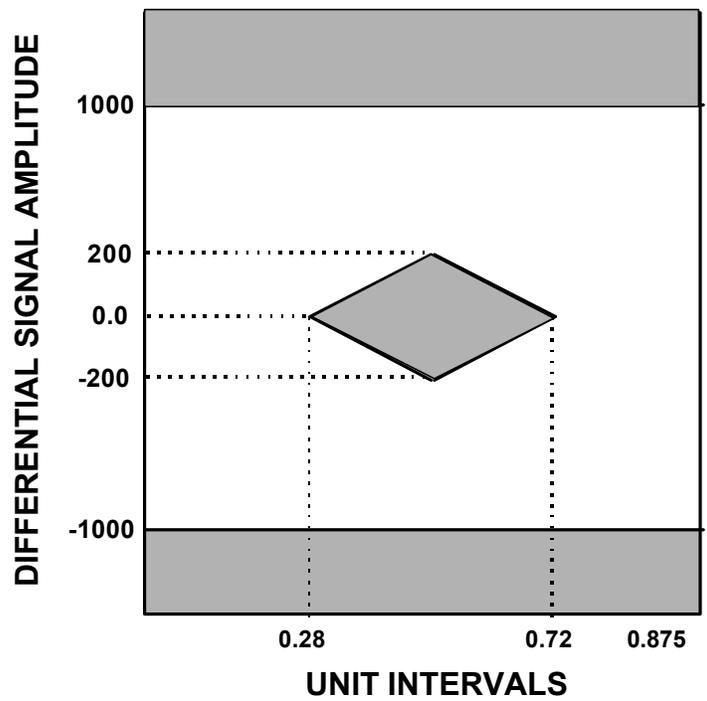


Figure 66 - Specified receive mask for full speed FC internal

### **8.3 Balance degradation**

Acceptable values for balance degradation are presently only directly defined in this document. Some standards documents note a line to line skew requirement (which only accounts for one component of balance degradation and is nearly never present alone). For example the latest FC standards allow a full 200 ps skew at the receiver - this value is much larger than is appropriate for a balanced signal. With a 200 ps skew there is almost no balance present in the signals since the rise and falls times are of the same magnitude.

### **8.4 EMC**

Acceptable values for EMC are presently only defined in this document.

### **8.5 NEXT (Quiescent noise)**

Acceptable values for NEXT are proposed for FC at 3% max but have not been accepted by the standard.